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Photometric Front Ends

Data Sheet

ADPD105/ADPD106/ADPD107

FEATURES

- Multifunction photometric front end
- Fully integrated AFE, ADC, LED drivers, and timing core
- Enables best-in-class ambient light rejection capability without the need for photodiode optical filters
- Three 370 mA LED drivers
- Flexible, multiple, short LED pulses per optical sample
- 20-bit burst accumulator enabling 20 bits per sample period
- On-board sample to sample accumulator, enabling up to 27 bits per data read
- Low power operation
- SPI, I^2C interface, and 1.8 V analog/digital core
- Flexible sampling frequency ranging from 0.122 Hz to 3820 Hz
- FIFO data operation

APPLICATIONS

- Wearable health and fitness monitors
- Clinical measurements, for example, SpO_2
- Industrial monitoring
- Background light measurements

GENERAL DESCRIPTION

The ADPD105/ADPD106/ADPD107 are highly efficient, photometric front ends, each with an integrated 14-bit analog-to-digital converter (ADC) and a 20-bit burst accumulator that works with flexible light emitting diode (LED) drivers. The accumulator is designed to stimulate an LED and measure the corresponding optical return signal. The data output and functional configuration occur over a 1.8 V I^2C interface on the ADPD105 or SPI on the ADPD106 and ADPD107. The control circuitry includes flexible LED signaling and synchronous detection.

The analog front end (AFE) features best-in-class rejection of signal offset and corruption due to modulated interference commonly caused by ambient light.

Couple the ADPD105/ADPD106/ADPD107 with a low capacitance photodiode of <100 pF for optimal performance. The ADPD105/ADPD106/ADPD107 can be used with any LED. The ADPD105 is available in a 2.46 mm × 1.4 mm WLCSP and a 4 mm × 4 mm LFCSP. The SPI only versions, ADPD106 and ADPD107, are available in a 2.46 mm × 1.4 mm WLCSP.

Rev. A

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7/2016—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

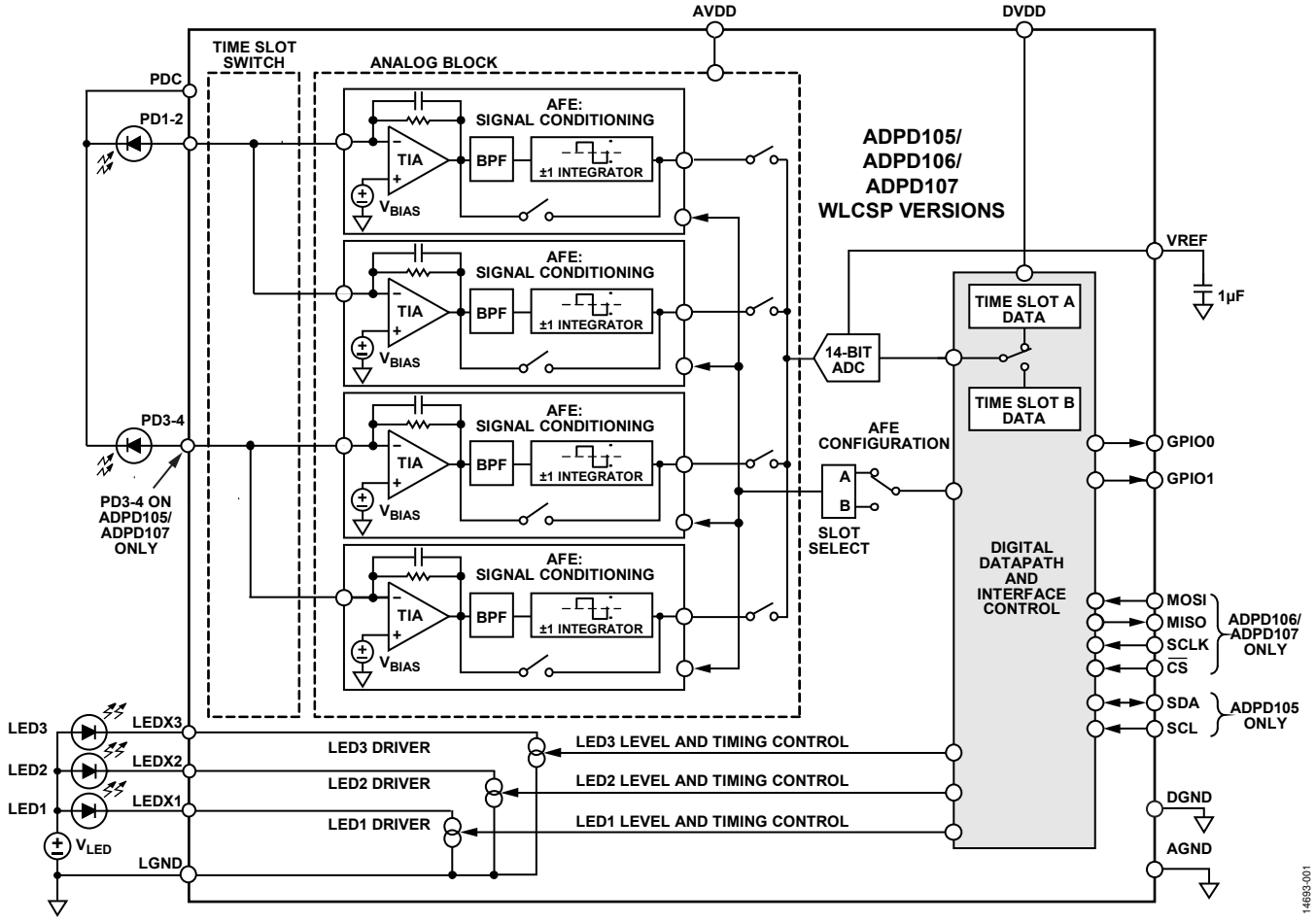

Figure 1. Block Diagram for ADPD105/ADPD106/ADPD107 WLCSP (Chip Scale Package) Versions

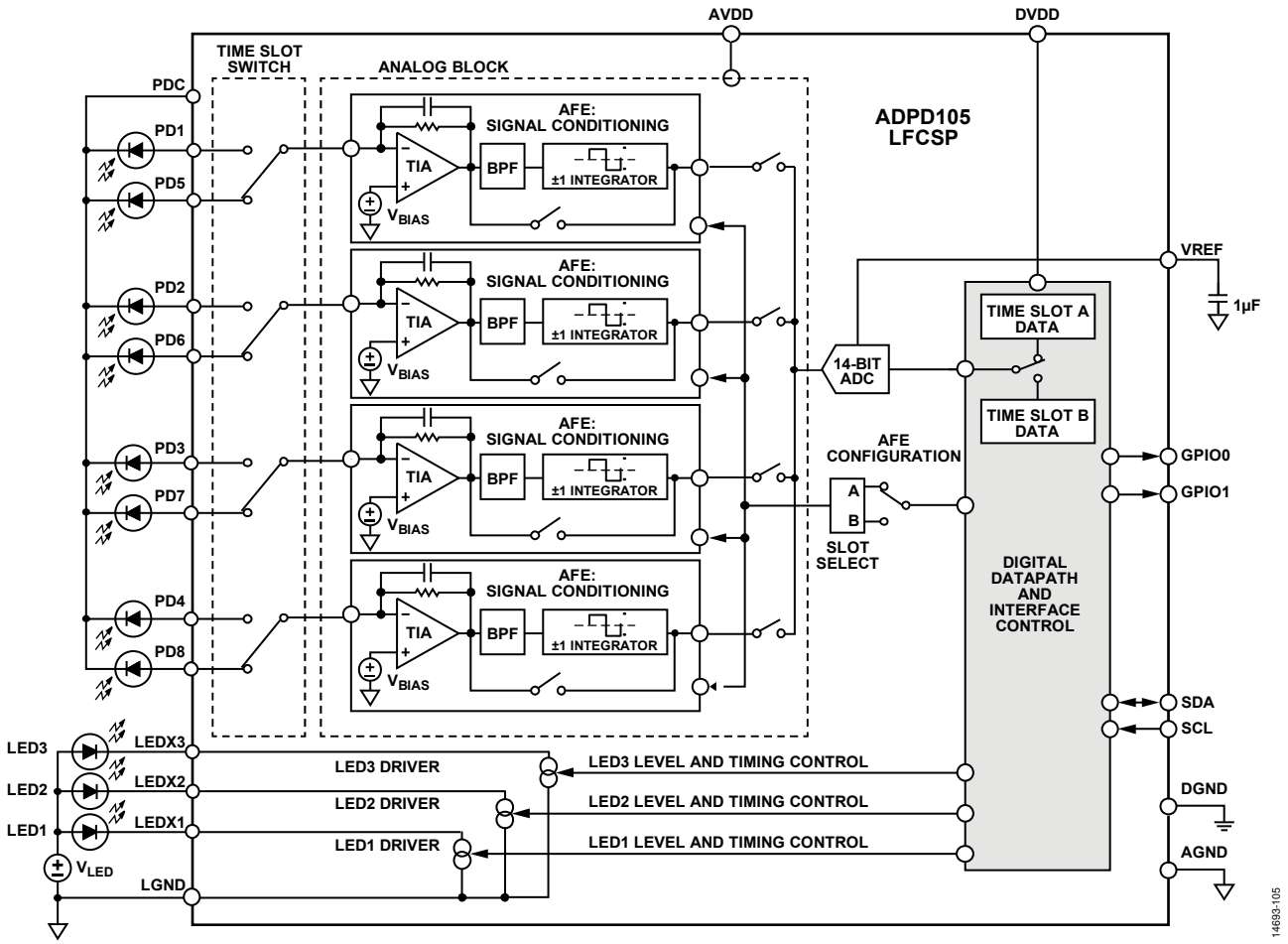

Figure 2. Block Diagram for ADPD105 LFCSP Version

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Operating Conditions

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating Range		−40		+85	°C
Storage Range		−65		+150	°C
POWER SUPPLY VOLTAGES					
V_{DD}	Applied at the AVDD and DVDD pins	1.7	1.8	1.9	V

AVDD = DVDD = 1.8 V, T_A = 25°C, unless otherwise noted.

Table 2. Current Consumption

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (V_{DD}) CURRENT						
V_{DD} Supply Current[1]		SLOTx_LED_OFFSET = 25 µs; LED_PERIOD =19 µs; LED peak current = 25 mA, single-channel mode				
1 Pulse		100 Hz data rate; Time Slot A only		92		µA
		100 Hz data rate; Time Slot B only		75		µA
		100 Hz data rate; both Time Slot A and Time Slot B		119		µA
10 Pulses		100 Hz data rate; Time Slot A only		175		µA
		100 Hz data rate; Time Slot B only		155		µA
		100 Hz data rate; both Time Slot A and Time Slot B		281		µA
Peak V_{DD} Supply Current (1.8 V)	IV_{DD_PEAK}					
4-Channel Operation				9.3		mA
1-Channel Operation				4.5		mA
Standby Mode Current	$IV_{DD\_STANDBY}$			0.3		µA
V_{LED} SUPPLY CURRENT[2]						
Average Supply Current						
V_{LEDA} or V_{LEDB}		Peak LED current = 25 mA; LED pulse width = 3 µs				
1 Pulse		50 Hz data rate		3.75		µA
		100 Hz data rate		7.5		µA
		200 Hz data rate		15		µA
10 Pulses		50 Hz data rate		38		µA
		100 Hz data rate		75		µA
		200 Hz data rate		150		µA

[1] V_{DD} is the voltage applied at the AVDD and DVDD pins.
[2] V_{LED} applies to the external LED supply voltage for any given LED being driven by the ADPD105/ADPD106/ADPD107 LED drivers under the listed conditions.

PERFORMANCE SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DATA ACQUISITION					
Resolution	Single pulse		14		Bits
Resolution/Sample	64 to 255 pulses		20		Bits
Resolution/Data Read	64 to 255 pulses and sample average = 128		27		Bits
LED DRIVER					
LED Current Slew Rate[1]					
Rise	Slew rate control setting = 0; T_A = 25°C; I_{LED} = 70 mA		240		mA/µs
	Slew rate control setting = 7; T_A = 25°C; I_{LED} = 70 mA		1400		mA/µs
Fall	Slew rate control setting = 0, 1, 2; T_A = 25°C; I_{LED} = 70 mA		3200		mA/µs
	Slew rate control setting = 6, 7; T_A = 25°C; I_{LED} = 70 mA		4500		mA/µs
LED Peak Current	LED pulse enabled			370	mA
Driver Compliance Voltage	Voltage above ground required for LED driver operation		0.6		V
LED PERIOD	AFE width = 4 µs[2]		19		µs
	AFE width = 3 µs		17		µs
Sampling Frequency[3]	Time Slot A only; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		3230	Hz
	Time Slot B only; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		3820	Hz
	Both time slots; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		1750	Hz
	Time Slot A only; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		2257	Hz
	Time Slot B only; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		2531	Hz
	Both time slots; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_LED_PERIOD = 19 µs	0.122		1193	Hz
CATHODE PIN (PDC) VOLTAGE					
During All Sampling Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1[4]		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
During Slot A Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x0[4]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x3[5]		0		V
During Slot B Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x0[4]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x3[5]		0		V
During Sleep Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x0		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x3		0		V
PHOTODIODE INPUT PINS/ ANODE VOLTAGE					
During All Sampling Periods			1.3		V
During Sleep Periods			Cathode voltage		V

[1] LED inductance is negligible for these values. The effective slew rate slows with increased inductance.
[2] Minimum LED period = (2 × AFE width) + 5 µs.
[3] The maximum values in this specification are the internal ADC sampling rates in normal mode. The I^2C read rates in some configurations may limit the output data rate.
[4] This mode may induce additional noise and is not recommended unless absolutely necessary. The 1.8 V setting uses V_{DD}, which contains greater amounts of differential voltage noise with respect to the anode voltage. A differential voltage between the anode and cathode injects a differential current across the capacitance of the photodiode of the magnitude of C × dV/dt.
[5] This setting is not recommended for photodiodes because it causes a 1.3 V forward bias of the photodiode.

ANALOG SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted. Compensation of the AFE offset is explained in the AFE Operation section.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CAPACITANCE				100	pF
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[1]	4 µs wide AFE integration; normal operation, Register 0x43/Register 0x45 = 0xADA5				
ADC Resolution[2]	Transimpedance amplifier (TIA) feedback resistor				
	25 kΩ		3.27		nA/LSB
	50 kΩ		1.64		nA/LSB
	100 kΩ		0.82		nA/LSB
	200 kΩ		0.41		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		26.8		µA
	50 kΩ		13.4		µA
	100 kΩ		6.7		µA
	200 kΩ		3.35		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		23.6		µA
	50 kΩ		11.8		µA
	100 kΩ		5.9		µA
	200 kΩ		2.95		µA
PULSED SIGNAL CONVERSIONS, 2 µs WIDE LED PULSE[1]	3 µs wide AFE integration; normal operation, Register 0x43/Register 0x45 = 0xADA5				
ADC Resolution[2]	TIA feedback resistor				
	25 kΩ		4.62		nA/LSB
	50 kΩ		2.31		nA/LSB
	100 kΩ		1.15		nA/LSB
	200 kΩ		0.58		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		37.84		µA
	50 kΩ		18.92		µA
	100 kΩ		9.46		µA
	200 kΩ		4.73		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		12.56		µA
	50 kΩ		6.28		µA
	100 kΩ		3.14		µA
	200 kΩ		1.57		µA
FULL SIGNAL CONVERSIONS[3]					
TIA Saturation Level of Pulsed Signal and Ambient Level	TIA feedback resistor				
	25 kΩ		50.4		µA
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode; per pulse; per channel; no LED; photodiode capacitance (C_{PD}) = 70 pF				
	25 kΩ; referred to ADC input		1.0		LSB rms
	25 kΩ; referred to peak input signal for 2 µs LED pulse		4.6		nA rms
	25 kΩ; referred to peak input signal for 3 µs LED pulse		3.3		nA rms
	25 kΩ; saturation signal-to-noise ratio (SNR) per pulse per channel[4]		78.3		dB
	50 kΩ; referred to ADC input		1.2		LSB rms
	50 kΩ; referred to peak input signal for 2 µs LED pulse		2.8		nA rms
	50 kΩ; referred to peak input signal for 3 µs LED pulse		2.0		nA rms
	50 kΩ; saturation SNR per pulse per channel[4]		76.6		dB
	100 kΩ; referred to ADC input		1.7		LSB rms
	100 kΩ; referred to peak input signal for 2 µs LED pulse		1.9		nA rms
	100 kΩ; referred to peak input signal for 3 µs LED pulse		1.4		nA rms
	100 kΩ; saturation SNR per pulse per channel[4]		73.6		dB
	200 kΩ; referred to ADC input		2.75		LSB rms
	200 kΩ; referred to peak input signal for 2 µs LED pulse		1.6		nA rms
	200 kΩ; referred to peak input signal for 3 µs LED pulse		1.1		nA rms
	200 kΩ; saturation SNR per pulse per channel[4]		69.5		dB
DC Power Supply Rejection Ratio (DC PSRR)			−37		dB

[1] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[2] ADC resolution is listed per pulse when the AFE offset is correctly compensated per the AFE Operation section. If using multiple pulses, divide by the number of pulses.
[3] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal.
[4] The noise term of the saturation SNR value refers to the receive noise only and does not include photon shot noise or any noise on the LED signal itself.

DIGITAL SPECIFICATIONS

DVDD = 1.7 V to 1.9 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (GPIOx, SCL, SDA, SCLK, MOSI, $\overline{CS}$)						
Input Voltage Level						
High	V_{IH}		0.7 × DVDD		3.6	V
Low	V_{IL}				0.3 × DVDD	V
Input Current Level						
High	I_{IH}		−10		+10	µA
Low	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
Output Voltage Level		GPIOx, MOSI				
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
Output Voltage Level		SDA				
Low	V_{OL1}	2 mA low level output current			0.2 × DVDD	V
Output Current Level		SDA				
Low	I_{OL}	V_{OL1} = 0.6 V	6			mA

TIMING SPECIFICATIONS

Table 6. I²C Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORT[1]		See Figure 3				
SCL						
Frequency				400		kHz
Minimum Pulse Width						
High	t_1		600			ns
Low	t_2		1300			ns
Start Condition						
Hold Time	t_3		600			ns
Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA						
Rise Time	t_6				1000	ns
Fall Time	t_7				300	ns
Stop Condition						
Setup Time	t_8		600			ns

[1] Guaranteed by design.

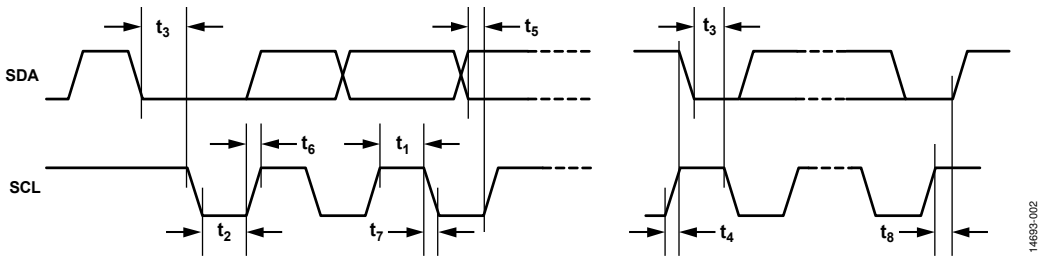

Figure 3. I²C Timing Diagram

Table 7. SPI Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI PORT						
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		20			ns
Low	$t_{SCLKPWL}$		20			ns
$\overline{CS}$						
Setup Time	$t_{\overline{CSS}}$	$\overline{CS}$ setup to SCLK rising edge	10			ns
Hold Time	$t_{\overline{CSH}}$	$\overline{CS}$ hold from SCLK rising edge	10			ns
Pulse Width High	$t_{\overline{CSPWH}}$	$\overline{CS}$ pulse width high	10			ns
MOSI						ns
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	10			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	10			
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge			20	ns

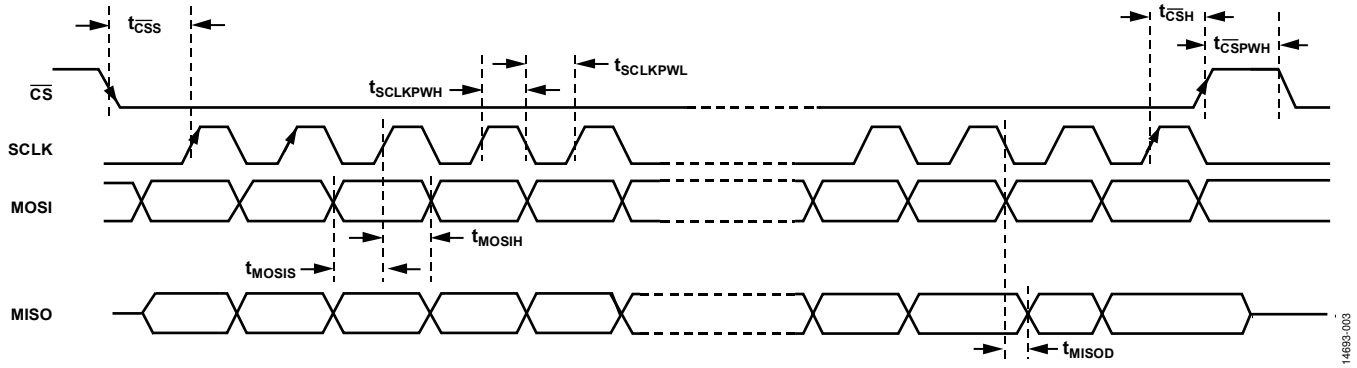

Figure 4. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
DVDD to DGND	−0.3 V to +2.2 V
GPIO0 to DGND	−0.3 V to +2.2 V
GPIO1 to DGND	−0.3 V to +2.2 V
LEDXx to LGND	−0.3 V to +3.6 V
SCL to DGND	−0.3 V to +3.9 V
SDA to DGND	−0.3 V to +3.9 V
Junction Temperature	150°C
ESD	
Human Body Model (HBM)	1500 V
Charged Device Model (CDM)	500 V
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 9. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-28-5	54.9	°C/W
CB-16-18	60	°C/W
CB-17-1	60	°C/W

RECOMMENDED SOLDERING PROFILE

Figure 5 and Table 10 provide details about the recommended soldering profile.

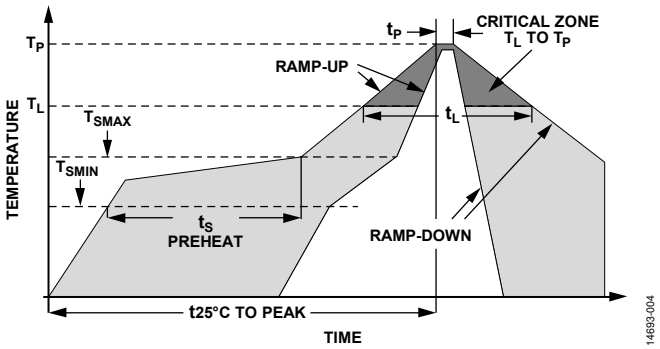

Figure 5. Recommended Soldering Profile

Table 10. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature	8 minutes maximum

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

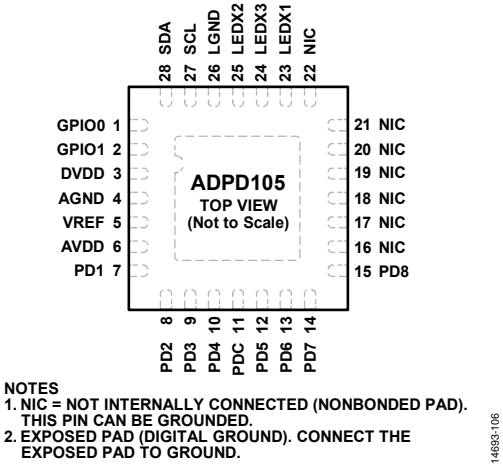

Figure 6. 28-Lead LFCSP Pin Configuration (ADPD105)

Table 11. 28-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	GPIO0	DIO	General-Purpose Input/Output (I/O). This pin is used for interrupts and various clocking options.
2	GPIO1	DIO	General-Purpose I/O. This pin is used for interrupts and various clocking options.
3	DVDD	S	1.8 V Digital Supply.
4	AGND	S	Analog Ground.
5	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
6	AVDD	S	1.8 V Analog Supply.
7	PD1	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
8	PD2	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
9	PD3	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
10	PD4	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
11	PDC	AO	Photodiode Common Cathode Bias.
12	PD5	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
13	PD6	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
14	PD7	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
15	PD8	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
16 to 22	NIC	R	Not Internally Connected (Nonbonded Pad). This pin can be grounded.
23	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
24	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
25	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
26	LGND	S	LED Driver Ground.
27	SCL	DI	I^2C Clock Input.
28	SDA	DIO	I^2C Data Input/Output.
	EPAD (DGND)	S	Exposed Pad (Digital Ground). Connect the exposed pad to ground.

[1] DIO means digital input/output, S means supply, REF means voltage reference, AI means analog input, AO means analog output, R means reserved, and DI means digital input.

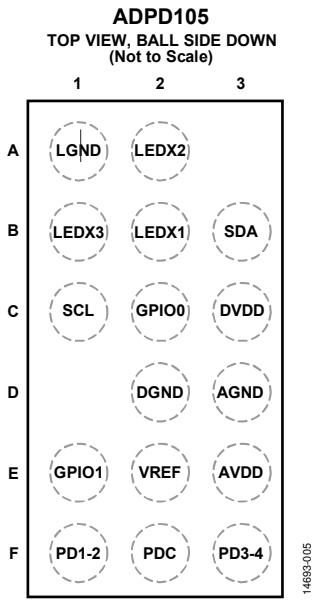

Figure 7. ADPD105 Pin Configuration

Table 12. ADPD105 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	LGND	S	LED Driver Ground.
A2	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
B1	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
B3	SDA	DIO	I^2C Data Input/Output (I/O).
C1	SCL	DI	I^2C Clock Input.
C2	GPIO0	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
C3	DVDD	S	1.8 V Digital Supply.
D2	DGND	S	Digital Ground.
D3	AGND	S	Analog Ground.
E1	GPIO1	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
E2	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
E3	AVDD	S	1.8 V Analog Supply.
F1	PD1-2	AI	Photodiode Combined Current Input of Photodiode 1 (PD1) and Photodiode 2 (PD2). If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD3-4	AI	Photodiode Combined Current Input of Photodiode 3 (PD3) and Photodiode 4 (PD4). If not in use, leave this pin floating.

[1] S means supply, AO means analog output, DIO means digital input/output, DI means digital input, REF means voltage reference, AI means analog input, and AO means analog output.

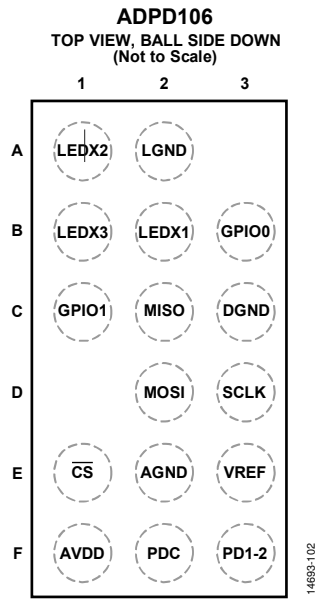

Figure 8. 16-Ball WLCSP Pin Configuration (ADPD106)

Table 13. 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
A2	LGND	S	LED Driver Ground
B1	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
B3	GPIO0	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
C1	GPIO1	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
C2	MISO	DO	SPI Data Output.
C3	DGND	S	Digital Ground.
D2	MOSI	DI	SPI Data Input.
D3	SCLK	DI	SPI Clock Input.
E1	$\overline{CS}$	DI	SPI Chip Select, Active Low.
E2	AGND	S	Analog Ground.
E3	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
F1	AVDD	S	1.8 V Analog Supply.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD1-2	AI	Photodiode Combined Current Input of PD1 and PD2. If not in use, leave this pin floating.

[1] AO means analog output, S means supply, DIO means digital input/output, DO means digital output, DI means digital input, REF means voltage reference, and AI means analog input.

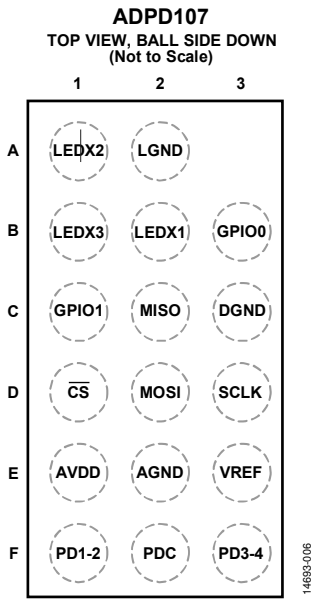

Figure 9. ADPD107 Pin Configuration

Table 14. ADPD107 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
A2	LGND	S	LED Driver Ground.
B1	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
B3	GPIO0	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
C1	GPIO1	DIO	General Purpose I/O. This pin is used for interrupts and various clocking options.
C2	MISO	DO	Master Input, Slave Output.
C3	DGND	S	Digital Ground.
D1	$\overline{CS}$	DI	SPI Chip Select. Active low.
D2	MOSI	DI	Master Output, Slave Input.
D3	SCLK	DI	SPI Clock Input.
E1	AVDD	S	1.8 V Analog Supply.
E2	AGND	S	Analog Ground.
E3	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
F1	PD1-2	AI	Photodiode Combined Current Input of PD1 and PD2. If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD3-4	AI	Photodiode Combined Current Input of PD3 and PD4. If not in use, leave this pin floating.

[1] AO means analog output, S means supply, DIO means digital input/output, DO means digital output, DI means digital input, REF means voltage reference, and AI means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

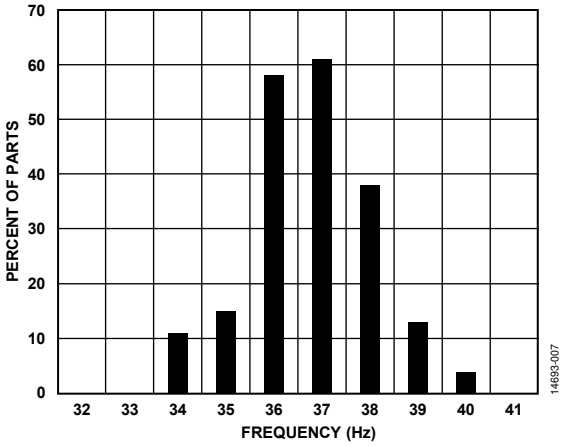

Figure 10. 32 kHz Clock Frequency Distribution (Default Settings, Before User Calibration: Register 0x4B = 0x2612)

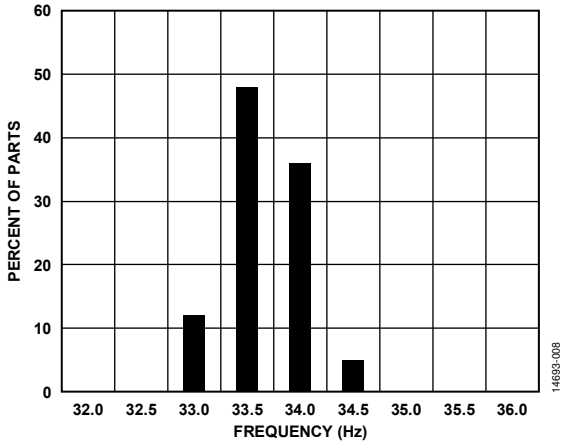

Figure 11. 32 MHz Clock Frequency Distribution (Default Settings, Before User Calibration: Register 0x4D = 0x0098)

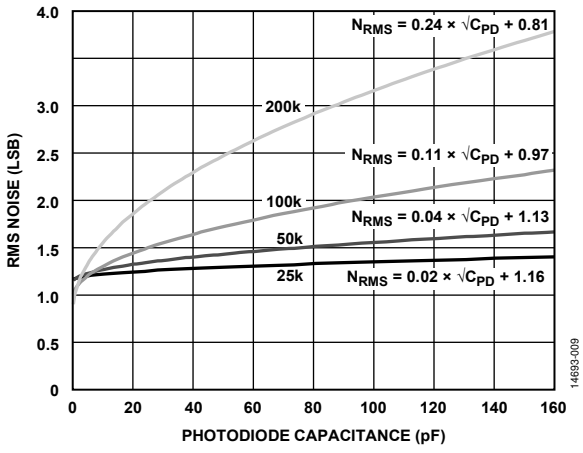

Figure 12. RMS Noise vs. Photodiode Capacitance

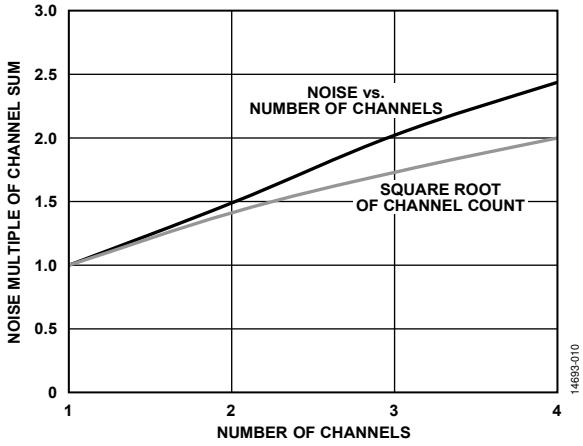

Figure 13. Noise Multiple of Channel Sum vs. Number of Channels

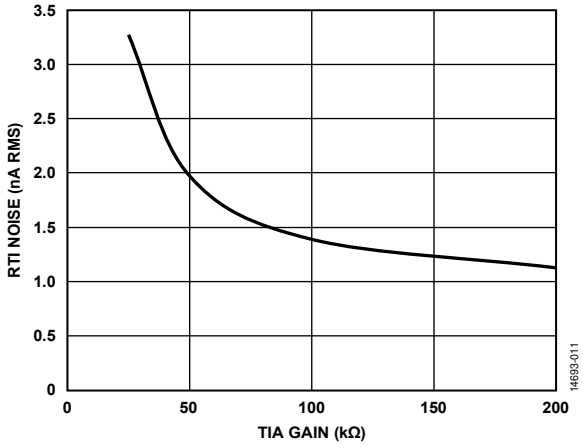

Figure 14. Referred to Input (RTI) Noise vs. TIA Gain

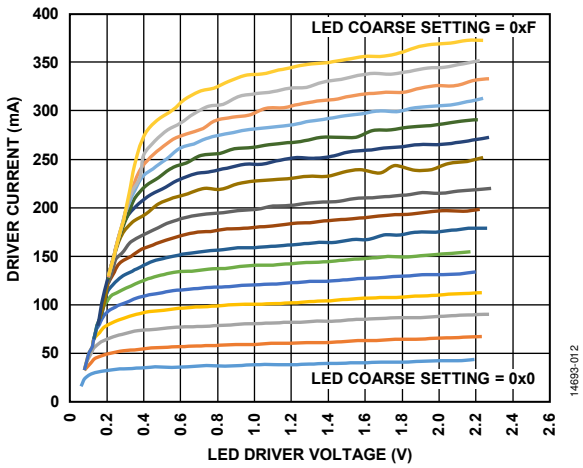

Figure 15. LED Driver Current vs. LED Driver Voltage at Various Coarse Settings

Figure 16. LED Driver Current vs. LED Fine Setting (Coarse Setting = 0x0)

Figure 17. LED Driver Current vs. LED Fine Setting (Coarse Setting = 0xF)

THEORY OF OPERATION

INTRODUCTION

The ADPD105/ADPD106/ADPD107 operate as a complete optical transceiver stimulating up to three LEDs and measuring the return signal on up to two separate current inputs. The core consists of a photometric front end coupled with an ADC, digital block, and three independent LED drivers. The core circuitry stimulates the LEDs and measures the return in the analog block through one to eight photodiode inputs, storing the results in discrete data locations. The two inputs can be configured to drive four simultaneous input channels. Data can be read directly by a register, or through a FIFO. This highly integrated system includes an analog signal processing block, digital signal processing block, I²C communication interface on the ADPD105 or an SPI port on the ADPD107, and programmable pulsed LED current sources.

The LED driver is a current sink and is agnostic to LED supply voltage and LED type. The photodiode (PDx) inputs can accommodate any photodiode with an input capacitance of less than 100 pF. The ADPD105/ADPD106/ADPD107 are designed to produce a high SNR for relatively low LED power while greatly reducing the effect of ambient light on the measured signal.

DUAL TIME SLOT OPERATION

The ADPD105/ADPD106/ADPD107 operate in two independent time slots, Time Slot A and Time Slot B, which are carried out sequentially. The entire signal path from LED stimulation to data capture and processing is executed during each time slot. Each time slot has a separate datapath that uses independent settings for the LED driver, AFE setup, and the resulting data. Time Slot A and Time Slot B operate in sequence for every sampling period, as shown in Figure 18.

The timing parameters are defined as follows:

$$t_A\ (\mu s) = SLOTA\_LED\_OFFSET + n_A \times SLOTA\_LED\_PERIOD$$

where n_A is the number of pulses for Time Slot A (Register 0x31, Bits[15:8]).

$$t_B\ (\mu s) = SLOTB\_LED\_OFFSET + n_B \times SLOTB\_LED\_PERIOD$$

where n_B is the number of pulses for Time Slot B (Register 0x36, Bits[15:8]).

Calculate the LED period using the following equation:

$$LED\_PERIOD,\ minimum = 2 \times AFE\_WIDTH + 11$$

t_1 and t_2 are fixed and based on the computation time for each slot. If a slot is not in use, these times do not add to the total active time. Table 15 defines the values for these LED and sampling time parameters.

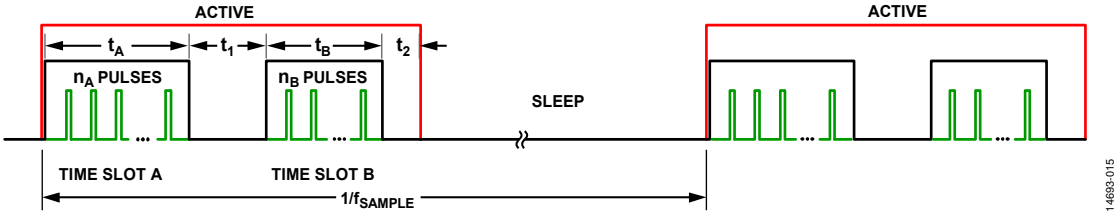

Figure 18. Time Slot Timing Diagram

Table 15. LED Timing and Sample Timing Parameters

Parameter	Register	Bits	Test Conditions/Comments	Min	Typ	Max	Unit
SLOTA_LED_OFFSET[1]	0x30	[7:0]	Delay from power-up to LEDA rising edge	23		63	µs
SLOTB_LED_OFFSET[1]	0x35	[7:0]	Delay from power-up to LEDB rising edge	23		63	µs
SLOTA_LED_PERIOD[2]	0x31	[7:0]	Time between LED pulses in Time Slot A; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
SLOTB_LED_PERIOD[2]	0x36	[7:0]	Time between LED pulses in Time Slot B; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
t_1			Compute time for Time Slot A		68		µs
t_2			Compute time for Time Slot B		20		µs
t_{SLEEP}			Sleep time between sample periods	222			µs

[1] Setting the SLOTx_LED_OFFSET below the specified minimum value may cause failure of ambient light rejection for large photodiodes.
[2] Setting the SLOTx_LED_PERIOD below the specified minimum value can cause invalid data captures.

TIME SLOT SWITCH

ADPD105 LFCSP Input Configurations

Up to eight photodiodes (PD1 to PD8) can be connected to the ADPD105 in the LFCSP package. The photodiode anodes are connected to the PD1 to PD8 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in three different configurations depending on the settings of Register 0x14 (see Figure 22, Figure 23, and Figure 21).

A switch sets which photodiode group is connected during Time Slot A and Time Slot B. See Table 17 for the time slot switch registers. It is important to leave any unused inputs floating for proper operation of the devices. The photodiode inputs are current inputs and as such, these pins are also considered to be voltage outputs. Tying these inputs to a voltage may saturate the analog block.

Register 0x14, PD1 to PD8 Input Configurations

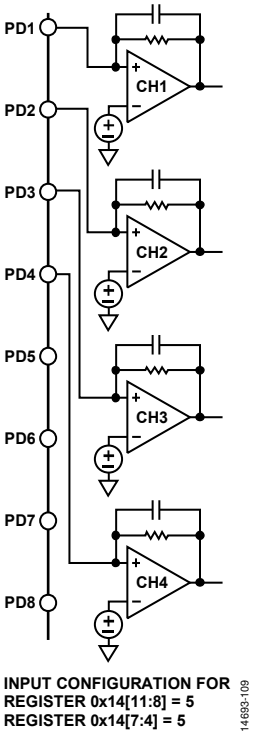

Figure 19. PD1 to PD4 Connection

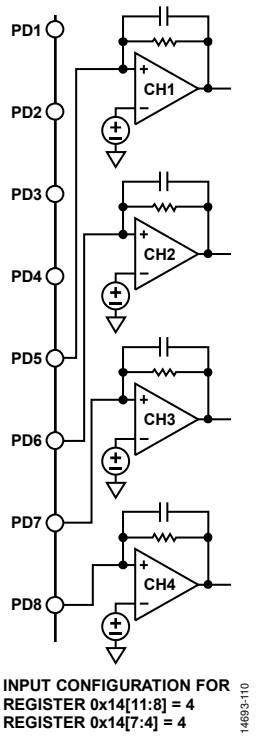

Figure 20. PD5 to PD8 Connection

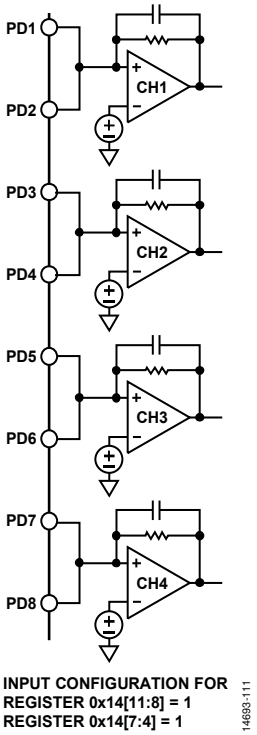

Figure 21. 2 to 1 PD Current Summation

Table 16. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	Selects connection of photodiode for Time Slot B as shown in Figure 22, Figure 23, and Figure 21. 0x0: inputs are floating in Time Slot B. 0x1: all PDx pins (PD1 to PD8) are connected during Time Slot B. 0x4: PD5 to PD8 are connected during Time Slot B. 0x5: PD1 to PD4 are connected during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	Selects connection of photodiode for Time Slot A as shown in Figure 22, Figure 23, and Figure 21. 0x0: inputs are floating in Time Slot A. 0x1: all PDx pins (PD1 to PD8) are connected during Time Slot A. 0x4: PD5 to PD8 are connected during Time Slot A. 0x5: PD1 to PD4 are connected during Time Slot A. Other: reserved.

WLCSP Input Configurations

Up to two photodiodes can be connected to four channels of the ADPD105 and ADPD107 WLCSP models. The ADPD106 accommodates a single photodiode that can be connected to Channel 1 and Channel 2. The photodiode anodes are connected to the PD1-2 and PD3-4 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in two different configurations depending on the settings of Register 0x14 (see Figure 22 and Figure 23).

Register 0x14, PD1 to PD4 Input Configurations

Figure 22 shows the configuration where each of the PD inputs is connected to two channels. This configuration is the high dynamic range mode used for large photodiode currents. Figure 23 shows the configuration where each of the inputs to the device is connected to a single channel. This mode allows the user to maximize SNR for situations where lower photodiode currents are expected.

A switch sets which photodiode group is connected during Time Slot A and Time Slot B. See Table 17 for the time slot switch registers. It is important to leave any unused inputs floating for proper operation of the devices. The photodiode inputs are current inputs and, as such, these pins are also considered to be voltage outputs. Tying these inputs to a voltage may saturate the analog block.

Note that the ADPD106 only includes the options shown for the PD1-2 input pin shown in Figure 22 and Figure 23.

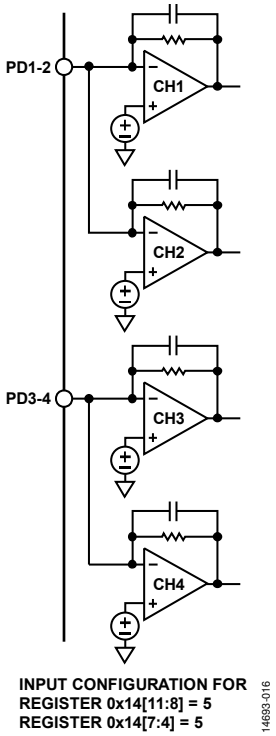

Figure 22. PD1 to PD4 Connection

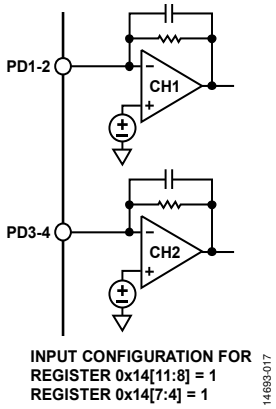

Figure 23. Current Summation—Two Photodiodes Summed into One Current

Table 17. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	Selects connection of photodiode for Time Slot B as shown in Figure 22 and Figure 23. 0x0: inputs are floating in Time Slot B. 0x1: PD1-2 is connected to Channel 1; PD3-4 is connected to Channel 2 during Time Slot B. 0x5: PD1-2 is connected to Channel 1 and Channel 2; PD3-4 is connected to Channel 3 and Channel 4 during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	Selects connection of photodiode for Time Slot A as shown in Figure 22 and Figure 23. 0x0: inputs are floating in Time Slot A. 0x1: PD1-2 is connected to Channel 1; PD3-4 is connected to Channel 2 during Time Slot A. 0x5: PD1-2 is connected to Channel 1 and Channel 2; PD3-4 is connected to Channel 3 and Channel 4 during Time Slot A. Other: reserved.

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 controls the sampling frequency setting of the ADPD105/ADPD106/ADPD107 and Register 0x4B, Bits[5:0] further tunes this clock for greater accuracy. The sampling frequency is governed by an internal 32 kHz sample rate clock that also drives the trans-ition of the internal state machine. The maximum sampling frequencies for some sample conditions are listed in Table 3. The maximum sample frequency for all conditions is determined by the following equation:

$$f_{SAMPLE,\,MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP,\,MIN})$$

where $t_{SLEEP,\,MIN}$ is the minimum sleep time required between samples.

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period and the new maximum sampling frequency is calculated as follows:

$$f_{SAMPLE,\,MAX} = 1/(t_B + t_2 + t_{SLEEP,\,MIN})$$

See the Dual Time Slot Operation section for the definitions of t_A, t_1, t_B, and t_2.

External Sync for Sampling

The ADPD105/ADPD106/ADPD107 provide an option to use an external sync signal to trigger the sampling periods. This external sample sync signal can be provided either on the GPIO0 pin or the GPIO1 pin. This functionality is controlled by Register 0x4F, Bits[3:2]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same as when the normal sample timer providesthe trigger. To enable the external sync signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write the appropriate value to Register 0x4F, Bits[3:2] to select whether the GPIO0 pin or the GPIO1 pin specifies when the next sample cycle occurs. Also, enable the appropriate input buffer using Register 0x4F, Bit 1, for the GPIO0 pin, or Register 0x4F, Bit 5, for the GPIO1 pin.
3. Write 0x4000 to Register 0x38.
4. Write 0x2 to Register 0x10 to start the sampling operations.
5. Apply the external sync signal on the selected pin at the desired rate; sampling occurs at that rate. As with normal sampling operations, read the data using the FIFO or the data registers.

The maximum frequency constraints also apply in this case.

Providing an External 32kHz Clock

The ADPD105/ADPD106/ADPD107 have an option for the user to provide an external 32 kHz clock to the devices for system synchronization or for situations where a clock with better accuracy than the internal 32 kHz clock is required. The external 32 kHz clock is provided on the GPIO1 pin. To enable the 32 kHz external clock, use the following procedure at startup:

1. Drive the GPIO1 pin to a valid logic level or with the desired 32 kHz clock prior to enabling the GPIO1 pin as an input. Do not leave the pin floating prior to enabling it.
2. Write 01 to Register 0x4F, Bits[6:5] to enable the GPIO1 pin as an input.
3. Write 10 to Register 0x4B, Bits[8:7] to configure the devices to use an external 32 kHz clock. This setting disables the internal 32 kHz clock and enables the external 32 kHz clock.
4. Write 0x1 to Register 0x10 to enter program mode.
5. Write additional control registers in any order while the devices are in program mode to configure the devices as required.
6. Write 0x2 to Register 0x10 to start the normal sampling operation.

STATE MACHINE OPERATION

During each time slot, the ADPD105/ADPD106/ADPD107 operate according to a state machine. The state machine operates in the following sequence, shown in Figure 24.

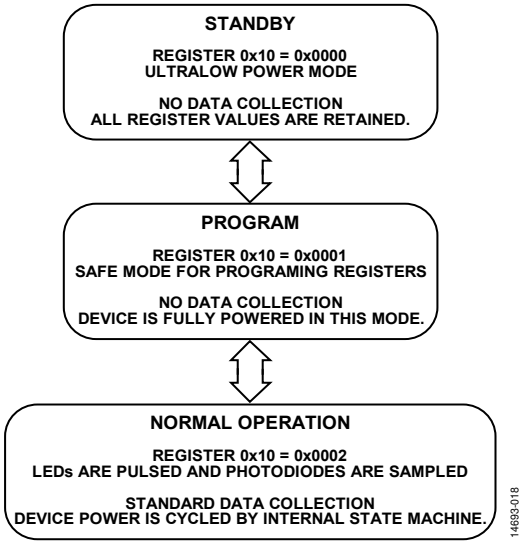

Figure 24. State Machine Operation Flowchart

The ADPD105/ADPD106/ADPD107 operate in one of three modes: standby, program, and normal sampling mode.

Standby mode is a power saving mode in which no data collection occurs. All register values are retained in this mode. To place the devices in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The devices power up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD105/ADPD106/ADPD107 through program mode when writing registers or changing modes. Because no power cycling occurs in this mode, the devices may consume higher current in program mode than in normal operation. To place the devices in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation, the ADPD105/ADPD106/ADPD107 pulse light and collect data. Power consumption in this mode depends on the pulse count and data rate. To place the devices in normal sampling mode, write 0x2 to Register 0x10, Bits[1:0].

NORMAL MODE OPERATION AND DATA FLOW

In normal mode, the ADPD105/ADPD106/ADPD107 follow a specific pattern set up by the state machine. This pattern is shown in the corresponding data flow in Figure 25. The pattern is as follows:

1. LED pulse and sample. The ADPD105/ADPD106/ADPD107 pulse external LEDs. The response of a photodiode or photodiodes to the reflected light is measured by the ADPD105/ADPD106/ADPD107. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

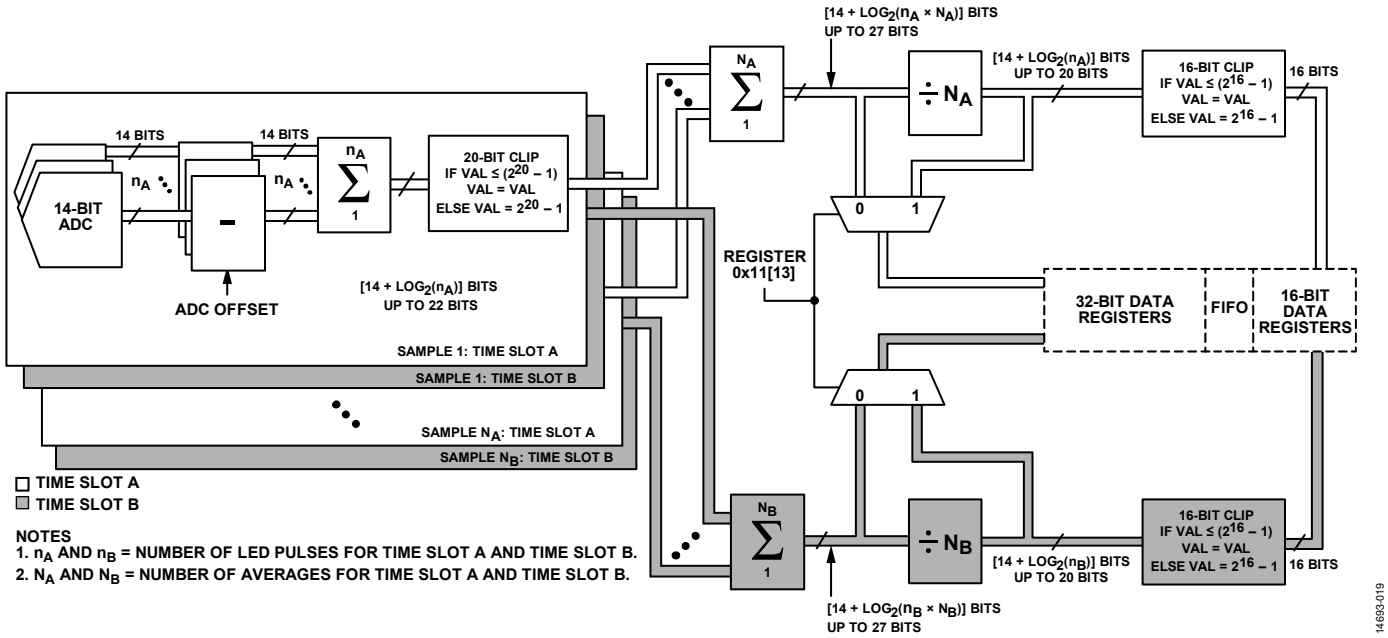

Figure 25. ADPD105/ADPD106/ADPD107 Datapath

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses, as shown in Figure 26. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light, that does not correspond to the LED pulse is rejected.

After each LED pulse, the photodiode output relating the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual sampling period. There is a 20-bit maximum range for each sampling period.

Averaging

The ADPD105/ADPD106/ADPD107 offer sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 256 sequential pulses. As shown in Figure 25, samples acquired by the AFE are clipped to 20 bits at the output of the AFE. Additional resolution, up to 27 bits, can be achieved by averaging between sampling periods. This accumulated data of N samples is stored as 27-bit values and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration.

When using the averaging feature set up by Register 0x15, subsequent pulses can be averaged by powers of 2. The user can select from 2, 4, 8 … up to 128 samples to be averaged. Pulse data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (Register 0x12), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 32-bit sum is stored in the 32-bit registers. However, before sending this data to the FIFO, a divide by N operation occurs. This divide operation maintains bit depth to prevent clipping on the FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x15 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width. This averaging can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADPD105/ADPD107 via the I²C protocol on the ADPD105 or the SPI port on the ADPD107. Data is read from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If they are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

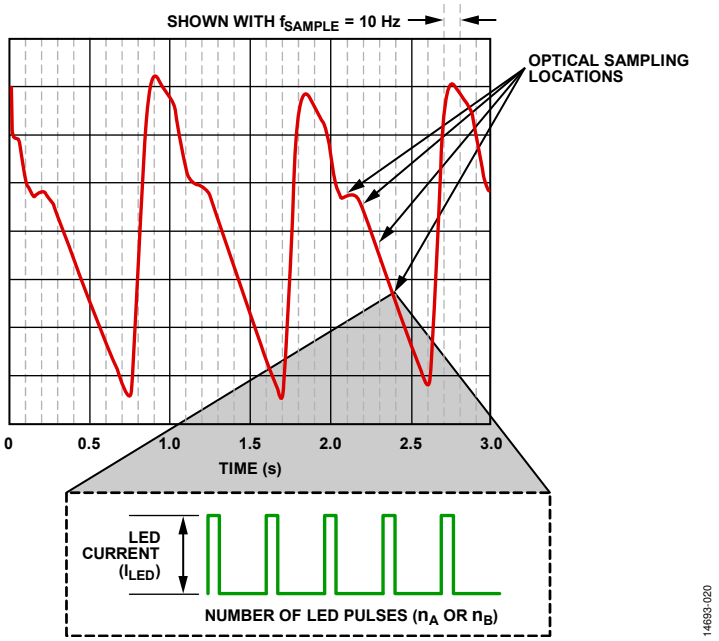

Figure 26. Example of a Photoplethysmography (PPG) Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

AFE OPERATION

The timing within each pulse burst is important for optimizing the operation of the ADPD105/ADPD106/ADPD107. Figure 27 shows the timing waveforms for a single time slot as an LED pulse response propagates through the analog block of the AFE. The first graph, shown in green, shows the ideal LED pulsed output. The filtered LED response, shown in blue, shows the output of the analog integrator. The third graph, shown in orange, illustrates an optimally placed integration window. When programmed to the optimized value, the full signal of the filtered LED response can be integrated. The AFE integration window is then applied to the output of the band-pass filter (BPF) and the result is sent to the ADC and summed for N pulses. If the AFE window is not correctly sized or located, all of the receive signal is not properly reported and system performance is not optimal; therefore, it is important to verify proper AFE position for every new hardware design or the LED width.

AFE INTEGRATION OFFSET ADJUSTMENT

The AFE integration width must be equal or larger than the LED width. As AFE width increases, the output noise increases and the ability to suppress high frequency content from the environment decreases. It is therefore desirable to keep the AFE integration width small. However, if the AFE width is too small, the LED signal is attenuated. With most hardware selections, the AFE width produces the optimal SNR at 1 µs more than the LED width. After setting LED width, LED offset, and AFE width, the ADC offset can then be optimized. The AFE offset must be manually set such that the falling edge of the first segment of the integration window matches the zero crossing of the filtered LED response.

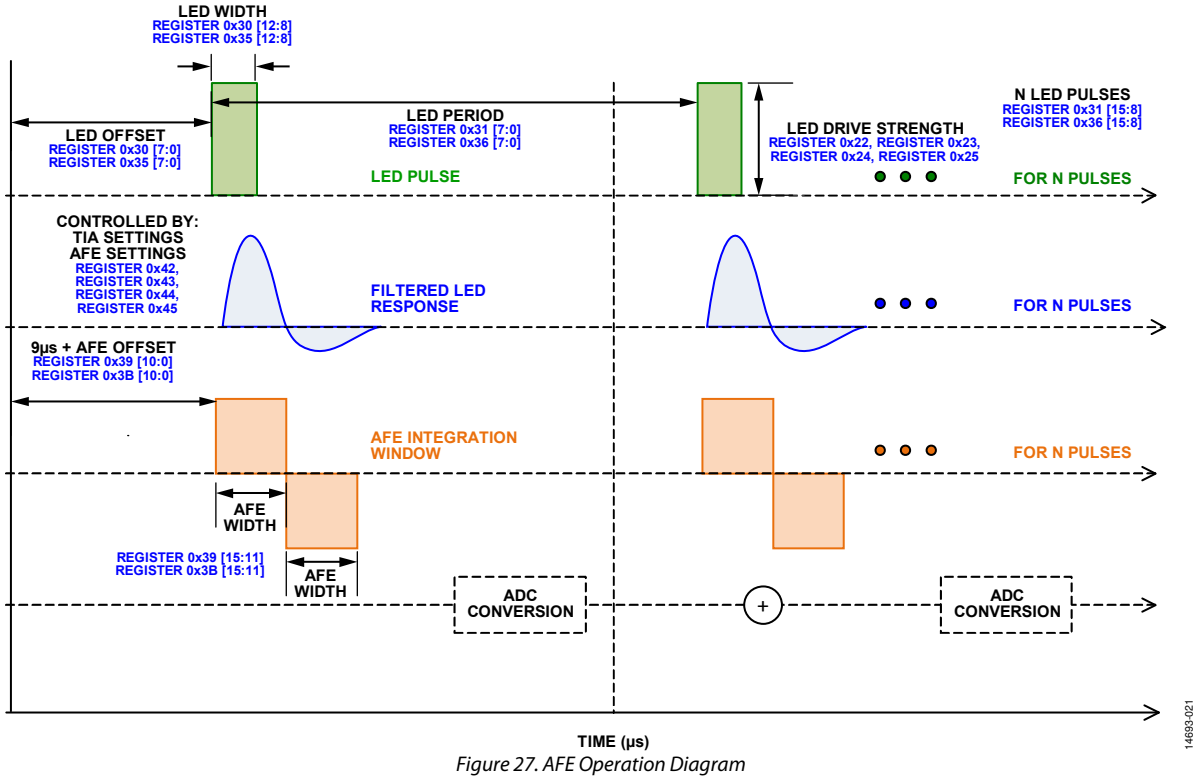

Figure 27. AFE Operation Diagram