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Integrated Optical Module with Ambient Light Rejection and Two LEDs

Data Sheet

ADPD188GG

FEATURES

- 3.8 mm × 5.0 mm × 0.9 mm module with integrated optical components
- 2 green LEDs, 2 PDs with IR cut filter
- 2 external sensor inputs
- 3, 370 mA LED drivers
- 20-bit burst accumulator enabling 20 bits per sample period
- On-board sample to sample accumulator enabling up to 27 bits per data read
- Custom optical package made to work under a glass window
- Optimized SNR for signal limited cases
- I²C or SPI communications

APPLICATIONS

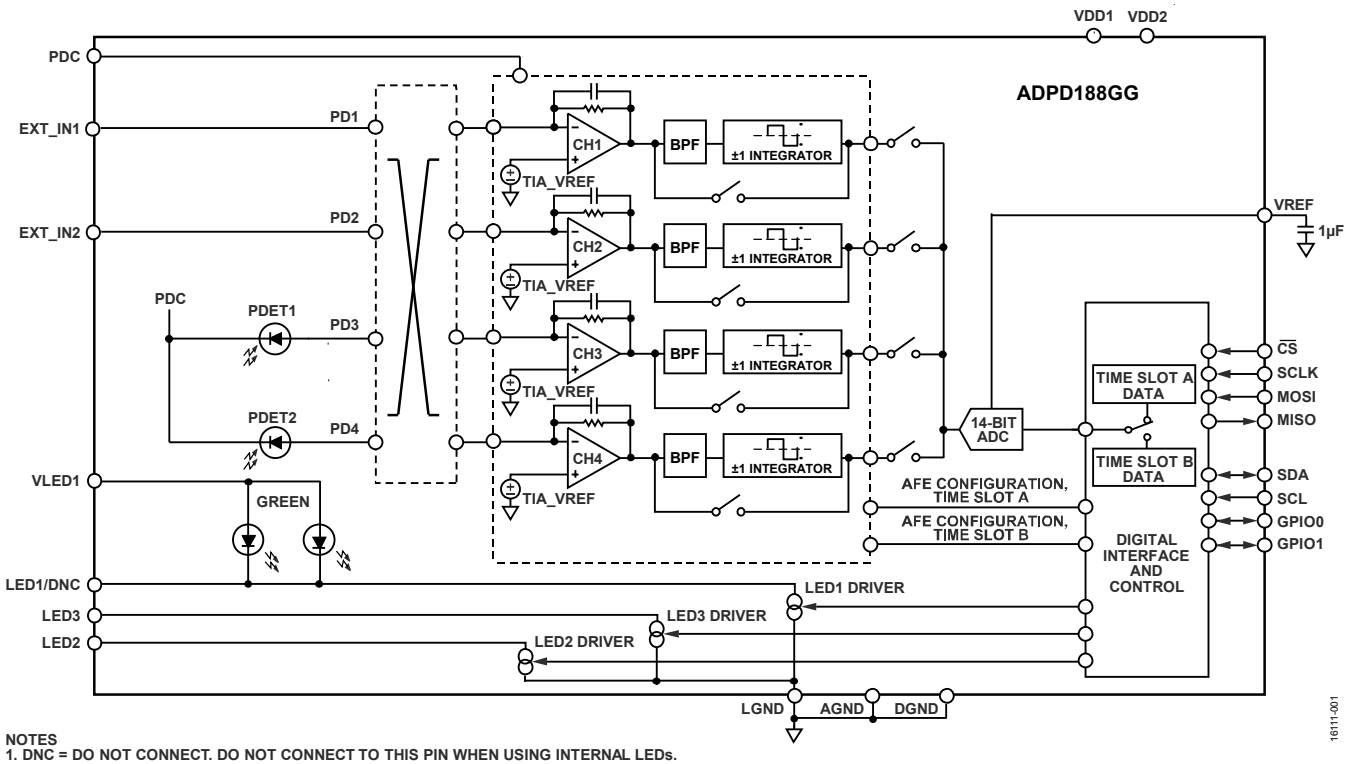
- Optical heart rate monitoring
- Reflective SpO_2 measurement
- CNIBP measurement

GENERAL DESCRIPTION

The ADPD188GG is a complete photometric system designed to measure optical signals from ambient light and from synchronous reflected light emitting diode (LED) pulses. Synchronous measurement offers best-in-class rejection of ambient light interference, both dc and ac. The module integrates a highly efficient photometric front end, two LEDs, and two photodiode (PD). All of these items are housed in a custom package that prevents light from going directly from the LED to the photodiode without first entering the subject.

The front end of the application specific integrated circuit (ASIC) consists of a control block, a 14-bit analog-to-digital converter (ADC) with a 20-bit burst accumulator, and three flexible, independently configurable LED drivers. The control circuitry includes flexible LED signaling and synchronous detection. The analog front end (AFE) features best-in-class rejection of signal offset and corruption due to modulated interference commonly caused by ambient light. The data output and functional configuration occur over a 1.8 V I²C interface or a serial peripheral interface (SPI) port.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN WHEN USING INTERNAL LEDs.

Figure 1.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

2/2018—Revision 0: Initial Version

SPECIFICATIONS

The voltage applied at the VDD1 and VDD2 pins (V_{DD}) = 1.8 V, and T_A = full operating temperature range, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT CONSUMPTION	See the Calculating Current Consumption section for the relevant equations				
Peak V_{DD} Supply Current	Single-channel (Register 0x3C, Bits[8:3] = 0x38)		4.5		mA
V_{DD} Standby Current			0.3		µA
Average V_{DD} Supply Current	100 Hz data rate; LED offset = 25 µs; LED pulse period (t_{LED_PERIOD}) = 13 µs; LED peak current = 25 mA				
1 Pulse	Time Slot A only		53		µA
	Time Slot B only		41		µA
	Both Time Slot A and Time Slot B		76		µA
10 Pulses	Time Slot A only		107		µA
	Time Slot B only		95		µA
	Both Time Slot A and Time Slot B		184		µA
Average V_{LED} Supply Current	LED peak current = 25 mA				
1 Pulse	50 Hz data rate		3.75		µA
	100 Hz data rate		7.5		µA
	200 Hz data rate		15		µA
10 Pulses	50 Hz data rate		38		µA
	100 Hz data rate		75		µA
	200 Hz data rate		150		µA
SATURATION ILLUMINANCE[1]	Blackbody color temperature (T = 5500 K)[2], PDET1 and PDET2 multiplexed into a single channel (1.2 mm^2 active area)				
Direct Illumination	Transimpedance amplifier (TIA) gain = 25 kΩ		58.8		kLux
	TIA gain = 50 kΩ		29.4		kLux
	TIA gain = 100 kΩ		14.7		kLux
	TIA gain = 200 kΩ		7.4		kLux
DATA ACQUISITION					
ADC Resolution	Single pulse		14		Bits
Per Sample	64 pulses to 255 pulses		20		Bits
Per Data Read	64 pulses to 255 pulses; 128 samples averaged		27		Bits
LED PERIOD	AFE width = 4 µs[3]	13	19		µs
	AFE width = 3 µs	11	17		µs
Sampling Frequency[4]	Time Slot A or Time Slot B; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		2000	Hz
	Both time slots; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1600	Hz
	Time Slot A or Time Slot B; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1600	Hz
	Both time slots; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1000	Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CATHODE PIN (PDC) VOLTAGE					
During All Sampling Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1[5]		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
During Time Slot A Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x0[5]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x2		TIA_VREF + 0.25		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x3[6]		0		V
During Time Slot B Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x0[5]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x2		TIA_VREF + 0.25		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x3[6]		0		V
During Sleep Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x0		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x2		TIA_VREF + 0.25		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x3		0		V
LEDs					
LED Peak Current Setting	Adjustable via the Register 0x22 through Register 0x25 settings	12		370	mA
Dominant Wavelength[7]					
LED1; Green LED	I_F = 40 mA		525		nm
Luminous Intensity	λ = 525 nm, I_F = 40 mA at 25°C	2800		3200	mcd
Photodiode					
Responsivity	Wavelength, λ = 525 nm		0.25		A/W
Active Area					
Photodiode 1			0.4		mm^2
Photodiode 2			0.8		mm^2
POWER SUPPLY VOLTAGES	The ADPD188GG does not require a specific power-up sequence				
V_{DD}	Applied at the VDD1 and VDD2 pins	1.7	1.8	1.9	V
V_{LED1}[8, 9]		4	4.5	5.0	V
DC Power Supply Rejection Ratio (PSRR)	At 75% full scale input signal		24		dB
TEMPERATURE RANGE					
Operating		−40		+85	°C

[1] Saturation illuminance refers to the amount of ambient light that saturates the ADPD188GG signal. Actual results may vary by factors of up to 2× from typical specifications. As a point of reference, Air Mass 1.5 (AM1.5) sunlight (brightest sunlight) produces 100 kLux.
[2] Blackbody color temperature (T = 5800 K) closely matches the light produced by solar radiation (sunlight).
[3] Minimum LED period = (2 × AFE width) + 5 µs.
[4] The maximum values in this specification are the internal ADC sampling rates in normal mode. The I^2C read rates in some configurations may limit the output data rate.
[5] This mode may induce additional noise and is not recommended unless necessary. The 1.8 V setting uses V_{DD}, which contains greater amounts of differential voltage noise with respect to the anode voltage. A differential voltage between the anode and cathode injects a differential current across the capacitance of the photodiode of the magnitude of C × dV/dt.
[6] This setting is not recommended for photodiodes because it causes a 1.3 V forward bias of the photodiode.
[7] I_F is the forward current of the diode.
[8] Set V_{LEDx} such that the maximum desired LED current is achievable with the turn on voltage of the LEDs that are wired to the LEDx/DNC pins. The LEDx/DNC pins are connected to the LEDx driver, which can be modeled as current sinks (see Figure 1). When an appropriate V_{LEDx} is used, the voltage at the LEDx/DNC pins adjusts automatically to accommodate the LED turn on voltage and the LED current.
[9] See Figure 9 for the current limitation at the minimum VLED supply voltage, V_{LED}.

ANALOG SPECIFICATIONS

VDD1 = VDD2 = 1.8 V, and T_A = full operating temperature range, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
EXT_INx SERIES RESISTANCE (R_IN)[1]	Measured from −3 µA to +3 µA		6.5		kΩ
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[2]	4 µs wide AFE integration; normal operation, Register 0x43 and Register 0x45 = 0xADA5				
ADC Resolution[3]	TIA feedback resistor				
	25 kΩ		3.27		nA/LSB
	50 kΩ		1.64		nA/LSB
	100 kΩ		0.82		nA/LSB
	200 kΩ		0.41		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		26.8		µA
	50 kΩ		13.4		µA
	100 kΩ		6.7		µA
	200 kΩ		3.35		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		23.6		µA
	50 kΩ		11.8		µA
	100 kΩ		5.9		µA
	200 kΩ		2.95		µA
PULSED SIGNAL CONVERSIONS, 2 µs WIDE LED PULSE[2]	3 µs wide AFE integration; normal operation, Register 0x43 and Register 0x45 = 0xADA5				
ADC Resolution[3]	TIA feedback resistor				
	25 kΩ		4.62		nA/LSB
	50 kΩ		2.31		nA/LSB
	100 kΩ		1.15		nA/LSB
	200 kΩ		0.58		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		37.84		µA
	50 kΩ		18.92		µA
	100 kΩ		9.46		µA
	200 kΩ		4.73		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		12.56		µA
	50 kΩ		6.28		µA
	100 kΩ		3.14		µA
	200 kΩ		1.57		µA
FULL SIGNAL CONVERSIONS[4]					
TIA Saturation Level Pulsed Signal and Ambient Level	TIA feedback resistor				
	25 kΩ		50.4		µA
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA
TIA Linear Range	TIA feedback resistor				
	25 kΩ		42.8		µA
	50 kΩ		21.4		µA
	100 kΩ		10.7		µA
	200 kΩ		5.4		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode; per pulse; per channel; no LED; photodiode capacitance (C_{PD}) = 25 pF				
	25 kΩ; referred to ADC input		1.0		LSB rms
	25 kΩ; referred to peak input signal for 2 µs LED pulse		4.6		nA rms
	25 kΩ; referred to peak input signal for 3 µs LED pulse		3.3		nA rms
	25 kΩ; saturation signal-to-noise ratio (SNR) per pulse per channel[5]		78.3		dB
	50 kΩ; referred to ADC input		1.1		LSB rms
	50 kΩ; referred to peak input signal for 2 µs LED pulse		2.5		nA rms
	50 kΩ; referred to peak input signal for 3 µs LED pulse		1.8		nA rms
	50 kΩ; saturation SNR per pulse per channel[5]		77.4		dB
	100 kΩ; referred to ADC input		1.2		LSB rms
	100 kΩ; referred to peak input signal for 2 µs LED pulse		1.4		nA rms
	100 kΩ; referred to peak input signal for 3 µs LED pulse		0.98		nA rms
	100 kΩ; saturation SNR per pulse per channel[5]		76.7		dB
	200 kΩ; referred to ADC input		1.4		LSB rms
	200 kΩ; referred to peak input signal for 2 µs LED pulse		0.81		nA rms
	200 kΩ; referred to peak input signal for 3 µs LED pulse		0.57		nA rms
	200 kΩ; saturation SNR per pulse per channel[5]		75.3		dB

[1] The R_IN value can be ignored for current source inputs or for PD inputs. This value is important for calculating correct voltages for voltage inputs through a resistor.
[2] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[3] ADC resolution is listed per pulse. If using multiple pulses, divide by the number of pulses.
[4] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal.
[5] The noise term of the saturation SNR value refers to the receive noise only and does not include photon shot noise or any noise on the LED signal itself.

DIGITAL SPECIFICATIONS

VDD1 = VDD2 = 1.7 V to 1.9 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS						
Input Voltage Level						
High	V_{IH}	GPIOx, SCLK, MOSI, $\overline{CS}$	0.7 × VDDx		VDDx	V
High	V_{IH}	SCL, SDA	0.7 × VDDx		3.6	
Low	V_{IL}				0.3 × VDDx	V
Input Current Level						
High	I_{IH}		−10		+10	µA
Low	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
Output Voltage Level		GPIOx, MISO				
High	V_{OH}	2 mA high level output current	VDDx − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
Output Voltage Level		SDA				
Low	V_{OL1}	2 mA low level output current			0.2 × VDDx	V
Output Current Level		SDA				
Low	I_{OL}	V_{OL1} = 0.6 V	6			mA

TIMING SPECIFICATIONS

I²C Timing Specifications

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SCL					
Frequency			1		Mb/sec
Minimum Pulse Width					
High	t_1	370			ns
Low	t_2	530			ns
START CONDITION					
Hold Time	t_3	260			ns
Setup Time	t_4	260			ns
SDA SETUP TIME	t_5	50			ns
SCL AND SDA					
Rise Time	t_6			120	ns
Fall Time	t_7			120	ns
STOP CONDITION					
Setup Time	t_8	260			ns

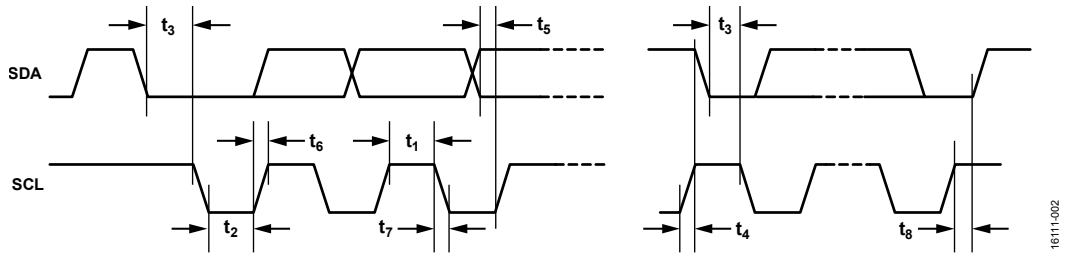

Figure 2. I²C Timing Diagram

SPI Timing Specifications

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		20			ns
Low	$t_{SCLKPWL}$		20			ns
$\overline{CS}$						
Setup Time	$t_{\overline{CSS}}$	$\overline{CS}$ setup to SCLK rising edge	10			ns
Hold Time	$t_{\overline{CSH}}$	$\overline{CS}$ hold from SCLK rising edge	10			ns
Pulse Width High	$t_{\overline{CSPWH}}$	$\overline{CS}$ pulse width high	10			ns
MOSI						ns
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	10			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	10			
MISO OUTPUT DELAY	t_{MISOD}	MISO valid output delay from SCLK falling edge			21	ns

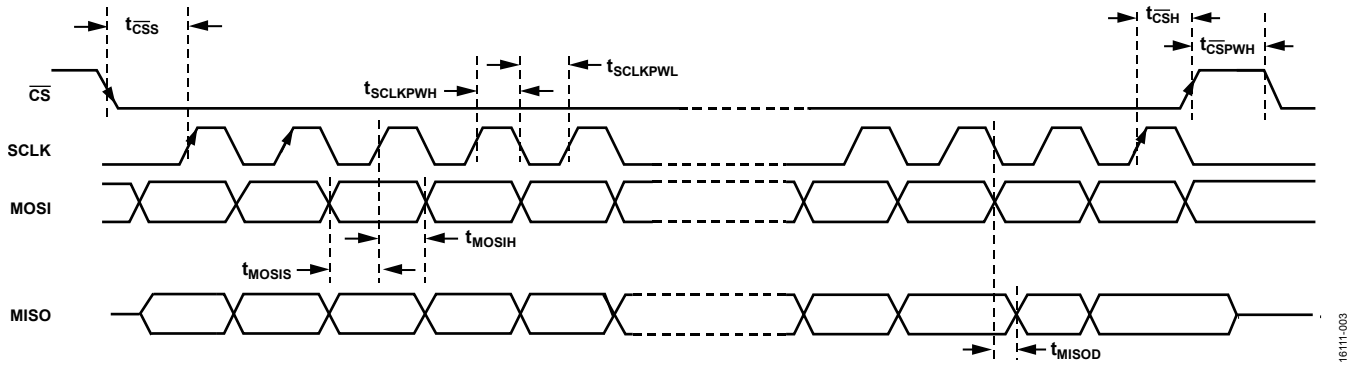

Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VDD1, VDD2 to AGND	−0.3 V to +2.2 V
VDD1, VDD2 to DGND	−0.3 V to +2.2 V
EXT_IN1/EXT_IN2	−0.3 V to +2.2V
GPIO0/GPIO1 to DGND	−0.3 V to +2.2 V
MISO/MOSI/SCLK/$\overline{CS}$ to DGND	−0.3 V to +2.2 V
LEDx/DNC to LGND	−0.3 V to +3.6 V
SCL/SDA to DGND	−0.3 V to +3.6 V
VLEDx to LGND[1]	−0.3 V to +5.0 V
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	3000 V
Charged Device Model (CDM)	1250 V
Machine Model (MM)	100 V
Solder Reflow (Pb-Free)	
Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	<30 sec
Temperature Range	
Powered	−40°C to +85°C
Storage	−40°C to +105°C
Junction Temperature	105°C

[1] The absolute maximum voltage allowable between VLEDx and LGND is the voltage that causes the LEDx/DNC pins to reach or exceed their absolute maximum voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type[1]	Supply Pins	θ_{JA}	Unit
CE-24-1			
ASIC	VDD1, VDD2	67	°C/W
LED1	VLED1	156	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P and two thermal vias. See JEDEC JESD51.

RECOMMENDED SOLDERING PROFILE

Figure 4 and Table 8 provide details about the recommended soldering profile.

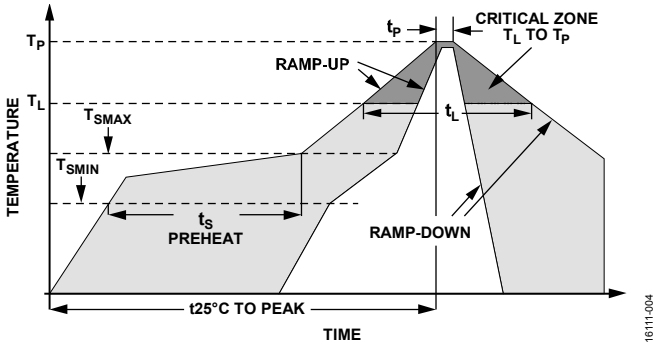

Figure 4. Recommended Soldering Profile

Table 8. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	2°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time, T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec
T_{SMAX} to T_L Ramp-Up Rate	2°C/sec max
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	3°C/sec max
Time 25°C to Peak Temperature	8 minutes max

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

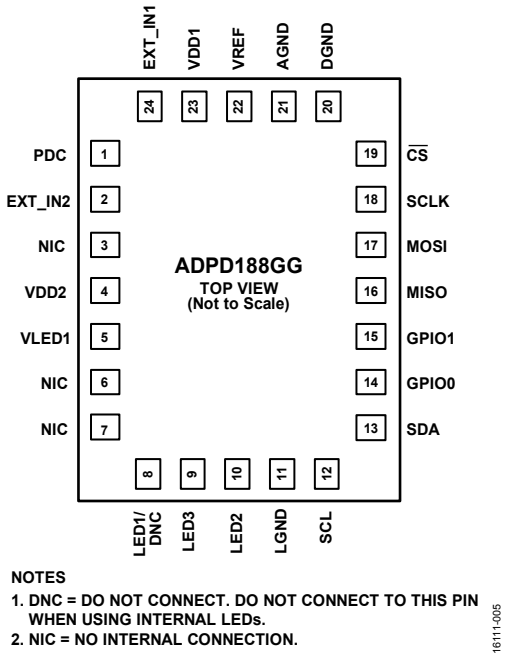

Figure 5. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	PDC	AO	Photodiode Common Cathode Bias.
2	EXT_IN2	AI	EXT_IN2 Current Input.
3	NIC	NIC	No Internal Connection. This pin is not internally connected.
4	VDD2	S	1.8 V Supply.
5	VLED1	S	Green LED Anode Supply Voltage.
6	NIC	NIC	No Internal Connection. This pin is not internally connected.
7	NIC	NIC	No Internal Connection. This pin is not internally connected.
8	LED1/DNC	AO/DNC	LED1 Driver Current Sink (LED1)/Do Not Connect (DNC). Do not connect to this pin when using internal LEDs.
9	LED3	AO	LED3 Driver Current Sink. If not in use, leave this pin floating.
10	LED2	AO	LED2 Driver Current Sink. If not in use, leave this pin floating.
11	LGND	S	LED Driver Ground.
12	SCL	DI	I^2C Clock Input.
13	SDA	DO	I^2C Data Output.
14	GPIO0	DIO	General-Purpose Input/Output 0.
15	GPIO1	DIO	General-Purpose Input/Output 1.
16	MISO	DO	SPI Master Input, Slave Output.
17	MOSI	DI	SPI Master Output, Slave Input.
18	SCLK	DI	SPI Clock Input.
19	$\overline{CS}$	DI	SPI Chip Select (Active Low).
20	DGND	S	Digital Ground.
21	AGND	S	Analog Ground.
22	VREF	REF	Internally Generated ADC Voltage Reference. Connect a 1 µF ceramic capacitor from VREF to ground.
23	VDD1	S	1.8 V Supply.
24	EXT_IN1	AI	EXT_IN1 Current Input.

[1] AO is analog output, AI is analog input, NIC is not internally connected, S is supply, DNC is do not connect, DI is digital input, DO is digital output, DIO is digital input/output, and REF is analog reference.

TYPICAL PERFORMANCE CHARACTERISTICS

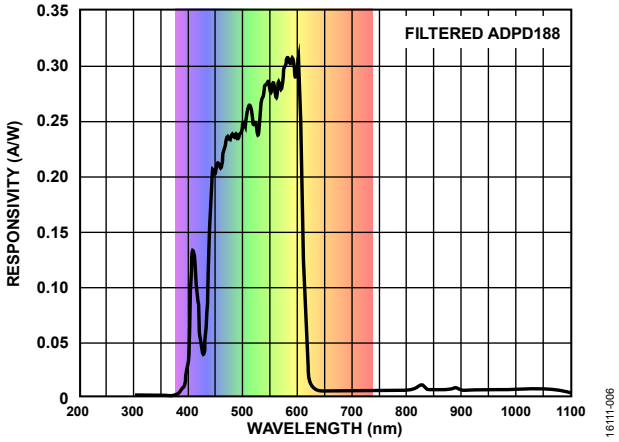

Figure 6. Typical Photodiode Responsivity

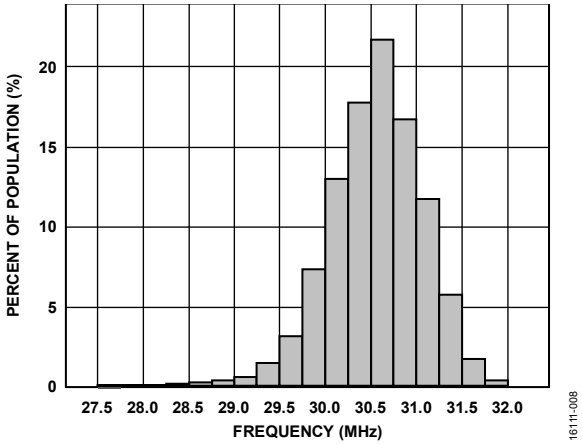

Figure 8. 32 MHz Clock Frequency Distribution; Default Settings; Before User Calibration, Register 0x4D = 0x425E

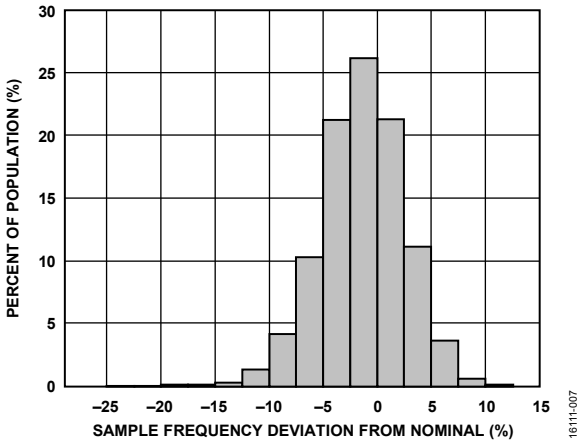

Figure 7. 32 kHz Clock Frequency Distribution; Default Settings; Before User Calibration, Register 0x4B = 0x2612

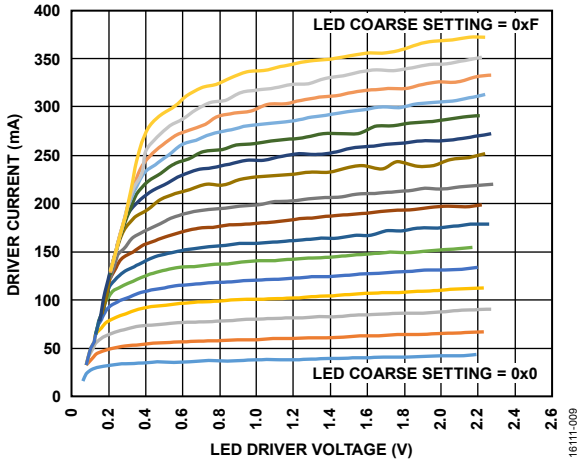

Figure 9. LED Driver Current vs. LED Driver Voltage at Various Coarse Settings

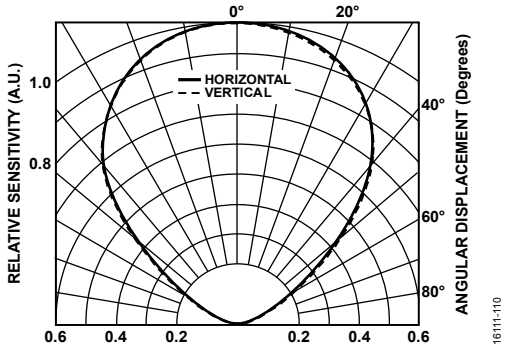

Figure 10. PD1 Relative Sensitivity vs. Angular Displacement

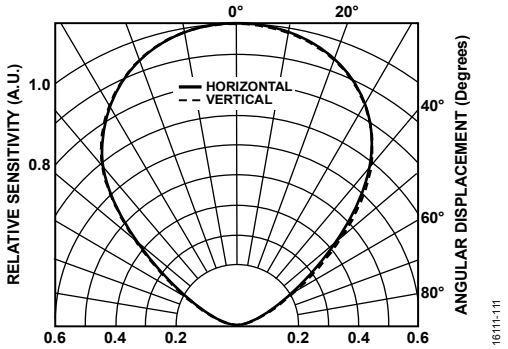

Figure 11. PD2 Relative Sensitivity vs. Angular Displacement

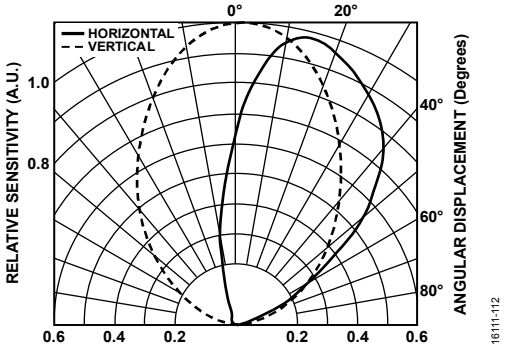

Figure 12. LED Relative Intensity vs. Angular Displacement

THEORY OF OPERATION

INTRODUCTION

The ADPD188GG is a complete, integrated, optical module designed for photoplethysmography (PPG) measurements. The module contains two optical detectors. Photodiode 1 (PDET1) has 0.4 mm^2 of active area and is connected to Channel 3 of the ASIC. Photodiode 2 (PDET2) has 0.8 mm^2 of active area and is connected to Channel 4 of the ASIC. The two photodiodes can be combined into a single detector with 1.2 mm^2 of active area. Both photo-diodes are coated with an infrared (IR) cut filter that maximizes ambient light rejection without the need for other light cancellation techniques.

The module combines the dual photodetector with two green LEDs, and a mixed-signal, photometric, front-end ASIC into a single compact device for optical measurements. The on-board ASIC includes an analog signal processing block, an ADC, a digital signal processing block, an I^{2}C and SPI communication interface, and three, independently programmable, pulsed LED current sources.

The core circuitry stimulates the LEDs and measures the corresponding optical return signals in discrete data locations. Data can be read from output registers directly or through a first in, first out (FIFO) buffer.

This highly integrated system works well in environments where ambient light is poorly controlled and the signal modulation ratio is low. As a result, the device produces high SNR for relatively low LED power.

OPTICAL COMPONENTS

Photodiode

The ADPD188GG integrates a 1.2 mm^2 deep junction photodiode. The optical sensing area is a dual detector that is connected to Channel PD3 and Channel PD4 in the ASIC. The photodiodes are accessible from Time Slot A or Time Slot B. The responsivity of the ADPD188GG photodiode is shown in Figure 6.

LEDs

The ADPD188GG module integrates two green LEDs.

Table 10. LED Dominant Wavelength

LED Color	Driver	Typical Wavelength (nm)
Green (2×)	LED1	525

In addition to the integrated LEDs, the ADPD188GG has the ability to drive external LEDs.

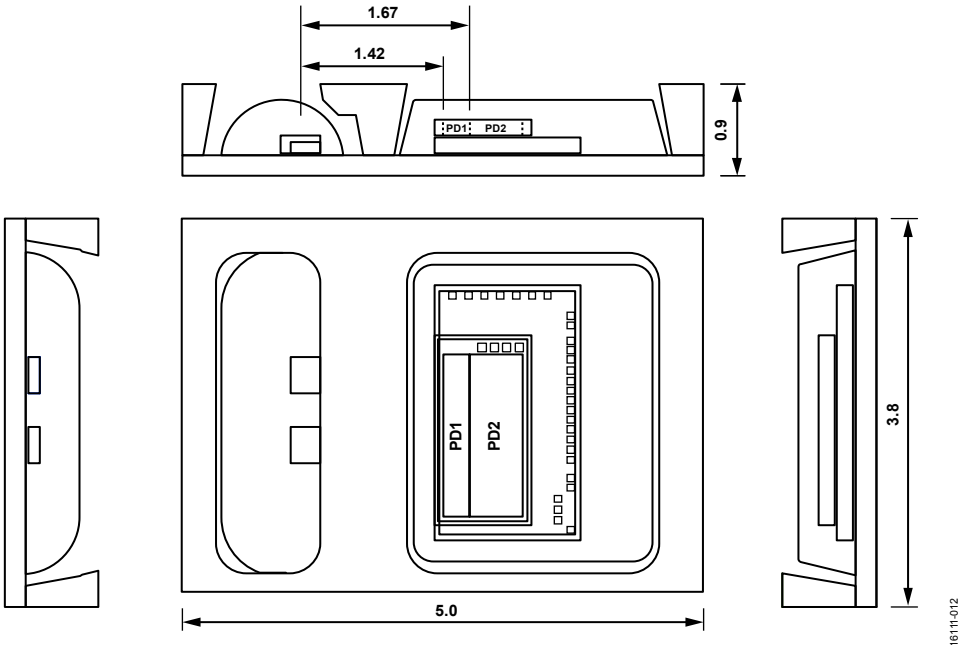

Figure 13. Optical Component Locations

DUAL TIME SLOT OPERATION

The ADPD188GG operates in two independent time slots, Time Slot A and Time Slot B, which are carried out sequentially. The entire signal path from LED stimulation to data capture and processing is executed during each time slot. Each time slot has a separate datapath that uses independent settings for the LED driver, AFE setup, and the resulting data. Time Slot A and Time Slot B operate in sequence for every sampling period, as shown in Figure 14.

The timing parameters in Figure 14 are defined as follows:

$$t_A\ (\mu s) = 25 + n_A \times 19$$

where n_A is the number of pulses for Time Slot A (Register 0x31, Bits[15:8]).

$$t_B\ (\mu s) = 25 + n_B \times 19$$

where n_B is the number of pulses for Time Slot B (Register 0x36, Bits[15:8]).

t_1 = 68 µs, the processing time for Time Slot A

t_2 = 20 µs, the processing time for Time Slot B

f_{SAMPLE} is the sampling frequency (Register 0x12, Bits[15:0]).

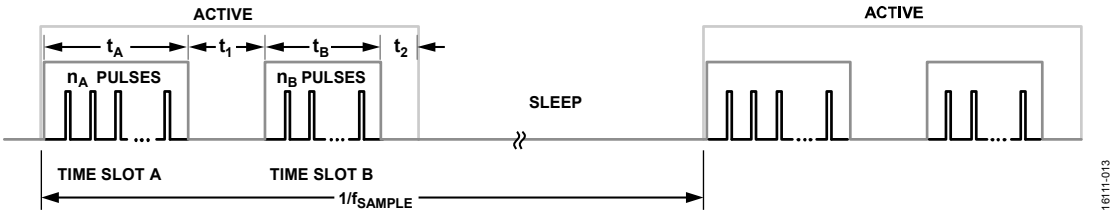

Figure 14. Time Slot Timing Diagram

Table 11. Recommended AFE and LED Timing Configuration

	Address		
Register Name	**Time Slot A**	**Time Slot B**	**Recommended Setting**
SLOTx_LEDMODE	0x30	0x35	0x0319
SLOTx_AFEMODE	0x39	0x3B	0x2209

TIME SLOT SWITCH

Multiple configurations of the four input channels are supported, depending on the settings of Register 0x14. The integrated photodiodes can either be routed to Channel 3 and Channel 4, or summed together into Channel 1. The external EXT_IN1 and EXT_IN2 inputs can be routed to Channel 1 and Channel 2, respectively, or summed into Channel 2. See Figure 15 and Figure 16 for the supported configurations. In Figure 15 and Figure 16, PDET1 is Photodiode 1, and PDET2 is Photodiode 2.

See Table 12 for the time slot switch registers. It is important to leave any unused inputs floating for proper operation of the devices. The photodiode inputs are current inputs and, as such, these pins are also considered to be voltage outputs. Tying these inputs to a voltage may saturate the analog block.

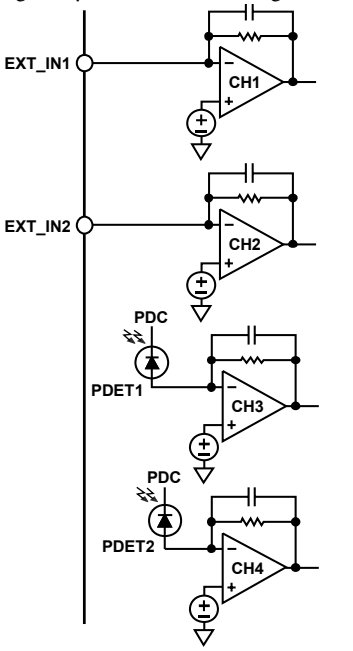

Figure 15. PD1 to PD4 Connection

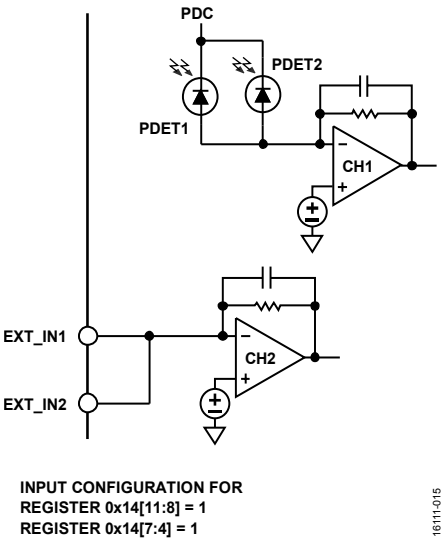

Figure 16. Current Summation

Table 12. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	These bits select the connection of input channels for Time Slot B as shown in Figure 15 and Figure 16. 0x0: inputs are floating in Time Slot B. 0x1: PDET1 and PDET2 are connected to Channel 1; EXT_IN1 and EXT_IN2 are connected to Channel 2 during Time Slot B. 0x5: EXT_IN1 is connected to Channel 1, EXT_IN2 is connected to Channel 2, PDET1 is connected to Channel 3, and PDET2 is connected to Channel 4 during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	These bits select the connection of input channels for Time Slot A as shown in Figure 15 and Figure 16. 0x0: inputs are floating in Time Slot A. 0x1: PDET1 and PDET2 are connected to Channel 1; EXT_IN1 and EXT_IN2 are connected to Channel 2 during Time Slot A. 0x5: EXT_IN1 is connected to Channel 1, EXT_IN2 is connected to Channel 2, PDET1 is connected to Channel 3, and PDET2 is connected to Channel 4 during Time Slot A. Other: reserved.

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 controls the sampling frequency setting of the ADPD188GG and Register 0x4B, Bits[5:0] further tunes this clock for greater accuracy. The sampling frequency is governed by an internal 32 kHz sample rate clock that also drives the transition of the internal state machine. The maximum sampling frequencies for some sample conditions are listed in Table 1. The maximum sample frequency for all conditions, $f_{SAMPLE,\_MAX}$, is determined by the following equation:

$$f_{SAMPLE\_MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP\_MIN})$$

where t_{SLEEP_MIN} is the minimum sleep time required between samples. See the Dual Time Slot Operation section for the definitions of t_A, t_1, t_B, and t_2.

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period and the new maximum sampling frequency is calculated as follows:

$$f_{SAMPLE,\_MAX} = 1/(t_B + t_2 + t_{SLEEP,\_MIN})$$

EXTERNAL SYNCHRONIZATION FOR SAMPLING

The ADPD188GG provides an option to use an external synchronization signal to trigger the sampling periods. This external sample synchronization signal can be provided either on the GPIO0 pin or the GPIO1 pin. This functionality is controlled by Register 0x4F, Bits[3:2]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same as when the normal sample timer provides the trigger. To enable the external synchronization signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write the appropriate value to Register 0x4F, Bits[3:2] to select whether the GPIO0 pin or the GPIO1 pin specifies when the next sample cycle occurs. Also, enable the appropriate input buffer using Register 0x4F, Bit 1, for the GPIO0 pin, or Register 0x4F, Bit 5, for the GPIO1 pin.
3. Write 0x4000 to Register 0x38.
4. Write 0x2 to Register 0x10 to start the sampling operations.
5. Apply the external synchronization signal on the selected pin at the desired rate; sampling occurs at that rate. As with normal sampling operations, read the data using the FIFO or the data registers. The maximum frequency constraints also apply in this case.

Providing an External 32 kHz Clock

The ADPD188GG has an option for the user to provide an external 32 kHz clock to the device for system synchronization or for situations where a clock with better accuracy than the internal 32 kHz clock is required. The external 32 kHz clock is provided on the GPIO1 pin only. To enable the 32 kHz external clock, use the following procedure at startup:

1. Drive the GPIO1 pin to a valid logic level or with the desired 32 kHz clock prior to enabling the GPIO1 pin as an input. Do not leave the pin floating prior to enabling it.
2. Write 0x1 to Register 0x4F, Bits[6:5] to enable the GPIO1 pin as an input.
3. Write 0x2 to Register 0x4B, Bits[8:7] to configure the devices to use an external 32 kHz clock. This setting disables the internal 32 kHz clock and enables the external 32 kHz clock.
4. Write 0x1 to Register 0x10 to enter program mode.
5. Write additional control registers in any order while the device is in program mode to configure the device as required.
6. Write 0x2 to Register 0x10 to start the normal sampling operation

STATE MACHINE OPERATION

During each time slot, the ADPD188GG operates according to a state machine. The state machine operates in the sequence shown in Figure 17.

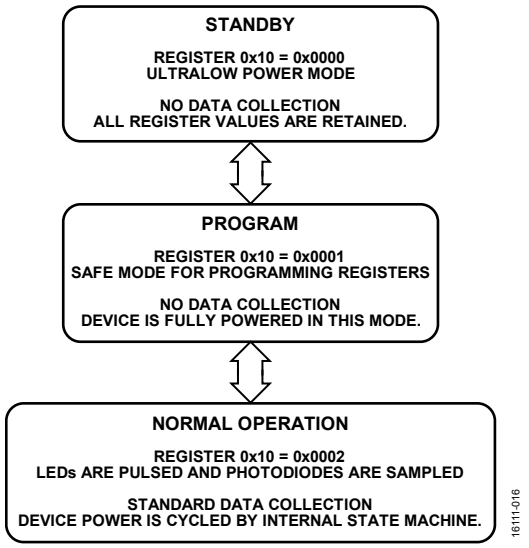

Figure 17. State Machine Operation Flowchart

The ADPD188GG operates in one of three modes: standby, program, or normal sampling mode.

Standby mode is a power saving mode in which data collection does not occur. All register values are retained in this mode. To place the device in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The device powers up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD188GG through program mode when writing registers or changing modes. Because power cycling does not occur in this mode, the device may consume higher current in program mode than in normal operation. To place the device in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation, the ADPD188GG pulses light and collects data. Power consumption in this mode depends on the pulse count and data rate. To place the device in normal sampling mode, write 0x2 to Register 0x10, Bits[1:0].

NORMAL MODE OPERATION AND DATA FLOW

In normal mode, the ADPD188GG follows a specific pattern set up by the state machine. This pattern is shown in the corresponding data flow diagram in Figure 18. The pattern, in order, is as follows:

1. LED pulse and sample. The ADPD188GG pulses external LEDs. The response of the photodiode to the reflected light is measured by the ADPD188GG. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

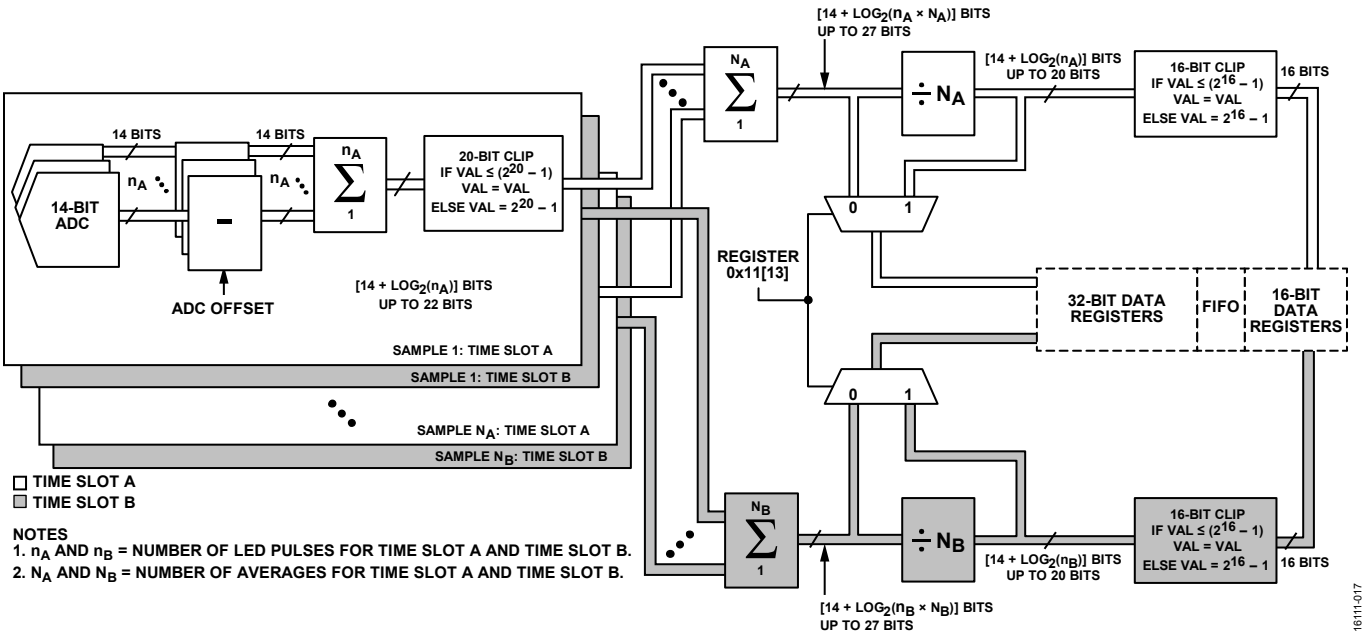

Figure 18. State Machine Operating Sequence (Datapath)

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses, as shown in Figure 19. The magnitude, duration, and number of pulses are programmable over the communications interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light that does not correspond to the LED pulse, is rejected.

After each LED pulse, the photodiode output relating to the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual sampling period. There is a 20-bit maximum range for each sampling period.

Averaging

The ADPD188GG offers sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 256 sequential pulses. As shown in Figure 18, samples acquired by the AFE are clipped to 20 bits at the output of the AFE. Additional resolution, up to 27 bits, can be achieved by averaging between sampling periods. This accumulated data of N samples is stored as 27-bit values and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration.

When using the averaging feature set up by the register, subsequent pulses can be averaged by powers of 2. The user can select from 2, 4, 8, …, up to 128 samples to be averaged. Pulse data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (see Register 0x12), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 32-bit sum is stored in the 32-bit registers. However, before sending this data to the FIFO, a divide by N operation occurs. This divide operation maintains bit depth to prevent clipping on the FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x15 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width. This setting can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADPD188GG via the communications interface, from the data registers, or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If the factors are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

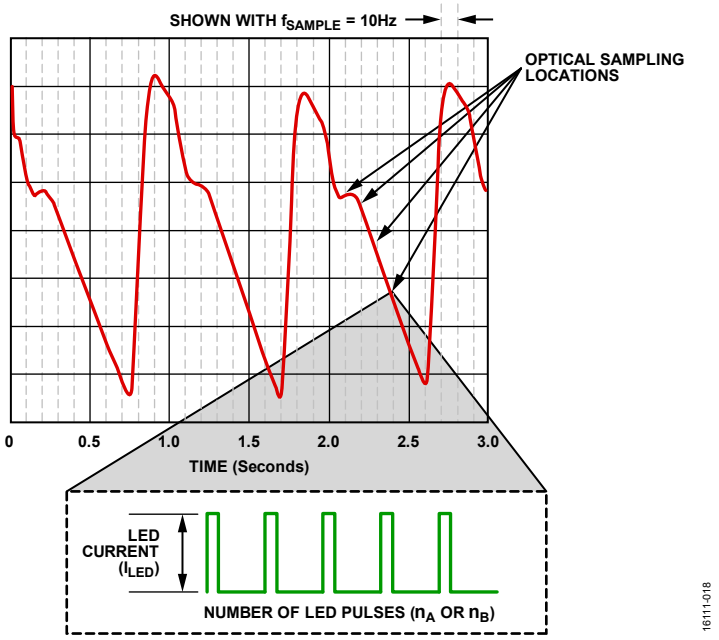

Figure 19. Example of a PPG Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

COMMUNICATIONS INTERFACE

The ADPD188GG supports both an SPI and I²C serial interface, although only one can be used at any given time in the actual application. All internal registers are accessed through the selected communications interface.

I²C INTERFACE

The ADPD188GG I²C conforms to the *UM10204 I²C-Bus Specification and User Manual, Rev. 05—9 October 2012*, available from NXP Semiconductors. The device supports fast mode (400 kbps) data transfer. Register read and write operations are supported, as shown in Figure 20. The 7-bit I²C slave address for the device is 0x64. If the I²C interface is being used, the $\overline{CS}$ pin must be pulled high to disable the SPI port.

Single-word and multiword read operations are supported. For a single register read, the host sends a no acknowledge (NACK) after the second data byte is read and a new register address is needed for each access.

For multiword operations, each pair of data bytes is followed by an acknowledge (ACK) from the host until the last byte of the last word is read. The host indicates the last read word by sending a no acknowledge. When reading from the FIFO (Register 0x60), the data is automatically advanced to the next word in the FIFO, and the space is freed. When reading from other registers, the register address is automatically advanced to the next register, allowing the user to read without readdressing each register, thereby reducing the amount of overhead required to read multiple registers. This autoincrement does not apply to the register that precedes the FIFO, Register 0x5F, or the last data register, Register 0x7E.

All register writes are single-word only and require 16 bits (one word) of data.

The software reset (Register 0x0F, Bit 0) returns an acknowledge. The device then returns to standby mode with all registers in the default state.

Table 13. Definitions of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by a master. The ADPD188GG operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high; all transactions begin with a start condition.
Start (Sr)	Repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the acknowledge (ACK) or no acknowledge (NACK) clock pulse, the SDA line is pulled low, and it remains low.
NACK	During the ACK or NACK clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

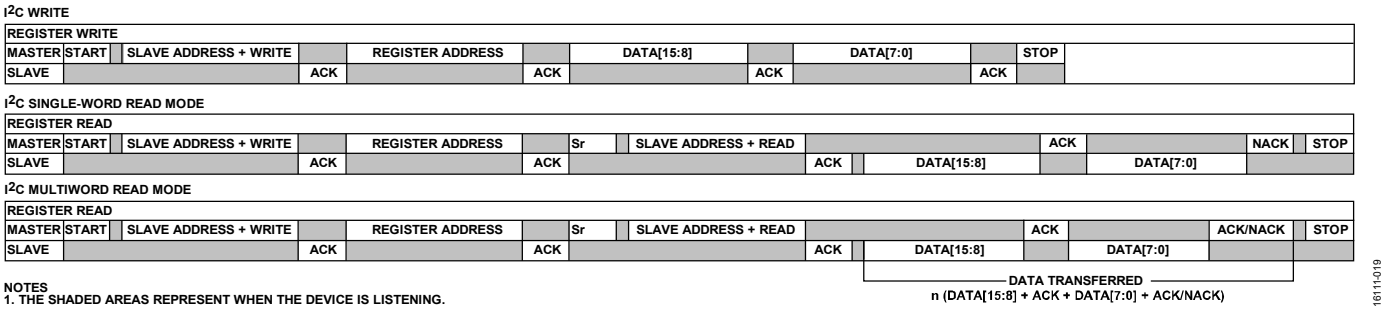

Figure 20. I²C Write and Read Operations

SPI PORT

The SPI port uses a 4-wire interface, consisting of the $\overline{CS}$, MOSI, MISO, and SCLK signals, and it is always a slave port. The $\overline{CS}$ signal goes low at the beginning of a transaction and high at the end of a transaction. The SCLK signal latches MOSI on a low to high transition. The MISO data is shifted out of the device on the falling edge of SCLK and must be clocked into a receiving device, such as a microcontroller, on the SCLK rising edge. The MOSI signal carries the serial input data, and the MISO signal carries the serial output data. The MISO signal remains three-state until a read operation is requested, which allows other SPI-compatible peripherals to share the same MISO line. All SPI transactions have the same basic format shown in Table 14. A timing diagram is shown in Figure 3. Write all data MSB first.

Table 14. Generic Control Word Sequence

Byte 0	Byte 1	Byte 2	Subsequent Bytes
Address[6:0], W/$\overline{R}$	Data[15:8]	Data[7:0]	Data[15:8], Data[7:0]

The first byte written in a SPI transaction is a 7-bit address, which is the location of the address being accessed, followed by the W/$\overline{R}$ bit. This bit determines whether the communication is a write (Logic Level 1) or a read (Logic Level 0). This format is shown in Table 15.

Table 15. SPI Address and Write/$\overline{R}$ Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
A6	A5	A4	A3	A2	A1	A0	W/$\overline{R}$

Data on the MOSI pin is captured on the rising edge of the clock, and data is propagated on the MISO pin on the falling edge of the clock. The maximum read and write speed for the SPI slave port is 10 MHz..

A sample timing diagram for a multiple word SPI write operation to a register is shown in Figure 21. A sample timing diagram of a single-word SPI read operation is shown in Figure 22. The MISO pin transitions from being three-state to being driven following the reception of a valid $\overline{R}$ bit. In this example, Byte 0 contains the address and the W/$\overline{R}$ bit, and subsequent bytes carry the data. A sample timing diagram of a multiple word SPI read operation is shown in Figure 23. In Figure 21 to Figure 23, rising edges on SCLK are indicated with an arrow, signifying that the data lines are sampled on the rising edge.

When performing multiple word reads or writes, the data address is automatically incremented to the next consecutive address for subsequent transactions except for Address 0x5F, Address 0x60 (FIFO), and Address 0x7F.

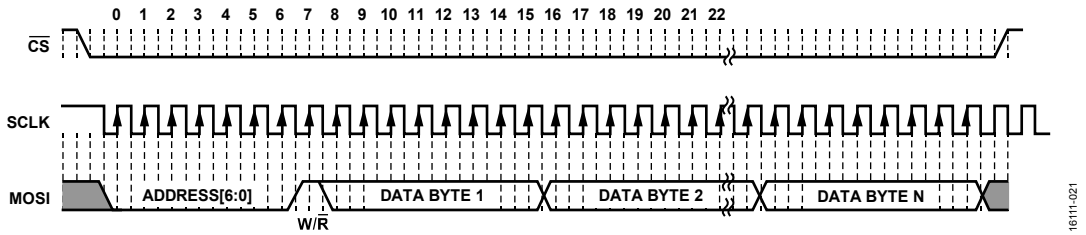

Figure 21. SPI Slave Write Clocking (Burst Write Mode, N Bytes)

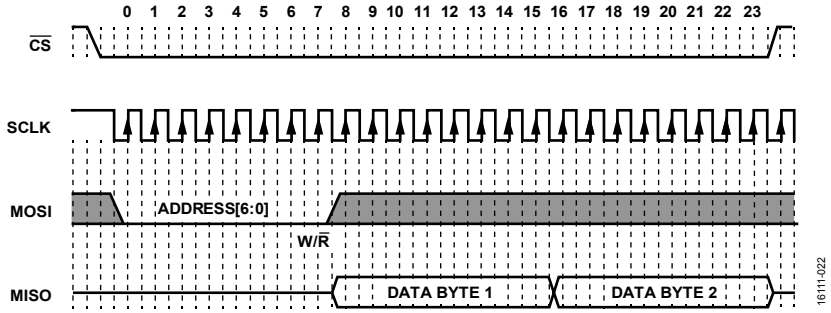

Figure 22. SPI Slave Read Clocking (Single-Word Mode, Two Bytes)

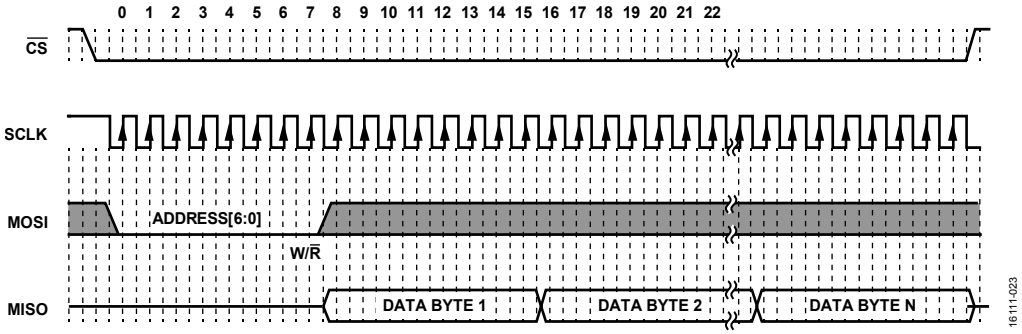

Figure 23. SPI Slave Read Clocking (Burst Read Mode, N Bytes)

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAM

Figure 24 shows the recommended connection diagram for the ADPD188GG using the SPI communications port. Figure 25 shows a circuit using the I²C port. The desired communications port, together with the GPIO0 and GPIO1 lines, connects to a system microprocessor or sensor hub. When using the SPI port, the I²C interface must be disabled by connecting the SDA and SCL pins high to 1.8 V. When using the I²C interface, the SPI is disabled by connecting $\overline{CS}$ to 1.8 V. Tie the unused inputs, SCLK and MOSI, to ground. The EXT_IN1 and EXT_IN 2 pins are current inputs and can be connected to external sensors. A voltage source can be connected to the EXT_IN1 and EXT_IN2 pins through a series resistance, effectively converting the voltage into a current (see the Using the EXT_IN 1 and EXT_IN 2 Inputs with a Voltage Source section).

Provide a regulated 1.8 V supply, tied to VDD1 and VDD2. The VLEDx level uses a standard regulator circuit according to the peak current requirements specified in Table 1 and calculated in the Calculating Current Consumption section. Place 0.1 µF ceramic decoupling capacitors as close as possible to VDD1 and VDD2; a 1.0 µF ceramic capacitor must be placed as close as possible to the VREF pin.

For best noise performance, connect AGND, DGND, and LGND together at a large conductive surface such as a ground plane, ground pour, or large ground trace.

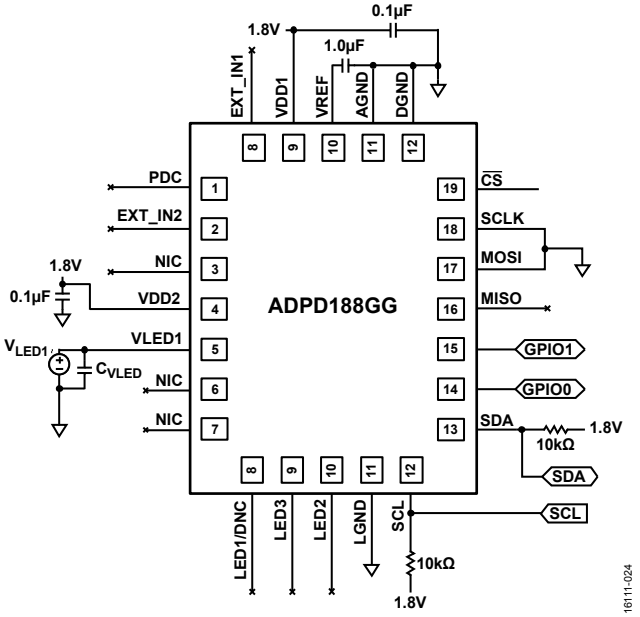

Figure 24. SPI Mode Connection Diagram

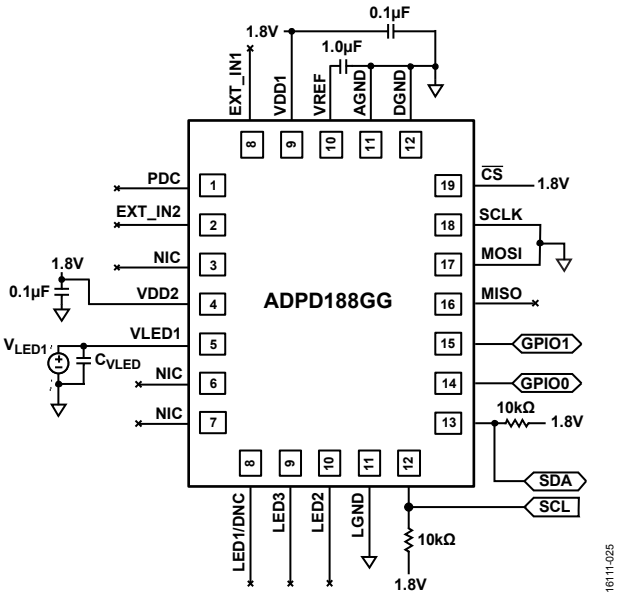

Figure 25. I²C Mode Connection Diagram

LAND PATTERN

Figure 26 shows the recommended PCB footprint (land pattern). Table 8 and Figure 4 provide the recommended soldering profile.

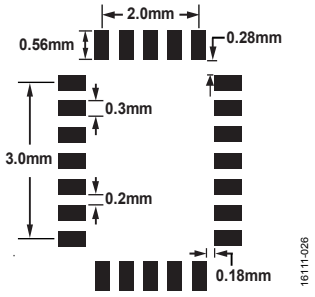

Figure 26. Land Pattern

RECOMMENDED START-UP SEQUENCE

At power-up, the device is in standby mode (Register 0x10 = 0x0), as shown in Figure 17. The ADPD188GG does not require a particular power-up sequence.

From standby mode, to begin measurement, initiate the ADPD188GG as follows:

1. Set the CLK32K_EN bit (Register 0x4B, Bit 7) to start the sample clock (32 kHz clock). This clock controls the state machine. If this clock is off, the state machine is not able to transition as defined by Register 0x10.
2. Write 0x1 to Register 0x10 to force the device into program mode. Step 1 and Step 2 can be swapped, but the actual state transition does not occur until both steps occur.
3. Write additional control registers in any order while the device is in program mode to configure the devices as required.
4. Write 0x2 to Register 0x10 to start normal sampling operation.

To terminate normal operation, follow this sequence to place the ADPD188GG in standby mode:

1. Write 0x1 to Register 0x10 to force the devices into program mode.
2. Write to the registers in any order while the devices are in program mode.
3. Write 0x00FF to Register 0x00 to clear all interrupts. If desired, clear the FIFO as well by writing 0x80FF to Register 0x00.
4. Write 0x0 to Register 0x10 to force the devices into standby mode.
5. Optionally, stop the 32 kHz clock by resetting the CLK32K_EN bit (Register 0x4B, Bit 7). Register 0x4B, Bit 7 = 0 is the only write that must be written when the device is in standby mode (Register 0x10 = 0x0). If 0 is written to this bit while in program mode or normal mode, the devices become unable to transition into any other mode, including standby mode, even if they are subsequently written to do so. As a result, the power consumption in what appears to be standby mode is greatly elevated. For this reason, and due to the very low current draw of the 32 kHz clock while in operation, it is recommended from an ease of use perspective to keep the 32 kHz clock running after it is turned on.

READING DATA

The ADPD188GG provides multiple methods for accessing the sample data. Each time slot can be independently configured to provide data access using the FIFO or the data registers. Interrupt signaling is also available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADPD188GG includes a 128-byte FIFO memory buffer that can be configured to store data from either or both time slots. Register 0x11 selects the type of data from each time slot to be written to the FIFO. Note that both time slots can be enabled to use the FIFO, but only if their output data rate is the same.

$$Output\ Data\ Rate = f_{SAMPLE}/Nx$$

where:
f_{SAMPLE} is the sampling frequency.
Nx is the averaging factor for each time slot (N_A for Time Slot A and N_B for Time Slot B). In other words, $N_A = N_B$ must be true to store data from both time slots in the FIFO.

Data packets are written to the FIFO at the output data rate. A data packet for the FIFO consists of a complete sample for each enabled time slot. Data for each photodiode channel can be stored as either 16 or 32 bits. Each time slot can store 2, 4, 8, or 16 bytes of data per sample, depending on the mode and data format. To ensure that data packets are intact, new data is only written to the FIFO if there is sufficient space for a complete packet. Any new data that arrives when there is not enough space is lost. The FIFO continues to store data when sufficient space exists. Always read FIFO data in complete packets to ensure that data packets remain intact.

The number of bytes currently stored in the FIFO is available in Register 0x00, Bits[15:8]. A dedicated FIFO interrupt is also available and automatically generates when a specified amount of data is written to the FIFO.

Interrupt-Based Method

To read data from the FIFO using an interrupt-based method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write Register 0x11 with the desired data format for each time slot.
3. Set FIFO_THRESH in Register 0x06, Bits[13:8] to the interrupt threshold. A recommended value for this is the number of 16-bit words in a data packet, minus 1. This causes an interrupt to generate when there is at least one complete packet in the FIFO.
4. Enable the FIFO interrupt by writing a 0 to the FIFO_INT_MASK in Register 0x01, Bit 8. Also, configure the interrupt pin (GPIO0) by writing the appropriate value to the bits in Register 0x02.
5. Enter normal operation mode by setting Register 0x10 to 0x2.
6. When an interrupt occurs,
   a. There is no requirement to read the FIFO_SAMPLES bits, because the interrupt is generated only if there is one or more full packets. Optionally, the interrupt routine can check for the presence of more than one available packet by reading these bits.
   b. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.

The FIFO interrupt automatically clears immediately upon reading any data from the FIFO and is set again only when the FIFO is written and the number of words is above the threshold.

Polling Method

To read data from the FIFO in a polling method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write Register 0x11 with the desired data format for each time slot.
3. Enter normal operation mode by setting Register 0x10 to 2.

Next, begin the polling operations.

1. Wait for the polling interval to expire.
2. Read the FIFO_SAMPLES bits (Register 0x00, Bits[15:8]).
3. If FIFO_SAMPLES ≥ the packet size, read a packet using the following steps:
   a. Read a complete packet using one or more multiword accesses via Register 0x60. Reading the FIFO automatically frees the space for new samples.
   b. Repeat Step 1.

When a mode change is required, or any other disruption to normal sampling is necessary, the FIFO must be cleared. Use the following procedure to clear the state and empty the FIFO:

1. Enter program mode by setting Register 0x10 to 0x1.
2. Write 1 to Register 0x00, Bit 15.

Reading Data from Registers Using Interrupts

The latest sample data is always available in the data registers and is updated simultaneously at the end of each time slot. The data value for each photodiode channel is available as a 16-bit value in Register 0x64 through Register 0x67 for Time Slot A, and Register 0x68 through Register 0x6B for Time Slot B. If allowed to reach their maximum value, Register 0x64 through Register 0x6B clip. If Register 0x64 through Register 0x6B saturate, the unsaturated (up to 27 bits) values for each channel are available in Register 0x70 through Register 0x77 for Time Slot A and Register 0x78 through Register 0x7F for Time Slot B. Sample interrupts are available to indicate when the registers are updated and can be read. To use the interrupt for a given time slot, use the following procedure:

1. Enable the sample interrupt by writing a 0 to the appropriate bit in Register 0x01. To enable the interrupt for Time Slot A, write 0 to Bit 5. To enable the interrupt for Time Slot B, write 0 to Bit 6. Either or both interrupts can be set.
2. Configure the interrupt pin (GPIOx) by writing the appropriate value to the bits in Register 0x02.
3. An interrupt generates when the data registers are updated.
4. The interrupt handler must perform the following:
   a. Read Register 0x00 and observe Bit 5 or Bit 6 to confirm which interrupt has occurred. This step is not required if only one interrupt is in use.
   b. Read the data registers before the next sample can be written. The system must have interrupt latency and service time short enough to respond before the next data update, based on the output data rate.
   c. Write a 1 to Bit 5 or Bit 6 in Register 0x00 to clear the interrupt.

If both time slots are in use, it is possible to use only the Time Slot B interrupt to signal when all registers can be read. It is recommended to use the multiword read to transfer the data from the data registers.

Reading Data from Registers Without Interrupts

If the system interrupt response is not fast or predictable enough to use the interrupt method, or if the interrupt pin (GPIOx) is not used, it is possible to obtain reliable data access by using the data hold mechanism. To guarantee that the data read from the registers is from the same sample time, it is necessary to prevent the update of samples while reading the current values. The method for doing register reads without interrupt timing is as follows:

1. Write a 1 to SLOTA_DATA_HOLD or SLOTB_DATA_HOLD (Register 0x5F, Bit 1 and Bit 2, respectively) for the time slot requiring access (both time slots can be accessed). This setting prevents sample updates.
2. Read the registers as desired.
3. Write a 0 to the SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits (Register 0x5F, Bit 1 and Bit 2, respectively) previously set. Sample updates are allowed again.

Because a new sample may arrive while the reads are occurring, this method prevents the new sample from partially overwriting the data being read.

CLOCKS AND TIMING CALIBRATION

The ADPD188GG operates using two internal time bases. A 32 kHz clock sets the sample timing, and a 32 MHz clock controls the timing of internal functions such as LED pulsing and data capture. Both clocks are internally generated and exhibit device to device variation of approximately 10% (typical).

Heart rate monitoring (HRM) applications require an accurate time base to achieve an accurate count of beats per minute. The ADPD188GG provides a simple calibration procedure for both clocks.

Calibrating the 32 kHz Clock

This procedure calibrates items associated with the output data rate. Calibration of this clock is important for items where an accurate data rate is important, such as heart rate measurements.

To calibrate the 32 kHz clock,

1. Set the sampling frequency to the highest the system can handle, such as 2000 Hz. Because the 32 kHz clock controls sample timing, its frequency is readily accessible via the GPIO0 pin. Configure the interrupt by writing the appropriate value to Bits[2:0] in Register 0x02 and set the interrupt to occur at the sampling frequency by writing 0x0 to Register 0x01, Bit 5 or Bit 6. Monitor the GPIO0 pin. The interrupt frequency must match the set sample frequency.

2. If the monitored interrupt frequency is less than the set sampling frequency, increase the CLK32K_ADJUST bits (Register 0x4B, Bits[5:0]). If the monitored interrupt frequency is larger than the set sampling frequency, decrease the CLK32K_ADJUST bits.
3. Repeat Step 1 until the monitored interrupt signal frequency is close to the set sampling frequency.

Calibrating the 32 MHz Clock

This procedure calibrates items associated with the fine timing within a sample period, such as LED pulse width and spacing, and assumes that the 32 kHz clock is already calibrated.

To calibrate the 32 MHz clock,

1. Write 0x1 to Register 0x5F, Bit 0.
2. Enable the CLK_RATIO calculation by writing 0x1 to Register 0x50, Bit 5 (CLK32M_CAL_EN). This function counts the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. With this function enabled, this value is stored in Register 0x0A, Bits[11:0] and nominally this ratio is 2000 (0x07D0).
3. Calculate the 32 MHz clock error as follows:
   Clock Error = 32 MHz × (1 − *CLK_RATIO*/2000)
4. Adjust the frequency by setting Bits[7:0] in Register 0x4D per the following equation:
   CLK32M_ADJUST = *Clock Error*/109 kHz
5. Write 0x0 to Register 0x50, Bit 5 to reset the CLK_RATIO function.
6. Repeat Step 1 through Step 5 until the desired accuracy is achieved.
7. Write 0x1 to Register 0x5F, Bit 0, and set the GPIO0 pin back to the mode desired for normal operation.

OPTIONAL TIMING SIGNALS AVAILABLE ON GPIO0 AND GPIO1

The ADPD188GG provides a number of different timing signals, available via the GPIO0 and GPIO1 pins, to enable ease of system synchronization and flexible triggering options. Each GPIOx pin can be configured as an open-drain output if they are sharing the bus with other drivers, or they can be configured to always drive the bus. Both outputs also have polarity control in situations where a timing signal must be inverted from the default.

Table 16. GPIOx Control Settings

Pin Name	Register, Bits	Setting Description
GPIO0	0x02, Bit 0	0: polarity active high 1: polarity active low
	0x02, Bit 1	0: always drives the bus 1: drives the bus when asserted
	0x02, Bit 2	0: disables the GPIO0 pin drive 1: enables the GPIO0 pin drive
GPIO1	0x02, Bit 8	0: polarity active high 1: polarity active low
	0x02, Bit 9	0: always drives the bus 1: drives the bus when asserted
	0x4F, Bit 6	0: disables the GPIO1 pin drive 1: enables the GPIO1 pin drive

The various available timing signals are controlled by the settings in Register 0x0B, Bits[12:8] of this register control the timing signals available on GPIO1, and Bits[4:0] control the timing signals available on GPIO0. All of the timing signals described in this data sheet are available on either (or both) of the GPIO0 and GPIO1 pins. Timing diagrams are shown in Figure 27 and Figure 28. The time slot settings used to generate the timing diagrams are described in Table 17.

Table 17. ADPD188GG Settings Used for the Timing Diagrams Shown in Figure 27 and Figure 28

Register	Setting	Description
0x31	0x0118	Time Slot A: 1 LED pulse
0x36	0x0418	Time Slot B: 4 LED pulses
0x15	0x0120	Time Slot A decimation = 4, Time Slot B decimation = 2

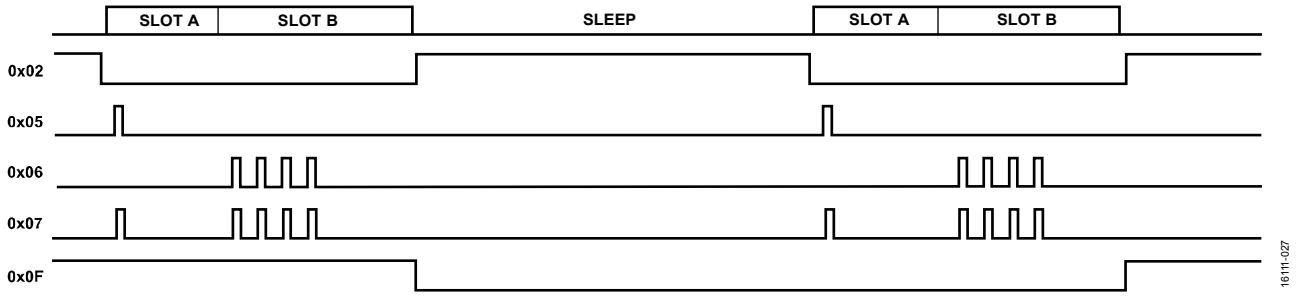

Figure 27. Optional Timing Signals Available on GPIOx—Register 0x0B, Bits[12:8] or Bits[4:0] = 0x02, 0x05, 0x06, 0x07, and 0x0F