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1100 MHz Variable Gain Amplifiers and Baseband Programmable Filters

Data Sheet

ADRF6518

FEATURES

- Matched pair of programmable filters and triple VGAs
- Continuous gain control range: 72 dB
- Digital gain control: 30 dB
- Filter bypass mode bandwidth (BW)
  - ±1 dB gain flatness: 300 MHz
  - −3 dB small signal bandwidth: 650 MHz/1100 MHz, VGA2 and VGA3 21 dB/12 dB, respectively
- 6-pole Butterworth filter: 1 MHz to 63 MHz
  - in 1 MHz steps, 0.5 dB corner frequency
- Peak detector
- IMD3: >65 dBc for 1.5 V p-p composite output
- HD2, HD3: >65 dBc for 1.5 V p-p output
- Differential input and output
- Flexible output and input common-mode ranges
- Optional dc output offset correction
- SPI programmable filter corners and gain steps
- Single 3.3 V supply operation with power-down feature

APPLICATIONS

- Point-to-point and point-to-multipoint radios
- Baseband IQ receivers
- Diversity receivers
- ADC drivers
- Instrumentation
- Medical

FUNCTIONAL BLOCK DIAGRAM

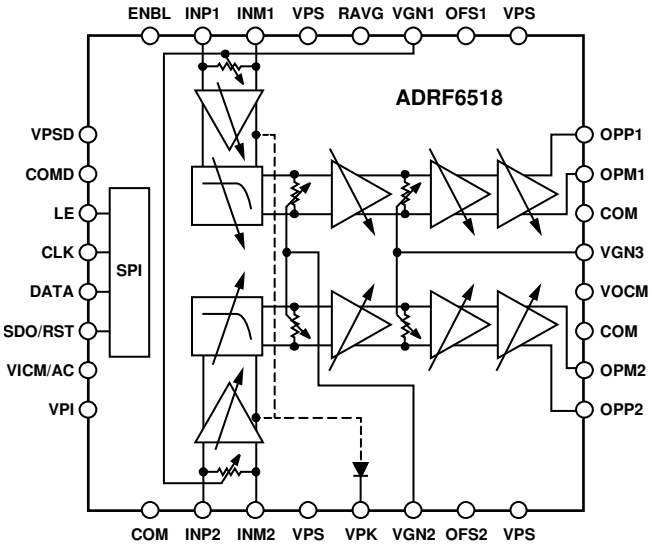

Figure 1

GENERAL DESCRIPTION

The ADRF6518 is a matched pair of fully differential low noise and low distortion programmable filters and variable gain amplifiers (VGAs). Each channel is capable of rejecting large out-of-band interferers while reliably boosting the wanted signal, thus reducing the bandwidth and resolution requirements on the analog-to-digital converters (ADCs). The excellent matching between channels and their high spurious-free dynamic range over all gain and bandwidth settings make the ADRF6518 ideal for quadrature-based (IQ) communication systems with dense constellations, multiple carriers, and nearby interferers. The various amplifier gains, filter corners and other features are all programmable via a serial port interface (SPI) port.

The first VGA that precedes the filters offers 24 dB of continuous gain control with fixed gain options of 9 dB, 12 dB, and 15 dB, and sets a differential input impedance of 400 Ω. The filters provide a six-pole Butterworth response with 0.5 dB corner frequencies from 1 MHz to 63 MHz in 1 MHz steps. For operation beyond 63 MHz, the filter can be disabled and completely bypassed, thereby extending the −3 dB BW up to 1100 MHz. A wideband peak detector is available to monitor the peak signal at the filter inputs. The pair of VGAs that follow the filters each provides 24 dB of continuous gain control with fixed gain options of 12 dB, 15 dB, 18 dB, and 21 dB. The output buffers offer an additional option of 3 dB or 9 dB gain and provide a differential output impedance of less than 10 Ω. They are capable of driving 1.5 V p-p into 400 Ω loads at better than 65 dBc HD3. The output common-mode voltage defaults to VPS/2 and can be adjusted down to 900 mV via the VOCM pin. Independent, built-in dc offset correction loops for each channel can be disabled via the SPI if fully dc-coupled operation is desired. The high-pass corner frequency is determined by external capacitors on the OFS1 and OFS2 pins and the postfilter VGA gain.

The ADRF6518 operates from a 3.15 V to 3.45 V supply and consumes a maximum supply current of 400 mA. When fully disabled, it consumes <1 mA. The ADRF6518 is fabricated in an advanced silicon-germanium BiCMOS process and is available in a 32-lead, exposed pad LFCSP. Performance is specified over the −40°C to +85°C temperature range.

Rev. 0 Document Feedback

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Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6518 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6518: 1100 MHz Variable Gain Amplifiers and Baseband Programmable Filters Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADRF6518 Evaluation Software
- Windows 7 Drivers for the SPI Software

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADRF6518 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6518 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

6/13—Revision 0: Initial Version

SPECIFICATIONS

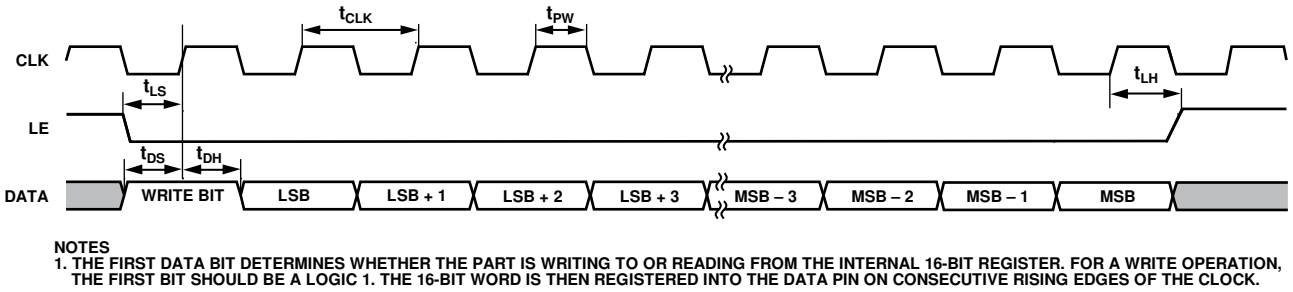
VPS, VPI, VPSD = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, power mode bit (B9) = 0 (low power mode), digital gain code bits (B8 to B2) = 0000001, and dc offset disable bit (B1) = 0 (enabled), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RESPONSE, FILTER BYPASS MODE					
±1 dB Gain Flatness Bandwidth			300		MHz
−3 dB Small Signal Bandwidth	VGA2 and VGA3 21 dB digital gain setting		650		MHz
	VGA2 and VGA3 12 dB digital gain setting		1100		MHz
FREQUENCY RESPONSE					
Low-Pass Corner Frequency, f_C	Six-pole Butterworth filter, 0.5 dB bandwidth	1		63	MHz
Step Size			1		MHz
Corner Frequency Absolute Accuracy	Over operating temperature range		±8		% f_C
Corner Frequency Matching	Channel A and Channel B at same gain and bandwidth settings		±0.5		% f_C
Pass-Band Ripple			0.5		dB p-p
Gain Matching	Channel A and Channel B at same gain and bandwidth settings		±0.1		dB
Group Delay Variation	From midband to peak				
Corner Frequency = 1 MHz			135		ns
Corner Frequency = 30 MHz			11		ns
Group Delay Matching	Channel A and Channel B at same gain				
Corner Frequency = 1 MHz			5		ns
Corner Frequency = 30 MHz			0.2		ns
Stop-Band Rejection					
Relative to Pass Band	2 × f_C		30		dB
	5 × f_C		75		dB
INPUT STAGE	INP1, INM1, INP2, INM2, VICM/AC				
Maximum Input Swing	At minimum gain, VGN1 = 0 V		5.0		V p-p
Differential Input Impedance			400		Ω
Input Common-Mode Range, DC-Coupled Mode	1.5 V p-p input voltage, HD3 > 65 dBc (VPI = 3.3 V), VICM/AC floating or logic high	1.35		1.95	V
	1.5 V p-p input voltage, HD3 > 65 dBc (VPI = 5.0 V), VICM/AC floating or logic high	1.35		3.1	V
Input Common-Mode, AC-Coupled Mode	VPI = 3.3 V to 5.0 V, VICM/AC = 0 V		VPS/2		V
VICM/AC Input Impedance			7.75		kΩ
PEAK DETECTOR	VPK, RAVG, SDO/RST				
Output Scaling	Relative to peak voltage at filter input		1		V/V peak
Reset Threshold	Logic high duration > 25 ns		>2.0		V
GAIN CONTROL	VGN1, VGN2, VGN3				
Gain Range	Maximum digital gains	−6		+66	dB
	Minimum digital gains	−36		+36	dB
Voltage Attenuation Range	Each attenuator; V_{GAIN} from 0 V to 1 V	−24		0	dB
Gain Slope			30		mV/dB
Gain Error	V_{GAIN} from 300 mV to 800 mV		0.2		dB
OUTPUT STAGE	OPP1, OPM1, OPP2, OPM2, VOCM				
Maximum Output Swing	At maximum gain, R_{LOAD} = 400 Ω		3		V p-p
	HD2 > 65 dBc, HD3 > 65 dBc, R_{LOAD} = 400 Ω		1.5		V p-p
Differential Output Impedance			<10		Ω
Output DC Offset	Inputs shorted, offset loop enabled		<20		mV
Output Common-Mode Range	1.5 V p-p output voltage	0.9		VPS − 1.2	V
	VOCM left floating		VPS/2		V
VOCM Input Impedance			23		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE/DISTORTION					
Corner Frequency = 63 MHz					
Output Noise Density	Minimum gain at $f_C/2$		−104.6		dBV/Hz
	Maximum gain at $f_C/2$		−104.3		dBV/Hz
Second Harmonic, HD2	16 MHz fundamental, 1.5 V p-p Output Level				
	Gain = 6 dB		65		dBc
	Gain = 54 dB		65		dBc
Third Harmonic, HD3	16 MHz fundamental, 1.5 V p-p Output Level				
	Gain = 6 dB		82		dBc
	Gain = 54 dB		81		dBc
IMD3	30 MHz and 31 MHz tones, 1.5 V p-p output level				
	Gain = 0 dB		60		dBc
	Gain = 30 dB		80		dBc
	Gain = 60 dB		80		dBc
DIGITAL LOGIC	LE, CLK, DATA, SDO				
Input High Voltage, V_{HIGH}			>2		V
Input Low Voltage, V_{LOW}			<0.8		V
Input Current, I_{HIGH}/I_{LOW}			<1		µA
Input Capacitance, C_{IN}			2		pF
SPI TIMING	LE, CLK, DATA, SDO				
f_{CLK}	$1/t_{CLK}$		20		MHz
t_{DH}	DATA hold time		5		ns
t_{DS}	DATA setup time		5		ns
t_{LH}	LE hold time		5		ns
t_{LS}	LE setup time		5		ns
t_{PW}	CLK high pulse width		5		ns
t_D	CLK to SDO delay		5		ns
POWER AND ENABLE	VPS, VPSD, COM, COMD, ENBL				
Supply Voltage Range		3.15	3.3	3.45	V
Total Supply Current	ENBL = 3.3 V				
	Maximum BW setting, high power filter		400		mA
	Minimum BW setting, low power filter		360		mA
	Filter bypassed, high power mode		260		mA
	Filter bypassed, low power mode		230		mA
Disable Current	ENBL = 0 V, with pull-down resistors on output		1		mA
Disable Threshold			1.6		V
Enable Response Time	Delay following ENBL low-to-high transition		20		µs
Disable Response Time	Delay following ENBL high-to-low transition		300		ns

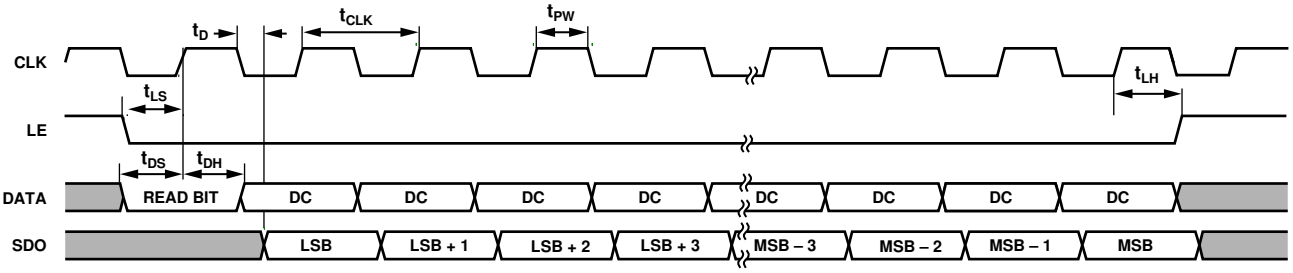
TIMING DIAGRAMS



NOTES
1. THE FIRST DATA BIT DETERMINES WHETHER THE PART IS WRITING TO OR READING FROM THE INTERNAL 16-BIT REGISTER. FOR A WRITE OPERATION, THE FIRST BIT SHOULD BE A LOGIC 1. THE 16-BIT WORD IS THEN REGISTERED INTO THE DATA PIN ON CONSECUTIVE RISING EDGES OF THE CLOCK.

11449-002

Figure 2. Write Mode Timing Diagram



NOTES
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11449-003

Figure 3. Read Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages, VPS, VPSD	3.45 V
VPI	5.25 V
ENBL, LE, CLK, DATA, SDO	VPSD + 0.5 V
INP1, INM1, INP2, INM2, VICM	VPS + 0.5 V
OPP1, OPM1, OPP2, OPM2, VOCM	VPS + 0.5 V
OFS1, OFS2, VPK, RAVG	VPS + 0.5 V
VGN1, VGN2, VGN3	VPS + 0.5 V
Internal Power Dissipation	1.25 W
θ_{JA} (Exposed Pad Soldered to Board)	37.4°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

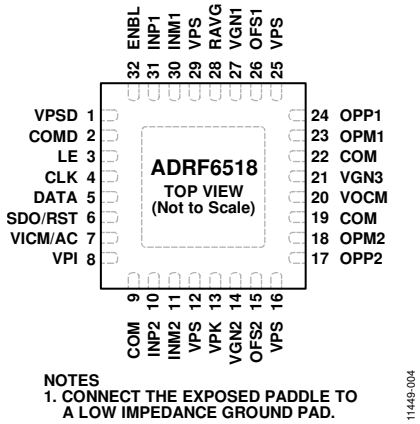

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPSD	Digital Positive Supply Voltage: 3.15 V to 3.45 V.
2	COMD	Digital Common. Connect this pin to an external circuit common using the lowest possible impedance.
3	LE	Latch Enable. SPI programming pin. TTL levels: V_{LOW} < 0.8 V, V_{HIGH} > 2 V.
4	CLK	SPI Port Clock. TTL levels: V_{LOW} < 0.8 V, V_{HIGH} > 2 V.
5	DATA	SPI Data Input. TTL levels: V_{LOW} < 0.8 V, V_{HIGH} > 2 V.
6	SDO/RST	SPI Data Output (SDO). TTL levels: V_{LOW} < 0.8 V, V_{HIGH} > 2 V. Peak Detector Reset (RST). A >25 ns high pulse is required on this pin to reset the detector.
7	VICM/AC	Input Common-Mode Reference (VICM). VPI/2 reference output for optimal common-mode level to drive the differential inputs. If this pin is used as a common-mode reference for the common-mode output of the previous stage, only connect high impedance nodes to this pin. AC Coupling/Internal Bias Activation (AC). Pull this pin low for ac coupling of the inputs.
8	VPI	Input Stage Supply Voltage: 3.15 V to 5.25 V. Connect VPI to VPS if the input common-mode range is narrow (1.35 V to 1.95 V). Connect VPI to 5 V if a common-mode input up to 3.1 V is desired.
9, 19, 22	COM	Analog Common. Connect COM to an external circuit common using the lowest possible impedance.
10, 11, 30, 31	INP2, INM2, INM1, INP1	Differential Inputs, 400 Ω Differential Input Impedance.
12, 16, 25, 29	VPS	Analog Positive Supply Voltage: 3.15 V to 3.45 V.
13	VPK	Peak Detector Output. Scaling of 1 V/V peak differential at filter inputs is performed, and the bigger peak of two channels is reported.
14, 21, 27	VGN2, VGN3, VGN1	VGA1, VGA2, and VGA3 Analog Gain Control. 0 V to 1 V, 30 mV/dB gain scaling.
15, 26	OFS2, OFS1	Offset Correction Loop Compensation Capacitors. Connect capacitors to a circuit common.
17, 18, 23, 24	OPP2, OPM2, OPM1, OPP1	Differential Outputs. These outputs have a <10 Ω output impedance. Common-mode range is 0.9 V to VPS − 1.2 V; default is VPS/2.
20	VOCM	Output Common-Mode Setpoint. VOCM defaults to VPS/2 if left open.
28	RAVG	Peak Detector Time-Constant Resistor. Connect this pin to VPS. Leave this pin open for the longest hold time. The RAVG range is ∞ to 1 kΩ.
32	ENBL	Chip Enable. Pull this pin high to enable the chip.
	EP	Exposed Ground Pad. Connect the exposed pad to a low impedance ground pad.

TYPICAL PERFORMANCE CHARACTERISTICS

FILTER MODE

VPS, VPI, VPSD = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, power mode bit (B9) = 0 (low power mode), digital gain code bits (B8 to B2) = 1111110, dc offset disable bit (B1) = 0 (enabled), filter corner = 63 MHz, ac coupling mode, fundamental at 31 MHz, unless otherwise noted. For HD2/HD3 vs. gain plots: 1.5 V p-p output target level, and reference Figure 67 for analog gain distribution.

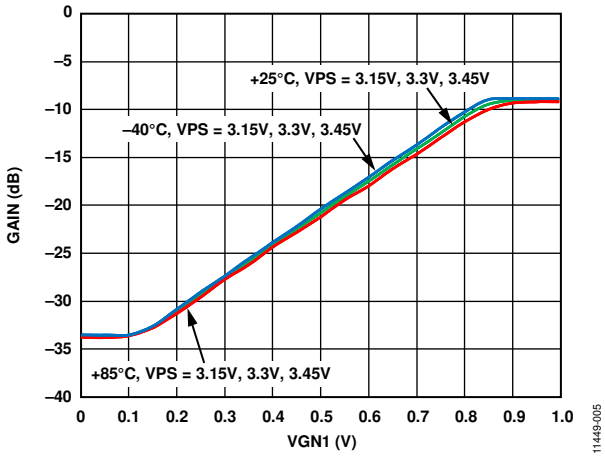

Figure 5. In-Band Gain vs. VGN1 over Supply and Temperature

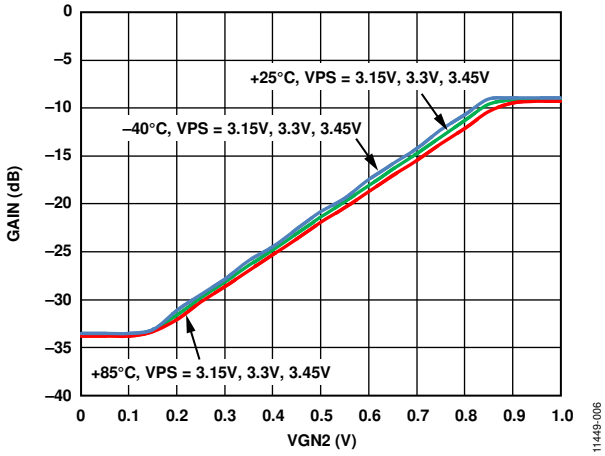

Figure 6. In-Band Gain vs. VGN2 over Supply and Temperature

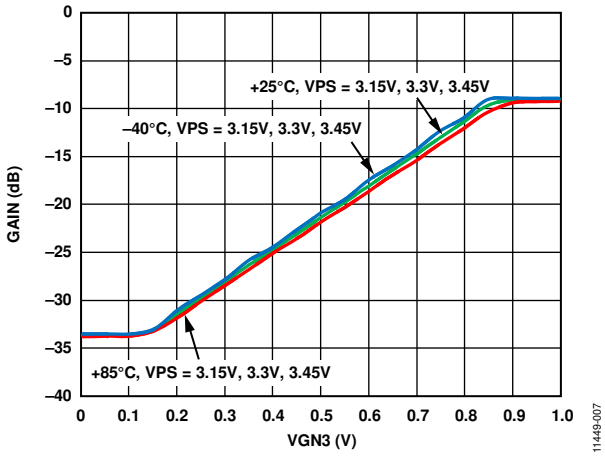

Figure 7. In-Band Gain vs. VGN3 over Supply and Temperature

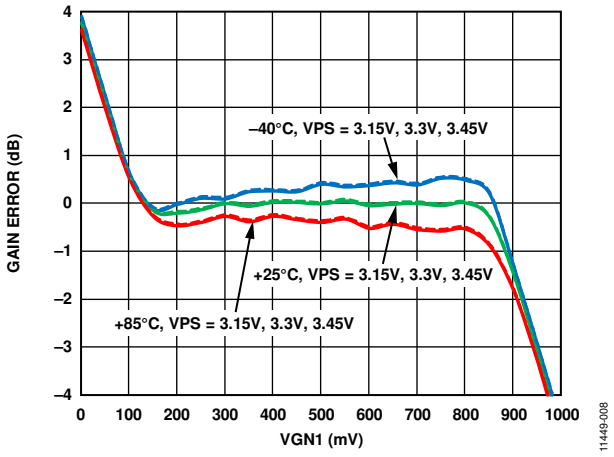

Figure 8. Gain Error vs. VGN1 over Supply and Temperature

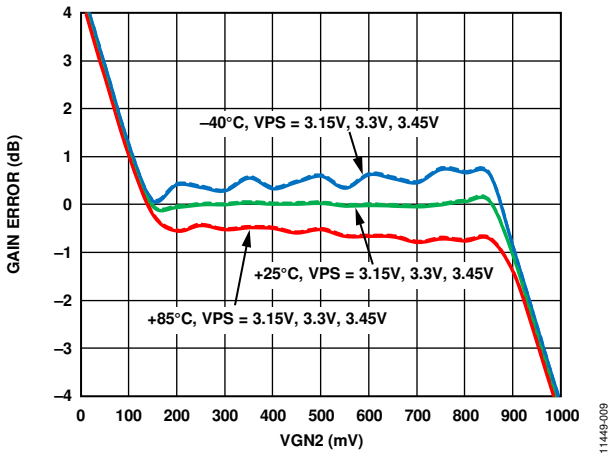

Figure 9. Gain Error vs. VGN2 over Supply and Temperature

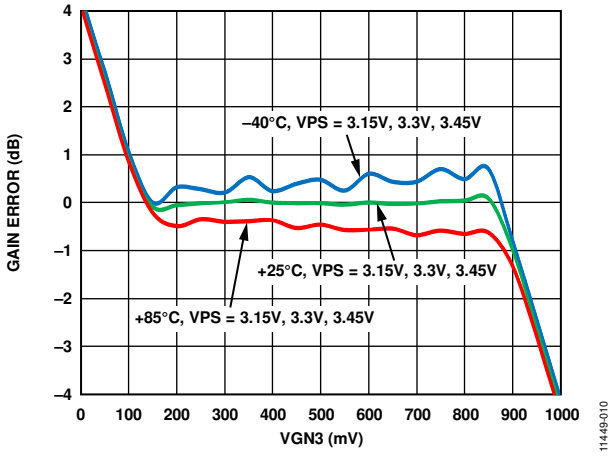

Figure 10. Gain Error vs. VGN3 over Supply and Temperature

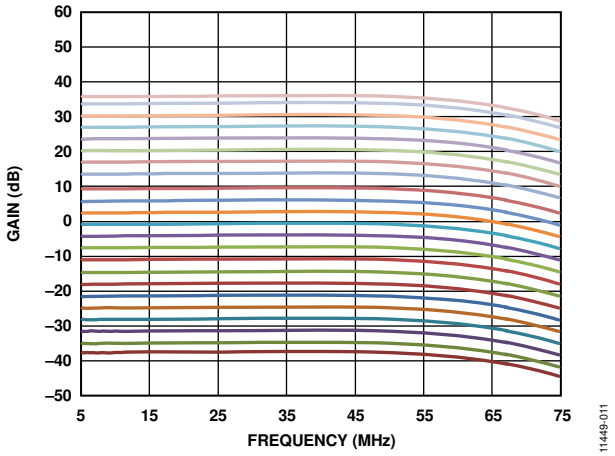

Figure 11. Gain vs. Frequency over VGN1/VGN2/VGN3

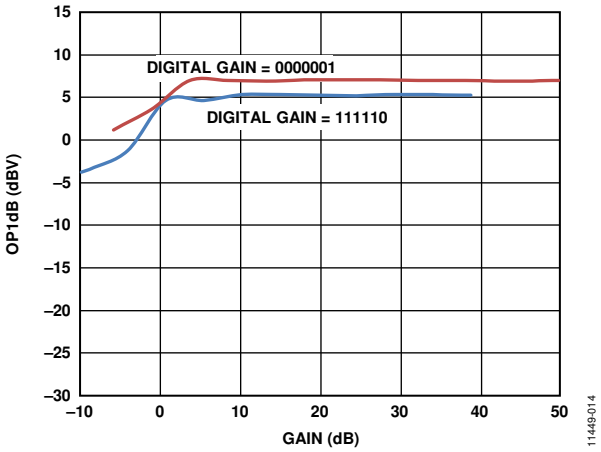

Figure 14. OP1dB vs. Gain at a Fundamental of 16 MHz

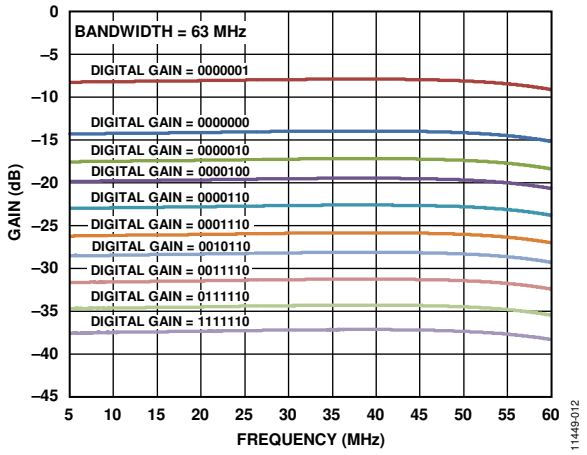

Figure 12. Digital Gain vs. Frequency; VGN1/VGN2/VGN3 = 0 V

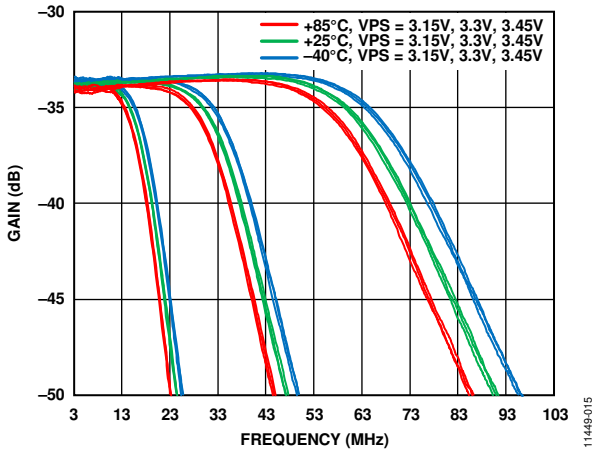

Figure 15. Frequency Response over Supply and Temperature; VGN1/VGN2/VGN3 = 0 V, Filter Corners = 15 MHz, 30 MHz, and 60 MHz

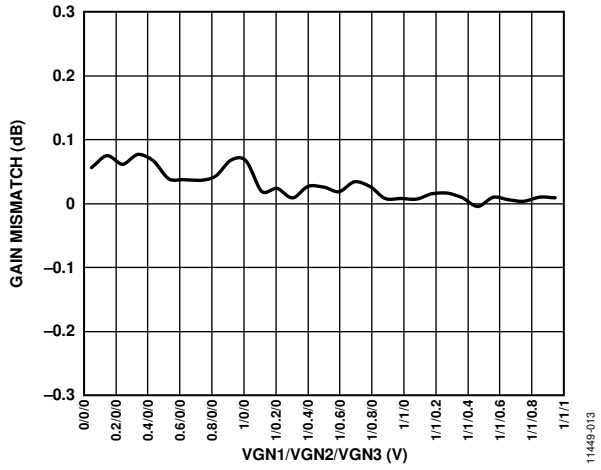

Figure 13. Gain Mismatch Between Channels vs. VGN1/VGN2/VGN3 Voltage

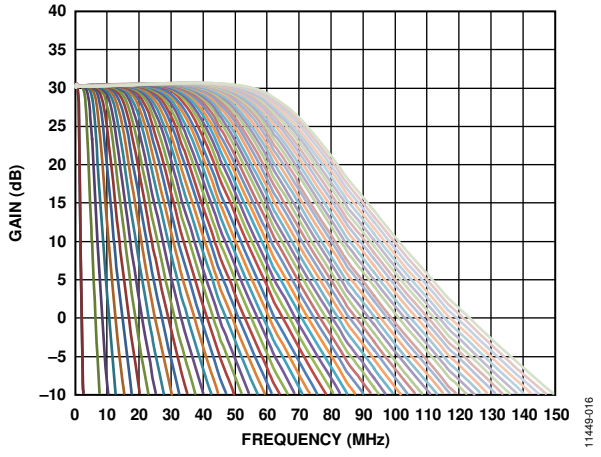

Figure 16. Gain vs. Frequency over BW Setting (Linear); VGN1/VGN2/VGN3 = 0 V

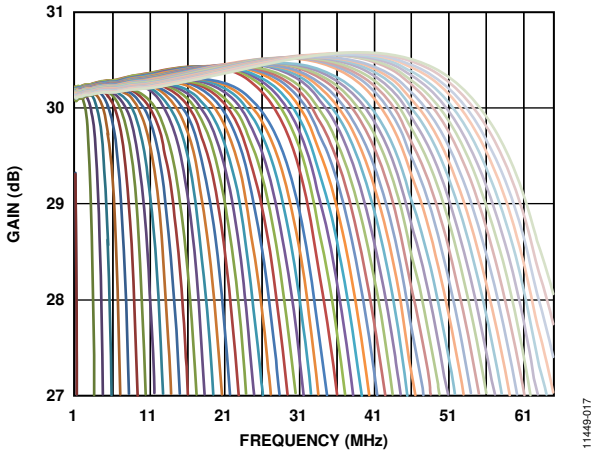

Figure 17. Gain vs. Frequency over BW Setting (Linear); Scaled to Show Peaking

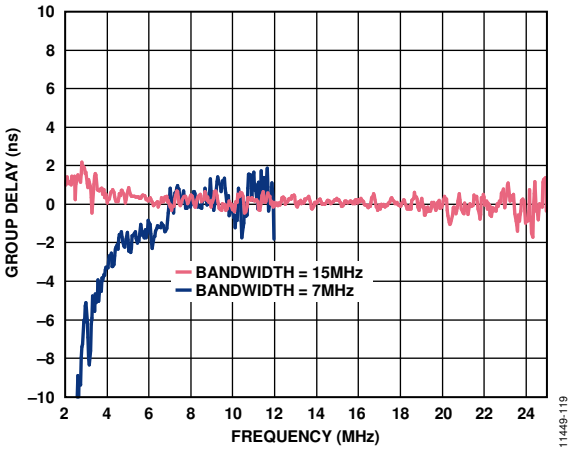

Figure 20. IQ Group Delay Mismatch vs. Frequency (BW = 7 MHz and BW = 15 MHz)

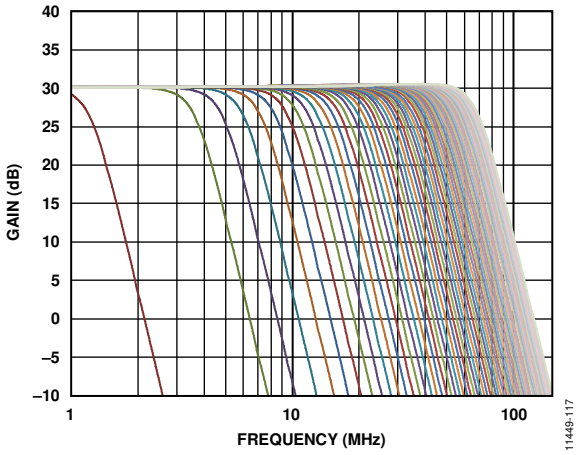

Figure 18. Gain vs. Frequency over BW Setting (Log); VGN1 = 1 V, VGN2 = 0.7 V, VGN3 = 0.75 V

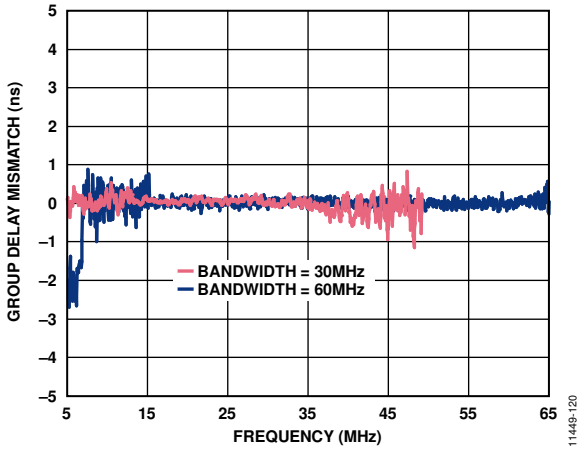

Figure 21. IQ Group Delay Mismatch vs. Frequency (BW = 30 MHz and BW = 60 MHz)

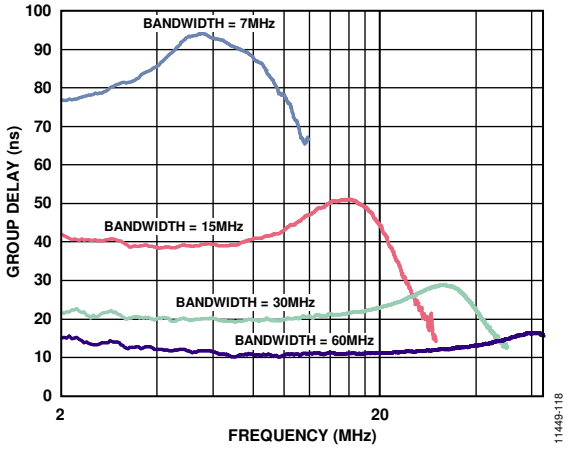

Figure 19. Group Delay vs. Frequency; VGN1/VGN2/VGN3 = 0 V

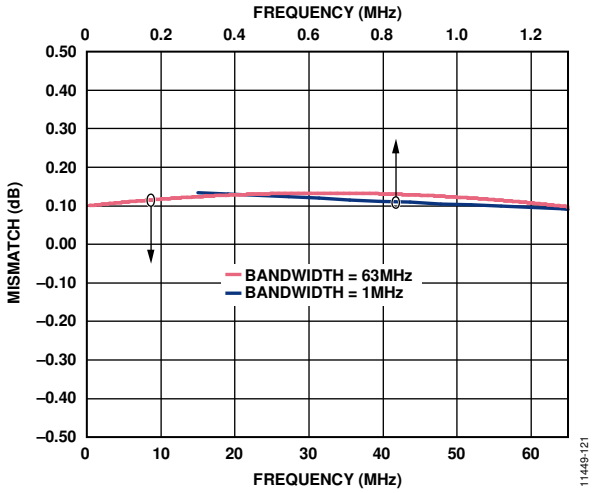

Figure 22. IQ Amplitude Mismatch vs. Frequency; VGN1/VGN2/VGN3 = 0 V

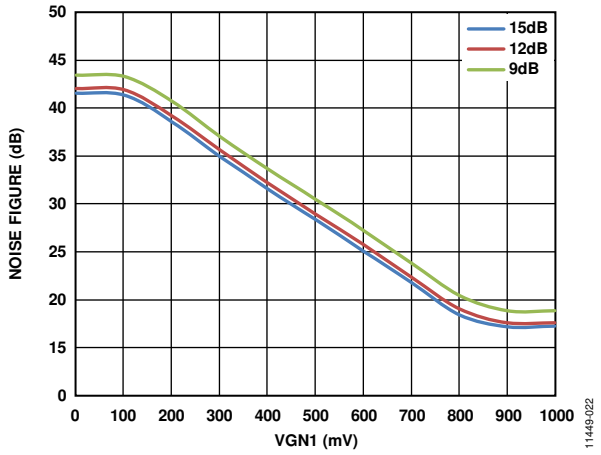

Figure 23. Noise Figure vs. VGN1 over VGA1 Digital Gain; Noise Density Measured at Half of Filter Corner

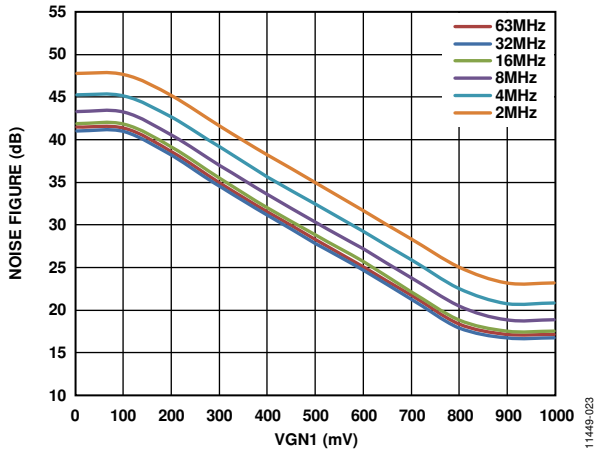

Figure 24. Noise Figure vs. VGN1 over Filter Corner; Digital Gain = 0000001, Noise Density Measured at Half of Filter Corner

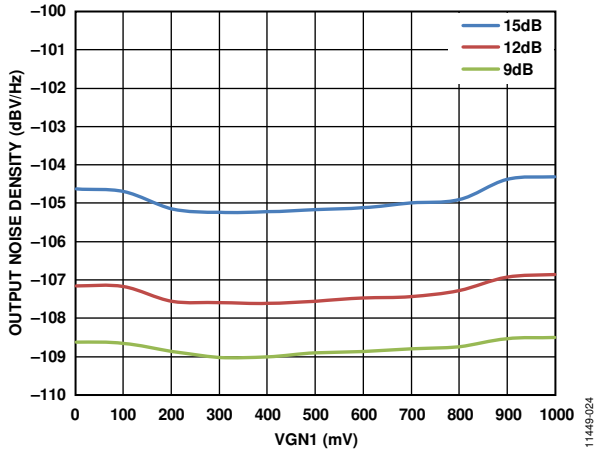

Figure 25. Output Noise Density vs. VGN1 over VGA1 Digital Gain; Noise Density Measured at Half of Filter Corner

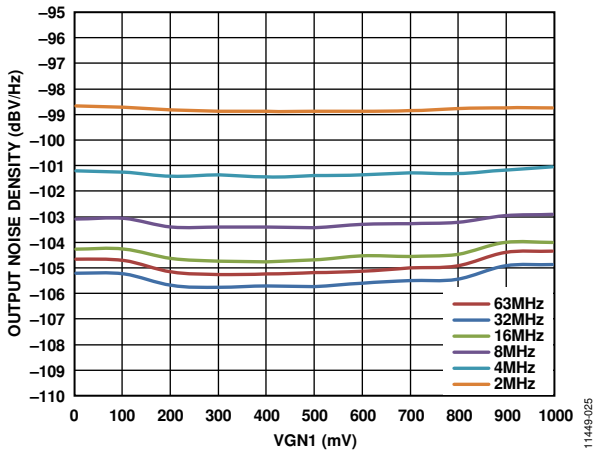

Figure 26. Output Noise Density vs. VGN1 over Bandwidth Setting; Digital Gain = 0000001, Noise Density Measured at Half of Filter Corner

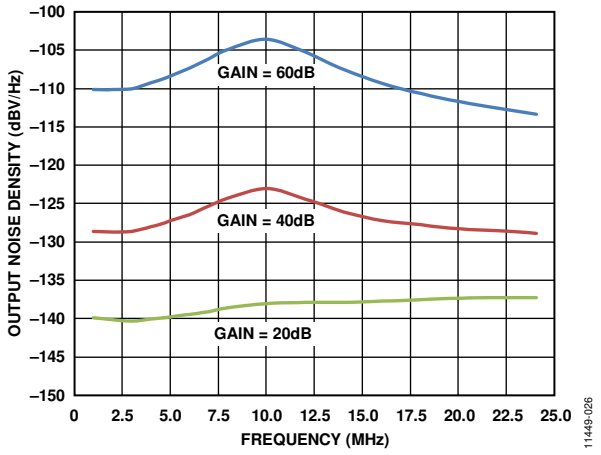

Figure 27. Output Noise Density vs. Frequency; Filter Corner = 7 MHz, Digital Gain = 0000001, Noise Density Measured at Half of Filter Corner

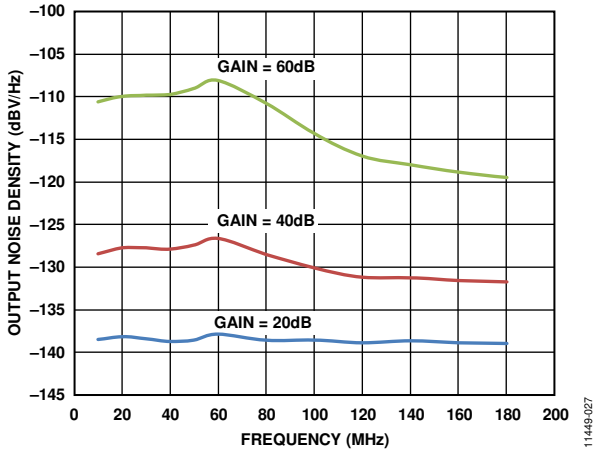

Figure 28. Output Noise Density vs. Frequency; Filter Corner = 60 MHz, Digital Gain = 0000001

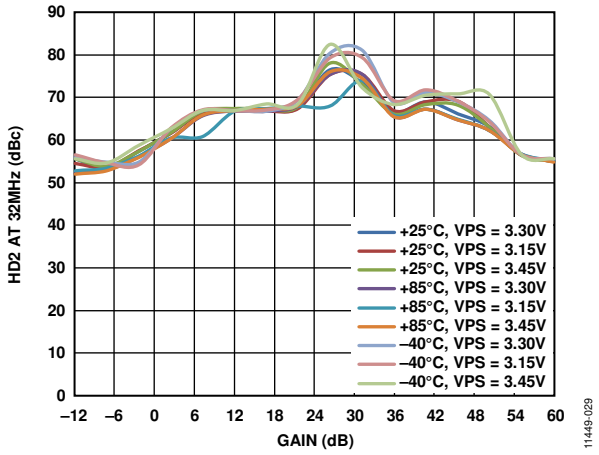

Figure 29. HD2 vs. Gain over Supply and Temperature; 16 MHz Fundamental Tone, Digital Gain = 0000000

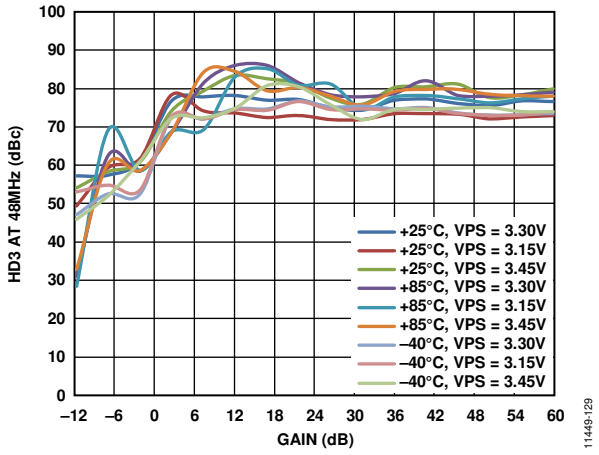

Figure 30. HD3 vs. Gain over Supply and Temperature; 16 MHz Fundamental Tone, Digital Gain = 0000000

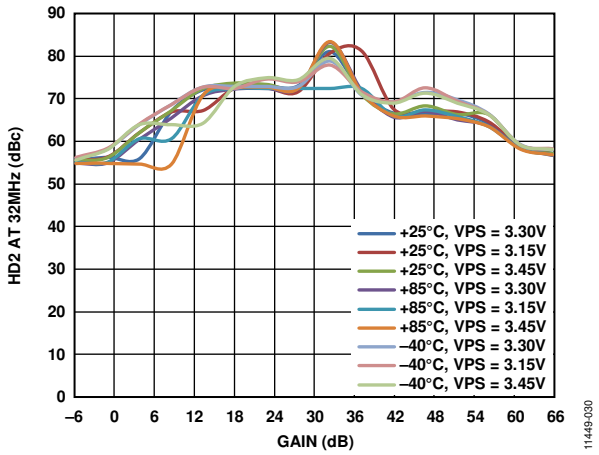

Figure 31. HD2 vs. Gain over Supply and Temperature; 16 MHz Fundamental Tone, Digital Gain = 0000001

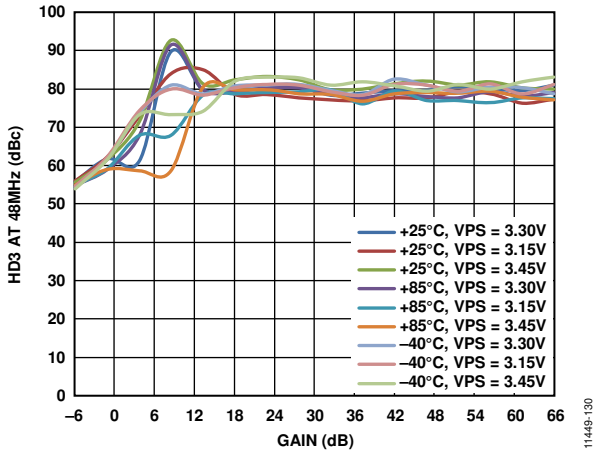

Figure 32. HD3 vs. Gain over Supply and Temperature; 16 MHz Fundamental Tone, Digital Gain = 0000001

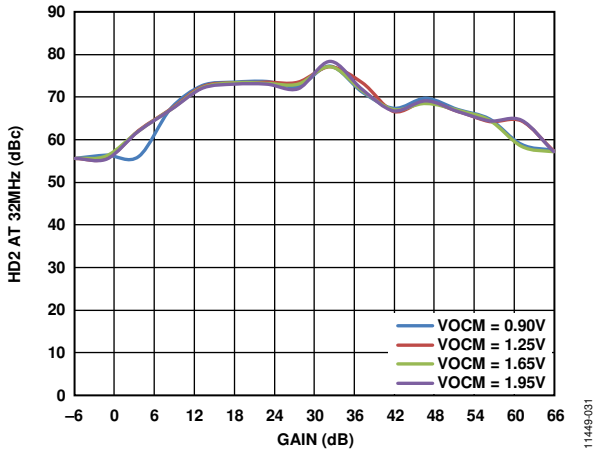

Figure 33. HD2 vs. Gain over VOCM; 16 MHz Fundamental Tone, Digital Gain = 0000001

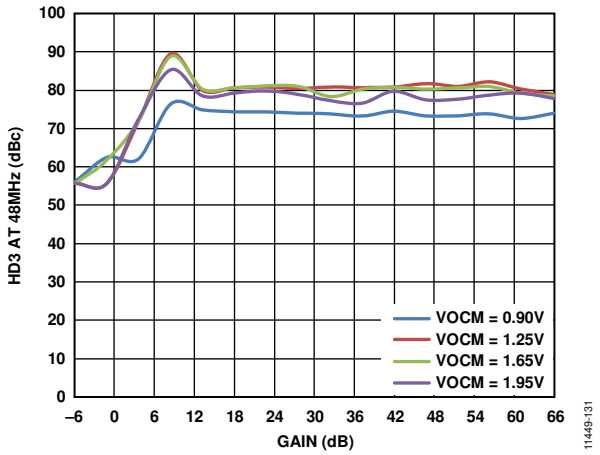

Figure 34. HD3 vs. Gain over VOCM; 16 MHz Fundamental Tone, Digital Gain = 0000001

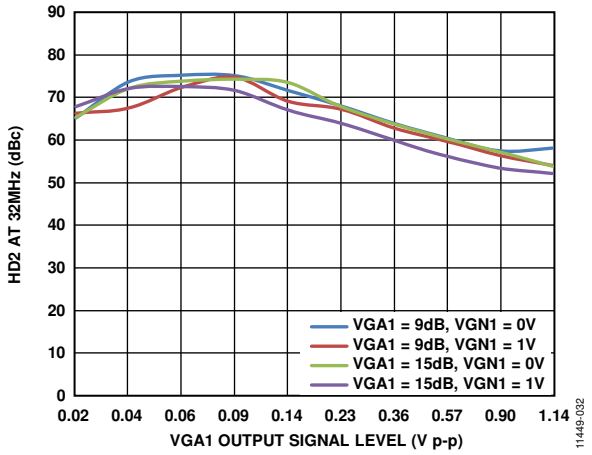

Figure 35. HD2 vs. VGA1 Output Signal Level (Inferred); 16 MHz Fundamental Tone, VGN2/VGN3 = 0 V

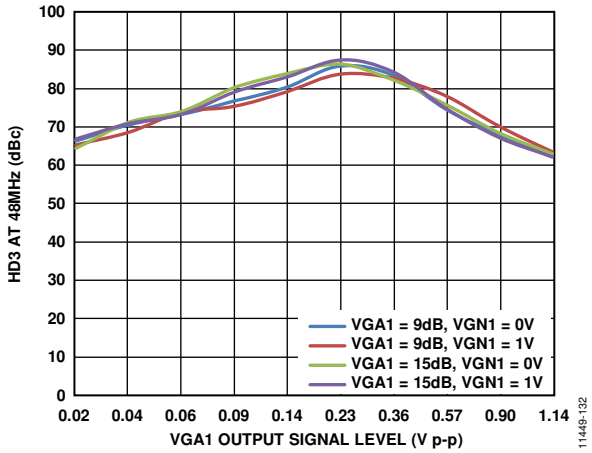

Figure 36. HD3 vs. VGA1 Output Signal Level (Inferred); 16 MHz Fundamental Tone, VGN2/VGN3 = 0 V

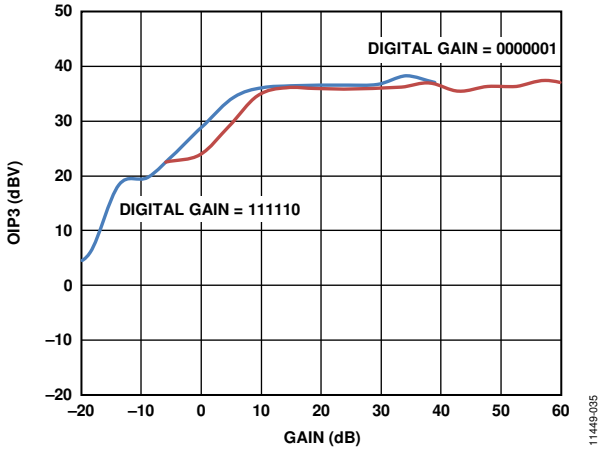

Figure 37. In-Band OIP3 vs. Gain over Digital Gain; 1.5 V p-p Composite Output Target, 30 MHz and 31 MHz Tones

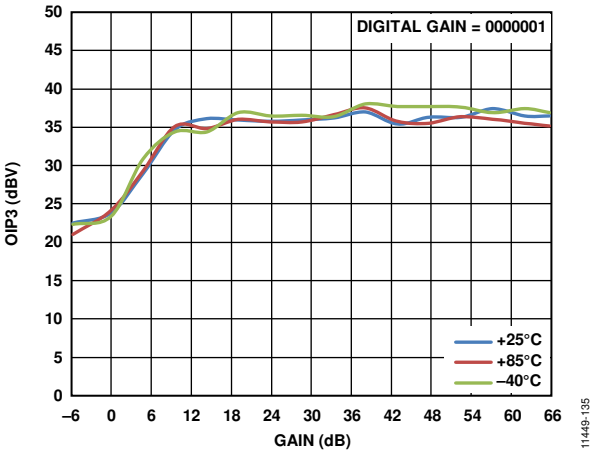

Figure 38. In-Band OIP3 vs. Gain over Temperature; 30 MHz and 31 MHz Tones, Digital Gain = 0000001

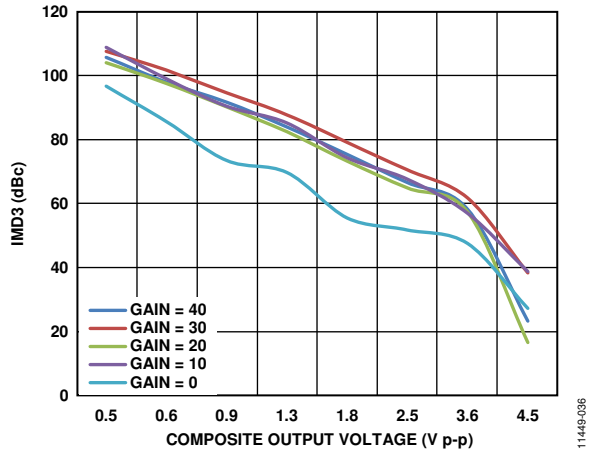

Figure 39. In-Band IMD3 vs. Composite Output Voltage over Gain; 30 MHz and 31 MHz Tones , Digital Gain = 1111110

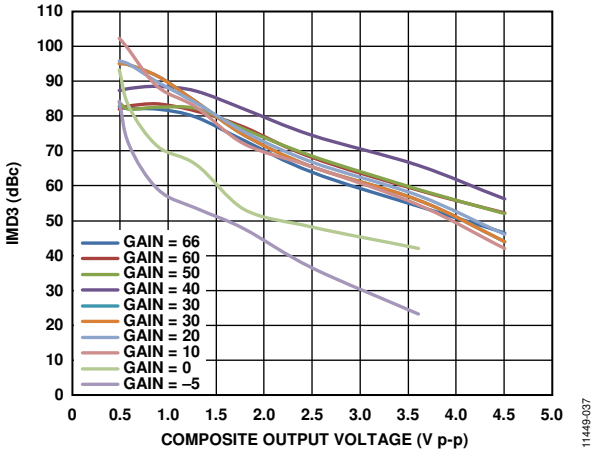

Figure 40. In-Band IMD3 vs. Composite Output Voltage over Gain; 30 MHz and 31 MHz Tones , Digital Gain = 0000001

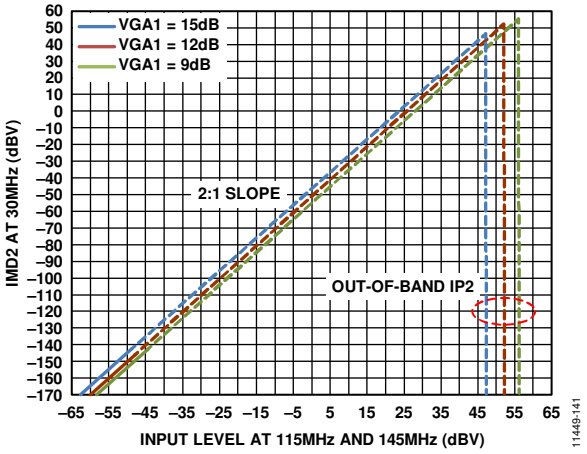

Figure 41. Out-of-Band IIP2, IMD2 vs. P_{IN} over Digital Gain; 115 MHz and 145 MHz Tones

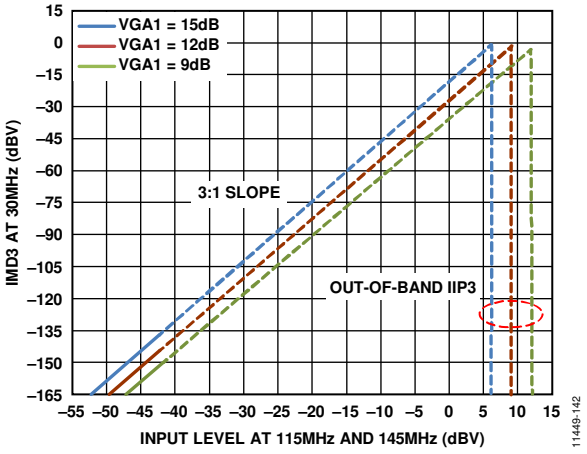

Figure 42. Out-of-Band IIP3, IMD3 vs. P_{IN} over Digital Gain; 115 MHz and 145 MHz Tones

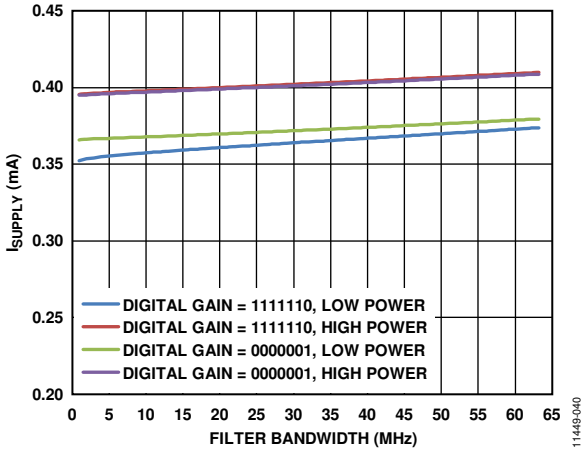

Figure 43. Supply Current vs. Filter Bandwidth over Digital Gain and Power Modes

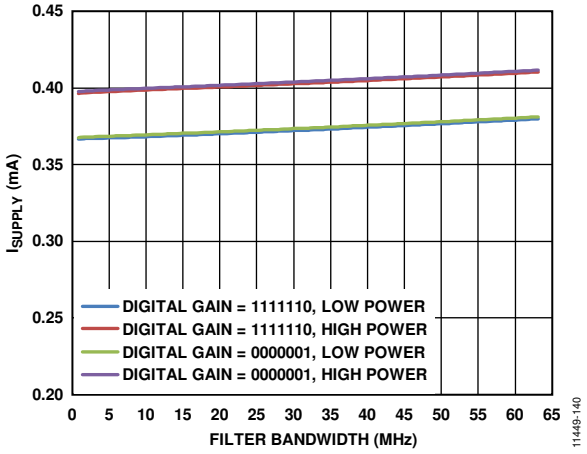

Figure 44. Supply Current vs. Filter Bandwidth over Digital Gain and Power Modes

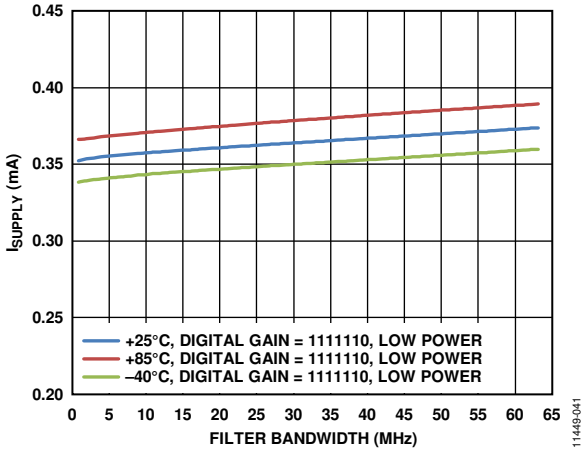

Figure 45. Supply Current vs. Filter Bandwidth over Temperature, Digital Gain, and Power Modes

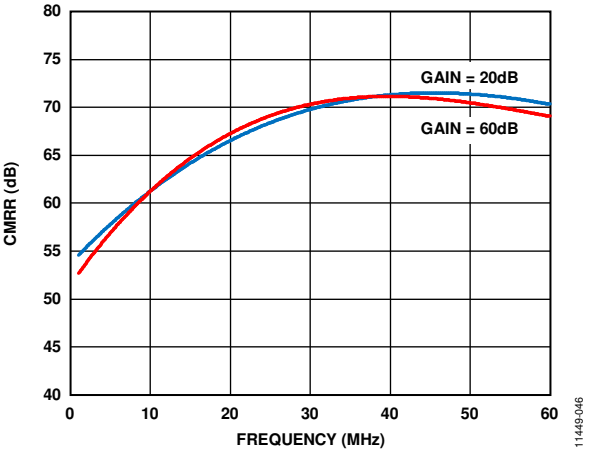

Figure 46. Common-Mode Rejection Ratio vs. Frequency

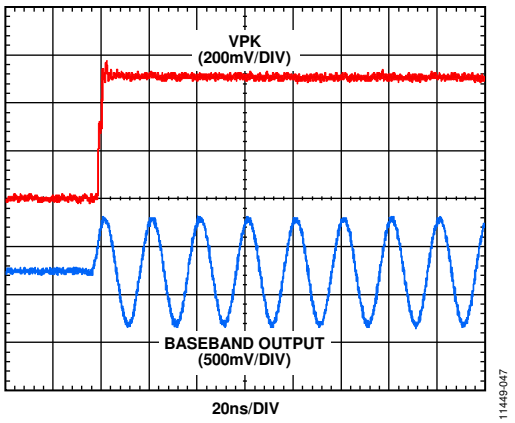

Figure 47. Peak Detector Time Domain Response

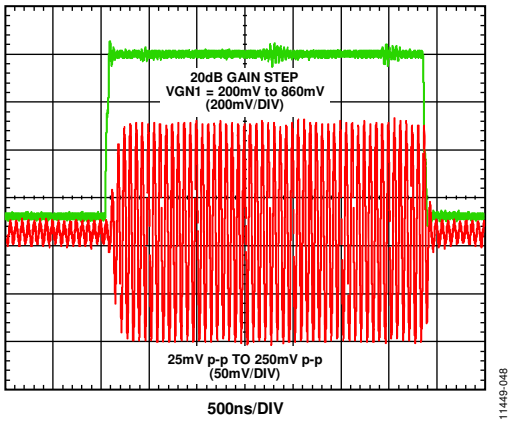

Figure 48. VGA1 Gain Step Response; VGN2/VGN3 = 0.5 V, −24 dBV RMS Input Signal Level, C27 = 100 pF

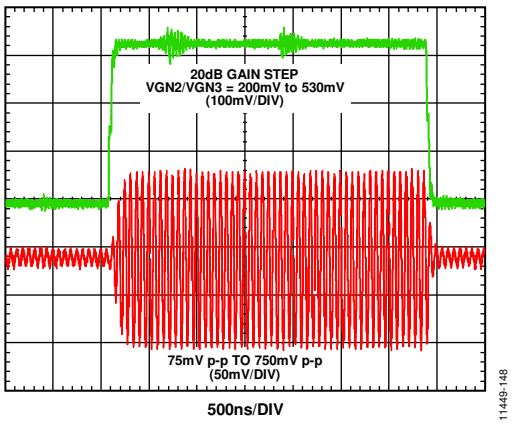

Figure 49. VGA2/VGA3 Gain Step Response; VGN1 = 0.5 V, −4 dBV RMS Input Signal Level, C17 and C32 = 100 pF

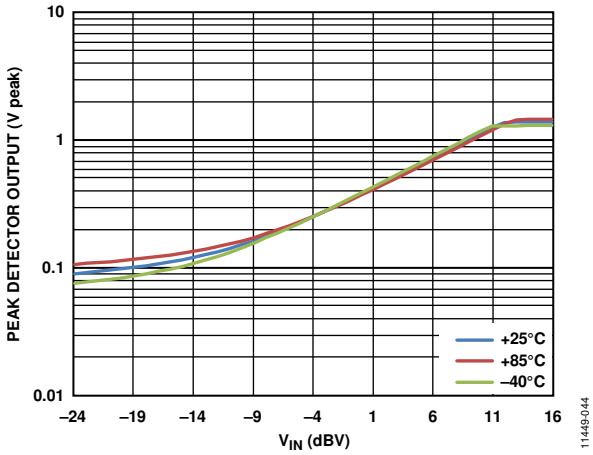

Figure 50. Peak Detector Output vs. V_{IN} over Temperature; VGN1 = 0.5 V, VGN2 = VGN3 = 0 V

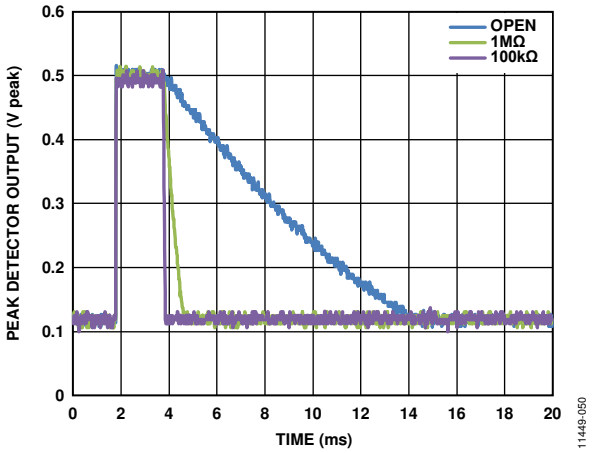

Figure 51. Peak Detector Hold Time over RAVG

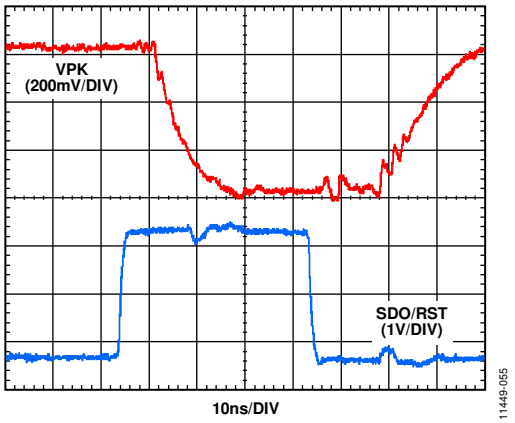

Figure 52. Peak Detector Reset Time Domain Response

BYPASS MODE

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, power mode bit (B9) = 1 (high power mode), digital gain code bits (B8 to B2) = 1111110, dc offset disable bit (B1) = 0 (enabled), unless otherwise noted.

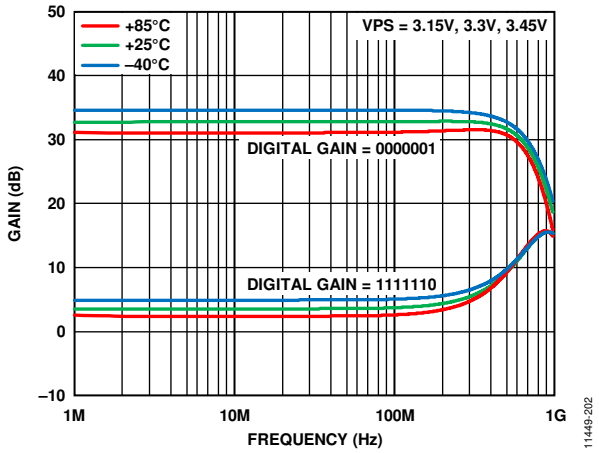

Figure 53. Frequency Response over Supply and Temperature

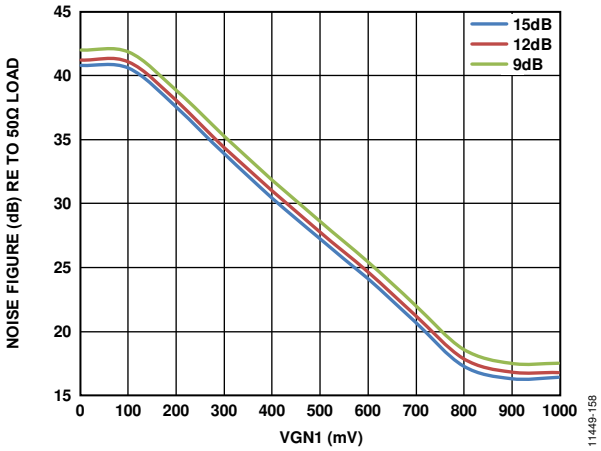

Figure 56. Noise Figure vs. VGN1 over Digital Gain

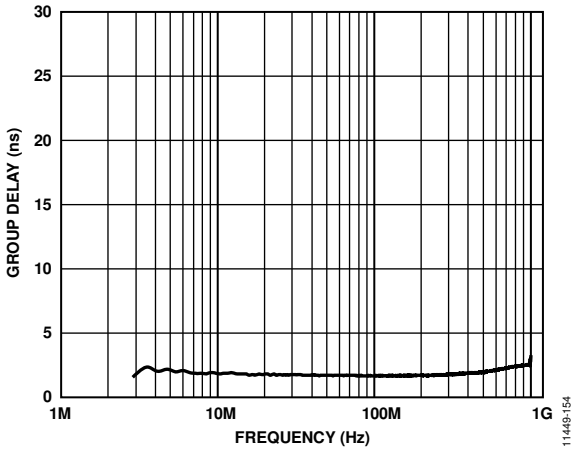

Figure 54. Group Delay vs. Frequency

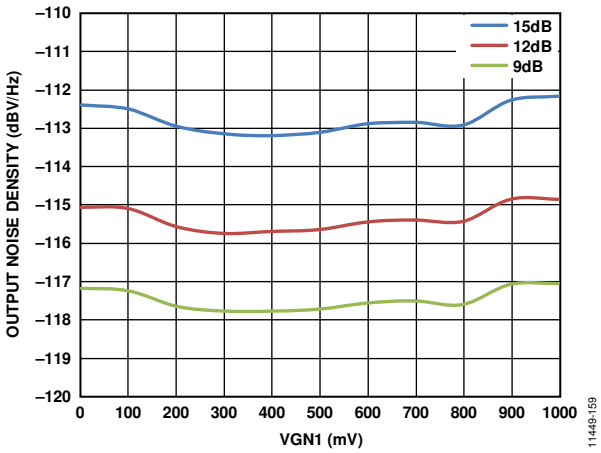

Figure 57. Output Noise Density vs. VGN1 over Digital Gain

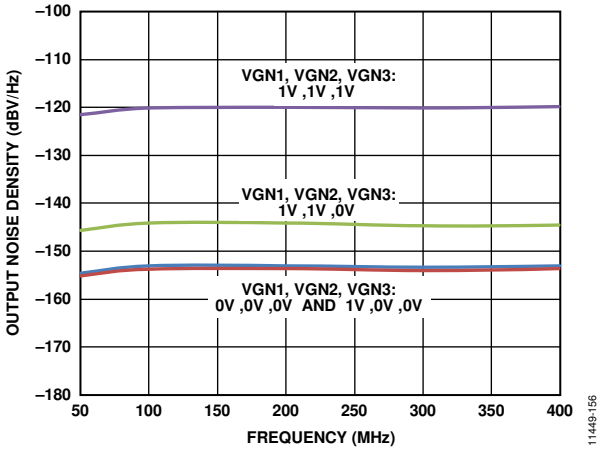

Figure 55. Output Noise Density vs. Frequency over Analog Gains; Digital Gain = 0000001

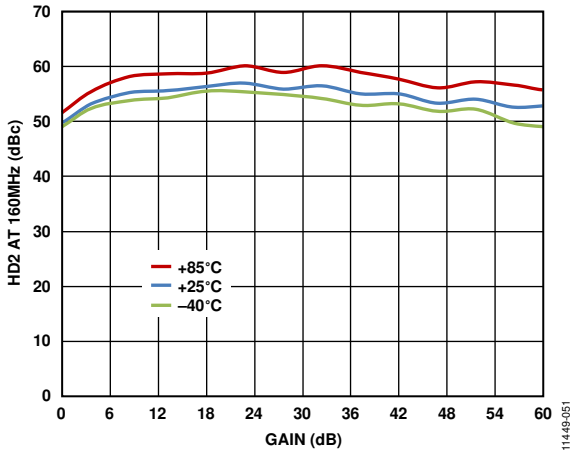

Figure 58. HD2 vs. Gain over Temperature; Fundamental at 80 MHz, Digital Gain = 0000001

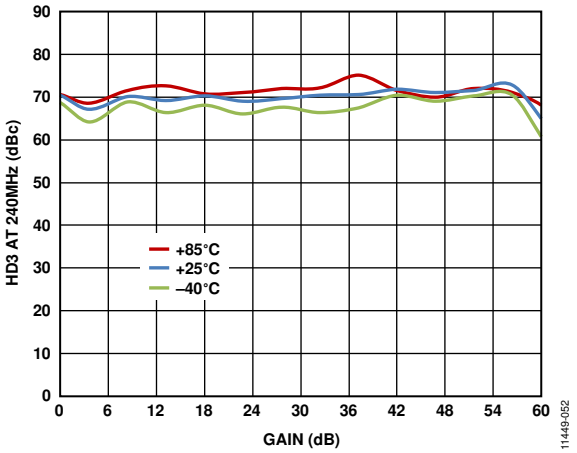

Figure 59. HD3 vs. Gain over Temperature; Fundamental at 80 MHz, Digital Gain = 0000001

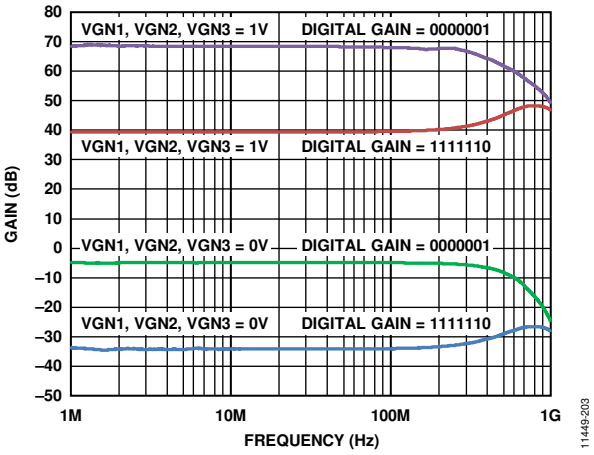

Figure 62. Gain vs. Frequency

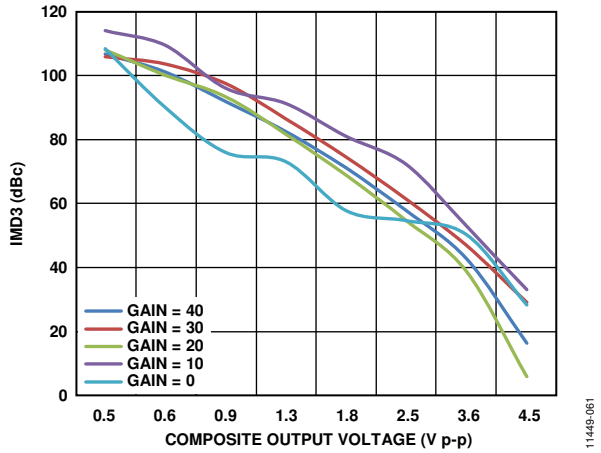

Figure 60. IMD3 vs. Composite Output Voltage over VOCM; VGN1/VGN2/VGN3 = 1 V, 125 MHz and 126 MHz Tones

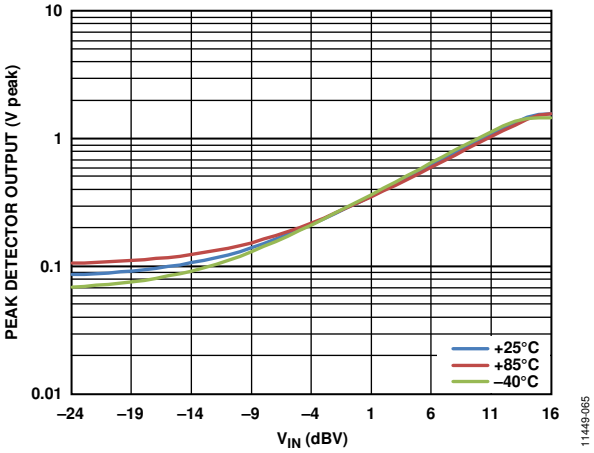

Figure 63. Peak Detector Output vs. V_{IN} over Temperature; VGN1 = 0.5 V, VGN2/VGN3 = 0 V; 125 MHz Tone

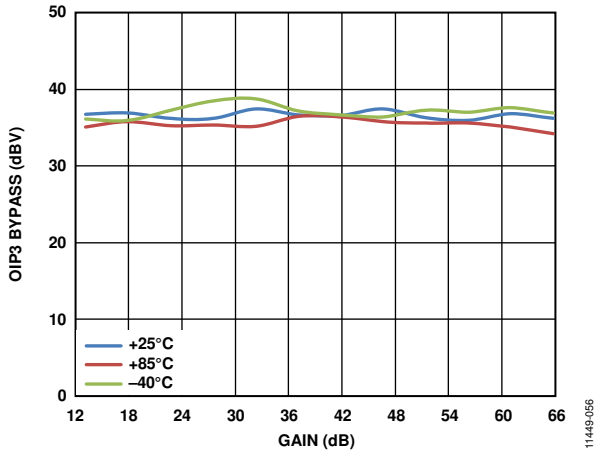

Figure 61. In-Band OIP3 Bypass vs. Gain over Temperature; Digital Gain = 0000001, 125 MHz and 126 MHz Tones

MIXED POWER AND FILTER MODES

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, digital gain code bits (B8 to B2) = 1111110, dc offset disable bit (B1) = 0 (enabled), unless otherwise noted.

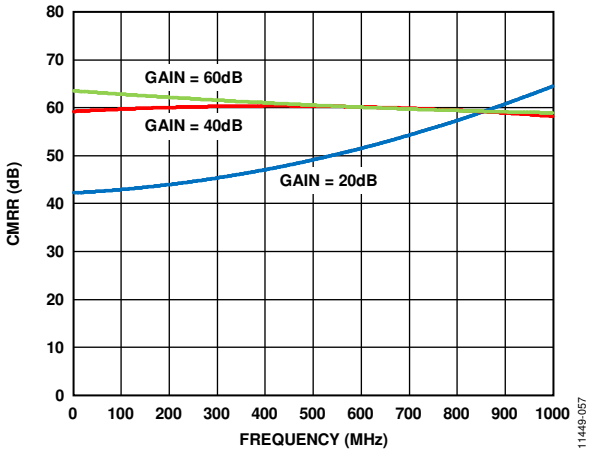

Figure 64. Common-Mode Rejection Ratio (CMRR) vs. Frequency

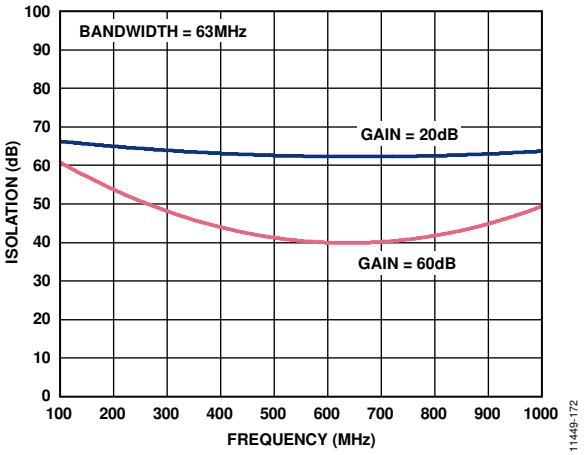

Figure 66. Channel Isolation (OPM1_SE to OPM2_SE) vs. Frequency, Bypass Mode

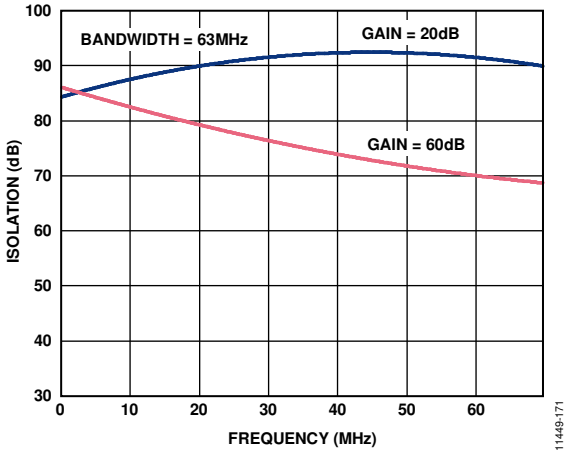

Figure 65. Channel Isolation (OPM1_SE to OPM2_SE) vs. Frequency, Filter Mode

CHARACTERIZATION

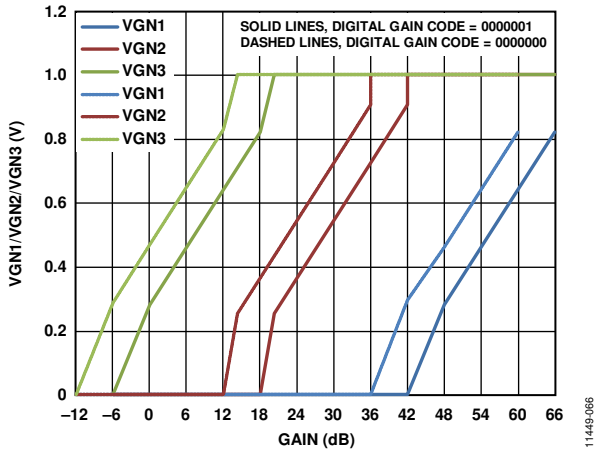

Figure 67. Gain Distribution for HD2/HD3 vs. Gain

Figure 67 shows the ADRF6518 analog gain distribution for the HD2 vs. gain and HD3 vs. gain plots while the gain and input voltage levels were swept and while keeping the output voltage level at 1.5 V p-p.

NOISE FIGURE CALCULATION

All of the noise figure plots (see Figure 23, Figure 24, and Figure 56) were completed by input referring the output noise density and then dividing it by the theoretical noise density of a 50 Ω resister. The input SMA on the evaluation board was terminated with a 50 Ω resistor to ground, which provided the ADRF6518 input with a 400 Ω differential impedance via the 8:1 balun. In signal chain calculations, it is often convenient to reference the noise figure to 50 Ω, even though the ADRF6518 input is terminated in 400 Ω.

The noise factor is calculated as follows:

$$Noise\ Factor = \frac{N_{OUT}/GAIN}{N_{50\Omega}}$$

where the noise densities are in nV/√Hz and *GAIN* is in linear terms. The noise figure is then

$$Noise\ Figure = 10 \log_{10}(Noise\ Factor)$$

REGISTER MAP AND CODES

The filter frequency, amplifier gains, filter bypass mode, and offset correction loops can be programmed using the SPI interface. Table 5 provides the bit map for the internal 15-bit register of the ADRF6518.

Table 4. Filter Mode and Power Mode Options

B9	Filter Bypass	Filter
0	VGA low power; filter off	VGA low power; filter low power
1	VGA high power; filter off	VGA low power; filter high power

Table 5. Register Map

MSB **LSB**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
Filter frequency code and filter bypass mode						Power mode	Digital gain code							DC offset disable
Code = 1 dB corner in MHz For example, 31 MHz = 011111 (MSB first) Use 000000 for filter bypass mode						0: low power 1: high power Use 1 for filter BW > 31 MHz, in filter mode Use 1 for channel BW > 60 MHz, in filter bypass mode	VGA1 gain 00: 15 dB 01: 12 dB 10: 9 dB 11: 9 dB		VGA2 gain 00: 21 dB 01: 18 dB 10: 15 dB 11: 12 dB		VGA3 gain 00: 21 dB 01: 18 dB 10: 15 dB 11: 12 dB		Postamp 0: 3 dB 1: 9 dB	0: enable 1: disable

THEORY OF OPERATION

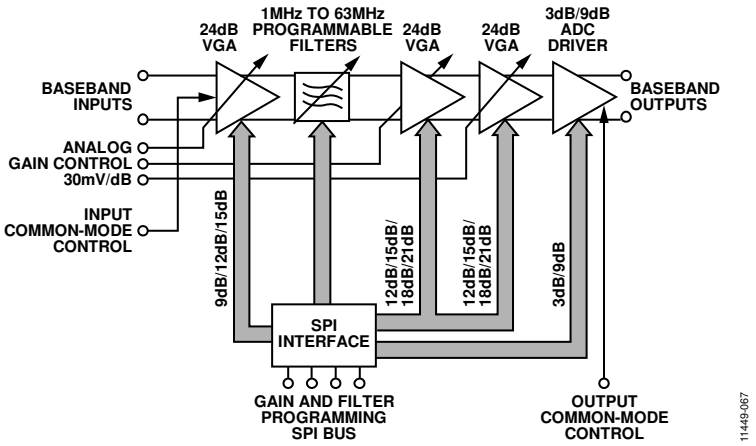

Figure 68. Signal Path Block Diagram for a Single Channel of the ADRF6518

The ADRF6518 consists of a matched pair of input VGAs followed by programmable filters, and then by a cascade of two variable gain amplifiers and output ADC drivers. The filters can be bypassed and powered down through the SPI interface for operation beyond the maximum filter bandwidth. The block diagram of a single channel is shown in Figure 68.

The programmability of the filter bandwidth and of the prefiltering and postfiltering fixed gains through the SPI interface offers great flexibility when coping with signals of varying levels in the presence of noise and large, undesired signals near the desired band. The entire differential signal chain is dc-coupled with flexible interfaces at the input and output. The bandwidth and gain setting controls for the two channels are shared, ensuring close matching of their magnitude and phase responses. The ADRF6518 can be fully disabled through the ENBL pin.

Filtering and amplification are fundamental operations in any signal processing system. Filtering is necessary to select the intended signal while rejecting out-of-band noise and interferers. Amplification increases the level of the desired signal to overcome noise added by the system. When used together, filtering and amplification can extract a low level signal of interest in the presence of noise and out-of-band interferers. Such analog signal processing alleviates the requirements on the analog, mixed signal, and digital components that follow.

INPUT VGAs

The input VGAs provide a convenient interface to the sensitive filter sections that follow. They are designed to have a low noise figure and high linearity. The combination of analog gain control and digital gain settings allow a wide range of input signal levels to be conditioned to drive the filters at up to 1.5 V p-p amplitude. The VGAs set a differential input impedance of 400 Ω.

The baseband input signal can be ac-coupled or dc-coupled via Pin 7 selection. When the signal is dc-coupled, the wide input common-mode voltage is supported by having an optional 5 V supply on Pin 8, VPI. The default common-mode voltage is VPI/2, which is available on the dual function Pin 7, VICM/AC, to set the output common-mode voltage of the driving circuit. However, this is optional and input common-mode can be independently set within the supported range. For a 3.3 V supply on VPI, the input common mode can range from 1.35 V to 1.95 V, while maintaining a 5 V p-p input level at >60 dBc HD2 and HD3. For a 5 V supply on VPI, the input common-mode range extends to 1.35 V to 3.1 V. Extra current is drawn from the VPI supply to support an input common mode greater than the midvalue of the main 3.3 V supply, that is, VPS/2.

The VICM/AC voltage is not buffered and must be sensed at a high impedance point to prevent it from being loaded down. When the baseband input signal is ac-coupled, pull the VICM/AC pin low to activate the internal bias for the input stage.

The input VGAs have analog gain control of 24 dB, followed by a digital gain settings of 9 dB, 12 dB, or 15 dB, selectable through the SPI (see the Register Map and Codes section). The VGAs are based on the Analog Devices, Inc., patented X-AMP® architecture, consisting of tapped 24 dB attenuators, followed by programmable gain amplifiers. The X-AMP architecture generates a continuous linear-in-dB monotonic gain response with low ripple. The analog gain of the VGA sections are controlled through the high impedance VGN1 pin with an accurate slope of 30 mV/dB. Adjust the VGA analog gain through an AGC mechanism, such that 1.5 V p-p at the output of the first VGA is not exceeded. If, however, the input signal is small enough, the first VGA can be set at full gain for best noise figure (NF) performance and gain control achieved in the second or third VGA.

Driving ADRF6518 Single-Ended

The input structure of the ADRF6518 is designed for differential drive. However, with some performance degradation, it can be driven single-ended, especially at low bandwidth signals. See the Applications Information section for guidance on single-ended drive.

PEAK DETECTOR

To measure the signal level at the critical interface of the VGA1 output and the programmable filter input, a peak detector has been implemented. The peak detector simultaneously measures both channels at the VGA1 output and reports the bigger of the two at the VPK pin. The on-chip holding capacitor and negligible leakage at the internal node ensure a large droop time of the order of a millisecond, which is a function of the peak voltage as well. Bigger peak voltage results in longer droop time. The droop time can be adjusted down by placing a resistor between the RAVG and VPS pins. Typical values of RAVG can range from 1 MΩ to 1 kΩ. As the RAVG resistor value is reduced, the peak voltage, VPK, appears as an envelope output. The peak detector has the attack bandwidth of 100 MHz.

The peak detector can be used in an AGC loop to set the appropriate signal level at the filter input. For such an implementation, filter VPK appropriately, considering that it is a peak hold output. A high pulse of 25 ns or longer duration applied to the SDO/RST dual function pin resets the VPK voltage to 0 V by discharging the internal holding capacitor.

PROGRAMMABLE FILTERS

The integrated programmable filter is the key signal processing function in the ADRF6518. The filters follow a six-pole Butterworth prototype response that provides a compromise between band rejection, ripple, and group delay. The 0.5 dB bandwidth is programmed from 1 MHz to 63 MHz in 1 MHz steps via the serial programming interface (SPI) as described in the Programming the ADRF6518 section.

The filters are designed so that the Butterworth prototype filter shape and group delay responses vs. frequency are retained for any bandwidth setting. Figure 69 and Figure 70 illustrate the ideal six-pole Butterworth response. The group delay, τ_g, is defined as

$$\tau_g = -\partial\varphi/\partial\omega$$

where:
φ is the phase in radians.
$\omega = 2\pi f$ is the frequency in radians per second.

Note that for a frequency scaled filter prototype, the absolute magnitude of the group delay scales inversely with the bandwidth; however, the shape is retained. For example, the peak group delay for a 28 MHz bandwidth setting is 14× less than for a 2 MHz setting.

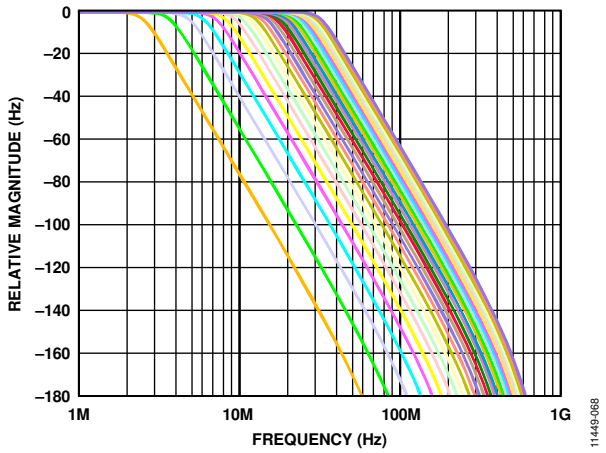

Figure 69. Sixth-Order Butterworth Magnitude Response for 0.5 dB Bandwidths Programmed from 2 MHz to 29 MHz in 1 MHz Steps

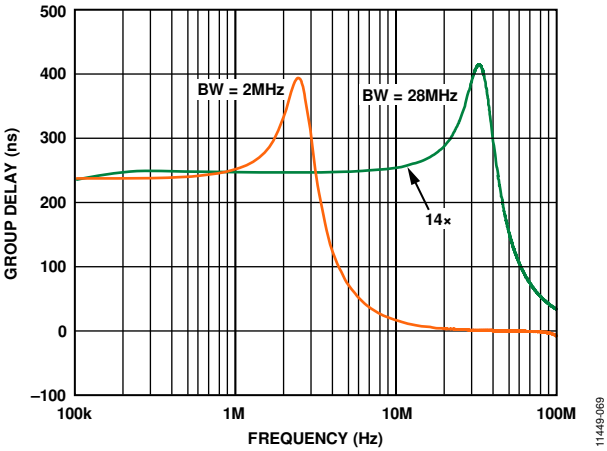

Figure 70. Sixth-Order Butterworth Group Delay Response for 0.5 dB Bandwidths Programmed to 2 MHz and 28 MHz

The corner frequency of the filters is defined by RC products, which can vary by ±30% in a typical process. Therefore, all the parts are factory calibrated for corner frequency, resulting in a residual ±8% corner frequency variation over the −40°C to +85°C temperature range. Although absolute accuracy requires calibration, the matching of RC products between the pair of channels is better than 1% by observing careful design and layout practices. Calibration and excellent matching ensure that the magnitude and group delay responses of both channels track together, a critical requirement for digital IQ-based communication systems.

Bypassing the Filters

For higher bandwidth applications, filters of the ADRF6518 can be bypassed via the SPI. In the filter bypass mode, filters are disabled and power consumption is significantly reduced. The bandwidth of cascaded VGAs, which is significantly larger than 63 MHz maximum of the filters, is fully realized in the filter bypass mode.

VARIABLE GAIN AMPLIFIERS (VGAs)

The cascaded VGA2 and VGA3 are also based on the X-AMP architecture, and each has 24 dB gain range with separate high impedance gain control inputs, VGN2 and VGN3. The VGA structures of the second and third VGAs are identical to that of the first VGA. However, these have slightly higher noise figure and less drive level capability. Their output is rated at 1 V p-p for >60 dBc HD2 and HD3. Depending on the input signal range, the second or third VGA or both can be used for AGC purposes. The critical level to consider while making this choice is the signal level at the output of the VGAs, which must not exceeded 1 V p-p to maintain low distortion.

The fixed gain following both of the variable gain sections can also be programmed to 12 dB, 15 dB, 18 dB, or 21 dB to maximize the dynamic range.

OUTPUT BUFFERS/ADC DRIVERS

The low impedance (<10 Ω) output buffers of the ADRF6518 are designed to drive either ADC inputs or subsequent amplifier stages. They are capable of delivering up to 4 V p-p composite two-tone signals into 400 Ω differential loads with >60 dBc IMD3. The output common-mode voltage defaults to VPS/2, but it can be adjusted from 900 mV to VPS − 1.2 V without loss of drive capability by presenting the VOCM pin with the desired common-mode voltage. The high input impedance of VOCM allows the ADC reference output to be connected directly. Even though the output common-mode voltage is adjustable, and the offset compensation loop can null the accumulated dc offsets (see the DC Offset Compensation Loop section), it may still be desirable to ac-couple the outputs by selecting the coupling capacitors according to the load impedance and desired bandwidth.

DC OFFSET COMPENSATION LOOP

In many signal processing applications, no information is carried in the dc level. In fact, dc voltages and other low frequency disturbances can often dominate the intended signal and consume precious dynamic range in the analog path and bits in the data converters. These dc voltages can be present with the desired input signal or can be generated inside the signal path by inherent dc offsets or other unintended signal-dependent processes such as self-mixing or rectification.

Because the ADRF6518 is fully dc-coupled, it may be necessary to remove these offsets to realize the maximum signal-to-noise ratio (SNR). The external offsets can be eliminated with ac-coupling capacitors at the input pins; however, that requires large value capacitors because the impedances can be fairly low, and high-pass corners may need to be <10 Hz in some cases. To address the issue of dc offsets, the ADRF6518 provides an offset correction loop that nulls the output differential dc level, as shown in Figure 71. If the correction loop is not required, it can be disabled through the SPI port.

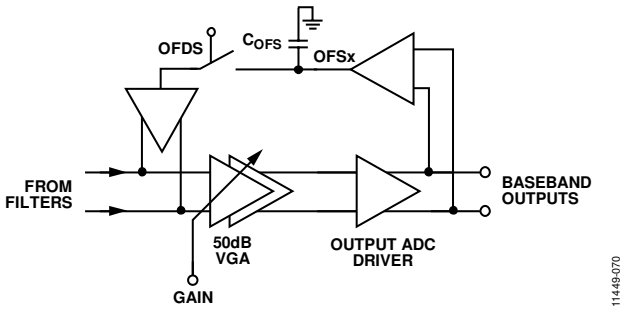

Figure 71. Offset Compensation Loop Operates Around the VGA and Output Buffer

The offset control loop creates a high-pass corner, f_{HP}, that is superimposed on the normal Butterworth filter response when filters are enabled. Typically, f_{HP} is many orders of magnitude lower than the lower programmed filter bandwidth so that there is no interaction between them. Setting f_{HP} is accomplished with capacitors, C_{OFS}, from the OFS1 and OFS2 pins to ground. Because the correction loop works around the VGA sections, f_{HP} is also dependent on the total gain of the cascaded VGAs. In general, the expression for f_{HP} is given by

$$f_{HP}\ (\text{Hz}) = 6.7 \times \textit{Post Filter Linear Gain}/C_{OFS}\ (\mu\text{F})$$

where *Post Filter Linear Gain* is expressed in linear terms, not in decibels (dB), and is the gain following the filters, which excludes the VGA1 gain.

Note that f_{HP} increases in proportion to the gain. For this reason, choose C_{OFS} at the highest operating gain to guarantee that f_{HP} is always below the maximum limit required by the system.

PROGRAMMING THE ADRF6518

The 0.5 dB corner frequencies for both filters, the digital gains of all the VGAs, and the output buffers are programmed simultaneously through the SPI port. In addition to these, enabling the dc offset compensation loop and power mode selection are also controlled through SPI port. A 16-bit register stores 15 data bits, including the 6-bit code for corner frequencies of 1 MHz through 63 MHz and filter bypass, as well as the codes for VGA gains, and the postamplifier gain (see Table 5). The SPI protocol not only allows these selections to be written to the DATA pin, but also allows the stored code to be read back via the SDO/RST pin.

The latch enable (LE) pin must first go to a Logic 0 for a read or write cycle to begin. On the next rising edge of the clock (CLK), a Logic 1 on the DATA pin initiates a write cycle, whereas a Logic 0 on the DATA pin initiates a read cycle. In a write cycle, the next 15 CLK rising edges latch the desired 15-bit code, LSB first. This results in 16-bit code, including the first Logic 1 to initiate a write cycle. When LE goes high, the write cycle is completed and different codes are presented various blocks that need programming. In a read cycle, the next 15 CLK falling edges present the stored 15-bit code, LSB first. When LE goes high, the read cycle is completed. Detailed timing diagrams are shown in Figure 2 and Figure 3.

NOISE CHARACTERISTICS

The output noise behavior of the ADRF6518 depends on the gain and bandwidth settings. VGA1 noise dominates in the filter bypass mode and at high filter corner settings. While at low corner settings, filter noise tends to dominate.

The filter contributes a noise spectral density profile that is flat at low frequencies, peaks near the corner frequency, and then rolls off as the filter poles roll off the gain and noise. The magnitude of the noise spectral density contributed by the filter, expressed in nV/√Hz, varies inversely with the square root of the bandwidth setting, resulting in filter noise in nV that is nearly constant with the bandwidth setting. However, with VGA1 NF being lower than the filter, VGA1 tends to dominate the overall NF. At higher frequencies, after the filter noise rolls off, the noise floor is set by the VGAs.

Each of the X-AMP VGA sections used in the ADRF6518 contributes a fixed noise spectral density to its respective output, independent of the analog gain setting. With the digital gain change, however, VGA output noise changes, because the gain setting resistors values change. As an example, the VGA1 NF corresponding to a 15 dB gain setting is 17.3 dB, whereas for a 9 dB gain, the NF is 19 dB. When cascaded, the total noise contributed by the VGAs at the output of the ADRF6518 increases gradually with higher gain. This is apparent in the noise floor variation at high frequencies at different VGA gain settings. The exact relationship depends on the programmed fixed gain of the amplifiers. At lower frequencies within the filter bandwidth setting, the VGAs translate the filter noise directly to the output by a factor equal to the gain following the filter.

At low values of VGA gain, the noise at the output is the flat spectral density contributed by the last VGA. As the gain increases, more of the filter and first VGA noise appears at the output. Because the intrinsic filter noise density increases at lower bandwidth settings, it is more pronounced than it is at higher bandwidth settings. In either case, the noise density asymptotically approaches the limit set by the VGAs at the highest frequencies. For other values of VGA gain and bandwidth setting, the detailed shape of the noise spectral density changes according to the relative contributions of the filters and VGAs.

Because the noise spectral density outside the filter bandwidth is limited by the VGA output noise, it may be necessary to use an external, fixed frequency, passive filter prior to analog-to-digital conversion to prevent noise aliasing from degrading the signal-to-noise ratio. A higher sampling rate, relative to the maximum required ADRF6518 corner frequency setting, reduces the order and complexity of this external filter.

DISTORTION CHARACTERISTICS

To maintain low distortion through the cascaded VGAs and filter of the ADRF6518, consider the distortion limits of each stage. The first VGA has higher signal handling capability and bandwidth than VGA2 and VGA3, because it must cope with out-of-band signals that can be larger than the in-band signals. In the filter mode, these out-of-band signals are filtered before reaching VGA2 and VGA3. It is important to understand the signals presented to the ADRF6518 and to match these signals with the input and output characteristics of the part. It is useful to partition the ADRF6518 into the front end, composed of VGA1 and the filter, and the back end, composed of VGA2 and VGA3 and the output buffers.

VGA1 can handle a 5 V p-p signal at a maximum analog attenuation setting, without experiencing appreciable distortion at the input. In most applications, VGA1 gain should be adjusted such that the maximum signal presented at the filter inputs (or VGA2 input in filter bypass mode) is <1.5 V p-p. At this level, the front end does not limit the distortion performance. The peak detector output, VPK, can be used as an indicator of the signal level present at this critical interface. Choose the second and third VGA gains such that their output levels do not exceed 1 V p-p. If the output signal level is expected to exceed 1.5 V p-p, it is recommended to set the postamplifier gain to 9 dB.

For these signal level considerations, it is recommended that the out-of-band signal, if larger than the desired in-band signal, be addressed. In filter mode, such an out-of-band signal only affects the VGA1 operation, because it is filtered out by the filter and does not affect the following stages. In this case, a high VGA2 and VGA3 gain may be needed to raise the small desired signal to a higher level at the output. In the filter bypass mode, such out-of-band signals may need to be filtered prior to the ADRF6518.

The overall distortion introduced by the part depends on the input drive level, including the out-of-band signals, and the desired output signal level. To achieve best distortion performance and the desired overall gain, keep in mind the maximum signal levels indicated previously when selecting different VGA gains.

To distinguish and quantify the distortion performance of the input section, two different IP3 specifications are presented. The first is called in-band IP3 and refers to a two-tone test where the signals are inside the filter bandwidth. This is exactly the same figure of merit familiar to communications engineers in which the third-order intermodulation level, IMD3, is measured.

To quantify the effect of out-of-band signals, a new out-of-band (OOB) IIP3 figure of merit is introduced. This test also involves a two-tone stimulus; however, the two tones are placed out-of-band so that the lower IMD3 product lands in the middle of the filter pass band. At the output, only the IMD3 product is visible because the original two tones are filtered out. To calculate the OOB IIP3 at the input, the IMD3 level is referred to the input by the overall gain. The OOB IIP3 allows the user to predict the impact of out-of-band blockers or interferers at an arbitrary signal level on the in-band performance. The ratio of the desired input signal level to the input-referred IMD3 at a given blocker level represents a signal-to-distortion limit imposed by the out-of-band signals.