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100 MHz to 4000 MHz, Digitally Controlled RF Dual VGA

Data Sheet

ADRF6573

FEATURES

- Operating frequency range: 100 MHz to 4000 MHz
- Dual independent, digitally controlled VGA
- Single serial interface control for both channels
- 6-bit, 0.5 dB digital step attenuator
- 30.8 dB gain control range with ±0.15 dB gain accuracy at 2140 MHz
- 17.8 dB gain at minimum attenuation at 2140 MHz
- P1dB of 19.2 dBm at 2140 MHz
- OIP3 of 40.0 dBm at 2140 MHz
- RF input and RF output internally matched to 50 Ω
- Channel to channel isolation of 50 dB at 2140 MHz
- Single-supply operation from 4.75 V to 5.25 V
- Thermally efficient, 7 mm × 7 mm × 1.0 mm, 32-terminal LGA
- The companion ADL5240 integrates a gain block with a DSA

APPLICATIONS

- Wireless infrastructure
- Automated test equipment
- RF/IF gain controls

FUNCTIONAL BLOCK DIAGRAM

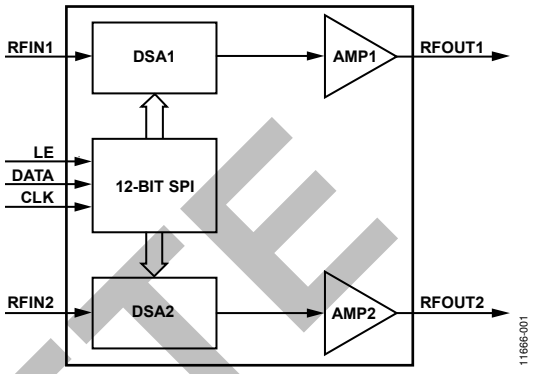

Figure 1.

GENERAL DESCRIPTION

The ADRF6573 is a high performance, digitally controlled, dual variable gain amplifier (VGA) operating from 100 MHz to 4000 MHz. Each channel includes a 6-bit digital step attenuator (DSA) with a 31.5 dB gain control range, 0.5 dB steps, and ±0.25 dB gain accuracy. The attenuation of the DSA is controlled using a serial peripheral interface (SPI). The SPI is a serial in, parallel out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: data, clock, and latch enable. The amplifier in each channel is a broadband linear amplifier that operates up to 4000 MHz.

The device is internally matched to 50 Ω at the input and output. Only input/output ac coupling capacitors and power supply decoupling capacitors are required for operation.

The ADRF6573 consumes 85 mA per channel and operates from a single supply ranging from 4.75 V to 5.25 V. It is fully specified for operation from −40°C to +85°C.

The ADRF6573 is packaged in a 32-terminal, 7 mm × 7 mm × 1.0 mm, land grid array (LGA) package.

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Rev. 0 Document Feedback

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REVISION HISTORY

7/14—Revision 0: Initial Version

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SPECIFICATIONS

VDD = 5 V, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		100		4000	MHz
Gain Control Range			31.5		dB
Gain Accuracy (Step Error)			±0.25		dB
FREQUENCY = 100 MHz					
Gain (Minimum Attenuation)			14.5		dB
Gain Control Range			27.0		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.27		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, output power (P_{OUT}) = −5 dBm/tone		18.5		dBm
Output 1dB Compression Point (P1dB)			16.5		dBm
Noise Figure (Minimum Attenuation)			4.8		dB
Channel to Channel Isolation			70		dB
Input Return Loss (S11)			−8.0		dB
Output Return Loss (S22)			−7.0		dB
Gain Flatness (Bandwidth = 100 MHz)			2.0		dB
FREQUENCY = 400 MHz					
Gain (Minimum Attenuation)			18.5		dB
Gain Control Range			30.5		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.15		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		36.0		dBm
Output 1dB Compression Point (P1dB)			21.0		dBm
Noise Figure (Minimum Attenuation)			4.4		dB
Channel to Channel Isolation			65		dB
Input Return Loss (S11)			−15.0		dB
Output Return Loss (S22)			−12.0		dB
Gain Flatness (Bandwidth = 100 MHz)			0.3		dB
FREQUENCY = 900 MHz					
Gain (Minimum Attenuation)		17.0	18.7	20.5	dB
Gain Control Range			30.8		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.15		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		37.5		dBm
Output 1dB Compression Point (P1dB)		17.5	19.5		dBm
Noise Figure (Minimum Attenuation)			4.6		dB
Channel to Channel Isolation			57		dB
Input Return Loss (S11)			−17.0		dB
Output Return Loss (S22)			−16.0		dB
Gain Flatness (Bandwidth = 100 MHz)			0.1		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY = 1900 MHz					
Gain (Minimum Attenuation)			18.0		dB
Gain Control Range			30.8		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.15		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		39.0		dBm
Output 1dB Compression Point (P1dB)			19.4		dBm
Noise Figure (Minimum Attenuation)			5.4		dB
Channel to Channel Isolation			57		dB
Input Return Loss (S11)			−9.0		dB
Output Return Loss (S22)			−10.0		dB
Gain Flatness (Bandwidth = 100 MHz)			0.1		dB
FREQUENCY = 2140 MHz					
Gain (Minimum Attenuation)			17.8		dB
Gain Control Range			30.8		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.15		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		40.0		dBm
Output 1dB Compression Point (P1dB)			19.2		dBm
Noise Figure (Minimum Attenuation)			5.5		dB
Channel to Channel Isolation			50		dB
Input Return Loss (S11)			−9.0		dB
Output Return Loss (S22)			−9.5		dB
Gain Flatness (Bandwidth = 100 MHz)			0.1		dB
FREQUENCY = 2600 MHz					
Gain (Minimum Attenuation)		15.0	17.3	19.0	dB
Gain Control Range			31.0		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.20		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		39.0		dBm
Output 1dB Compression Point (P1dB)		17.0	18.5		dBm
Noise Figure (Minimum Attenuation)			5.6		dB
Channel to Channel Isolation			50		dB
Input Return Loss (S11)			−10.0		dB
Output Return Loss (S22)			−9.5		dB
Gain Flatness (Bandwidth = 100 MHz)			0.1		dB
FREQUENCY = 3500 MHz					
Gain (Minimum Attenuation)			17.3		dB
Gain Control Range			31.8		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.30		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		33.5		dBm
Output 1dB Compression Point (P1dB)			17.9		dBm
Noise Figure (Minimum Attenuation)			6.1		dB
Channel to Channel Isolation			50		dB
Input Return Loss (S11)			−11.0		dB
Output Return Loss (S22)			−11.0		dB
Gain Flatness (Bandwidth = 100 MHz)			0.1		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY = 4000 MHz					
Gain (Minimum Attenuation)			16.6		dB
Gain Control Range			32.0		dB
Gain Control Step			0.5		dB
Gain Accuracy (Step Error)			±0.40		dB
Output Third-Order Intercept (OIP3)	Δf = 1 MHz, P_{OUT} = −5 dBm/tone		33.0		dBm
Output 1dB Compression Point (P1dB)			15.9		dBm
Noise Figure (Minimum Attenuation)			6.8		dB
Channel to Channel Isolation			42		dB
Input Return Loss (S11)			−8.0		dB
Output Return Loss (S22)			−8.0		dB
Gain Flatness (Bandwidth = 100 MHz)			0.4		dB
DIGITAL STEP ATTENUATOR GAIN SETTLING					
Minimum Attenuation to Maximum Attenuation			54		ns
Maximum Attenuation to Minimum Attenuation			54		ns
LOGIC INPUTS	CLK, DATA, LE, PUP				
Input High Voltage, V_{INH}		2.5			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{INH}/I_{INL}			0.1		µA
Input Capacitance, C_{IN}			1.5		pF
POWER SUPPLIES					
Voltage	VCC1, VCC2, VDD	4.75	5.0	5.25	V
Supply Current	Per channel, VCC1 or VCC2		85	110	mA
	VDD		0.5		mA

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VDD, VCC1, VCC2	6.5 V
Lead Temperature (Soldering, 60 sec)	240°C
Internal Power Dissipation	1.0 W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}[1, 2]	Maximum Allowable Temperature on Top Surface of Package
32-Terminal LGA	36°C/W	138°C

[1] See JEDEC standards JESD51-31, JESD51-9, and JESD51-5 for information on a multichip package.
[2] θ_{JA} is the junction to ambient thermal resistance value for the die with the highest thermal resistance.

See the Thermal Considerations section for additional information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

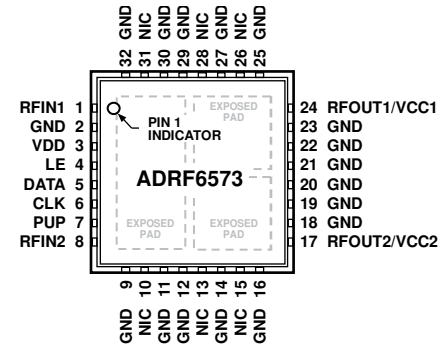

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN1	RF Input to the internal DSA1.
2, 9, 11, 12, 14, 16, 18 to 23, 25, 27, 29, 30, 32	GND	Ground.
3	VDD	Supply Voltage for DSA1 and DS2. Connect this pin to a 5 V supply.
4	LE	SPI Latch Enable Signal for the Internal DSA1 and the Internal DSA2.
5	DATA	SPI Data Signal for the Internal DSA1 and the Internal DSA2.
6	CLK	SPI Clock Signal for the Internal DSA1 and the Internal DSA2..
7	PUP	Initial Gain Selection Pin. Connect this pin to the supply voltage pins to get the maximum gain, and connect this pin to ground to achieve the minimum gain.
8	RFIN2	RF Input to the Internal DSA2.
10, 13, 15, 26, 28, 31	NIC	No Internal Connection.
17	RFOUT2/VCC2	RF Output from AMP2/Supply Voltage for Amplifier 2. A bias to the amplifier is provided through a choke inductor connected to this pin.
24	RFOUT1/VCC1	RF Output from AMP1/Supply Voltage for Amplifier 1. A bias to the amplifier is provided through a choke inductor connected to this pin.
	EPAD	Exposed Pads. Solder the exposed pads to a low impedance ground plane.

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TYPICAL PERFORMANCE CHARACTERISTICS

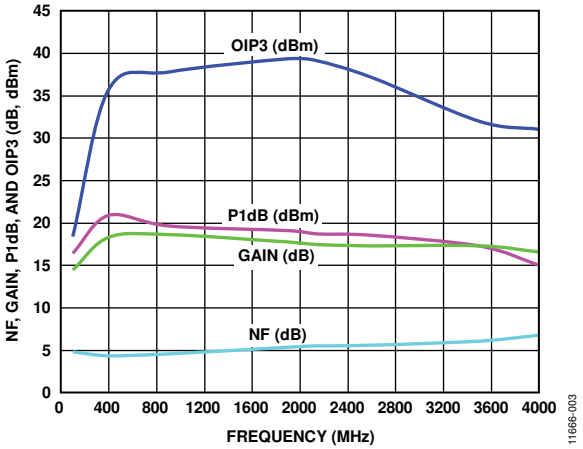

Figure 3. Noise Figure (NF), Gain, P1dB, and OIP3 at P_{OUT} = −5 dBm/Tone vs. Frequency, Minimum Attenuation State

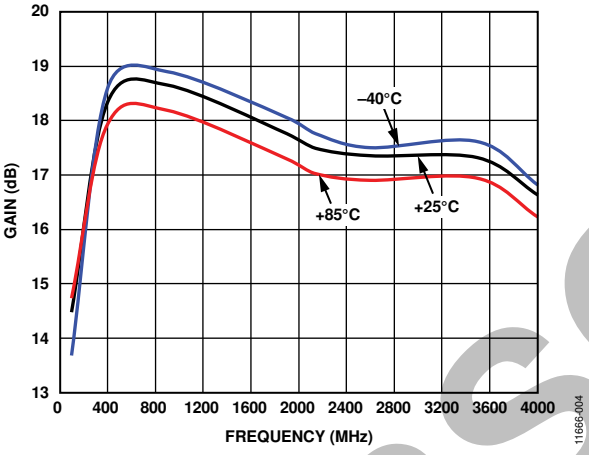

Figure 4. Gain vs. Frequency at Various Temperatures, Minimum Attenuation State

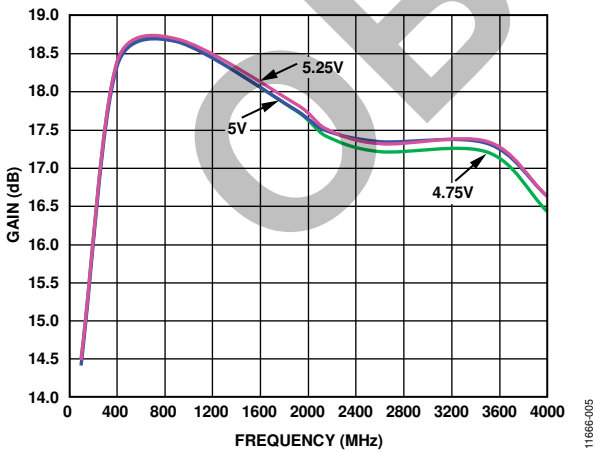

Figure 5. Gain vs. Frequency at Various Power Supplies, Minimum Attenuation State

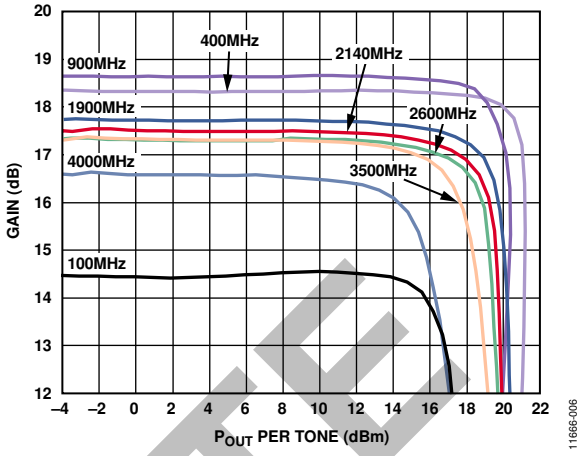

Figure 6. Gain vs. P_{OUT} per Tone at Various Frequencies, Minimum Attenuation State

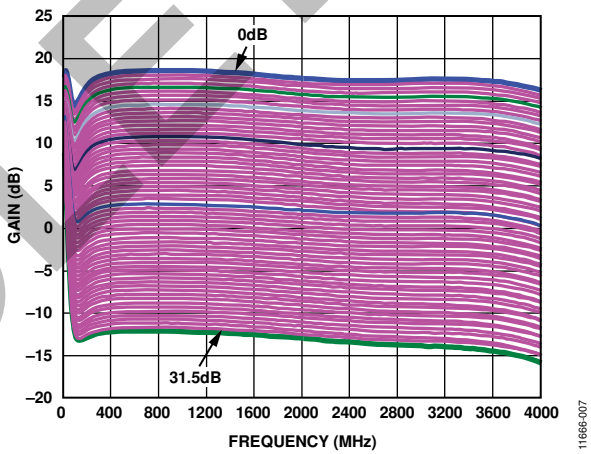

Figure 7. Gain vs. Frequency, All Attenuation States

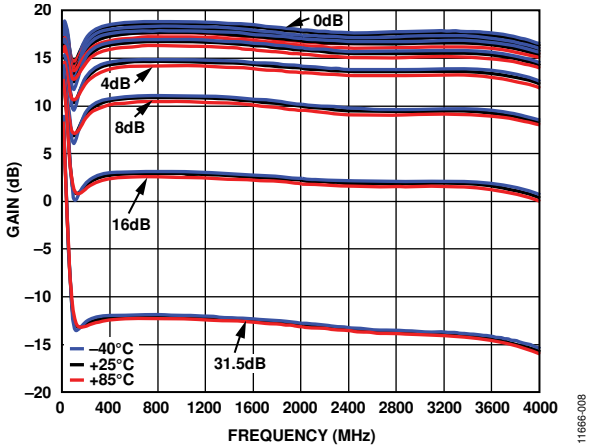

Figure 8. Gain vs. Frequency at Various Temperatures, Major Attenuation States

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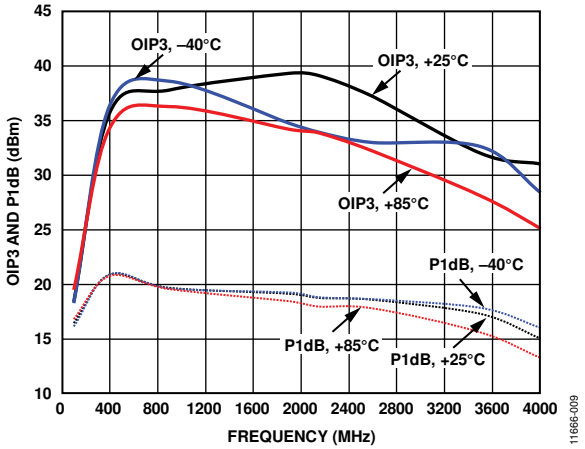

Figure 9. OIP3 and P1dB at P_{OUT} = –5 dBm/Tone vs. Frequency at Various Temperatures, Minimum Attenuation State

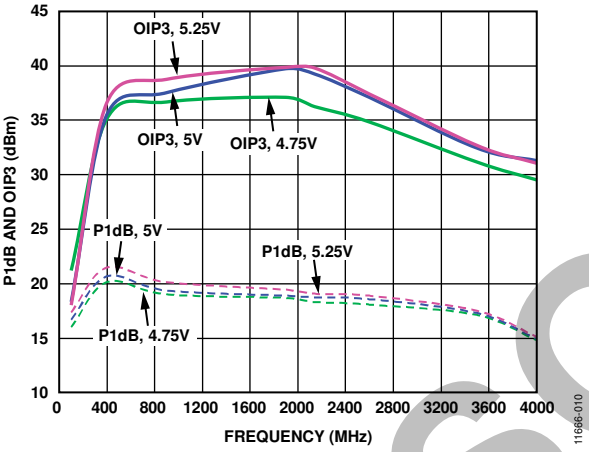

Figure 10. P1dB and OIP3 at P_{OUT} = –5 dBm/Tone vs. Frequency at Various Power Supplies, Minimum Attenuation State

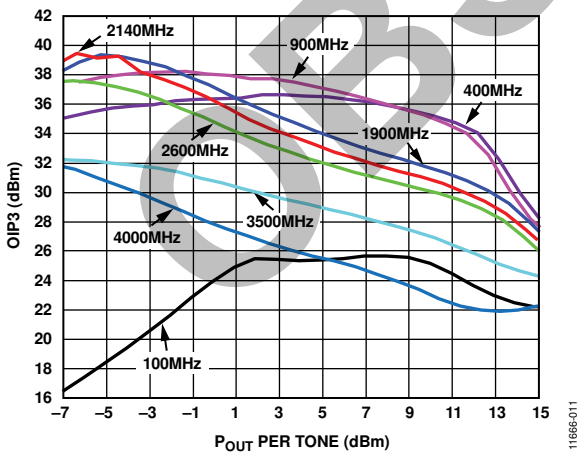

Figure 11. OIP3 vs. P_{OUT} per Tone at Various Frequencies, Minimum Attenuation State

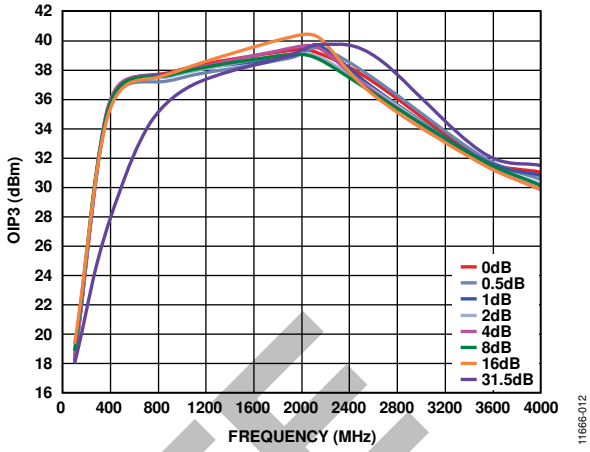

Figure 12. OIP3 at P_{OUT} = –5 dBm/Tone vs. Frequency, Major Attenuation States

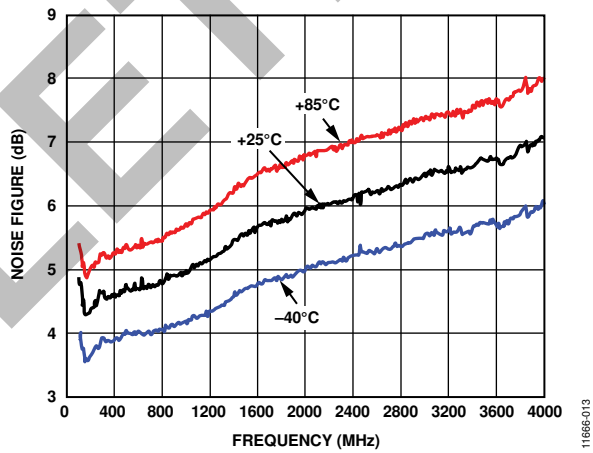

Figure 13. Noise Figure vs. Frequency at Various Temperatures, Minimum Attenuation State

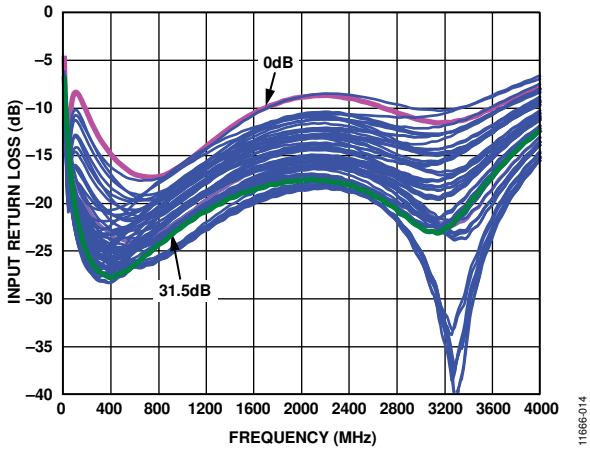

Figure 14. Input Return Loss (S11) vs. Frequency, All Attenuation States

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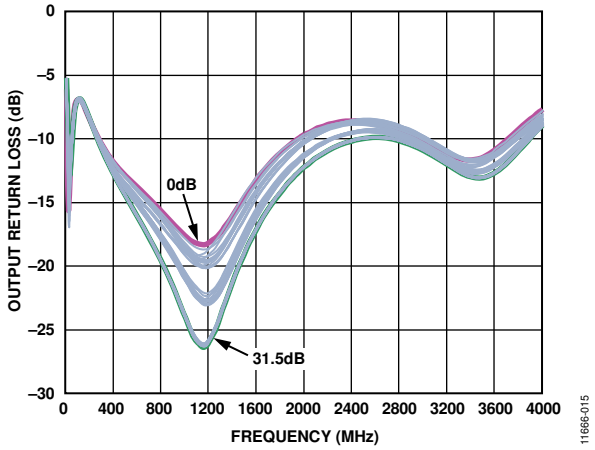

Figure 15. Output Return Loss (S22) vs. Frequency, All Attenuation States

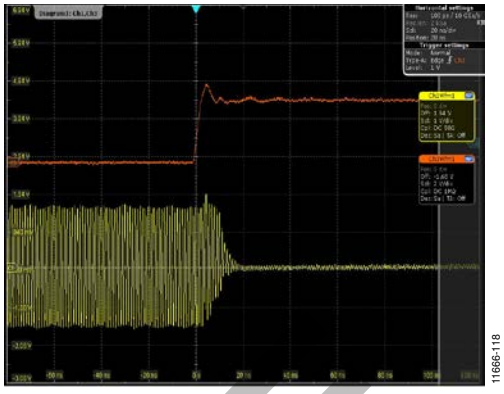

Figure 18. Gain Settling Time, 0 dB to 31.5 dB

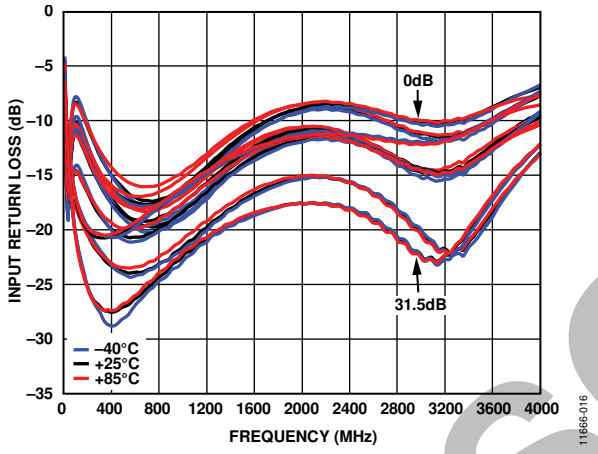

Figure 16. Input Return Loss (S11) vs. Frequency at Various Temperatures, Major Attenuation States

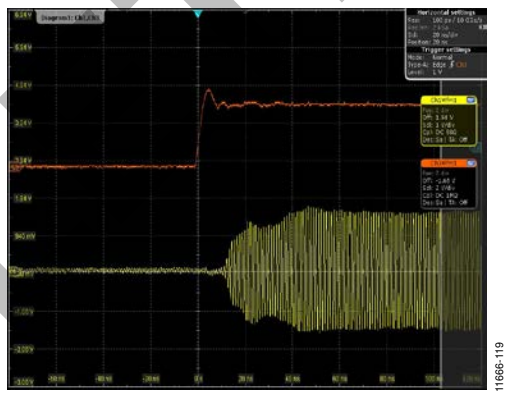

Figure 19. Gain Settling Time, 31.5 dB to 0 dB

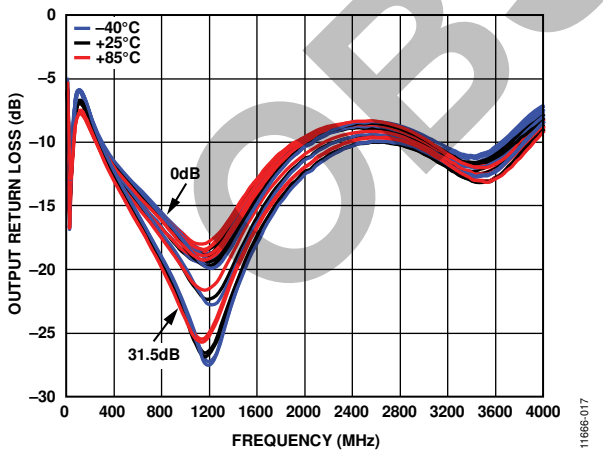

Figure 17. Output Return Loss (S22) vs. Frequency at Various Temperatures, Major Attenuation States

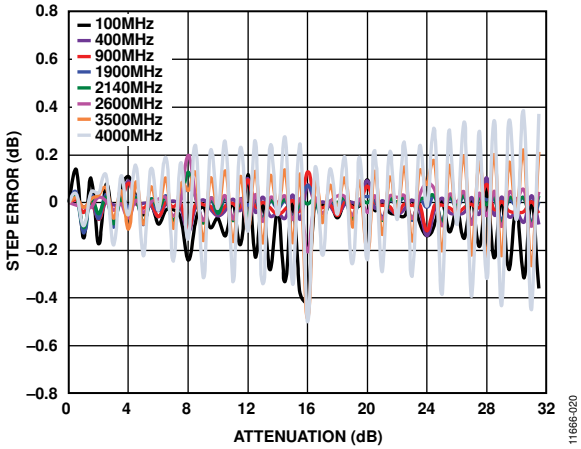

Figure 20. Step Error vs. Attenuation at Various Frequencies

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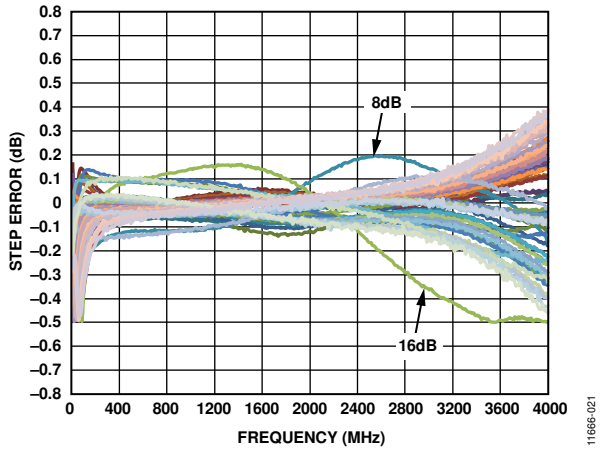

Figure 21. Step Error vs. Frequency, All Attenuation States

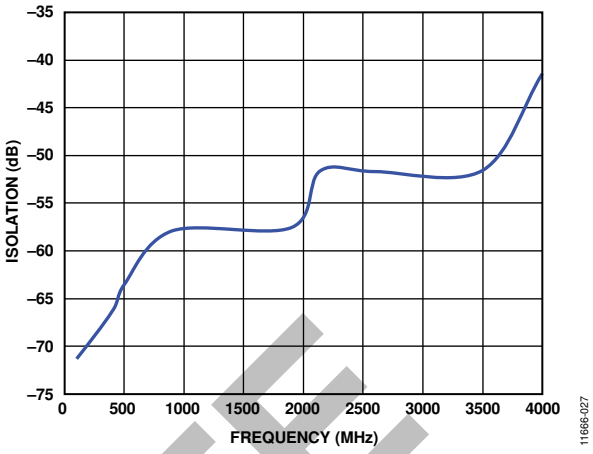

Figure 24. Channel to Channel Isolation

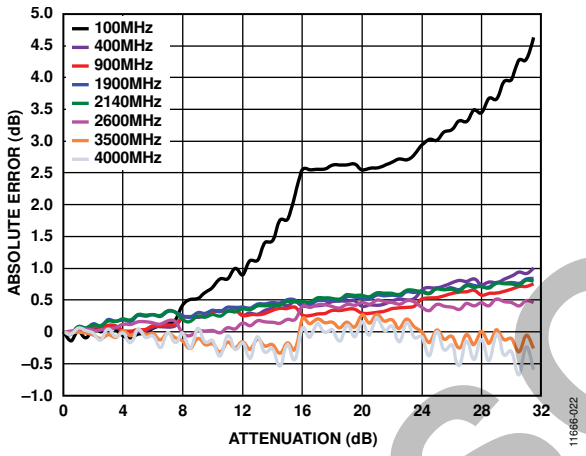

Figure 22. Absolute Error vs. Attenuation at Various Frequencies

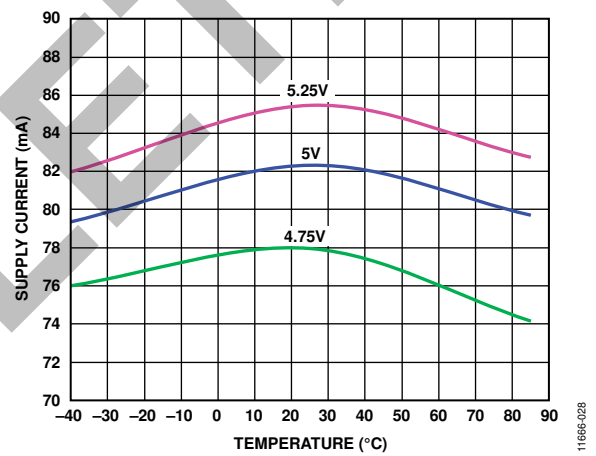

Figure 25. Supply Current vs. Temperature at Various Supply Voltages

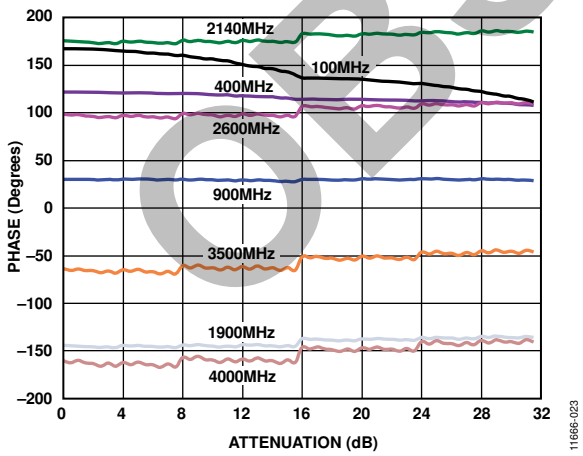

Figure 23. Phase vs. Attenuation at Various Frequencies

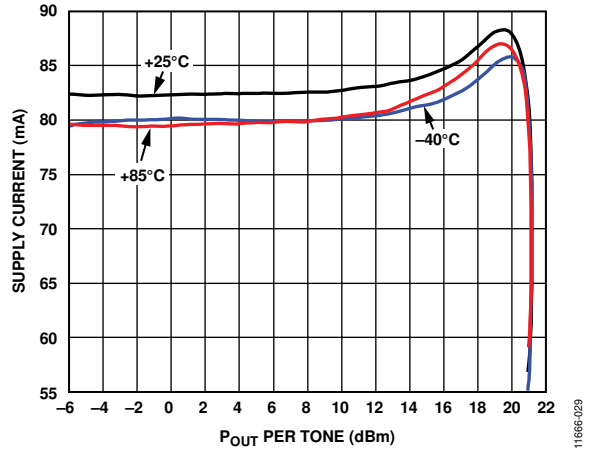

Figure 26. Supply Current vs. P_{OUT} per Tone at Various Temperatures

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APPLICATIONS INFORMATION

BASIC LAYOUT CONNECTIONS

The basic layout connections for operating the ADRF6573 are shown in Figure 27.

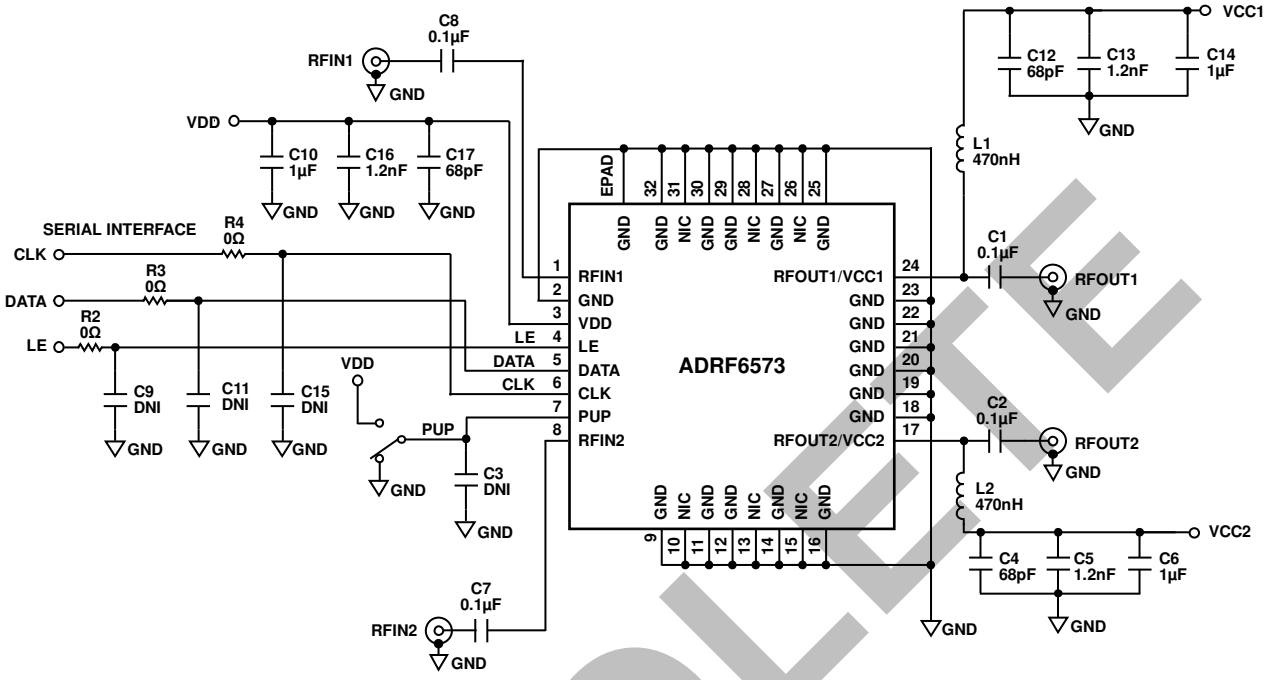

Figure 27. Basic Layout Connections

RFOUTx Biases

The dc biases for the amplifiers of RFOUT1 and RFOUT2 in the ADRF6573 are supplied through the L1 and L2 inductors and are connected to the RFOUT1 and RFOUT2 pins. Three decoupling capacitors for each pin are used to prevent RF signals from propagating onto the dc lines. The dc supply ranges from 4.75 V to 5.25 V, and it must be connected to the VCC1 and VCC2 test points on the evaluation board.

Digital Step Attenuators (DSAs) Biases

The biases for the DSAs are provided through the VDD pin. Decoupling capacitors are recommended on the VDD trace. The voltage ranges from 4.75 V to 5.25 V and must be connected to the VDD test point on the evaluation board. The DSAs work for dc voltages as low as 2.5 V.

RF Inputs Interface

RFIN1 (Pin 1) and RFIN2 (Pin 8) are the RF inputs for the DSA of the ADRF6573. The input impedance of the DSA is close to 50 Ω over the entire frequency range; therefore, no external components are required. Only dc blocking capacitors are required.

RF Outputs Interface

RFOUT2 (Pin 17) and RFOUT1 (Pin 24) are the RF outputs for the amplifiers of the ADRF6573. The amplifiers are internally matched to a 50 Ω impedance at the output; therefore, no external components are required. Only dc blocking capacitors are required. The biases are provided through these pins via choke inductors.

DSAs SPI Interface

The DSAs of the ADRF6573 can operate in serial mode. Pin 4 is the latch enable (LE), Pin 5 is the data (DATA), and Pin 6 is the clock (CLK). To prevent noise from coupling onto the digital signals, an RC filter can be used on each data line.

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SPI TIMING

Table 5 lists the timing characteristics for the SPI signals, including the CLK, LE, and DATA signals. Figure 28 shows the corresponding SPI timing diagram.

SPI TIMING SEQUENCE

Figure 29 is the timing sequence for the SPI function using 12-bit operation. The clock can be as fast as 20 MHz. D11 (MSB) comes in first and D0 (LSB) comes in last. D6 to D11 control Channel 1, and D0 to D5 control Channel 2 (see Table 6).

Table 5. SPI Timing Specifications

Parameter	Limit	Unit	Description
f_{CLK}	10	MHz	Serial clock frequency
t_1	25	ns min	Minimum period CLK in logic high state
t_2	25	ns min	Minimum period CLK in logic low state
t_3	10	ns min	Setup time between data and rising edge of CLK
t_4	10	ns min	Hold time between data and rising edge of CLK
t_5	10	ns min	Clock low to LE setup time
t_6	30	ns min	LE pulse width
t_7	10	ns min	Setup time between falling edge of LE and CLK

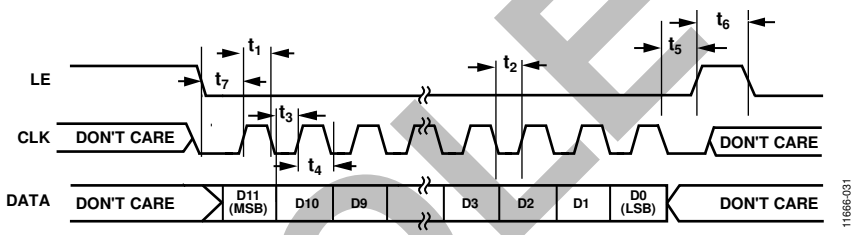

Figure 28. SPI Timing Specifications

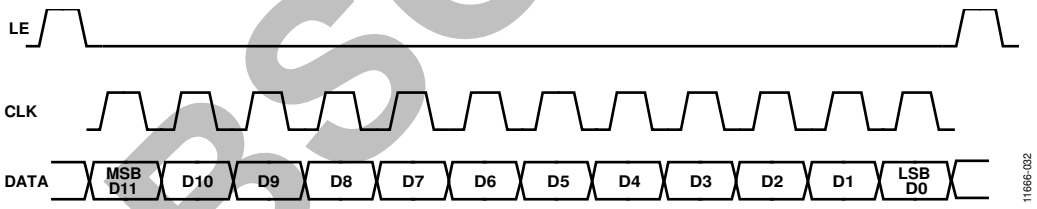

Figure 29. SPI Timing Sequence

Table 6. Channel 1 and Channel 2 DSA Attenuation Truth Table

	Channel 1						Channel 2					
Channel 1/Channel 2 Gain Relative to Maximum Gain (dB)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	1	1	1	1	1	1
−0.5	1	1	1	1	1	0	1	1	1	1	1	0
−1.0	1	1	1	1	0	1	1	1	1	1	0	1
−2.0	1	1	1	0	1	1	1	1	1	0	1	1
−4.0	1	1	0	1	1	1	1	1	0	1	1	1
−8.0	1	0	1	1	1	1	1	0	1	1	1	1
−16.0	0	1	1	1	1	1	0	1	1	1	1	1
−31.5	0	0	0	0	0	0	0	0	0	0	0	0

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Table 7. Initial Gain Selection

PUP	Relative to Maximum Gain (dB)
Connect to ground	−31.5
Connect to the supply voltage pins	0

The PUP pin is used to set up the initial gain relative to the maximum gain when the ADRF6573 is powered on. After the first LE pulse, PUP does not have any significance, and the SPI timing sequence takes over.

THERMAL CONSIDERATIONS

The ADRF6573 is packaged in a thermally efficient, 7 mm × 7 mm × 1.0 mm LGA package with a 5.3 mm × 5.3 mm center exposed pad. The thermal values detailed in Table 3 are extracted using the standard JEDEC 2s2p test board that is specified in the JESD51-9 and JESD51-5 standards with 25 thermal via holes under the exposed pad of the 32-terminal LGA package.

The ADRF6573 consumes approximately 85 mA per channel with a 5 V supply voltage. Even though the device dissipates less than 1 W, for the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LGA. Figure 30 shows a close up of the recommended thermal via distribution under the exposed pad.

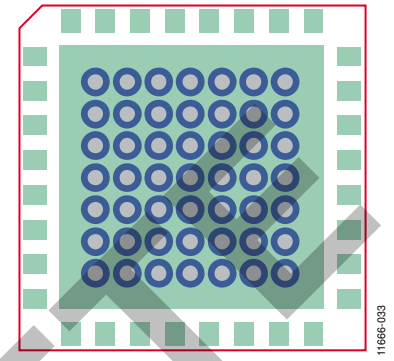

Figure 30. Recommended Printed Circuit Board (PCB) Footprint with the Recommended Thermal Via Distribution

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EVALUATION BOARD

The schematic of the ADRF6573 evaluation board is shown in Figure 34, the evaluation board configuration options are detailed in Table 8, and the layout of the ADRF6573 evaluation board is shown in Figure 32 and Figure 33. Each RF trace on the evaluation board has a characteristic impedance of 50 Ω and is fabricated on RO3003® material. In addition, each trace is a coplanar waveguide (CPWG) with a width of 25 mils, a spacing of 20 mils, and a dielectric thickness of 10 mils. Connecting a choke inductor to the RFOUTx pins provides the bias to the amplifiers. Bypassing capacitors are recommended on all supply lines to minimize the RF coupling. The DSAs and the amplifiers can be individually biased or connected to the VDD plane using the R1, R5, and R6 resistors.

The digital signal traces incorporate a footprint for an RC filter to prevent potential noise from coupling onto the signal. In normal operation, series resistors are 0 Ω, and shunt resistors and capacitors are open.

The evaluation board is controlled through an USB adaptor board from the PC USB port. USB-based programming software is available to download from the ADRF6573 product page. Figure 31 shows the window of the programming software. It is highly recommended to refer to the evaluation board layout for the optimal and stable performance of each block as well as for the improvement of thermal efficiency.

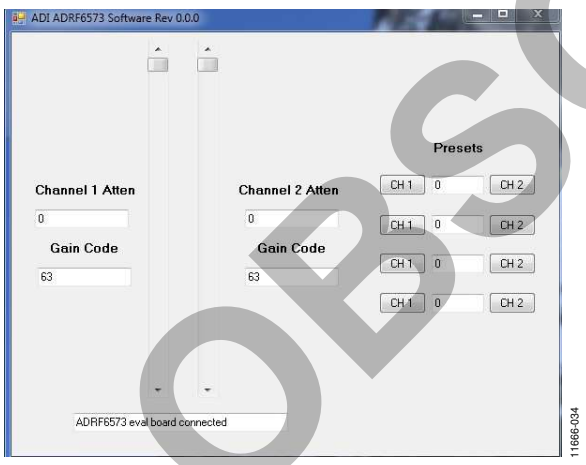

Figure 31. Evaluation Board Control Software

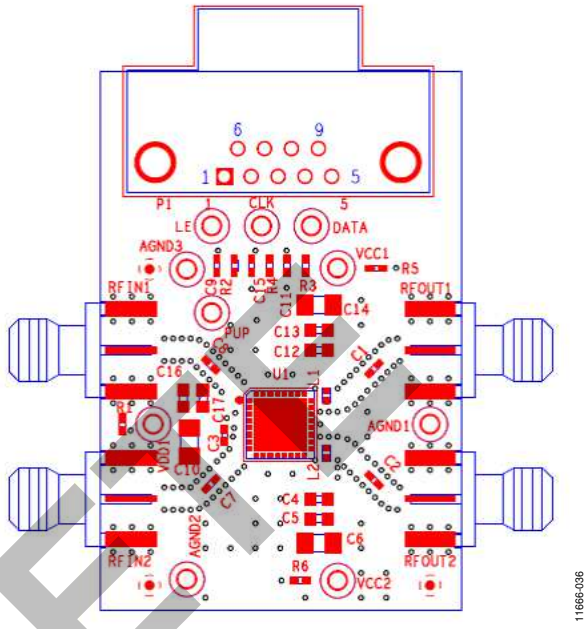

Figure 32. Evaluation Board Layout, Top

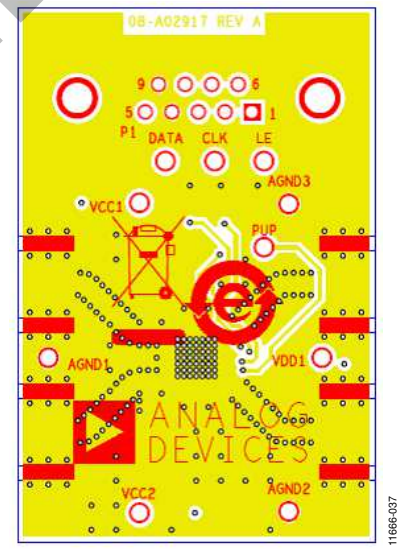

Figure 33. Evaluation Board Layout, Bottom

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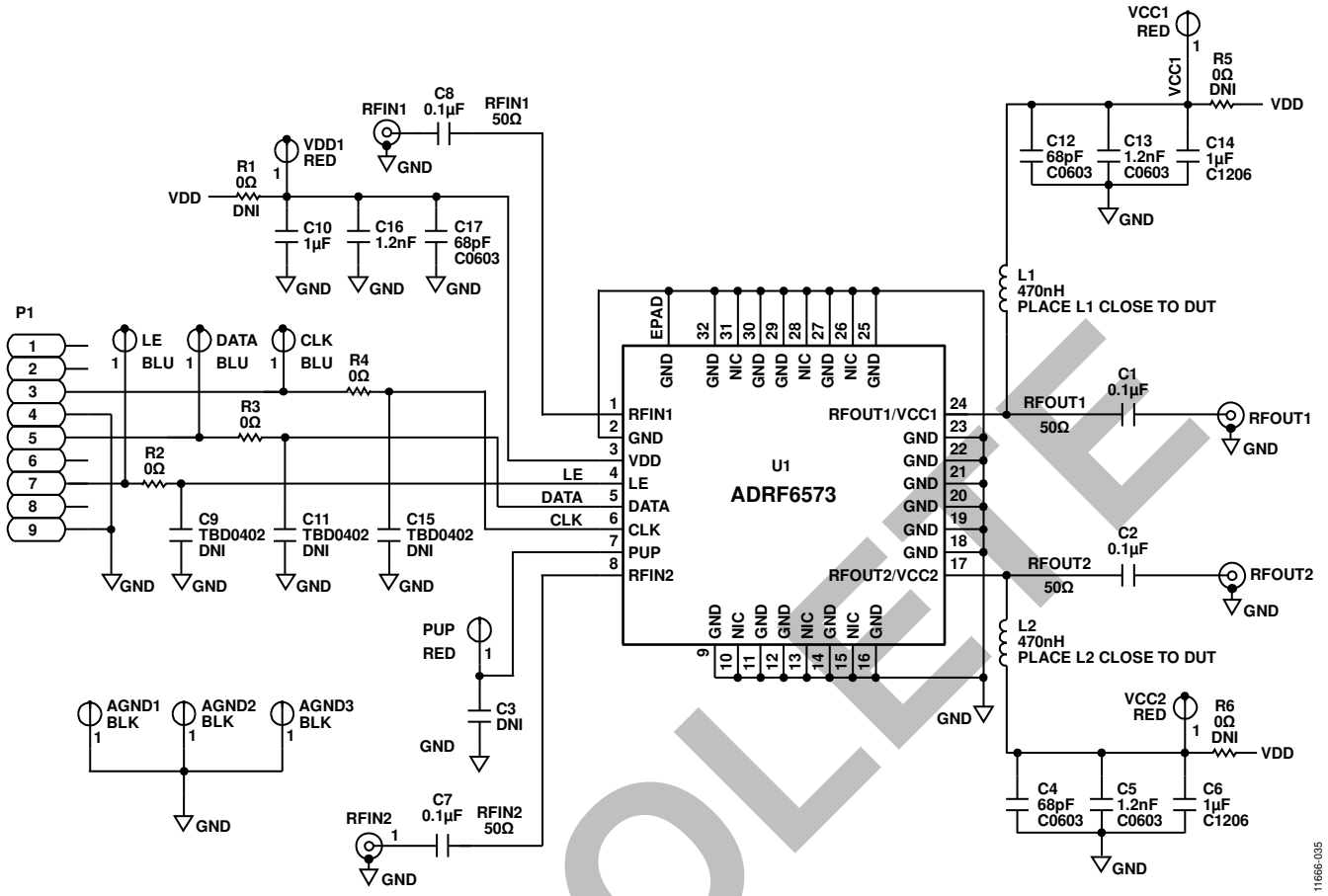

Figure 34. ADRF6573 Evaluation Board

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Table 8. Evaluation Board Configuration Options

Component	Function/Comments	Default Value
C1, C2	Output dc blocking capacitors for RFOUT1 and RFOUT2.	C1, C2 = 0.1 µF
C7, C8	Input dc blocking capacitors for RFIN1 and RFIN2.	C7, C8 = 0.1 µF
C4, C5, C6, C12, C13, C14	Power supply decoupling for amplifiers. The biases associated with the RFOUTx pins are the most sensitive to noise because the biases are connected directly to the output. Place the smallest capacitors (C4, C12) closest to the RFOUTx pins.	C4, C12 = 68 pF, C5, C13 = 1.2 nF, C6, C14 = 1 µF
C10, C16, C17	Power supply decoupling for the DSAs.	C10 = 1 µF, C16 = 1.2 nF, C17 = 68 pF
C3	Power supply decoupling for the PUP pin.	C3 = open
L1, L2	The bias for the amplifiers comes through L1 and L2 when VCC1 and VCC2 are connected to a 5 V supply. L1and L2 must be high impedance for the frequency of operation while providing low resistance for the dc current.	L1, L2 = 470 nH
R1, R5, R6	Resistors to connect the supply for the amplifiers and the DSA to the same VDD plane.	R1, R5, R6 = open
R2, R3, R4	Resistors of the RC filter on the digital signals leading to the SPI chip.	R2, R3, R4 = 0 Ω
C9, C11,C15	Capacitors of the RC filter on the digital signals leading to the SPI chip.	C9, C11, C15 = open

OUTLINE DIMENSIONS

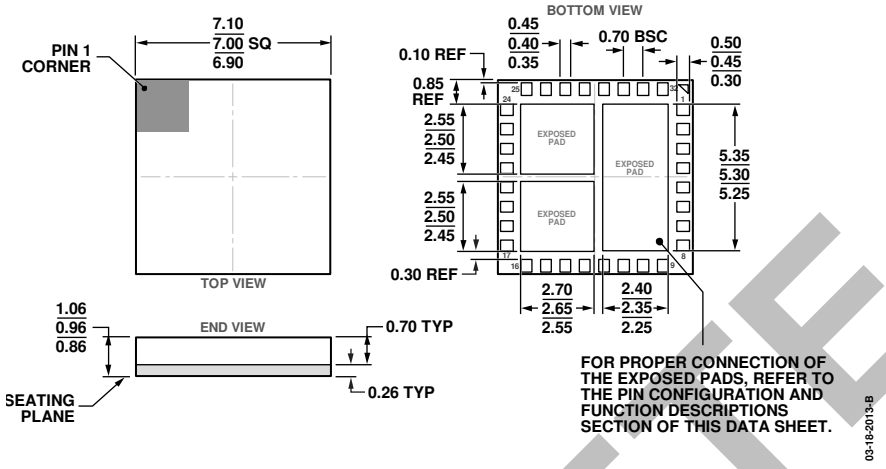

Figure 35. 32-Terminal Land Grid Array [LGA]
(CC-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6573ACCZ-R7	−40°C to +85°C	32-Terminal Land Grid Array [LGA]	CC-32-1
ADRF6573-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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