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700 MHz to 3000 MHz Dual Passive Receive Mixer with Integrated PLL and VCO

Data Sheet

ADRF6612

FEATURES

- RF frequency: 700 MHz to 3000 MHz, continuous
- LO input frequency: 200 MHz to 2700 MHz, high-side or low-side injection
- IF range: 40 MHz to 500 MHz
- Power conversion gain of 9.0 dB
- Single sideband (SSB) noise figure of 11.3 dB
- Input IP3 of 30 dBm
- Input P1dB of 10.6 dBm
- Typical LO input drive of 0 dBm
- Single-ended, 50 Ω RF port
- Single-ended or balanced LO input port
- Serial port interface (SPI) control on all functions
- Exposed pad, 7 mm × 7 mm, 48-lead LFCSP

APPLICATIONS

- Multiband/multistandard cellular base station diversity receivers
- Wideband radio link diversity downconverters
- Multimode cellular extenders and picocells

FUNCTIONAL BLOCK DIAGRAM

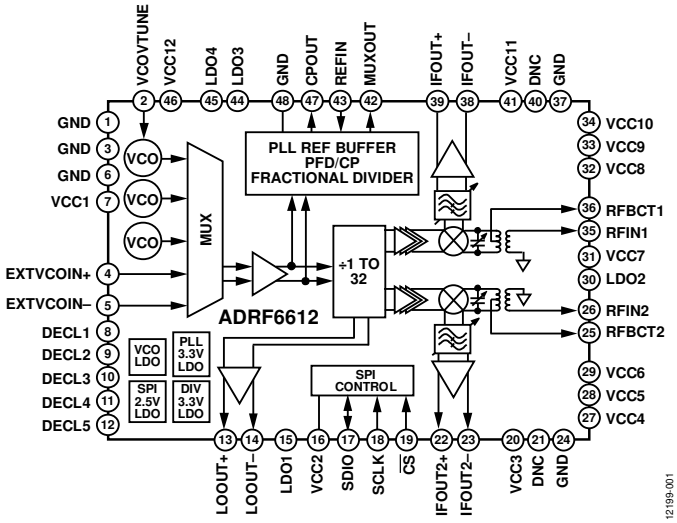

Figure 1.

GENERAL DESCRIPTION

The ADRF6612 is a dual radio frequency (RF) mixer and intermediate frequency (IF) amplifier with an integrated phase-locked loop (PLL) and voltage controlled oscillators (VCOs). The ADRF6612 uses revolutionary broadband square wave limiting local oscillator (LO) amplifiers to achieve an unprecedented RF bandwidth of 700 MHz to 3000 MHz. Unlike narrow-band sine wave LO amplifier solutions, the LO can be applied above or below the RF input over an extremely wide bandwidth. Energy storage elements are not utilized in the LO amplifier, thus dc current consumption also decreases with decreasing LO frequency.

The ADRF6612 utilizes highly linear, doubly balanced passive mixer cores with integrated RF and LO balancing circuits to allow single-ended operation. Integrated RF baluns allow optimal performance over the 700 MHz to 3000 MHz RF input frequency. The balanced passive mixer arrangement provides outstanding LO to RF and LO to IF leakages, excellent RF to IF isolation, and excellent intermodulation performance over the full RF bandwidth.

The balanced mixer cores provide extremely high input linearity, allowing the device to be used in demanding wideband applications where in band blocking signals may otherwise result in the degradation of dynamic range. Noise performance under blocking is comparable to narrow-band passive mixer designs. High linearity IF buffer amplifiers follow the passive mixer cores, yielding typical power conversion gains of 9 dB, and can be matched to a wide range of output impedances.

The PLL architecture supports both integer-N and fractional-N operation and can generate the entire LO frequency range of 200 MHz to 2700 MHz using an external reference input frequency anywhere in the range of 12 MHz to 320 MHz. An external loop filter provides flexibility in trading off phase noise vs. acquisition time. To reduce fractional spurs in fractional-N mode, a sigma-delta (Σ-Δ) modulator controls the post-VCO programmable divider. The VCO consists of multiple VCO cores.

All features of the ADRF6612 are controlled via a 3-wire SPI resulting in optimum performance and minimum external components.

The ADRF6612 is fabricated using a BiCMOS, high performance IC process. The device is available in a 7 mm × 7 mm, 48-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is available.

Rev. A

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ADRF6612* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6612 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6612: 700 MHz to 3000MHz Dual Passive Receive Mixer with Integrated PLL and VCO Data Sheet

User Guides

- UG-968: Evaluating the ADRF6612/ADRF6614, 700 MHz to 3000 MHz Rx Dual Mixer with Integrated Fractional-N PLL and VCO

REFERENCE MATERIALS

Press

- Analog Devices Introduces High-Performance RF ICs for Multi-band Base Stations and Microwave Point-to-Point Radios

DESIGN RESOURCES

- ADRF6612 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6612 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

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5/2016—Rev. 0 to Rev. A

Changes to Table 19 ... 32
Changes to Address: 0x22, Reset: 0x000A, Name: VCO_CTRL1
Section and Table 34 ... 45
Updated Outline Dimensions ... 57
Changes to Ordering Guide ... 57

12/2014—Revision 0: Initial Version

SPECIFICATIONS

RF SPECIFICATIONS

T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, Z_O = 50 Ω, frequency of the reference (f_{REF}) = 122.88 MHz, f_{REF} power = 4 dBm, f_{PFD} = 1.536 MHz, low-side LO injection, optimum RF balun (RFB) and low-pass filter (LPF) settings, unless otherwise noted.

Table 1. High Performance Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INTERFACE					
Return Loss	Tunable to >20 dB broadband via serial port		17.9		dB
Input Impedance			50		Ω
RF Frequency Range (f_{RF})		700		3000	MHz
IF OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		300||1.5		Ω||pF
IF Frequency Range		40		500	MHz
DC Bias Voltage[1]	Externally generated		IFOUTx±		V
EXTERNAL LO INPUT					
External LO Power Input		−5	0	+5	dBm
Return Loss			−11		dB
Input Impedance			50		Ω
External VCO Input Frequency	External VCO input supports divide by 1, 2, 4, 8, 16, and 32	250		5700	MHz
LO Frequency Range	Low-side or high-side LO, internally or externally generated	250		2850	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	4:1 IF port transformer and printed circuit board (PCB) loss removed		9.0		dB
Voltage Conversion Gain	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 200 Ω		15.0		dB
SSB Noise Figure			11.3		dB
IF Output Phase Noise Under Blocking	10 dBm blocker present 10 MHz above desired RF input, f_{RF} = 1900 MHz, f_{BLOCK} = 1910 MHz, f_{LO} = 1697 MHz, IF = 203 MHz, $IF_{BLOCKER}$ = 213 MHz		−153		dBc/Hz
Input Third-Order Intercept (IIP3)	f_{RF1} = 1900 MHz, f_{RF2} = 1901 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		30		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 1900 MHz, f_{RF2} = 1950 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		60		dBm
Input 1 dB Compression Point (P1dB)			10.6		dBm
LO to IF Output Leakage	Unfiltered IF output		−35		dBm
LO to RF Input Leakage			−45		dBm
RF to IF Output Isolation			−22		dB
IF/2 Spurious	−10 dBm input power		−72		dBc
IF/3 Spurious	−10 dBm input power		−69		dBc
POWER INTERFACE					
VCC12, VCC7, VCC2, VCC1					
Supply Voltage		3.55	3.7	3.85	V
Quiescent Current			260		mA
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−					
Supply Voltage		3.55	5	5.25	V
Quiescent Current			214		mA
LO OUTPUT (LOOUT+, LOOUT−)					
Frequency Range		200		2700	MHz
Output Level	Adjustable via SPI in four steps, in 50 Ω balanced load	−5		+7	dBm
Output Impedance	Balanced		50		Ω

[1] Supply voltage must be applied from the external circuit through choke inductors.

T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, Z_O = 50 Ω, f_{REF} = 122.88 MHz, f_{REF} power = 4 dBm, f_{PFD} = 1.536 MHz, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

Table 2. High Efficiency Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Gain	4:1 IF port transformer and PCB loss removed		8.7		dB
Voltage Conversion Gain	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 200 Ω		14.7		dB
SSB Noise Figure			10.7		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 1900 MHz, f_{RF2} = 1901 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		20.5		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 1900 MHz, f_{RF2} = 1950 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		53		dBm
Input 1 dB Compression Point (P1dB)			8.2		dBm
LO to IF Output Leakage	Unfiltered IF output		−45.0		dBm
LO to RF Input Leakage			−52.0		dBm
RF to IF Output Isolation			−22.8		dB
IF/2 Spurious	−10 dBm input power		−58		dBc
IF/3 Spurious	−10 dBm input power		−58		dBc
POWER INTERFACE					
VCC12, VCC7, VCC2, VCC1					
Supply Voltage		3.55	3.7	3.85	V
Quiescent Current			260		mA
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−					
Supply Voltage		3.55	3.7	5.25	V
Quiescent Current			210		mA

SYNTHESIZER/PLL SPECIFICATIONS

High performance mode, T_A = 25°C, measured on LO output, f_{LO} = 1700 MHz, Z_O = 50 Ω, f_{REF} =122.88 MHz, f_{PFD} = 1.536 MHz, f_{REF} power = 4 dBm, CSCALE = 8 mA, bleed = 0 µA, ABLDLY = 0.9 ns, integer mode loop filter, unless otherwise noted.

Table 3. Integer Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to 1 × LO				
Frequency Range	Internally generated LO	200		2700	MHz
Figure of Merit (FOM)[1]	P_{REFIN} = 6.5 dBm		−223		dBc/Hz/Hz
Phase and Frequency Detector (PFD) Frequency (f_{PFD})		0.8		70	MHz
Reference Spurs	f_{PFD} = 1.536 MHz				
	1 × f_{PFD}		−105		dBc
	4 × f_{PFD}		−105		dBc
	>4 × f_{PFD}		−90		dBc
CHARGE PUMP					
Pump Current	Programmable to 250 µA, 500 µA, …, 8 mA		8	8.75	mA
Output Compliance Range		0.7		2.5	V
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
REFIN Input Frequency		12		320	MHz
REFIN Input Capacitance			4		pF
Reference Divider Value	Programmable to 0.5, 1, 2, 3, …, 2047	0.5		2047	
MUXOUT Output Level	VOL (lock detect output selected)			0.25	V
	VOH (lock detect output selected)	2.7			V
MUXOUT Duty Cycle	Reference output selected		50		%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO_0					
Phase Noise, Locked	f_{LO} = 5.1 GHz				
	1 kHz offset		−87		dBc/Hz
	50 kHz offset		−94.9		dBc/Hz
	100 kHz offset		−103.3		dBc/Hz
	1 MHz offset		−132.9		dBc/Hz
	10 MHz offset		−154.1		dBc/Hz
	40 MHz offset		−155.2		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.87		°rms
VCO_1					
Phase Noise, Locked	f_{LO} = 4.45 GHz				
	1 kHz offset		−90		dBc/Hz
	50 kHz offset		−98.4		dBc/Hz
	100 kHz offset		−106.5		dBc/Hz
	1 MHz offset		−136.1		dBc/Hz
	10 MHz offset		−154.8		dBc/Hz
	40 MHz offset		−155.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.63		°rms
VCO_2					
Phase Noise, Locked	f_{LO} = 3.8 GHz				
	1 kHz offset		−90		dBc/Hz
	50 kHz offset		−98.1		dBc/Hz
	100 kHz offset		−109.8		dBc/Hz
	1 MHz offset		−137.1		dBc/Hz
	10 MHz offset		−155.7		dBc/Hz
	40 MHz offset		−156.2		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.61		°rms
VCO_3					
Phase Noise, Locked	f_{LO} = 3.2 GHz				
	1 kHz offset		−89		dBc/Hz
	50 kHz offset		−97.2		dBc/Hz
	100 kHz offset		−107		dBc/Hz
	1 MHz offset		−136.2		dBc/Hz
	10 MHz offset		−155.7		dBc/Hz
	40 MHz offset		−157.3		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.64		°rms

[1] The FOM is computed as phase noise (dBc/Hz) − 10Log10(f_{PFD}) − 20Log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 122.88 MHz and f_{REF} power = 6.5 dBm with a 1.536 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

High performance mode, T_A = 25°C, measured on LO output, f_{LO} = 1700 MHz, Z_O = 50 Ω, f_{REF} =122.88 MHz, f_{PFD} = 30.72 MHz, f_{REF} power = 4 dBm, CSCALE = 250 µA, bleed = 93.75 µA, ABLDLY = 0 ns, fractional mode loop filter, unless otherwise noted.

Table 4. Fractional Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to 1 × LO				
FOM[1]	P_{REFIN} = 6.5 dBm		219		dBc/Hz/Hz
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
VCO_0					
Phase Noise, Locked	f_{LO} = 2.55 GHz				
	1 kHz offset		−92.5		dBc/Hz
	50 kHz offset		−97.4		dBc/Hz
	100 kHz offset		−109.7		dBc/Hz
	1 MHz offset		−137.6		dBc/Hz
	10 MHz offset		−153.6		dBc/Hz
	40 MHz offset		−155.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.36		°rms
VCO_1					
Phase Noise, Locked	f_{LO} = 2.22 GHz				
	1 kHz offset		−93.6		dBc/Hz
	50 kHz offset		−101.8		dBc/Hz
	100 kHz offset		−112.5		dBc/Hz
	1 MHz offset		−140.5		dBc/Hz
	10 MHz offset		−154.3		dBc/Hz
	40 MHz offset		−155.3		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.32		°rms
VCO_2	f_{LO} = 1.9 GHz				
Phase Noise, Locked	1 kHz offset		−94.2		dBc/Hz
	50 kHz offset		−101.7		dBc/Hz
	100 kHz offset		−112.4		dBc/Hz
	1 MHz offset		−141.3		dBc/Hz
	10 MHz offset		−155.8		dBc/Hz
	40 MHz offset		−156.8		dBc/Hz
	1 kHz to 40 MHz integration bandwidth		0.32		°rms
Integrated Phase Noise					
VCO_3	f_{LO} = 1.6 GHz				
Phase Noise, Locked	1 kHz offset		−93.1		dBc/Hz
	50 kHz offset		−99.8		dBc/Hz
	100 kHz offset		−110.9		dBc/Hz
	1 MHz offset		−140.2		dBc/Hz
	10 MHz offset		−155.7		dBc/Hz
	40 MHz offset		−157.2		dBc/Hz
	1 kHz to 40 MHz integration bandwidth		0.33		°rms

[1] The FOM is computed as phase noise (dBc/Hz) − 10Log10(f_{PFD}) − 20Log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 122.88 MHz and f_{REF} power = 6.5 dBm with a 30.72 MHz f_{PFD}. The FOM was computed at 45 kHz offset.

VCO SPECIFICATIONS, OPEN-LOOP

High performance mode, T_A = 25°C, measured on LO output, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO_0 PHASE NOISE	f_{VCO} = 5.15 GHz				
	1 kHz offset		−50		dBc/Hz
	50 kHz offset		−104.4		dBc/Hz
	100 kHz offset		−112.6		dBc/Hz
	1 MHz offset		−137.7		dBc/Hz
	10 MHz offset		−154		dBc/Hz
	40 MHz offset		−155.1		dBc/Hz
VCO_1 PHASE NOISE	f_{VCO} = 4.3 GHz				
	1 kHz offset		−54		dBc/Hz
	50 kHz offset		−106.1		dBc/Hz
	100 kHz offset		−115		dBc/Hz
	1 MHz offset		−138.9		dBc/Hz
	10 MHz offset		−155.8		dBc/Hz
	40 MHz offset		−155.2		dBc/Hz
VCO_2 PHASE NOISE	f_{VCO} = 3.8 GHz				
	1 kHz offset		−53.6		dBc/Hz
	50 kHz offset		−106.6		dBc/Hz
	100 kHz offset		−114.6		dBc/Hz
	1 MHz offset		−140.8		dBc/Hz
	10 MHz offset		−155.4		dBc/Hz
	40 MHz offset		−156.3		dBc/Hz
VCO_3 PHASE NOISE	f_{VCO} = 3.2 GHz				
	1 kHz offset		−48.5		dBc/Hz
	50 kHz offset		−106		dBc/Hz
	100 kHz offset		−115.3		dBc/Hz
	1 MHz offset		−140.2		dBc/Hz
	10 MHz offset		−157.7		dBc/Hz
	40 MHz offset		−156.3		dBc/Hz

LOGIC INPUT AND POWER SPECIFICATIONS

T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, Z_O = 50 Ω, f_{REF} = 122.88 MHz, f_{REF} power = 4 dBm, f_{PFD} = 1.536 MHz, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	SCLK, SDIO, $\overline{CS}$				
Input High Voltage, V_{IH}		1.4		3.3	V
Input Low Voltage, V_{IL}		0		0.7	V
Input Current, I_{INH}/I_{INL}			0.1		µA
POWER SUPPLIES					
High Performance Mode					
Voltage Range					
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−		4.75	5	5.25	V
VCC12, VCC7, VCC2, VCC1		3.55	3.7	5.25	V
Power Dissipation	Internal LO mode (internal PLL)				
	External LO output enabled		2.7		W
	External LO output disabled		2.5		W
High Efficiency Mode					
Voltage Range					
VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, VCC10, VCC11,VCC12, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−		3.55	3.7	3.85	V
Power Dissipation	Internal LO mode (internal PLL)				
	External LO output enabled		2.0		W
	External LO output disabled		1.8		W

DIGITAL LOGIC SPECIFICATIONS

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.70	V
Output Voltage High	V_{OH}	I_{OH} = −100 µA	2.3			V
Output Voltage Low	V_{OL}	I_{OL} = 100 µA			0.2	V
Serial Clock Period	t_{CLK}		38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}		8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}		8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	t_S		10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	t_H		10			ns
Minimum Period for SCLK to Be in a Logic High State	t_{HIGH}		10			ns
Minimum Period for SCLK to Be in a Logic Low State	t_{LOW}		10			ns
Maximum Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}				231	ns
Maximum Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	t_Z				5	ns

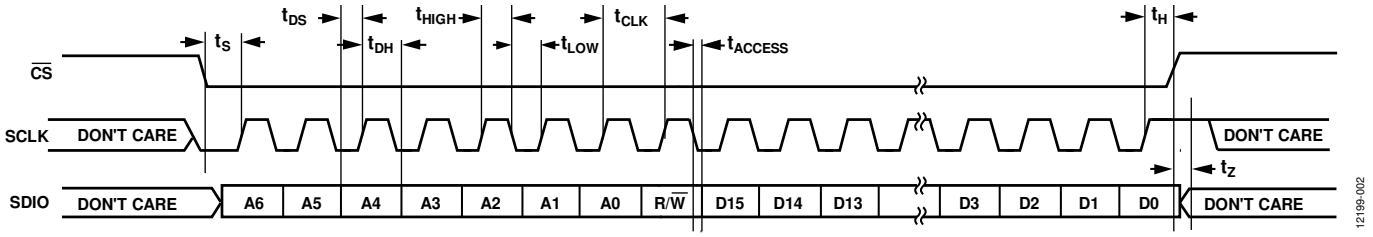

Figure 2. Setup and Hold Timing Measurements

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply Voltage (VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, VCC10, VCC11,VCC12, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−)	−0.5 V to +5.5 V
Digital Input/Output (SCLK, SDIO, $\overline{CS}$)	−0.3 V to +3.6 V
RFINx	20 dBm
EXTVCOIN+, EXTVCOIN−	13 dBm
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JC} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	θ_{JC}	Unit
48-Lead LFCSP	1.62	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

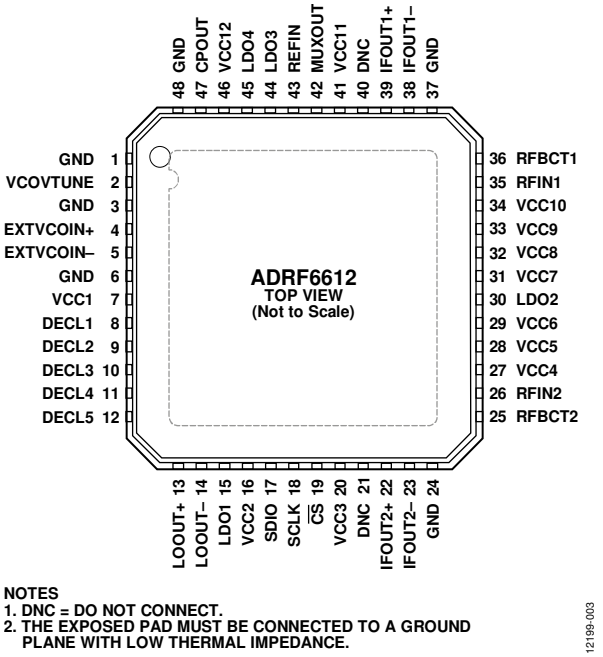

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Common Ground Connection for External Loop Filter.
2	VCOVTUNE	Control Voltage for Internal VCO.
3, 6	GND	Common Ground for External VCO.
4, 5	EXTVCOIN+, EXTVCOIN–	Inputs from External VCO to Internal Divider.
7	VCC1	3.7 V VCO Supply.
8, 9	DECL1, DECL2	LDO Output Decouplers for VCO.
10, 11	DECL3, DECL4	External Decouplers for VCO Buffer.
12	DECL5	External Decoupler for VCO Circuitry.
13, 14	LOOUT+, LOOUT–	Differential Outputs of Internally Generated LO.
15	LDO1	External Decoupling for Internal 2.5 V SPI Port LDO.
16	VCC2	3.7 V Supply for Programmable SPI Port.
17	SDIO	Serial Data Input/Output for Programmable SPI Port.
18	SCLK	Clock for Programmable SPI Port.
19	$\overline{CS}$	SPI Chip Select, Asserted Low.
20, 41	VCC3, VCC11	5 V Biases for Channel 1 and Channel 2 IF.
21, 40	DNC	Do Not Connect. Do not connect this pin externally.
22, 23	IFOUT2+, IFOUT2–	Channel 2 Differential IF Outputs.
24, 37	GND, GND	Ground Connections for Channel 1 and Channel 2 IF Stage.
25	RFBCT2	Balun Center Tap Connection for Channel 2 RF Input.
26	RFIN2	Channel 2 RF Input.
27, 28, 29	VCC4, VCC5, VCC6	5 V Supplies for Mixer LO Amplifiers.
30	LDO2	External Decoupling for Internal 3.3 V PLL/Divider LDO.
31	VCC7	3.7 V Supply for Mixer LO Divider Chain.
32, 33, 34	VCC8, VCC9, VCC10	5 V Supplies for Mixer LO Amplifiers.
35	RFIN1	Channel 1 RF Input.
36	RFBCT1	Balun Center Tap Connection for Channel 1 RF Input.
38, 39	IFOUT1–, IFOUT1+	Channel 1 Differential IF Outputs.
42	MUXOUT	Internal Multiplexer Output.

Pin No.	Mnemonic	Description
43	REFIN	Reference Input for Internal PLL (Single-Ended, CMOS).
44	LDO3	External Decoupling for Internal 2.5 V PLL LDO.
45	LDO4	External Decoupling for Internal 3.3 V PLL LDO.
46	VCC12	3.7 V Supply for Internal PLL.
47	CPOUT	Charge Pump Output.
48	GND	Common Ground for External Charge Pump.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

MIXER, HIGH PERFORMANCE MODE

T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, Z_O = 50 Ω, f_{REF} = 122.88 MHz, f_{REF} power = 4 dBm, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted. For integer mode: f_{PFD} = 1.536 MHz, CSCALE = 8 mA, bleed = 0 µA, ABLDLY = 0.9 ns. For fractional mode: f_{PFD} = 30.72 MHz, CSCALE = 250 µA, bleed = 93.75 µA, ABLDLY = 0.0 ns.

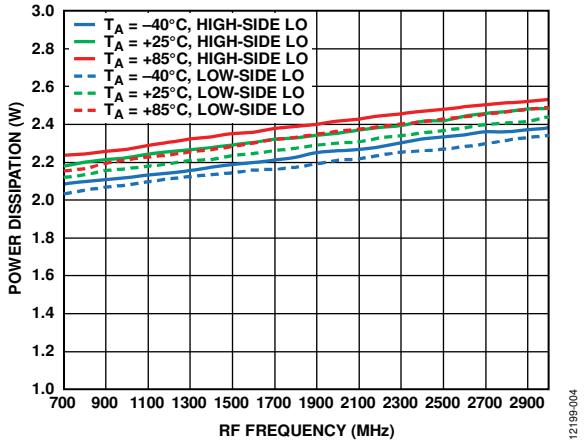

Figure 4. Power Dissipation vs. RF Frequency over Three Temperatures

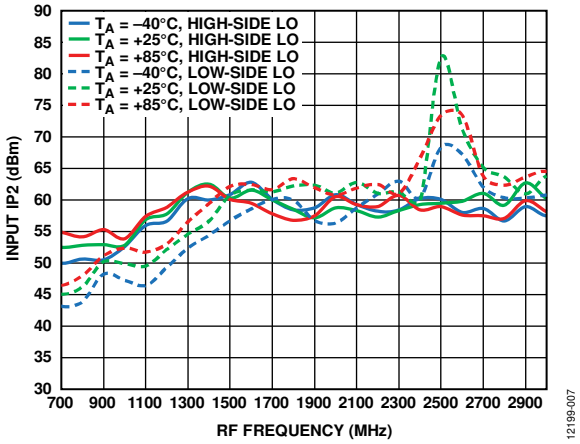

Figure 7. Input IP2 vs. RF Frequency over Three Temperatures

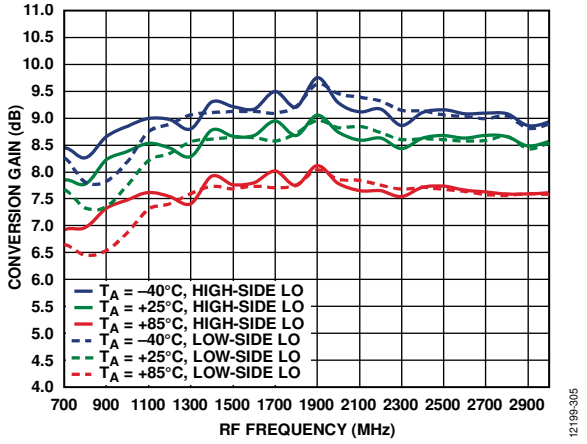

Figure 5. Power Conversion Gain vs. RF Frequency over Three Temperatures, IF Balun and Board Loss Removed

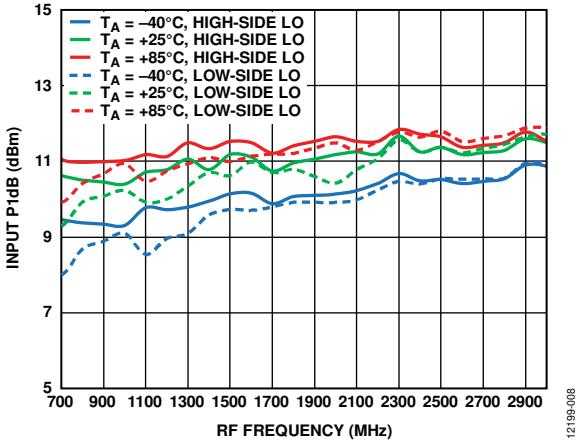

Figure 8. Input P1dB vs. RF Frequency over Three Temperatures

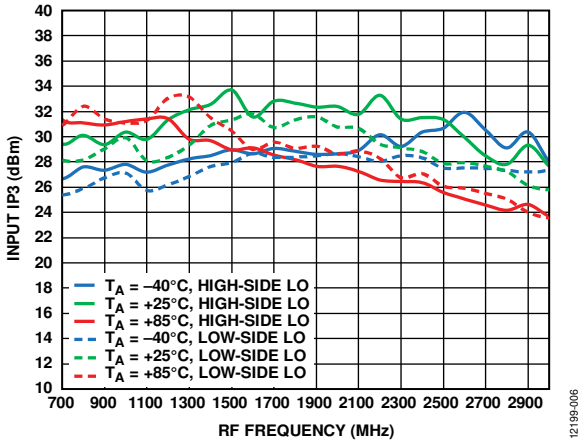

Figure 6. Input IP3 vs. RF Frequency over Three Temperatures

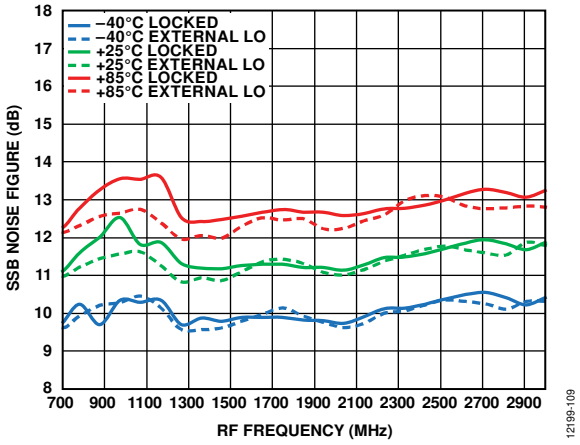

Figure 9. SSB Noise Figure vs. RF Frequency over Three Temperatures

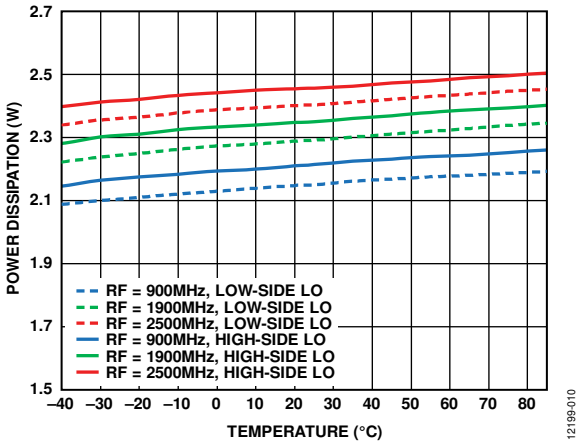

Figure 10. Power Dissipation vs. Temperature for Three RF Frequencies

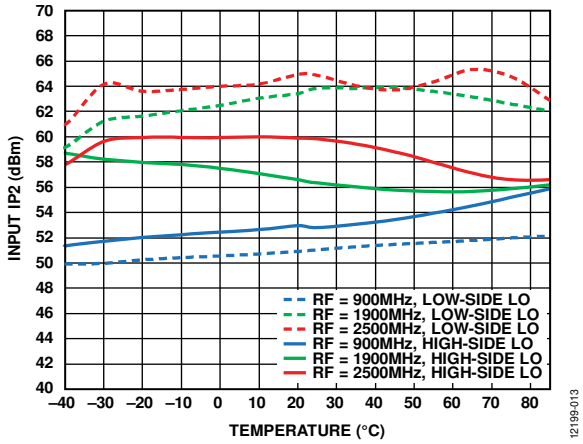

Figure 13. Input IP2 vs. Temperature for Three RF Frequencies

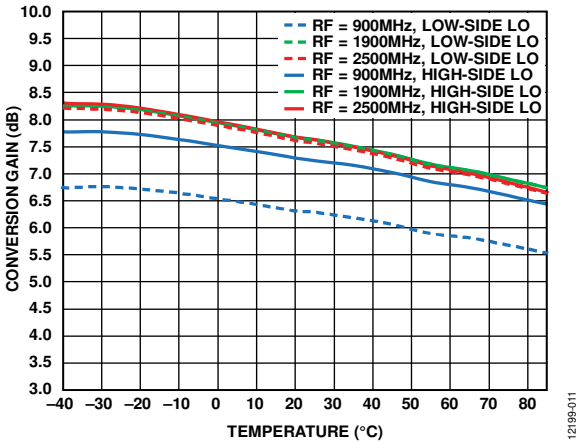

Figure 11. Power Conversion Gain vs. Temperature for Three RF Frequencies

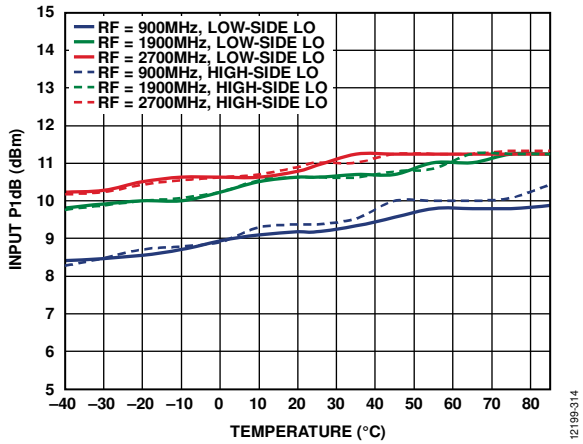

Figure 14. Input P1dB vs. Temperature for Three RF Frequencies

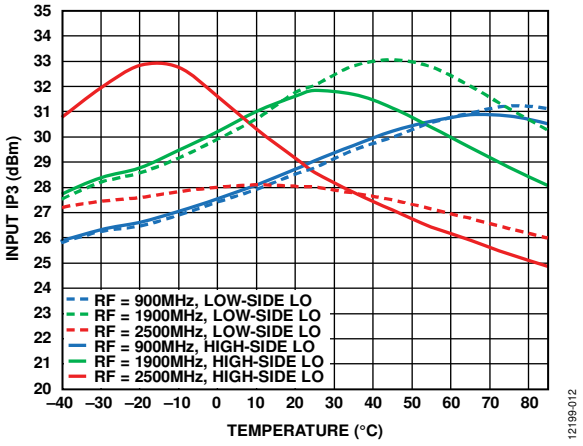

Figure 12. Input IP3 vs. Temperature for Three RF Frequencies

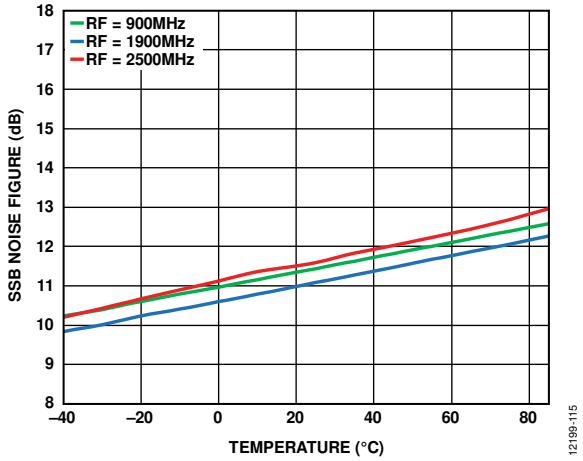

Figure 15. SSB Noise Figure vs. Temperature for Three RF Frequencies

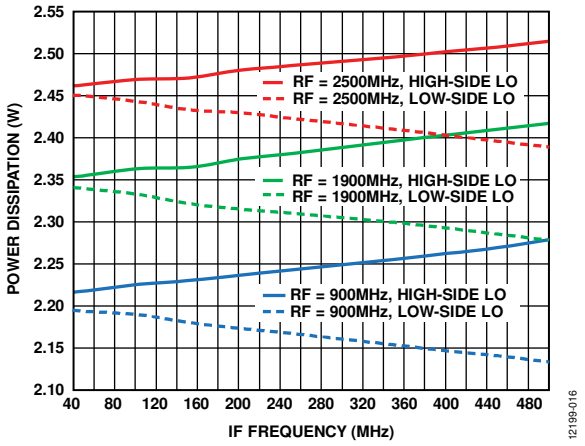

Figure 16. Power Dissipation vs. IF Frequency for Three RF Frequencies

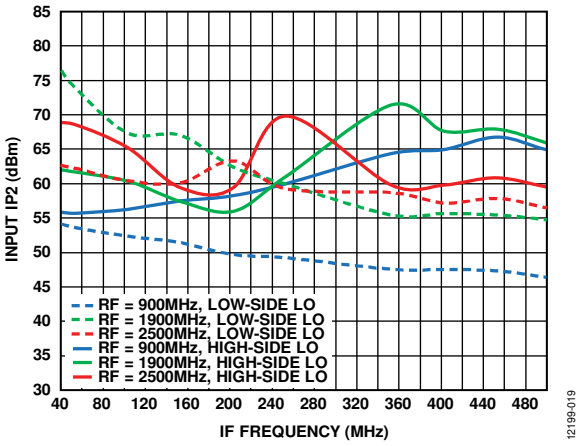

Figure 19. Input IP2 vs. IF Frequency for Three RF Frequencies

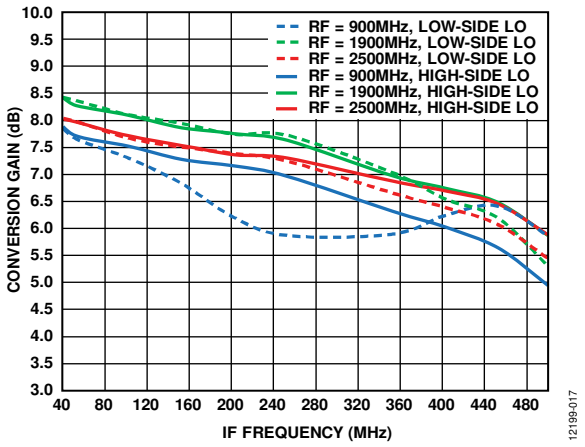

Figure 17. Power Conversion Gain vs. IF Frequency for Three RF Frequencies

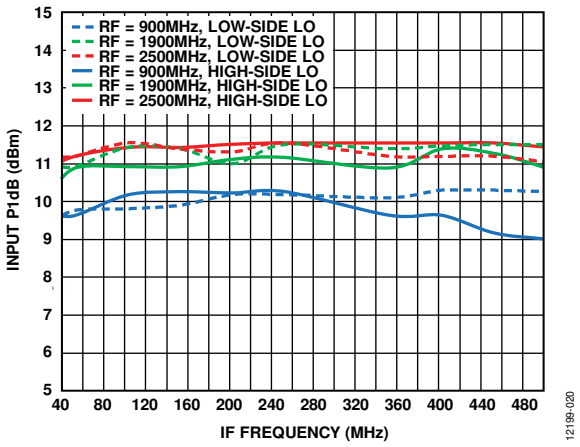

Figure 20. Input P1dB vs. IF Frequency for Three RF Frequencies

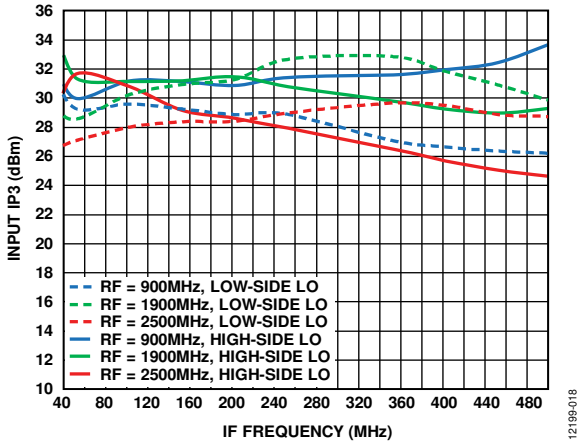

Figure 18. Input IP3 vs. IF Frequency for Three RF Frequencies

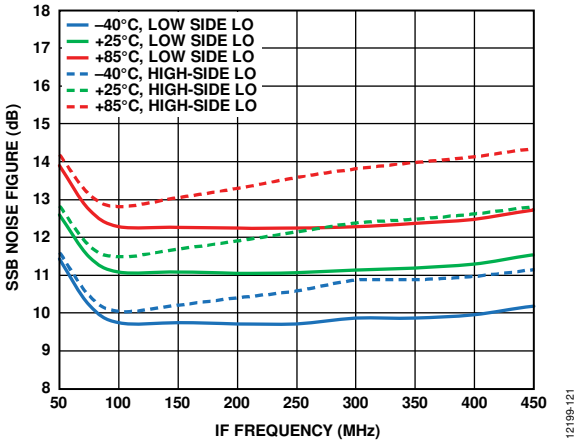

Figure 21. SSB Noise Figure vs. IF Frequency for Three RF Frequencies

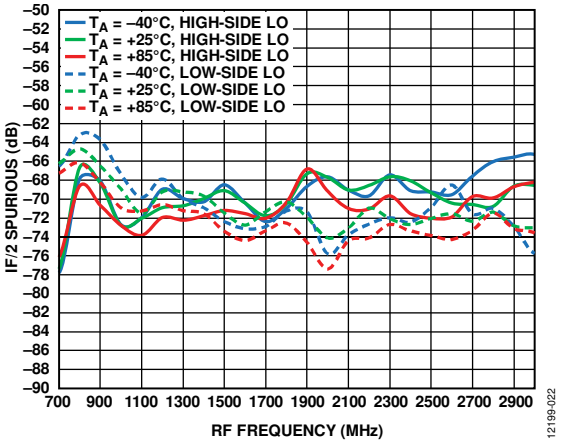

Figure 22. IF/2 Spurious vs. RF Frequency over Three Temperatures

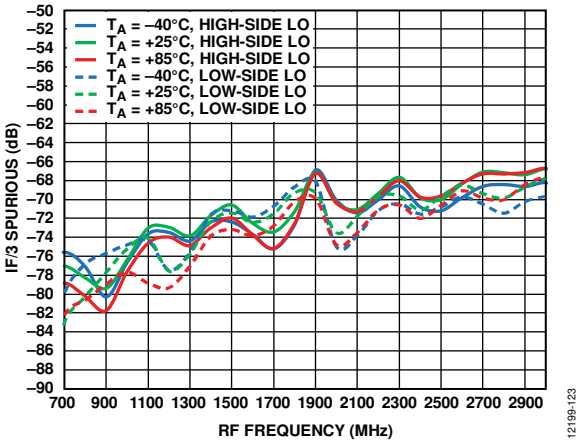

Figure 23. IF/3 Spurious vs. RF Frequency over Three Temperatures

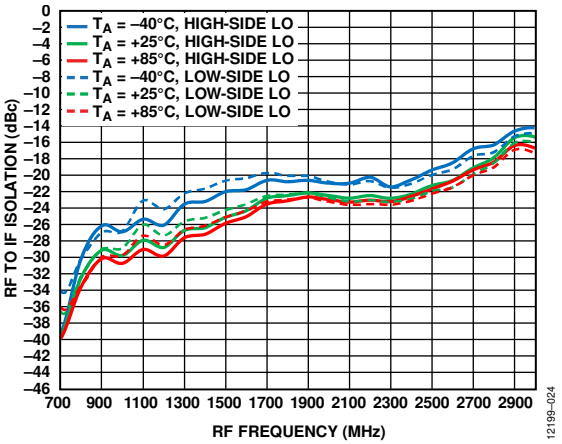

Figure 24. RF to IF Isolation vs. RF Frequency over Three Temperatures

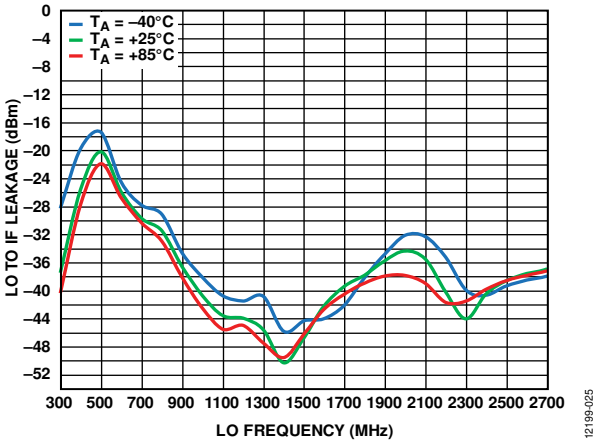

Figure 25. LO to IF Leakage vs. LO Frequency over Three Temperatures

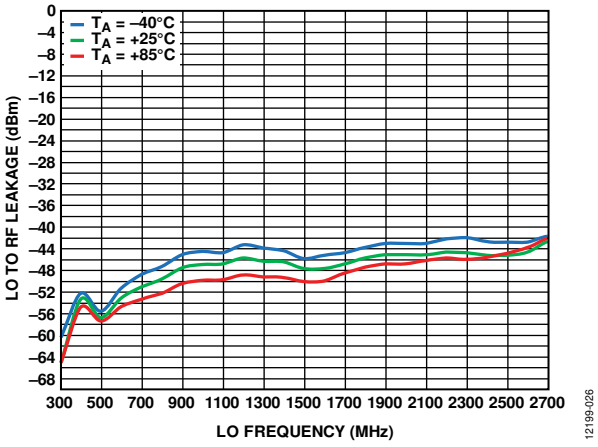

Figure 26. LO to RF Leakage vs. LO Frequency over Three Temperatures

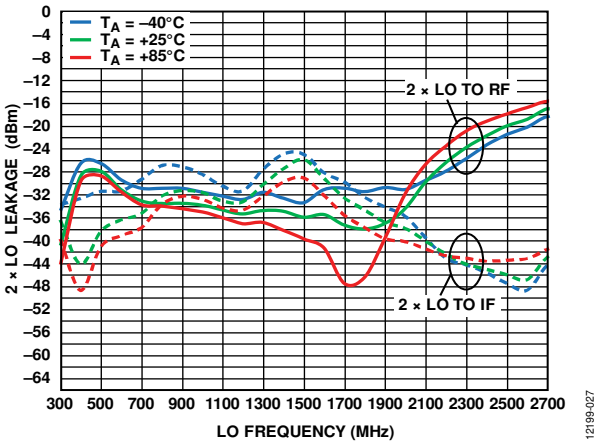

Figure 27. 2 × LO Leakage vs. LO Frequency (2 × LO to RF and 2 × LO to IF)

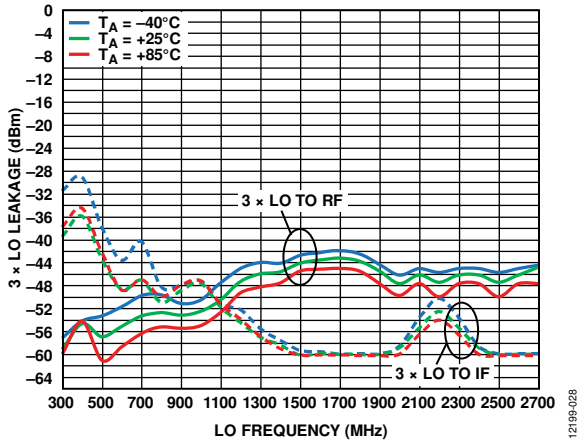

Figure 28. 3 × LO Leakage vs. LO Frequency (3 × LO to RF and 3 × LO to IF)

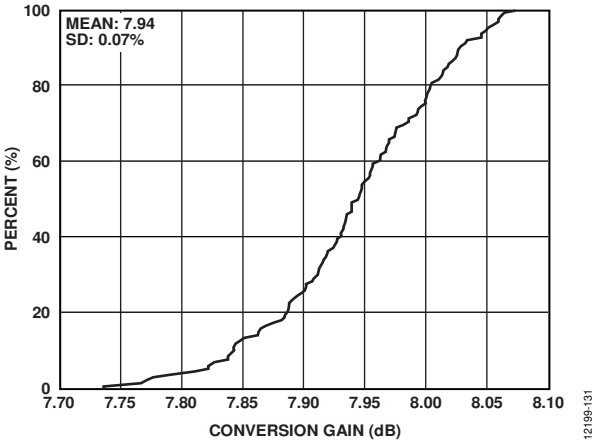

Figure 31. Conversion Gain Distribution

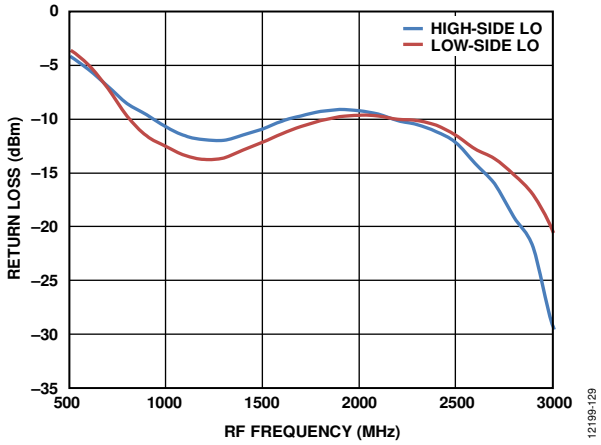

Figure 29. RF Port Return Loss, Fixed IF LO Return Loss

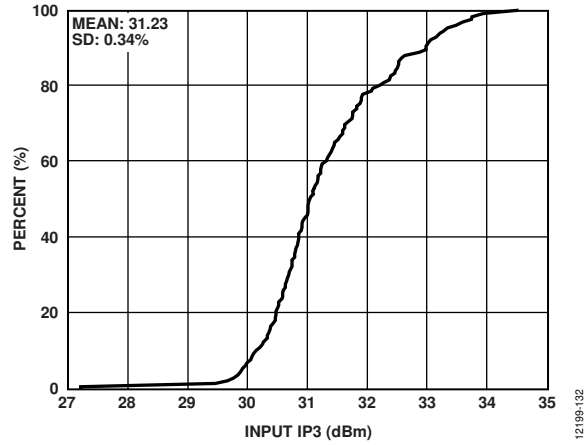

Figure 32. Input IP3 Distribution

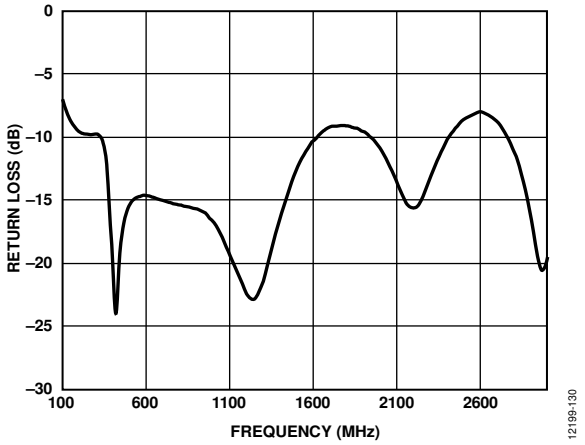

Figure 30. LO Return Loss

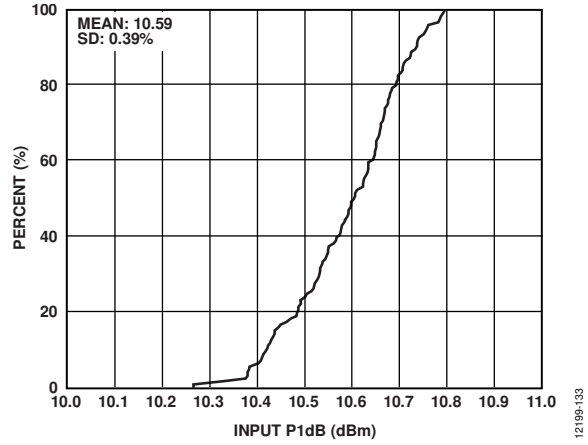

Figure 33. Input P1dB Distribution

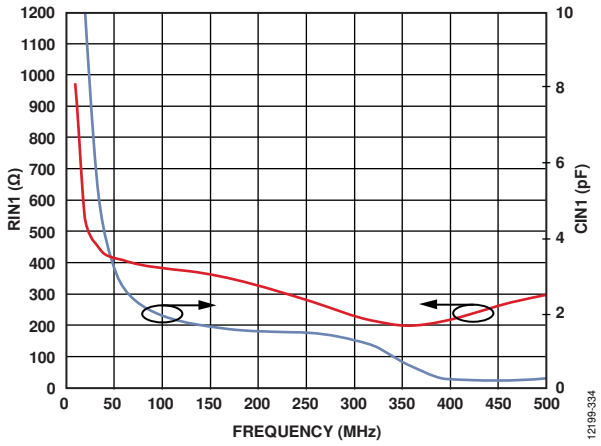

Figure 34. IF Output Impedance (R Parallel C Equivalent)

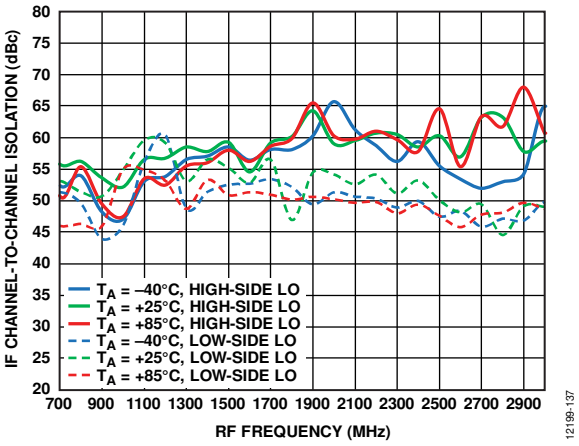

Figure 37. IF Channel-to-Channel Isolation vs. RF Frequency over Three Temperatures

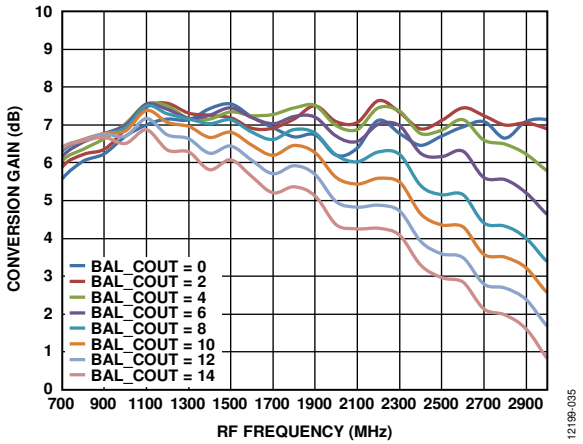

Figure 35. Conversion Gain vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

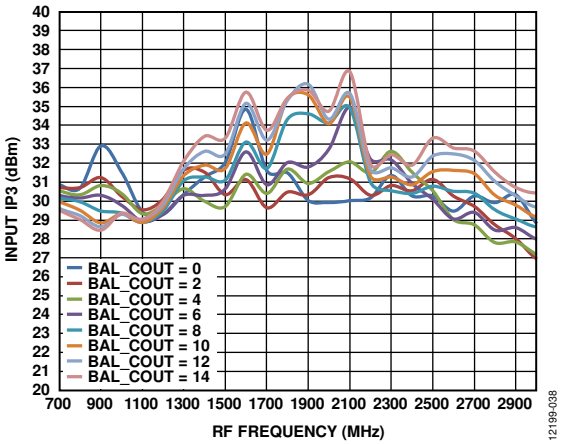

Figure 38. Input IP3 vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

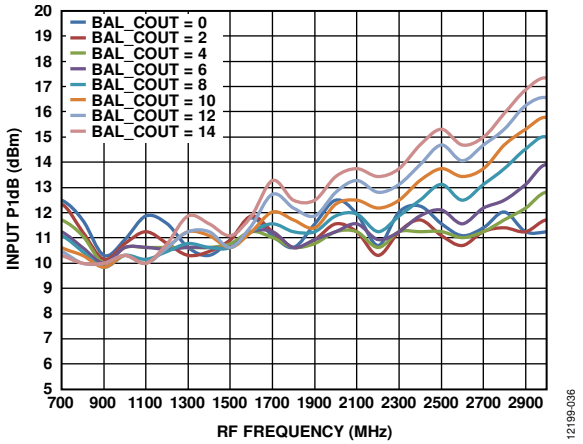

Figure 36. Input P1dB vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

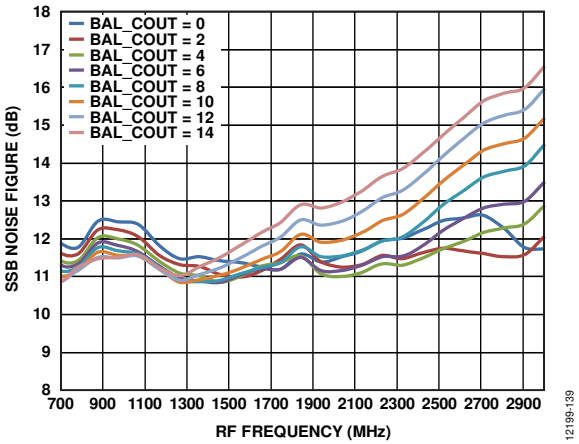

Figure 39. SSB Noise Figure vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

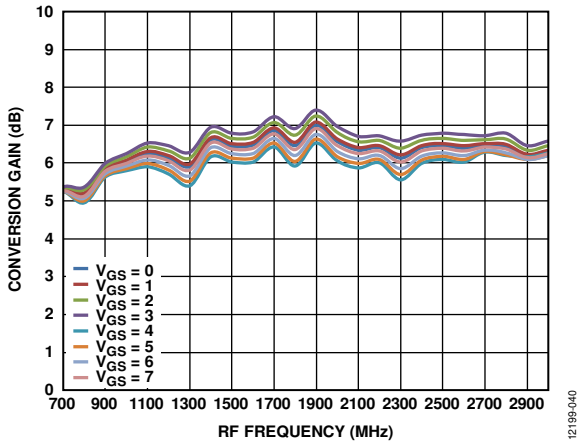

Figure 40. Conversion Gain vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

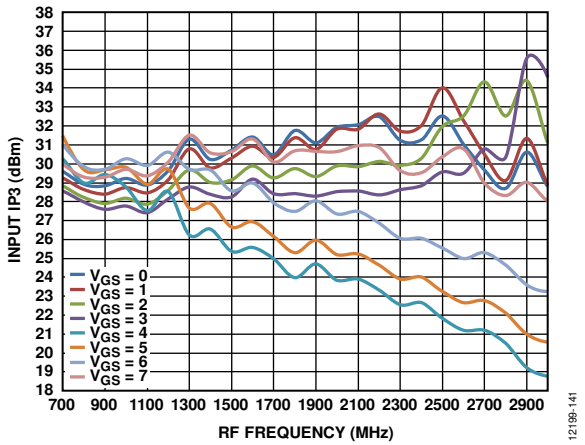

Figure 41. Input IP3 vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

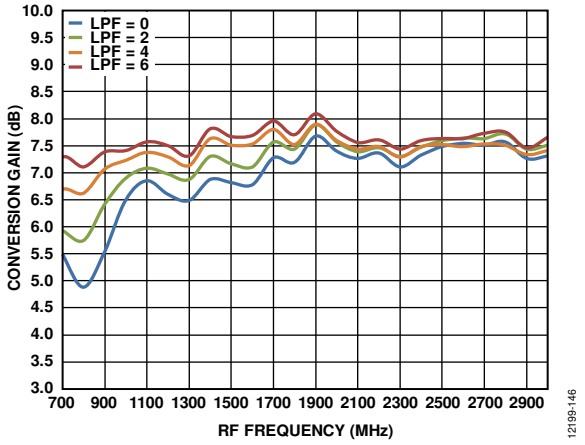

Figure 42. Conversion Gain vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

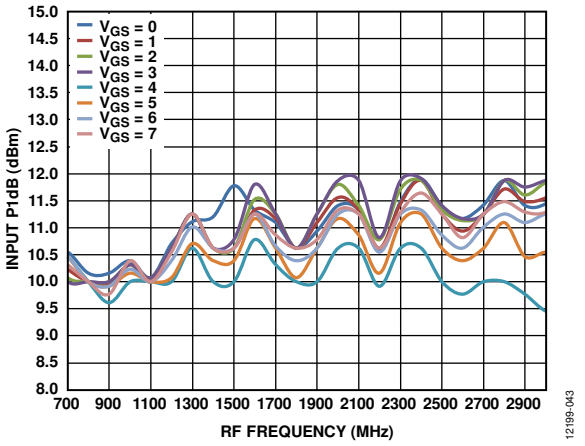

Figure 43. Input P1dB vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

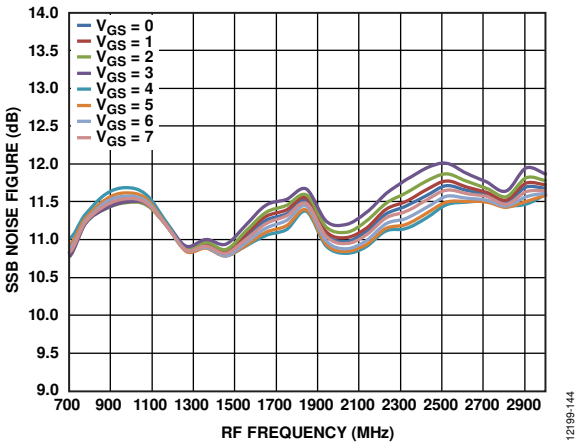

Figure 44. SSB Noise Figure vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

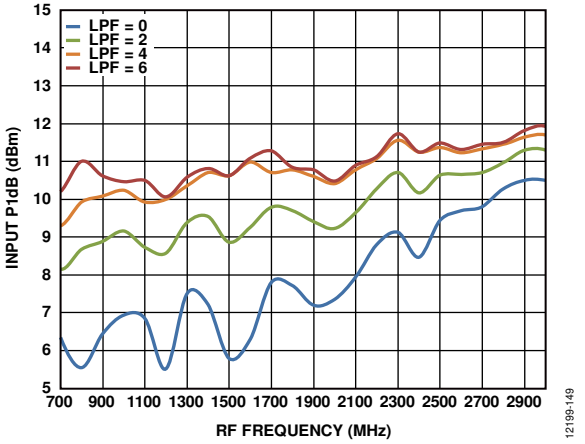

Figure 45. Input P1dB vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

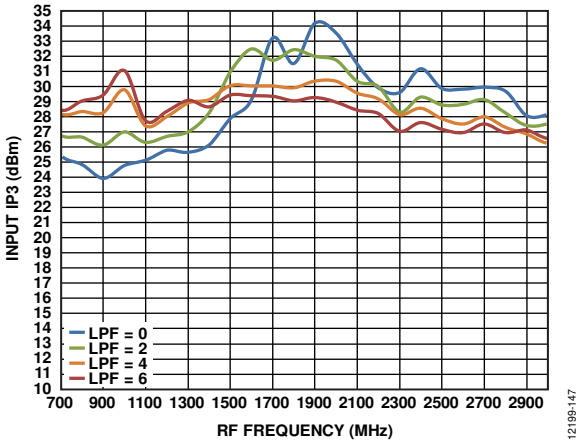

Figure 46. Input IP3 vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

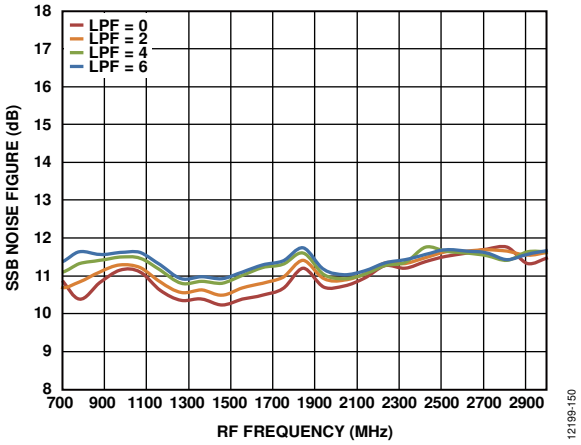

Figure 49. SSB Noise Figure vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

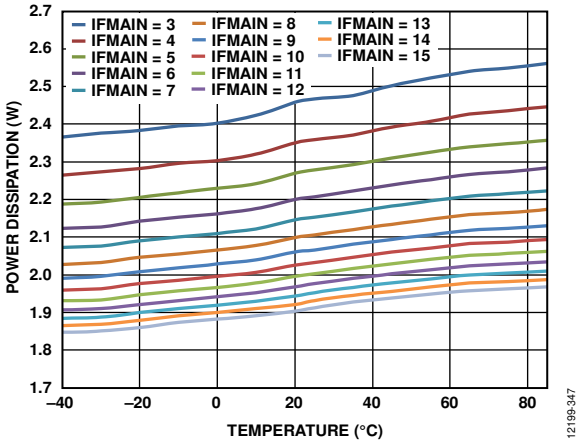

Figure 47. Power Dissipation vs. Temperature for IF Main Settings

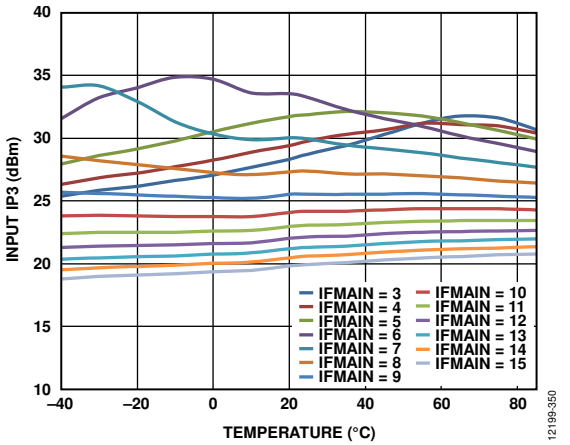

Figure 50. Input IP3 vs. Temperature for IF Main Settings

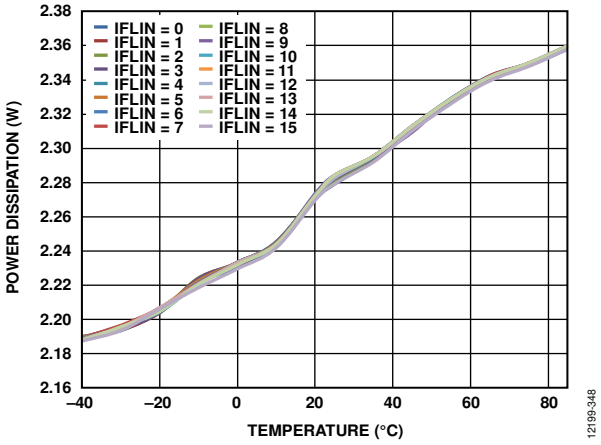

Figure 48. Power Dissipation vs. Temperature for IF LIN Settings

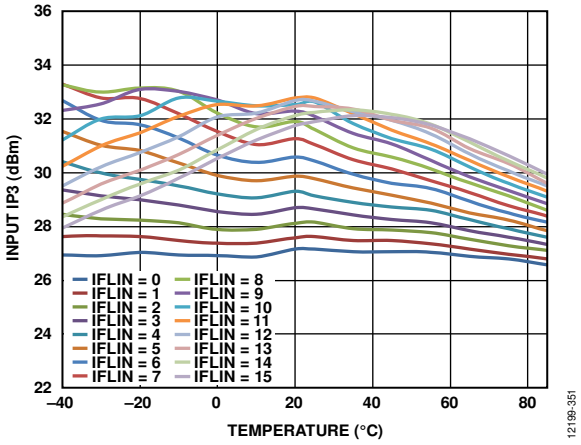

Figure 51. Input IP3 vs. Temperature for IF LIN Settings

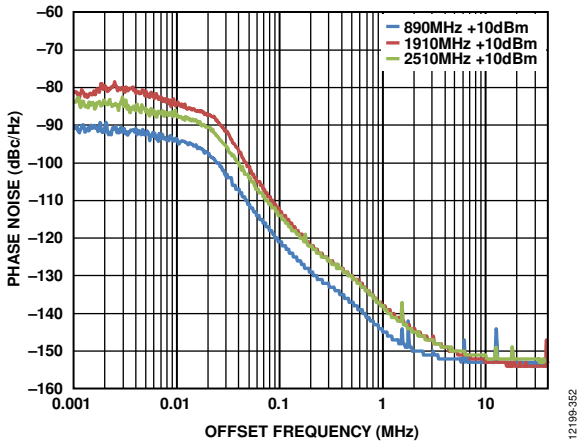

Figure 52. Phase Noise at IF Output vs. Offset Frequency with 10 dBm Blocker in Integer Mode

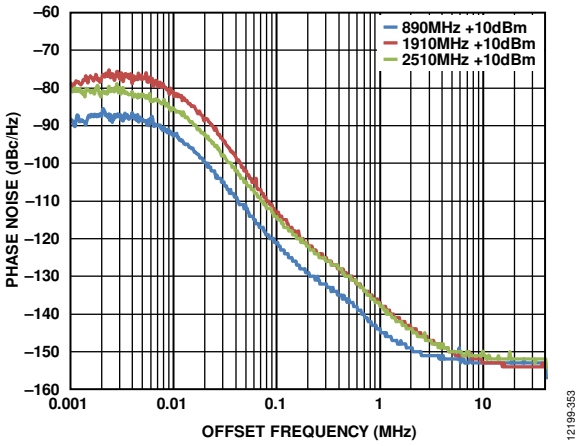

Figure 53. Phase Noise at IF Output vs. Offset Frequency with 10 dBm Blocker in Fractional Mode

MIXER, HIGH EFFICIENCY MODE

T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, Z_O = 50 Ω, f_{REF} = 122.88 MHz, f_{REF} power = 4 dBm, f_{PFD} = 1.536 MHz, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

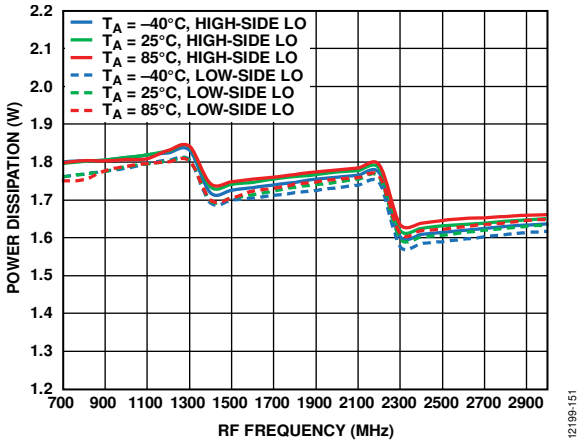

Figure 54. Power Dissipation vs. RF Frequency over Three Temperatures

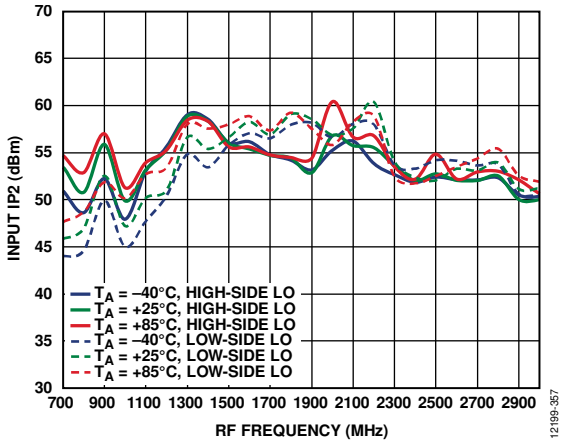

Figure 57. Input IP2 vs. RF Frequency over Three Temperatures

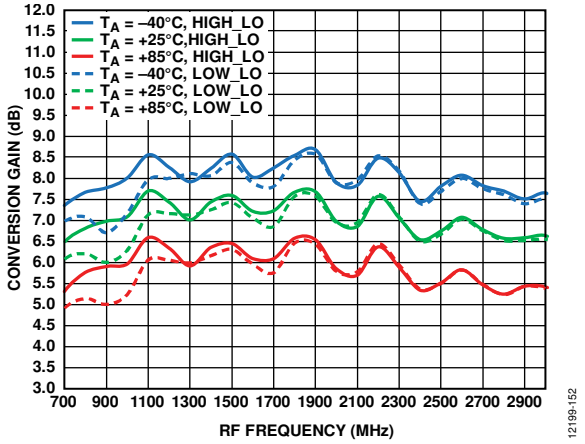

Figure 55. Conversion Gain vs. RF Frequency over Three Temperatures

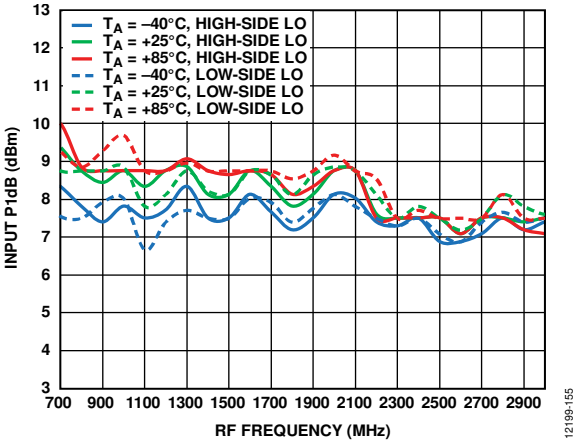

Figure 58. Input P1dB vs. RF Frequency over Three Temperatures

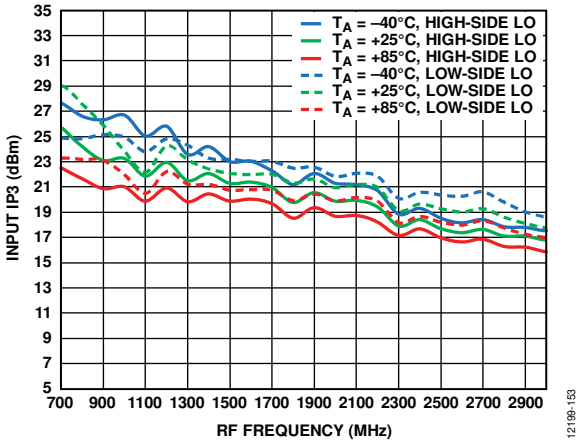

Figure 56. Input IP3 vs. RF Frequency over Three Temperatures

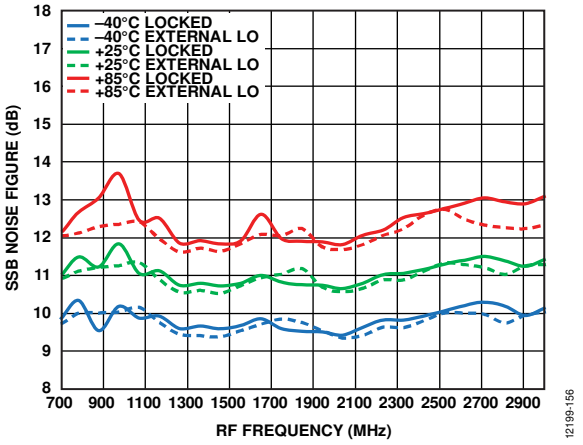

Figure 59. SSB Noise Figure vs. RF Frequency over Three Temperatures

SYNTHESIZER

V_S = high performance mode, T_A = 25°C, measured on LO output, f_{LO} = 1700 MHz, Z_O = 50 Ω, f_{REF} = 122.88 MHz, f_{PFD} = 1.536 MHz, f_{REF} power = 4 dBm, integer mode loop filter, unless otherwise noted.

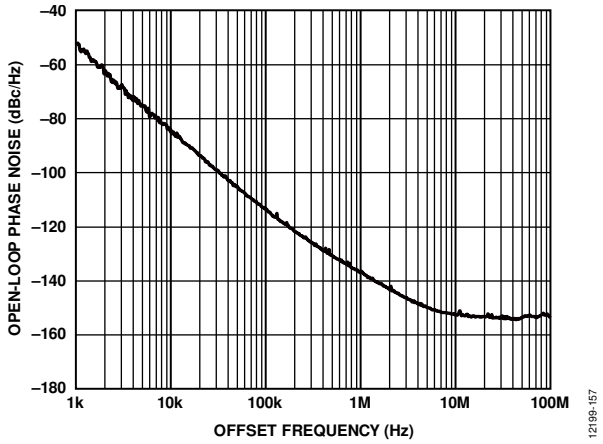

Figure 60. VCO_0 Open-Loop Phase Noise vs. Offset Frequency, f_{VCO_0} = 5.1 GHz, Divide by Two Selected, VCOVTUNE = 1.5 V

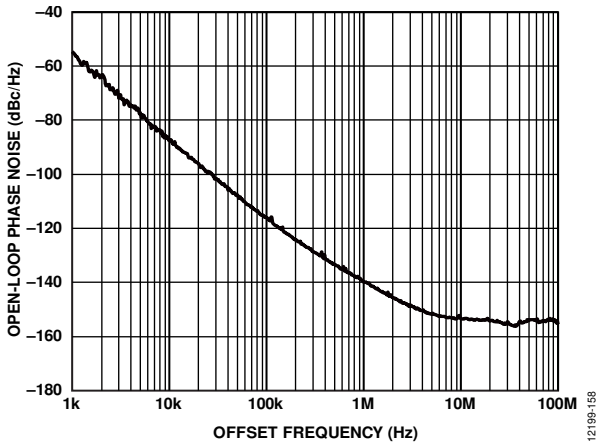

Figure 61. VCO_1 Open-Loop Phase Noise vs. Offset Frequency, f_{VCO_1} = 4.5 GHz, Divide by Two Selected, VCOVTUNE = 1.5 V

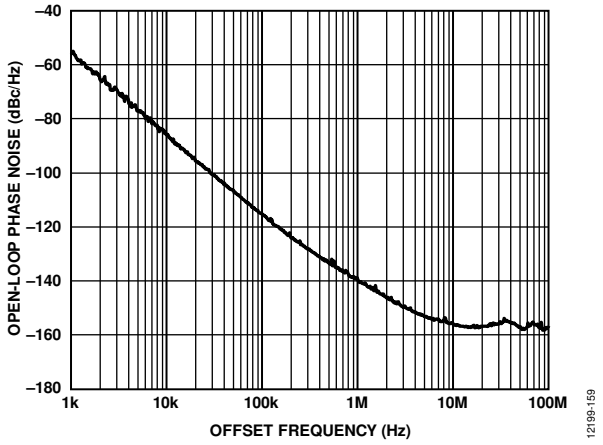

Figure 62. VCO_2 Open-Loop Phase Noise vs. Offset Frequency, f_{VCO_2} = 3.8 GHz, Divide by Two Selected, VCOVTUNE = 1.5 V

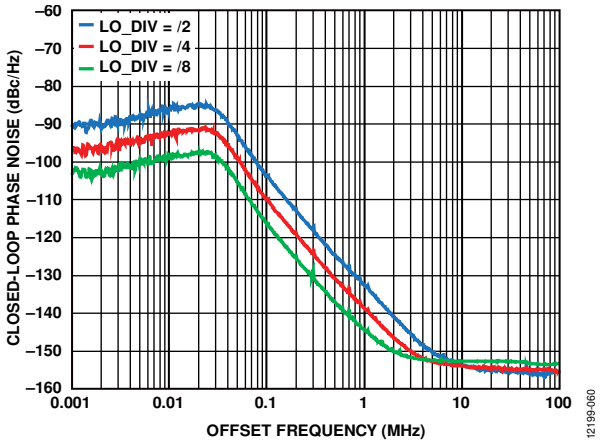

Figure 63. VCO_0 Closed-Loop Phase Noise for Various LO_DIV Dividers vs. Offset Frequency, f_{VCO_0} = 5.1 GHz

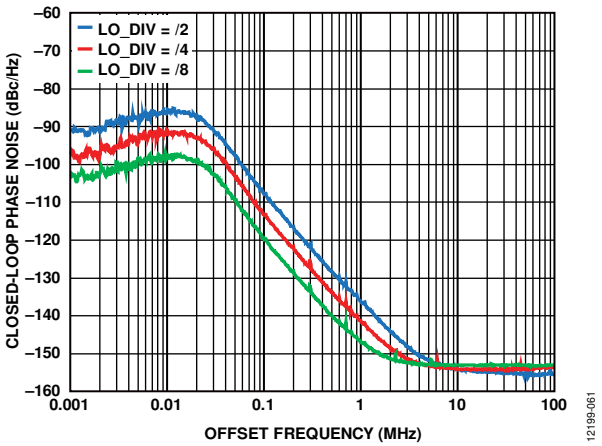

Figure 64. VCO_1 Closed-Loop Phase Noise for Various LO_DIV Dividers vs. Offset Frequency, f_{VCO_1} = 4.5 GHz

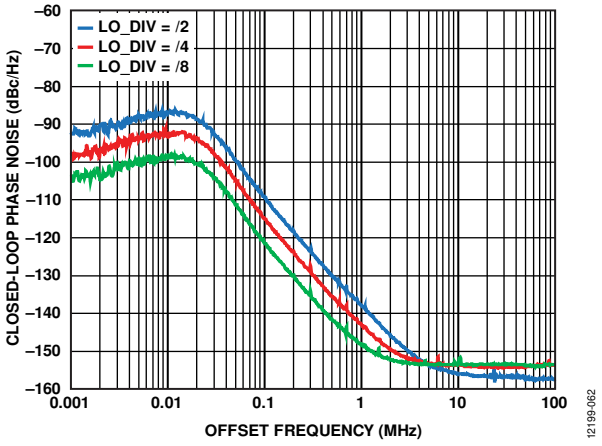

Figure 65. VCO_2 Closed-Loop Phase Noise for Various LO_DIV Dividers vs. Offset Frequency, f_{VCO_2} = 3.8 GHz

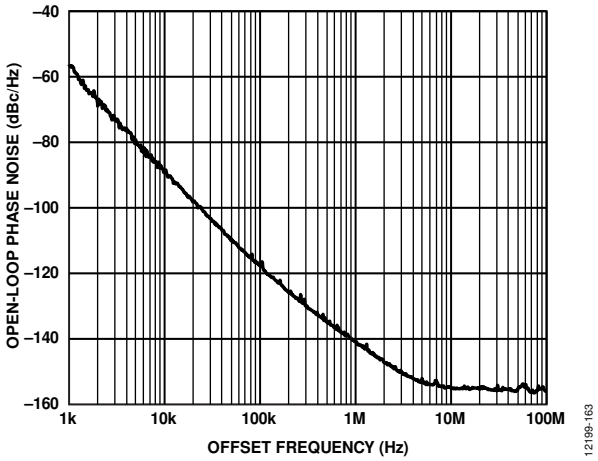

Figure 66. VCO_3 Open-Loop Phase Noise vs. Offset Frequency, f_{VCO_3} = 3.2 GHz, Divide by Two Selected, VCOVTUNE = 1.5 V

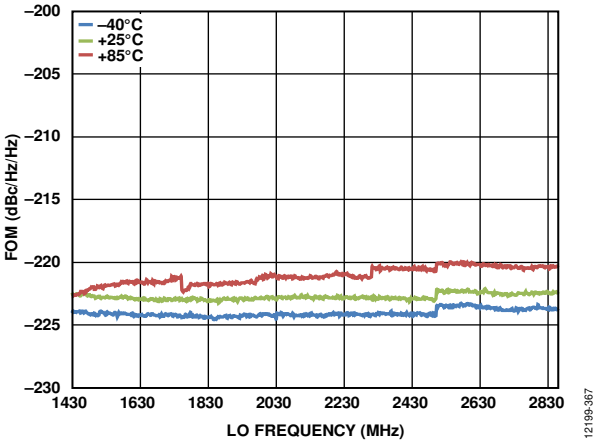

Figure 67. PLL Figure of Merit (FOM) vs. LO Frequency, Integer Mode

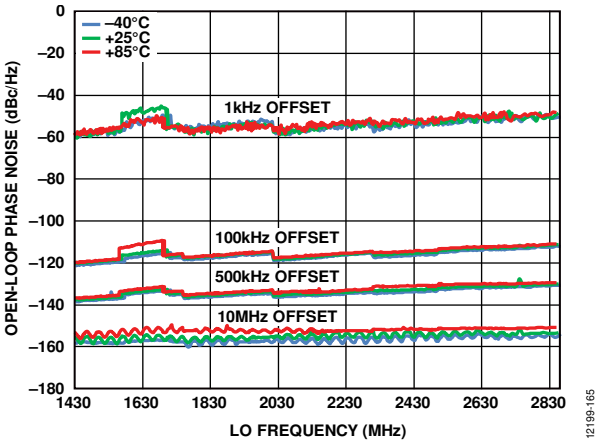

Figure 68. Open-Loop Phase Noise vs. LO Frequency, Divide by Two Selected

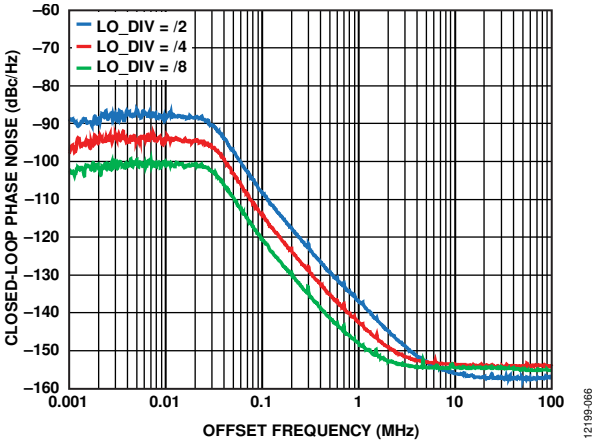

Figure 69. VCO_3 Closed-Loop Phase Noise for Various LO_DIV Dividers vs. Offset Frequency, f_{VCO_3} = 3.2 GHz

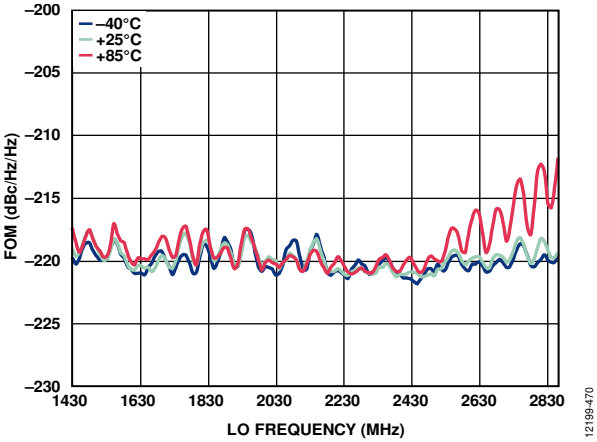

Figure 70. PLL Figure of Merit (FOM) vs. LO Frequency, Fractional Mode Offset = 45 kHz, Bleed = 125 µA

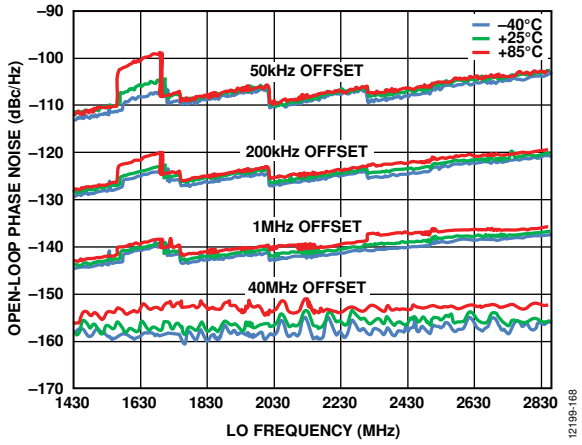

Figure 71. Open-Loop Phase Noise vs. LO Frequency, Divide by Two Selected