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700 MHz to 2700 MHz Rx Mixer with Integrated IF DGA, Fractional-N PLL, and VCO

Data Sheet

ADRF6620

FEATURES

- Integrated fractional-N phase-locked loop (PLL)
- RF input frequency range: 700 MHz to 2700 MHz
- Internal local oscillator (LO) frequency range: 350 MHz to 2850 MHz
- Input P1dB: 17 dBm
- Output IP3: 45 dBm
- Single-pole four-throw (SP4T) RF input switch
- Digital step attenuator (DSA) range: 0 dB to 15 dB
- Integrated RF tunable balun allowing single-ended 50 Ω input
- Multicore integrated voltage controlled oscillator (VCO)
- Digitally programmable variable gain amplifier (DGA)
  - −3 dB bandwidth: >600 MHz
- Balanced 150 Ω IF output impedance
- Programmable via 3-wire serial port interface (SPI)
- Single 5 V supply

APPLICATIONS

- Wireless receivers
- Digital predistortion (DPD) receivers

FUNCTIONAL BLOCK DIAGRAM

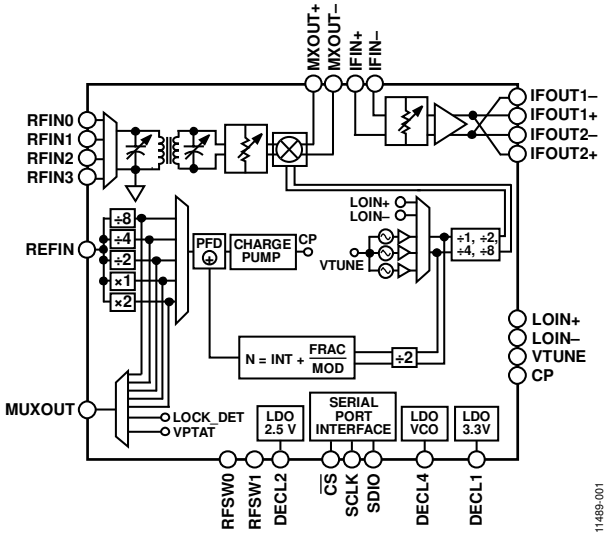

Figure 1.

GENERAL DESCRIPTION

The ADRF6620 is a highly integrated active mixer and synthesizer that is ideally suited for wireless receiver subsystems. The feature rich device consists of a high linearity broadband active mixer; an integrated fractional-N PLL; low phase noise, multicore VCO; and IF DGA. In addition, the ADRF6620 integrates a 4:1 RF switch, an on-chip tunable RF balun, programmable RF attenuator, and low dropout (LDO) regulators. This highly integrated device fits within a small 7 mm × 7 mm footprint.

The high isolation 4:1 RF switch and on-chip tunable RF balun enable the ADRF6620 to support four single-ended 50 Ω terminated RF inputs. A programmable attenuator ensures optimal RF input drive to the high linearity mixer core. The integrated DSA has an attenuation range of 0 dB to 15 dB with a step size of 1 dB.

The ADRF6620 offers two alternatives for generating the differential LO input signal: externally, via a high frequency, low phase noise LO signal, or internally, via the on-chip fractional-N PLL synthesizer. The integrated synthesizer enables continuous LO coverage from 350 MHz to 2850 MHz. The PLL reference input can support a wide frequency range because the divide and multiply blocks can be used to increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD).

The integrated high linearity DGA provides an additional gain range from 3 dB to 15 dB in steps of 0.5 dB for maximum flexibility in driving an analog-to-digital converter (ADC).

The ADRF6620 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 48-lead, RoHS-compliant, 7 mm × 7 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +85°C temperature range.

Rev. 0 Document Feedback

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Tel: 781.329.4700

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ADRF6620* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6620 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6620: 700 MHz to 2700 MHz Rx Mixer with Integrated IF DGA, Fractional-N PLL, and VCO Data Sheet

User Guides

- UG-558: Evaluating the ADRF6620, a 700 MHz to 2700 MHz Rx Mixer with Integrated IF Amplifier, Fractional-N PLL, and VCO

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADRF6620 Evaluation Board Software

TOOLS AND SIMULATIONS

- ADRF6620 S-Parameters

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADRF6620 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6620 EngineerZone Discussions.

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TABLE OF CONTENTS

REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO INPUT					
Internal LO Frequency Range		350		2850	MHz
External LO Frequency Range	LO_DIV_A = 00	350		3200	MHz
LO Input Level		−6	0	+6	dBm
LO Input Impedance			50		Ω
RF INPUT					
Input Frequency		700		2700	MHz
Input Return Loss			12		dB
Input Impedance			50		Ω
RF DIGITAL STEP ATTENUATOR					
Attenuation Range	Step size = 1 dB	0		15	dB
POWER SUPPLY		4.75	5.0	5.25	V
Power Consumption	LO output buffer disabled				
	External LO + IF DGA enabled		1.3		W
	Internal LO + IF DGA enabled		1.7		W
	Only IF DGA enabled		0.6		W
Power-Down Current			6		mA

RF INPUT TO IF DGA OUTPUT SYSTEM SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, high-side LO injection, f_{IF} = 200 MHz, internal LO frequency, IF DGA output load = 150 Ω, and 2 V p-p differential output with third-order low-pass filter, unless otherwise noted. For mixer settings for maximum linearity, see Table 16. All losses from input and output traces and baluns are de-embedded from results

Table 2. RF Switch + Balun + RF Attenuator + Mixer + IF DGA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT f_{RF} = 900 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			12		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		43		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		78		dBm
Noise Figure	Noise figure optimized		16		dB
DYNAMIC PERFORMANCE AT f_{RF} = 1900 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			11		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		75		dBm
Noise Figure	Noise figure optimized		18.5		dB
DYNAMIC PERFORMANCE AT f_{RF} = 2100 MHz	f_{IF} = 200 MHz				dB
Voltage Conversion Gain			10.5		dBm
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		66		dBm
Noise Figure	Noise figure optimized		19		dB
DYNAMIC PERFORMANCE AT f_{RF} = 2700 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			9		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		44		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		74		dBm
Noise Figure	Noise figure optimized		21		dB

SYNTHESIZER/PLL SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm, f_{PFD} = 38.4 MHz, and loop filter bandwidth = 120 kHz, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
PLL Reference Frequency		12		464	MHz
PLL Reference Level	For PLL lock condition	−15	+4	+14	dBm
PFD FREQUENCY		24		58	MHz
INTERNAL VCO RANGE		2800		5700	MHz
OPEN-LOOP VCO PHASE NOISE	VTUNE = 2 V, LO_DIV_A = 00				
f_{VCO2} = 3.4 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−81		dBc/Hz
	100 kHz offset		−103		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−155		dBc/Hz
	VCO sensitivity (K_V)		88		MHz/V
f_{VCO1} = 4.6 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−74		dBc/Hz
	100 kHz offset		−101		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−156		dBc/Hz
	VCO sensitivity (K_V)		89		MHz/V
f_{VCO0} = 5.5 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−69		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−121		dBc/Hz
	1 MHz offset		−124		dBc/Hz
	6 MHz offset		−142		dBc/Hz
	10 MHz offset		−146		dBc/Hz
	40 MHz offset		−155		dBc/Hz
	VCO sensitivity (K_V)		72		MHz/V
SYNTHESIZER SPECIFICATIONS	Measured at LO output, LO_DIV_A = 01				
f_{LO} = 1.710 GHz, f_{VCO2} = 3.420 GHz	f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz, 120 kHz loop filter				
f_{PFD} Spurs	$f_{PFD} \times 1$		−83		dBc
	$f_{PFD} \times 2$		−89		dBc
	$f_{PFD} \times 3$		−90		dBc
	$f_{PFD} \times 4$		−93		dBc
Closed-Loop Phase Noise	1 kHz offset		−97		dBc/Hz
	10 kHz offset		−110		dBc/Hz
	100 kHz offset		−107		dBc/Hz
	800 kHz offset		−128		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−152		dBc/Hz
	40 MHz offset		−158		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.21		° rms
Figure of Merit (FOM)[1]			−222		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{LO} = 2.305 GHz, f_{VCO1} = 4.610 GHz					
f_{PFD} Spurs	$f_{PFD} \times 1$		−84		dBc
	$f_{PFD} \times 2$		−87		dBc
	$f_{PFD} \times 3$		−91		dBc
	$f_{PFD} \times 4$		−92		dBc
Closed-Loop Phase Noise	1 kHz offset		−93		dBc/Hz
	10 kHz offset		105		dBc/Hz
	100 kHz offset		−103		dBc/Hz
	800 kHz offset		−116		dBc/Hz
	1 MHz offset		−130		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−152		dBc/Hz
	40 MHz offset		−156		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.3		° rms
Figure of Merit[1]			−222		dBc/Hz
f_{LO} = 2.75 GHz, f_{VCO2} = 5.5 GHz					
f_{PFD} Spurs	$f_{PFD} \times 1$		−82		dBc
	$f_{PFD} \times 2$		−88		dBc
	$f_{PFD} \times 3$		−93		dBc
	$f_{PFD} \times 4$		−96		dBc
Closed-Loop Phase Noise	1 kHz offset		−93		dBc/Hz
	10 kHz offset		−101		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−122		dBc/Hz
	1 MHz offset		−128		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−151		dBc/Hz
	40 MHz offset		−154		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.38		° rms
Figure of Merit[1]			−222		dBc/Hz

[1] Figure of merit (FOM) is computed as phase noise (dBc/Hz) − 10 log 10(f_{PFD}) − 20 log 10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 160 MHz and f_{REF} power = 4 dBm (500 V/µs slew rate) with a 40 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

RF INPUT TO MIXER OUTPUT SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, high-side LO injection, f_{IF} = 200 MHz, external LO frequency, and RF attenuation = 0 dB, unless otherwise noted. Mixer settings configured for maximum linearity (see Table 16). All losses from input and output traces and baluns are de-embedded from results.

Table 4. RF Switch + Balun + RF Attenuator + Mixer

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE GAIN	Differential 255 Ω load		−4		dB
MIXER OUTPUT IMPEDANCE	Differential (see Figure 87)		255		Ω
DYNAMIC PERFORMANCE AT f_{RF}= 900 MHz					
Voltage Conversion Gain			−2		dB
Input P1dB			17		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		65		dBm
Noise Figure			15		dB
LO to RF Leakage			−70		dBm
RF to LO Leakage			−60		dBc
LO to IF Leakage			−32		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−45		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−52		dBc
DYNAMIC PERFORMANCE AT f_{RF} =1900 MHz					
Voltage Conversion Gain			−3		dB
Input P1dB			17		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		62		dBm
Noise Figure			17		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−50		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−43		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−47		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 2100 MHz					
Voltage Conversion Gain			−3.5		dB
Input P1dB			18		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		54.5		dBm
Noise Figure			18		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−40		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−40		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−45		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 2700 MHz					
Voltage Conversion Gain			−4.7		dB
Input P1dB			19		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		56		dBm
Noise Figure			21		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−45		dBc
LO to IF Leakage			−40		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−42		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−41		dBc

[1] Isolation between RF inputs. An input signal was applied to RFIN0 while RFIN1 to RFIN3 were terminated with 50 Ω. The IF signal amplitude was measured at the mixer output. The internal switch was then configured for RFIN3, and the feedthrough was measured as a delta from the fundamental.

IF DGA SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, R_S = R_L = 150 Ω differential, f_{IF} = 200 MHz, 2 V p-p differential output,unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BANDWIDTH					
−1 dB Bandwidth	V_{OUT} = 2 V p-p		500		MHz
−3 dB Bandwidth	V_{OUT} = 2 V p-p		700		MHz
SLEW RATE			5.5		V/ns
INPUT STAGE					
Input P1dB	At minimum gain		17		dBm
Input Impedance			150		Ω
Common-Mode Input Voltage			1.5		V
Common-Mode Rejection Ratio (CMRR)			50		dB
GAIN					
Power/Voltage Gain, Step Size = 0.5 dB		3		15	dB
Gain Flatness	50 MHz < f_C < 200 MHz		0.2		dB
Gain Conformance Error			±0.1		dB
Gain Temperature Sensitivity			0.008		dB/C
Gain Step Response			15		ns
OUTPUT STAGE					
Output P1dB			18		dBm
Output Impedance	See Figure 88		150		Ω
NOISE/HARMONIC PERFORMANCE at 200 MHz					
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		63		dBm
HD2	V_{OUT} = 2 V p-p		−87		dBc
HD3	V_{OUT} = 2 V p-p		−84		dBc
Noise Figure			10		dB

DIGITAL LOGIC SPECIFICATIONS

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL PORT INTERFACE TIMING						
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.70	V
Output Voltage High	V_{OH}	I_{OH} = −100 µA	2.3			V
Output Voltage Low	V_{OL}	I_{OL} = +100 µA	0.2			V
Serial Clock Period	t_{SCLK}		38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}		8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}		8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	t_S		10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	t_H		10			ns
Minimum Period SCLK Can Be in Logic High State	t_{HIGH}		10			ns
Minimum Period SCLK Can Be in Logic Low State	t_{LOW}		10			ns
Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}				231	ns
Maximum Time Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	t_Z				5	ns

Timing Diagram

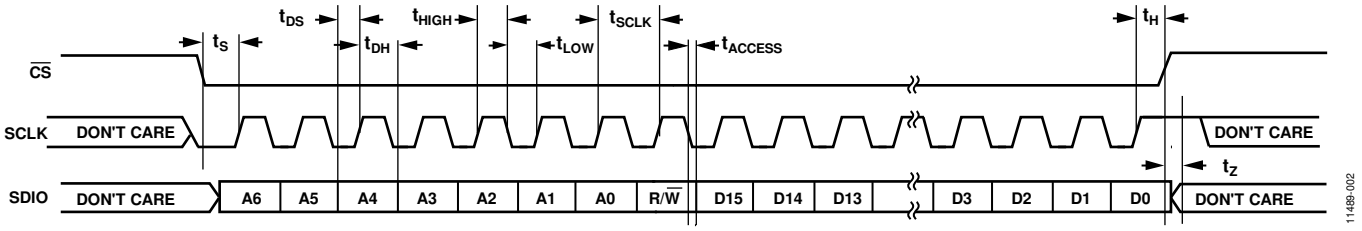

Figure 2. Serial Port Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCCx	−0.5 V to +5.5 V
RFSW0, RFSW1	−0.3 V to +3.6 V
RFIN0, RFIN1, RFIN2, RFIN3	20 dBm
LOIN−, LOIN+	16 dBm
REFIN	−0.3 V to +3.6 V
IFIN−, IFIN+	−1.2 V to +3.6 V
$\overline{CS}$, SCLK, SDIO	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JC}	Unit
48-Lead LFCSP	1.62	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

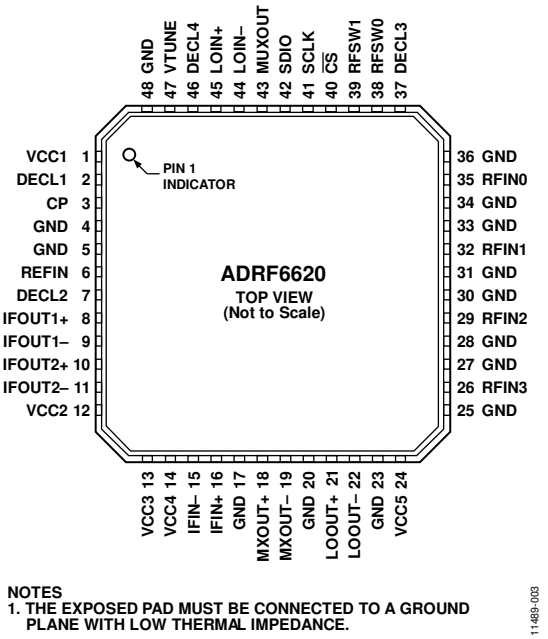

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1, 12, 13, 14, 24	VCC1, VCC2, VCC3, VCC4, VCC5	5 V Power Supplies. Decouple all power supply pins to ground, using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors near the pins.
2, 7, 37, 46	DECL1, DECL2, DECL3, DECL4	Decouple all DECLx pins to ground, using 100 pF, 0.1 µF, and 10 µF capacitors. Place the decoupling capacitors near the pins.
3	CP	Synthesizer Charge Pump Output. Connect this pin to the VTUNE pin through the loop filter.
4, 5, 17, 20, 23, 25, 27, 28, 30, 31, 33, 34, 36, 48	GND	Ground.
6	REFIN	Synthesizer Reference Frequency Input.
8 to 11	IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−	IF DGA Outputs. Connect the positive pins such that IFOUT1+ and IFOUT2+ are tied together. Similarly, connect the negative pins such that IFOUT1− and IFOUT2− are tied together. Refer to the Layout section for a recommended layout that minimizes parasitic capacitance and optimizes performance.
15, 16	IFIN−, IFIN+	Differential IF DGA Inputs. AC couple the mixer outputs to the IF DGA inputs.
18, 19	MXOUT+, MXOUT−	Differential Mixer Outputs. AC couple the mixer outputs to the IF DGA inputs.
21, 22	LOOUT+, LOOUT−	Differential LO Outputs. The differential output impedance is 50 Ω.
26, 29, 32, 35	RFIN3, RFIN2, RFIN1, RFIN0	RF Inputs. These single-ended RF inputs have a 50 Ω input impedance and must be ac-coupled.
38, 39	RFSW0, RFSW1	External Pin Control of RF Input Switches. For logic high, connect these pins to 2.5 V logic.
40	$\overline{CS}$	SPI Chip Select, Active Low. 3.3 V tolerant logic levels.
41	SCLK	SPI Clock. 3.3 V tolerant logic levels.
42	SDIO	SPI Data Input or Output. 3.3 V tolerant logic levels.
43	MUXOUT	Multiplexer Output. This output pin provides the PLL reference signal or the PLL lock detect signal.
44, 45	LOIN−, LOIN+	Differential Local Oscillator Inputs. The differential input impedance is 50 Ω.
47	VTUNE	VCO Tuning Voltage. Connect this pin to the CP pin through the loop filter.
49	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

[1] For more connection information about these pins, see Table 14.

TYPICAL PERFORMANCE CHARACTERISTICS

RF INPUT TO DGA OUTPUT SYSTEM PERFORMANCE

VCCx = 5 V, T_A = 25°C, RFDSA_SEL = 00 (0 dB), RFSW_SEL = 00 (RFIN0), BAL_CIN and BAL_COUT optimized for maximum gain; MIXER_BIAS, MIXER_RDAC, and MIXER_CDAC optimized for highest linearity, DGA at maximum gain; third-order low-pass filter between the mixer output and IF DGA input; high-side LO, internal LO frequency, IF frequency = 200 MHz, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

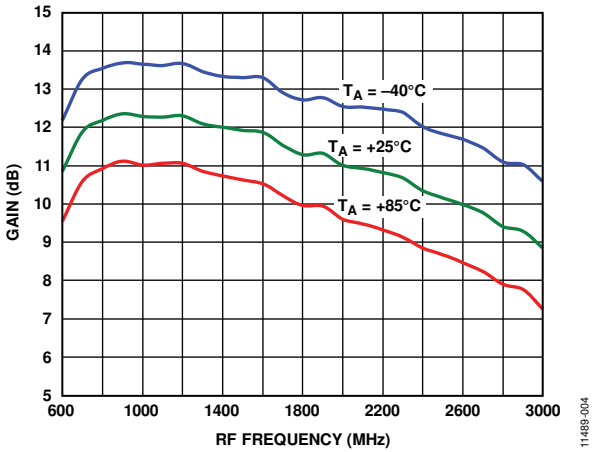

Figure 4. Gain vs. RF Frequency; IF Frequency = 200 MHz

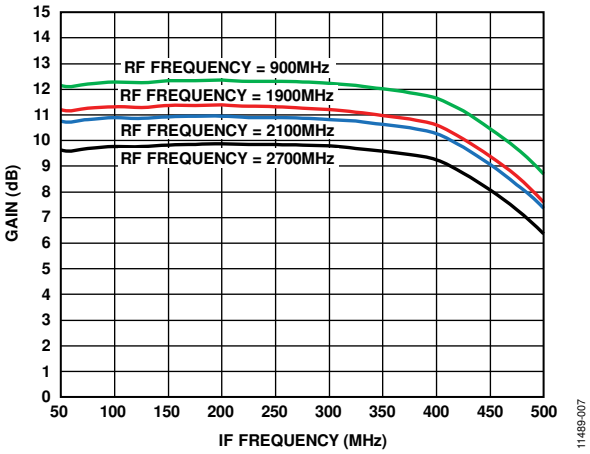

Figure 6. Gain vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

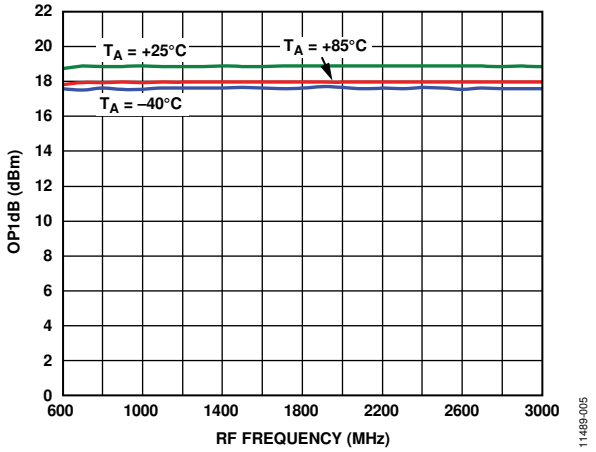

Figure 5. OP1dB vs. RF Frequency

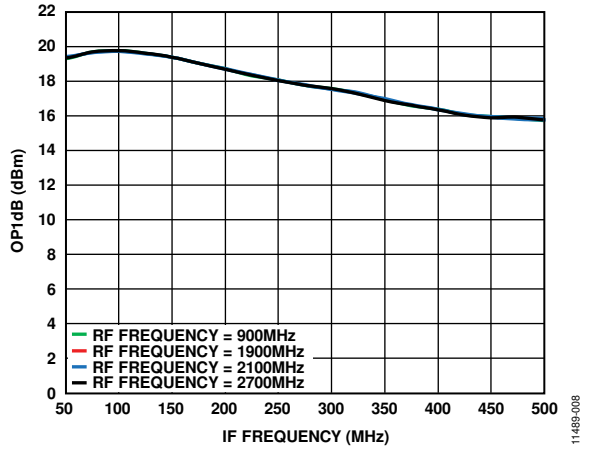

Figure 7. OP1dB vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

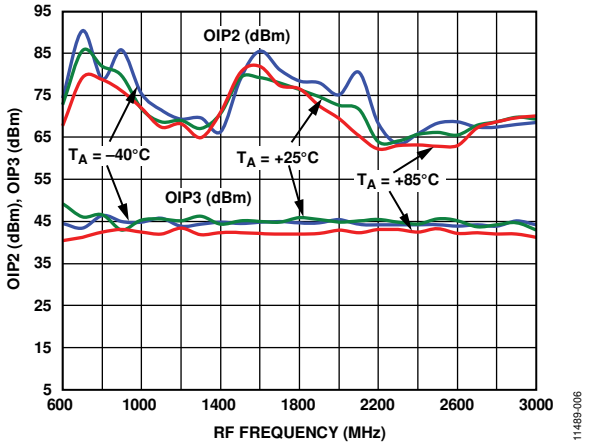

Figure 8. OIP2/OIP3 vs. RF Frequency; Measured on 1 V p-p on Each Tone at DGA Output

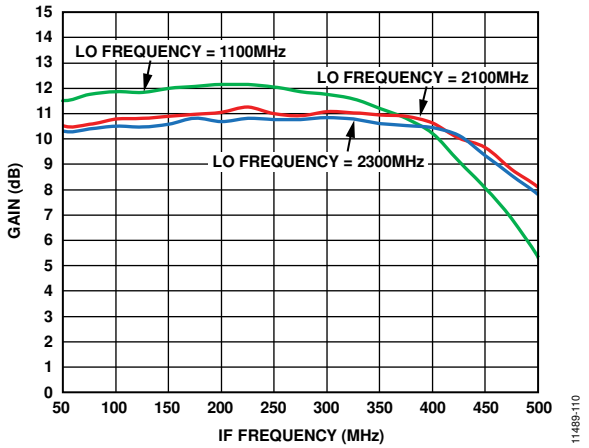

Figure 9. Gain vs. IF Frequency; RF Sweep with Fixed LO; IF and RF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

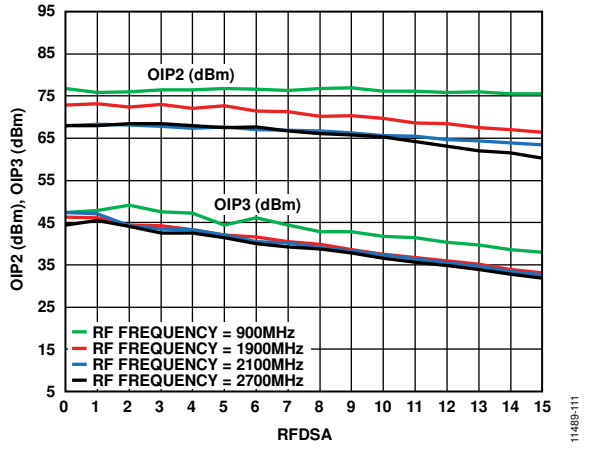

Figure 10. OIP2/OIP3 vs. RFDSA; Measured on 1 V p-p on Each Tone at DGA Output

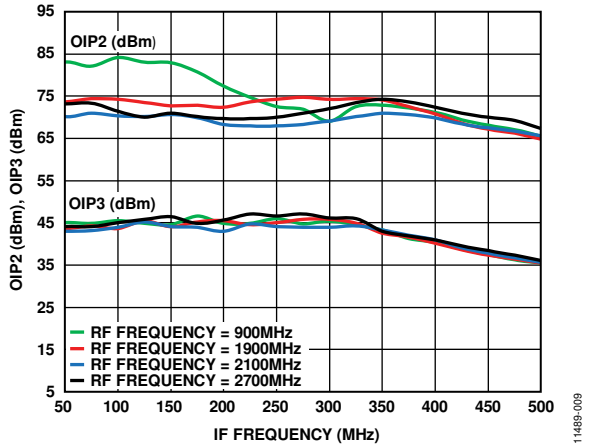

Figure 11. OIP2/OIP3 vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

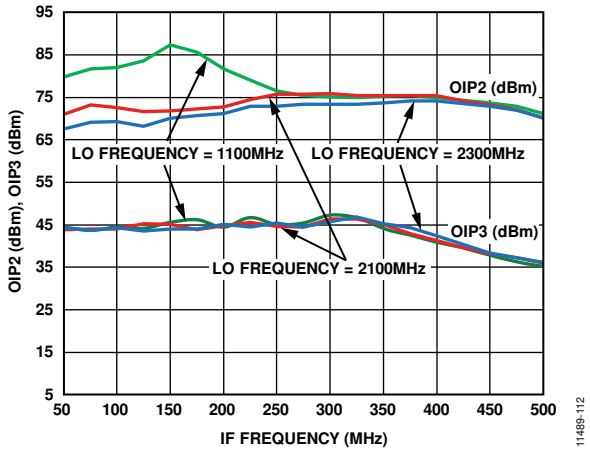

Figure 12. OIP2/OIP3 vs. IF Frequency; RF Sweep with Fixed LO; IF and RF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

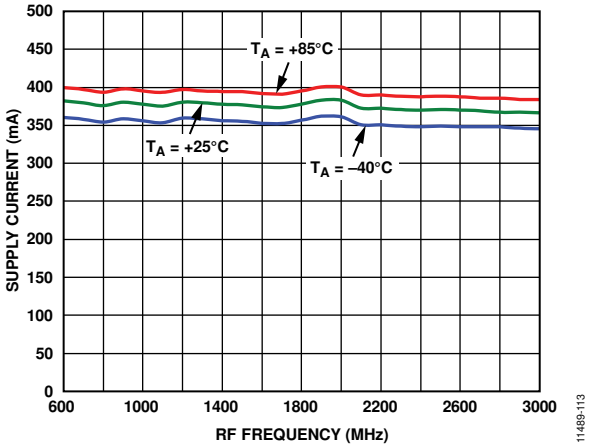

Figure 13. Supply Current vs. RF Frequency

PHASE-LOCKED LOOP (PLL)

VCCx = 5 V, T_A = 25°C, 120 kHz loop filter, f_{REF} = 153.6 MHz, PLL reference amplitude = 4 dBm, f_{PFD} = 38.4 MHz, measured at LO output, unless otherwise noted.

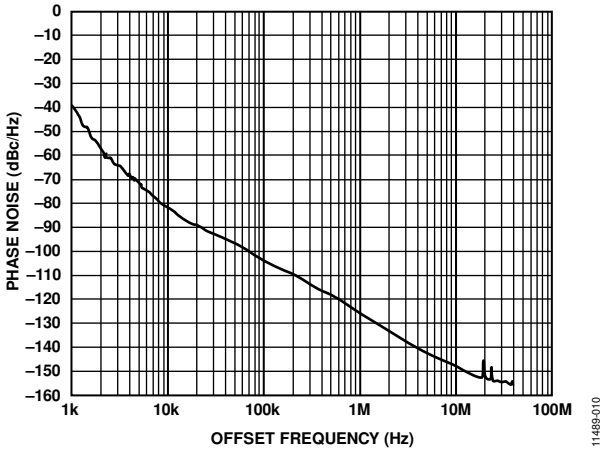

Figure 14. VCO2 Open-Loop VCO Phase Noise vs. Offset Frequency; f_{VCO2} = 3.4 GHz, LO_DIV_A = 00, VTUNE = 2 V

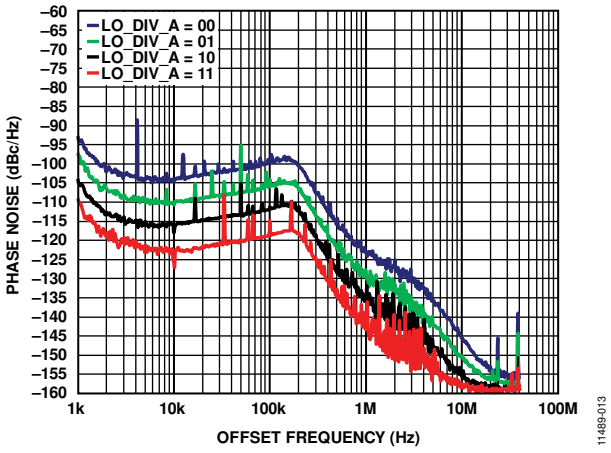

Figure 17. VCO2 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO2} = 3.4 GHz

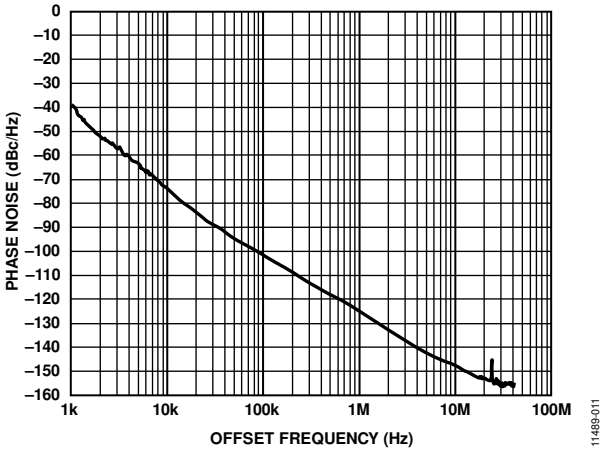

Figure 15. VCO1 Open-Loop Phase Noise vs. Offset Frequency; f_{VCO1} = 4.6 GHz, LO_DIV_A = 00, VTUNE = 2 V

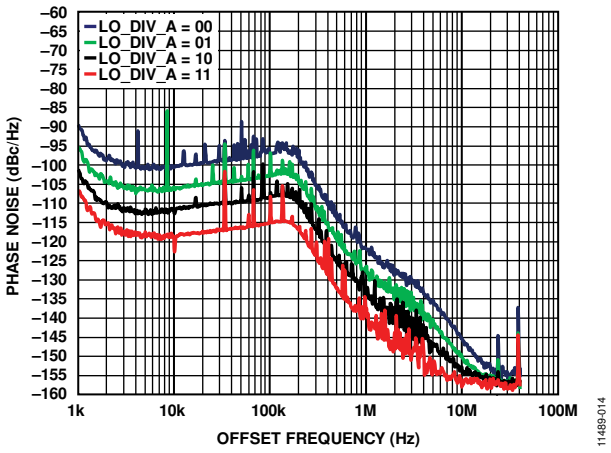

Figure 18. VCO1 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO1} = 4.6 GHz

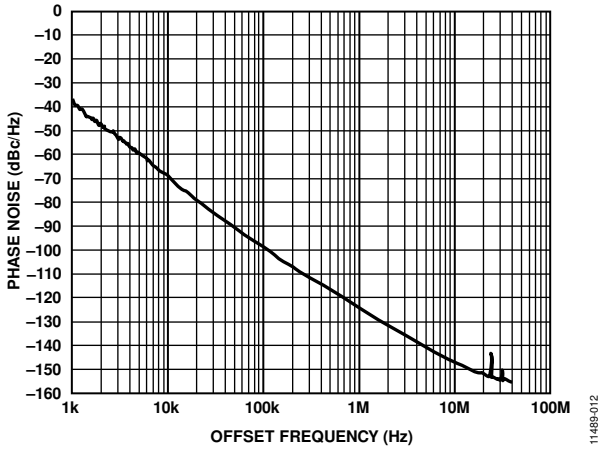

Figure 16. VCO0 Open-Loop Phase Noise vs. Offset Frequency; f_{VCO0} = 5.5 GHz, LO_DIV_A = 00, VTUNE = 2 V

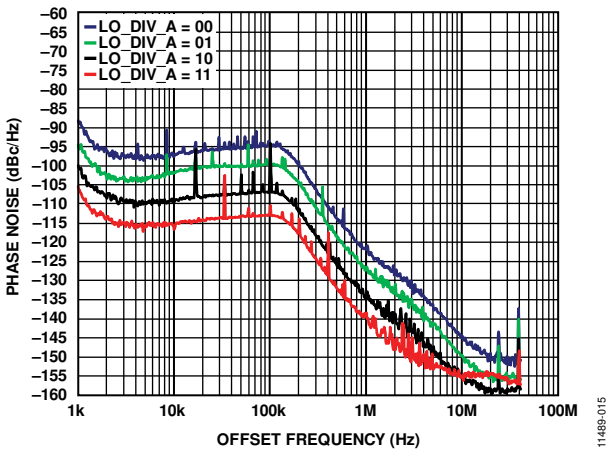

Figure 19. VCO0 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO0} = 5.532 GHz

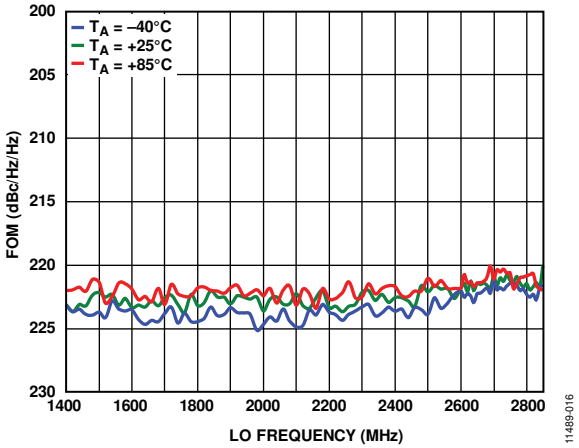

Figure 20. PLL Figure of Merit (FOM) vs. LO Frequency

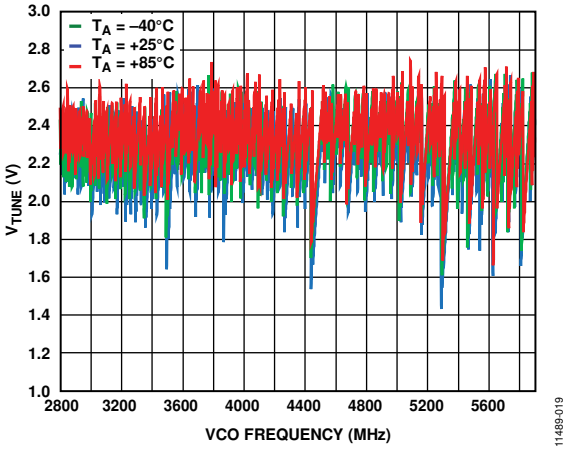

Figure 23. V_{TUNE} vs. VCO Frequency

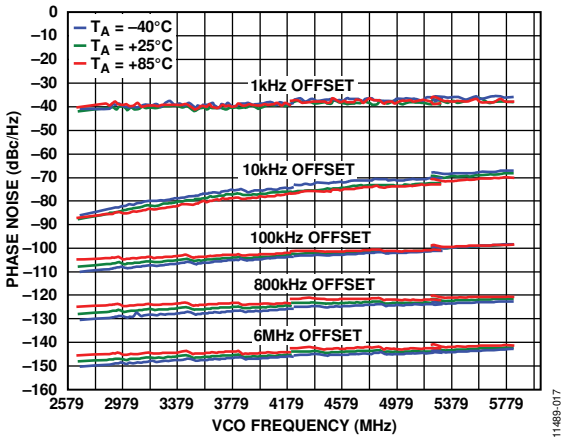

Figure 21. Open-Loop Phase Noise vs. VCO Frequency; LO_DIV_A = 00

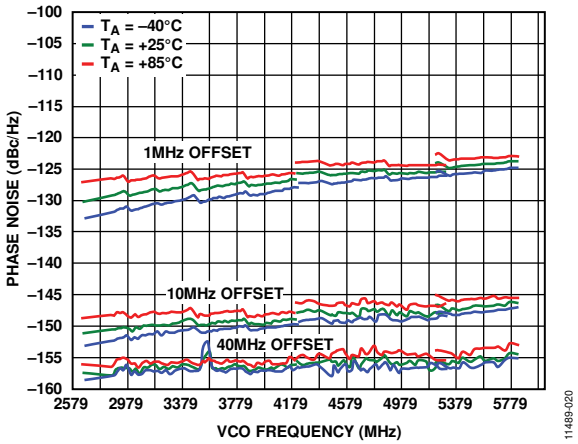

Figure 24. Open-Loop Phase Noise vs. VCO Frequency; LO_DIV_A = 00

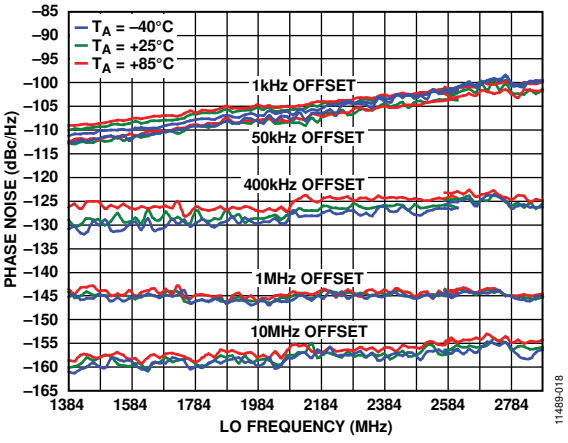

Figure 22. 120 kHz Bandwidth Loop Phase Noise, LO_DIV_A = 01; Offset = 1 kHz, 50 kHz, 400 kHz, 1 MHz, and 10 MHz

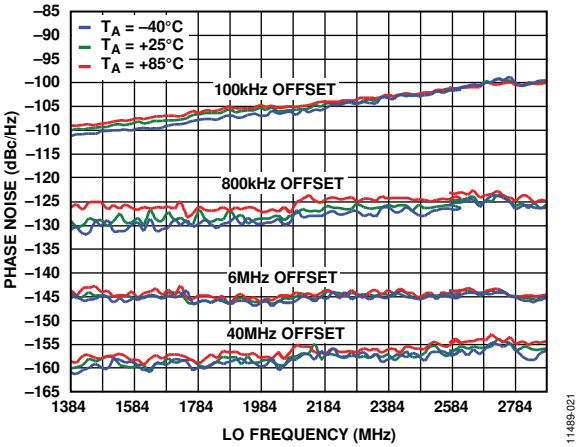

Figure 25. 120 kHz Bandwidth Loop Phase Noise, LO_DIV_A = 01; Offset = 100 kHz, 800 kHz, 6 MHz, and 40 MHz

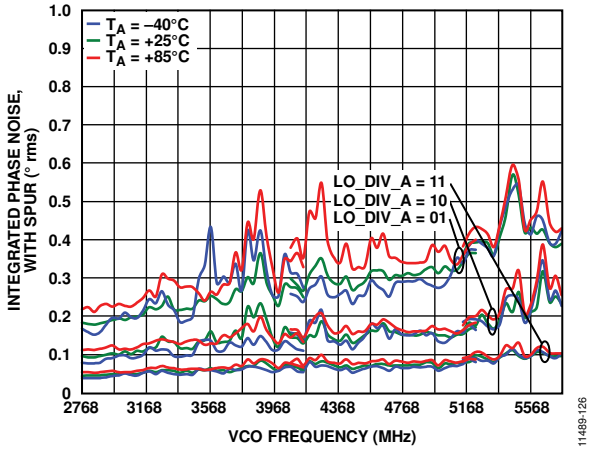

Figure 26. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency; LO_DIV_A = 01, 10, and 11, Including Spurs, for Various LO Divider Ratios

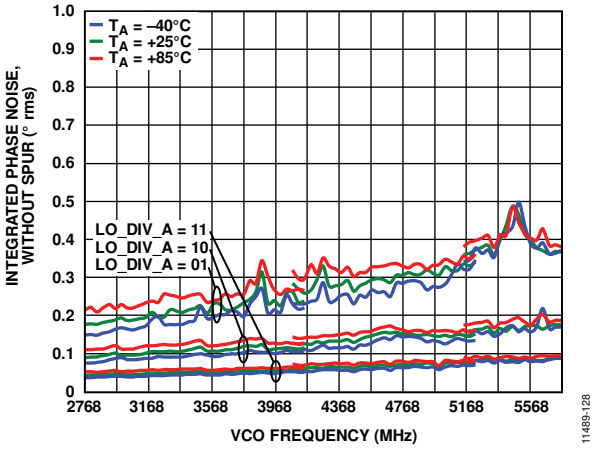

Figure 29. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency; LO_DIV_A = 01, 10, and 11, Excluding Spurs, for Various LO Divider Ratios

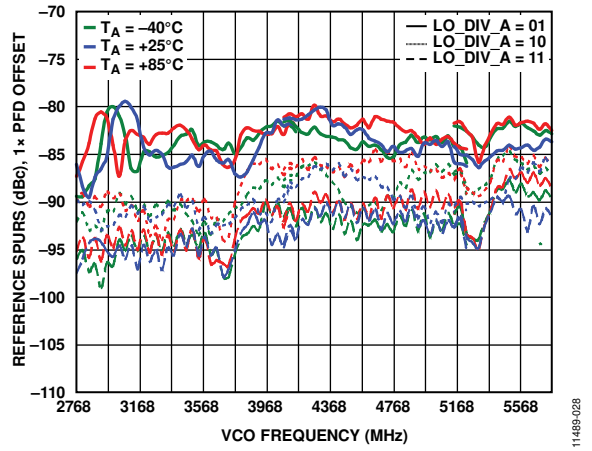

Figure 27. f_{PFD} Spurs vs. VCO Frequency; 1× PFD Offset; Measured at LO Output

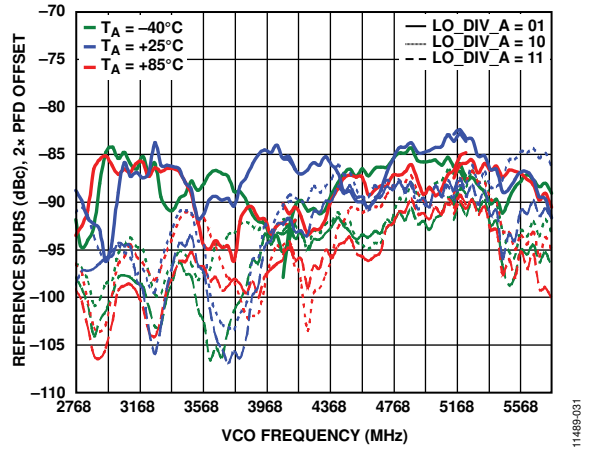

Figure 30. f_{PFD} Spurs vs. VCO Frequency; 2× PFD Offset; Measured at LO Output

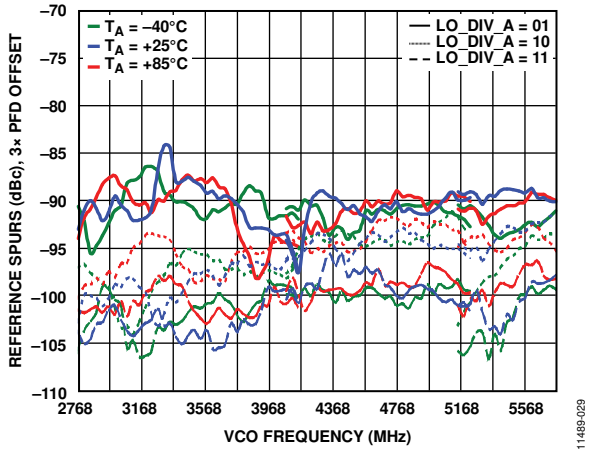

Figure 28. f_{PFD} Spurs vs. VCO Frequency; 3× PFD Offset; Measured at LO Output

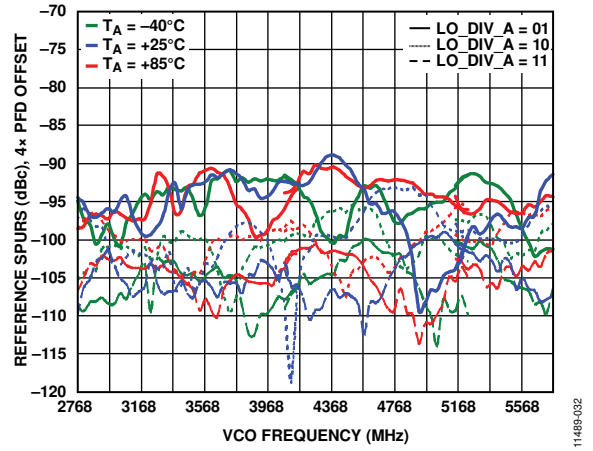

Figure 31. f_{PFD} Spurs vs. VCO Frequency; 4× PFD Offset; Measured at LO Output

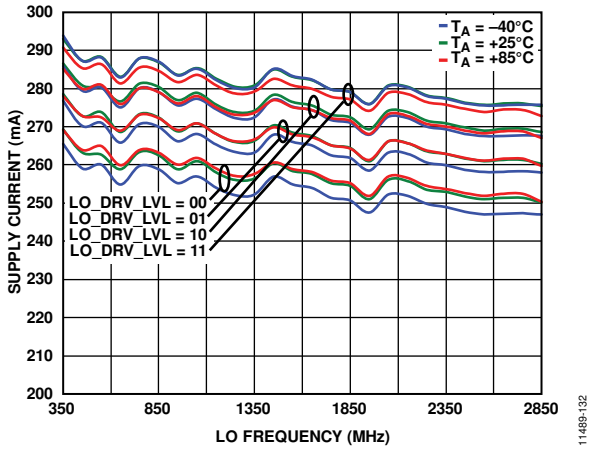

Figure 32. Supply Current vs. LO Frequency; LO_DRV_LVL = 00, 01, 10, and 11

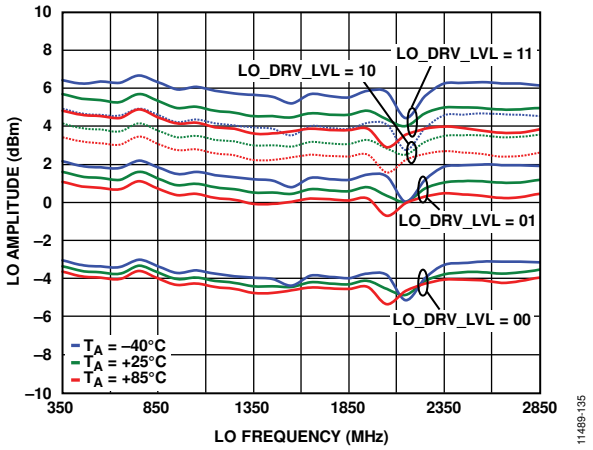

Figure 35. LO Amplitude vs. LO Frequency; LO_DRV_LVL = 00, 01, 10, and 11

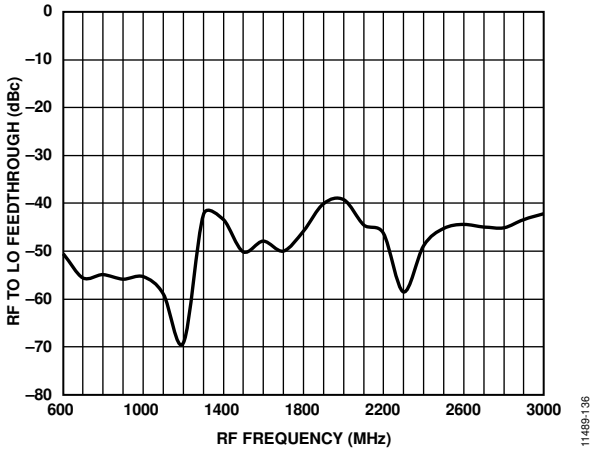

Figure 33. RF to LO Output Feedthrough, LO_DRV_LVL = 00

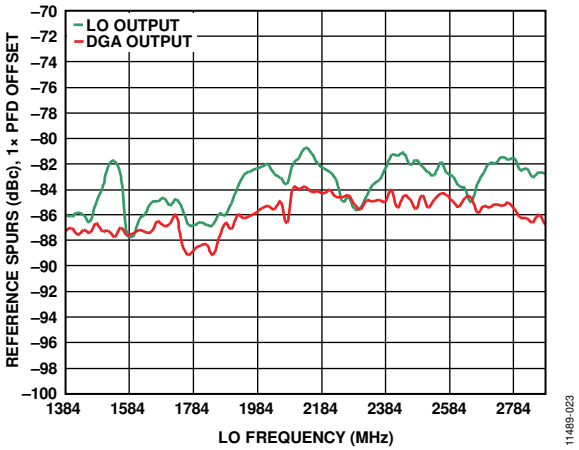

Figure 36. f_{PFD} Spurs, LO_DIV_A = 01, 1× PFD Offset; Measured on LO Output and DGA Output

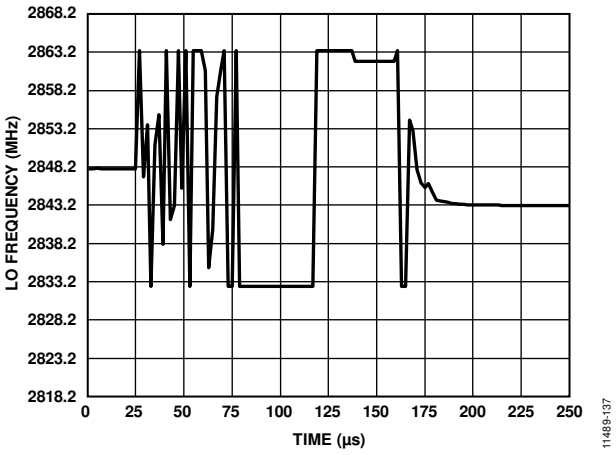

Figure 34. LO Frequency Settling Time, Loop Filter Bandwidth = 120 kHz

RF INPUT TO MIXER OUTPUT PERFORMANCE

VCCx = 5 V, T_A = 25°C, R_L = 250 Ω, external LO, P_{LO} = 0 dBm, RFDSA_SEL = 00 (0 dB), RFSW_SEL = 00 (RFIN0), BAL_CIN and BAL_COUT optimized, MIXER_BIAS, MIXER_RDAC, and MIXER_CDAC optimized for highest linearity, DGA and LO output disabled, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

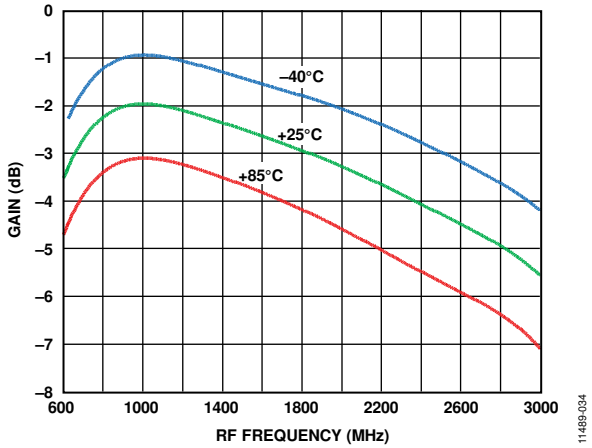

Figure 37. Mixer Gain vs. RF Frequency

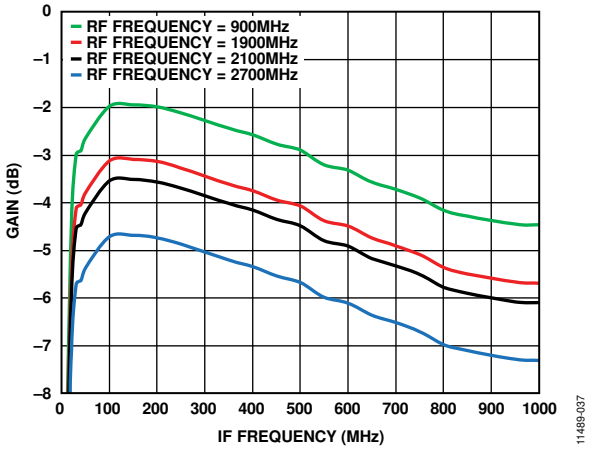

Figure 40. Mixer Gain vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

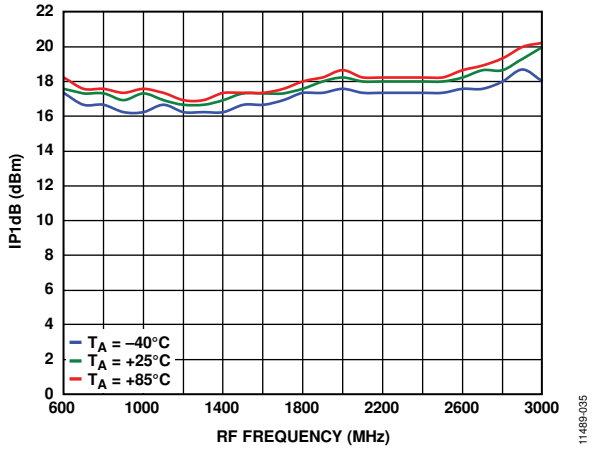

Figure 38. Mixer IP1dB vs. RF Frequency

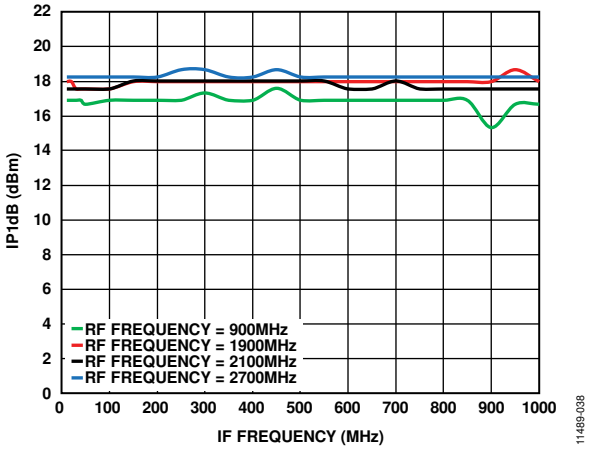

Figure 41. Mixer IP1dB vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

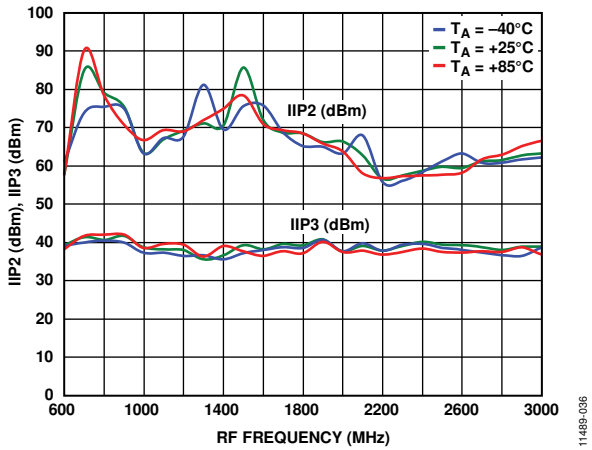

Figure 39. Mixer IIP2/IIP3 vs. RF Frequency; P_{IN} = –5 dBm/Tone, 1 MHz Spacing

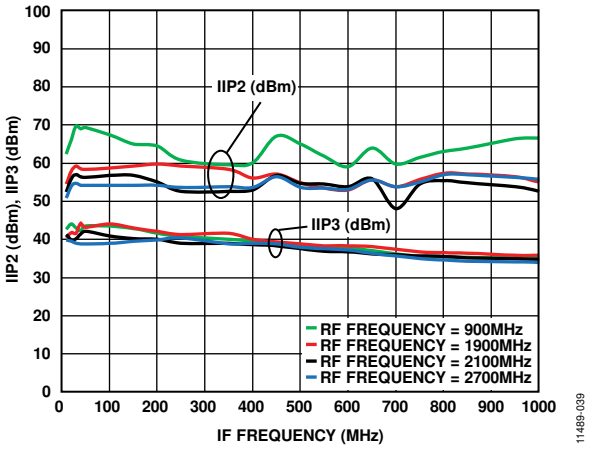

Figure 42. Mixer IIP2/IIP3 vs. IF Frequency; P_{IN} = –5 dBm/Tone, 1 MHz Spacing, LO Sweep with Fixed RF, IF Roll-Off

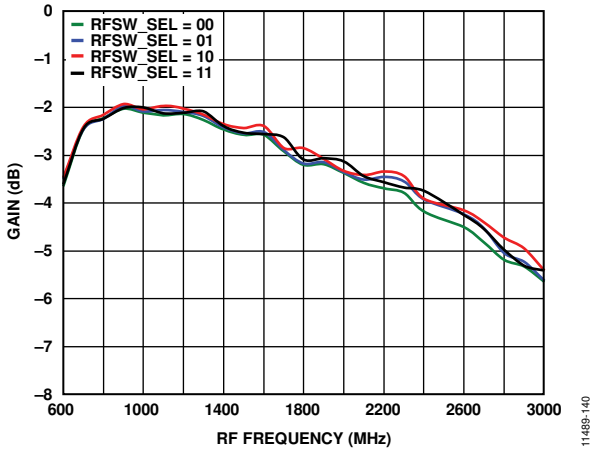

Figure 43. Mixer Gain vs. RF Frequency; RFSW_SEL = 00, 01, 10, and 11

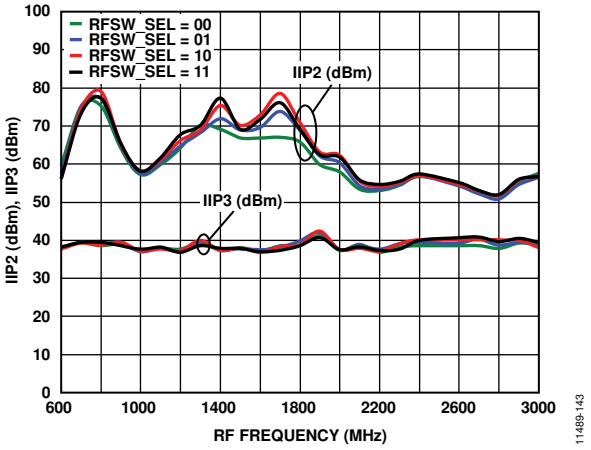

Figure 46. Mixer IIP2/IIP3 vs. RF Frequency; RFSW_SEL = 00, 01, 10, and 11

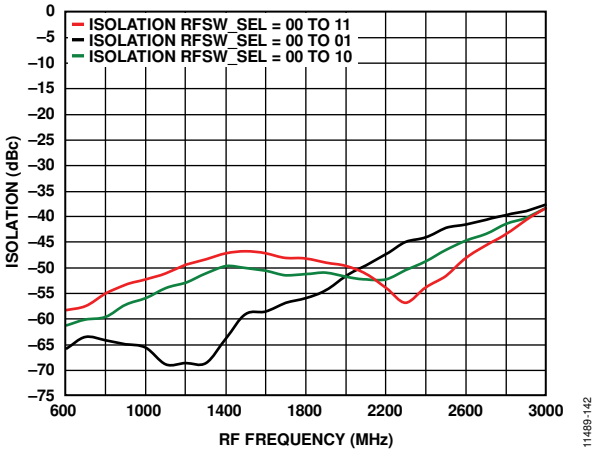

Figure 44. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 00 Driven

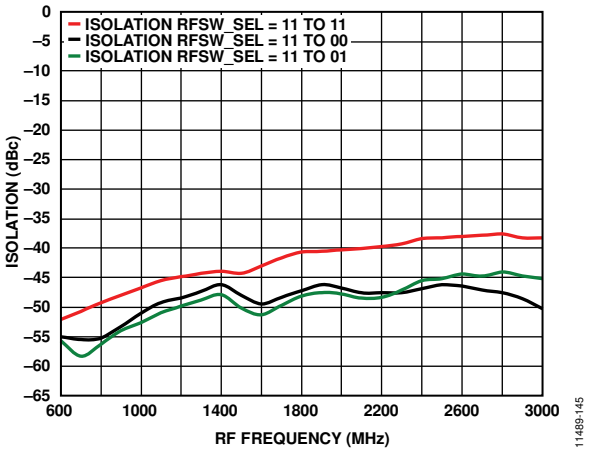

Figure 47. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 11 Driven

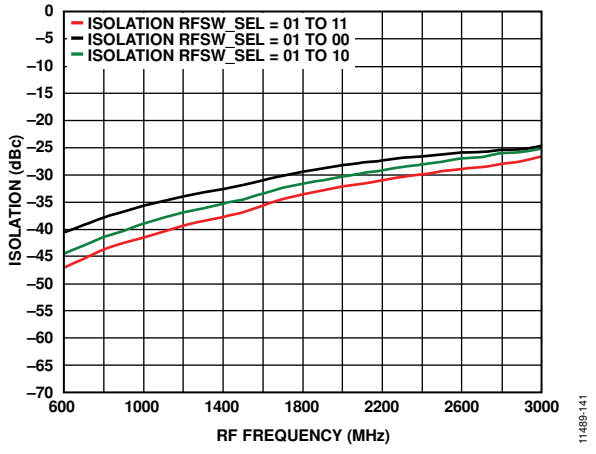

Figure 45. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 01 Driven

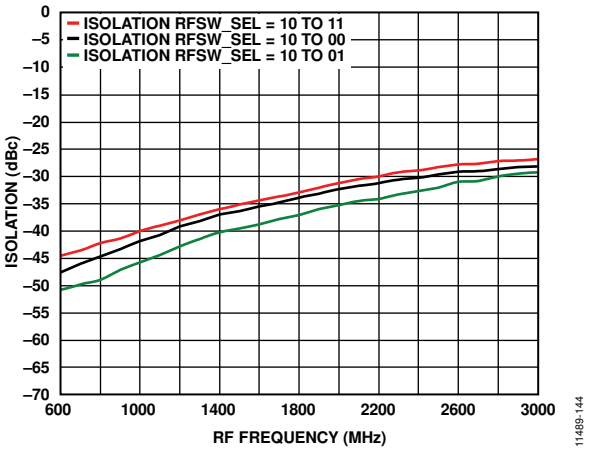

Figure 48. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 10 Driven

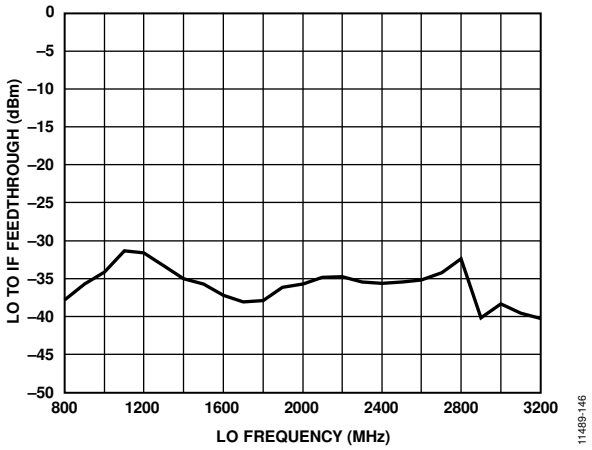

Figure 49. LO to IF Feedthrough at Mixer Output Without Filtering

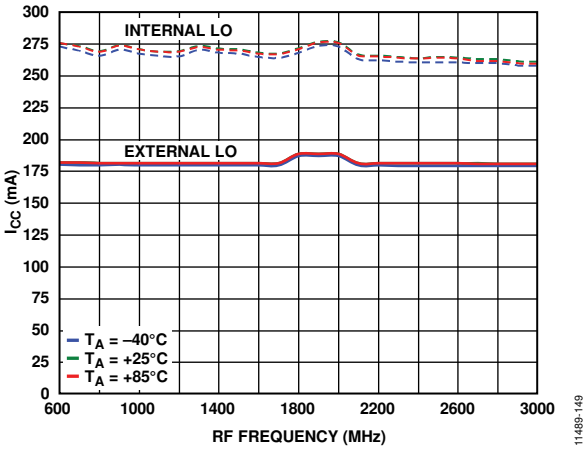

Figure 52. I_{CC} vs. RF Frequency; DGA and LO Output Disabled

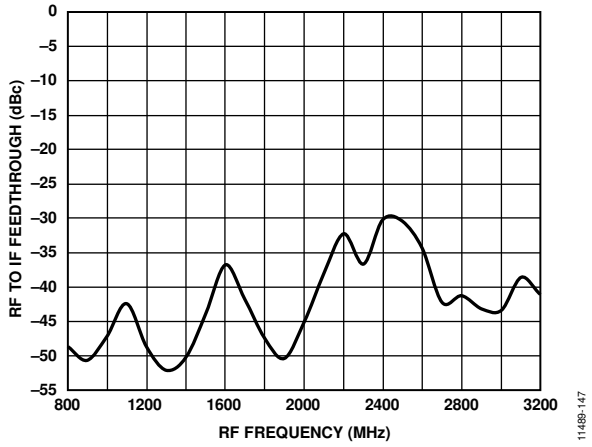

Figure 50. RF to IF Feedthrough at Mixer Output Without Filtering; Mixer Input Power = 0 dBm

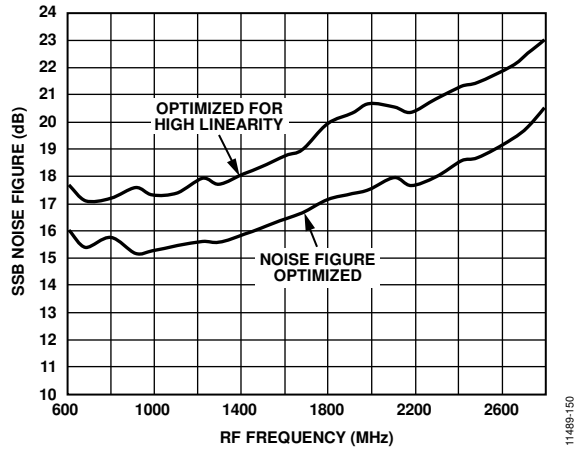

Figure 53. SSB Noise Figure vs. RF Frequency (see Table 16)

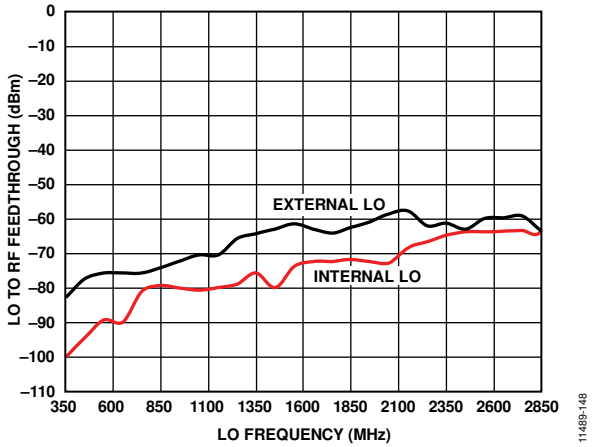

Figure 51. LO to RF Feedthrough; P_{LO} = 0 dBm

IF DGA

VCCx = 5 V, T_A = 25°C, R_S = R_L = 150 Ω, IF = 200 MHz, 2 V p-p differential output, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

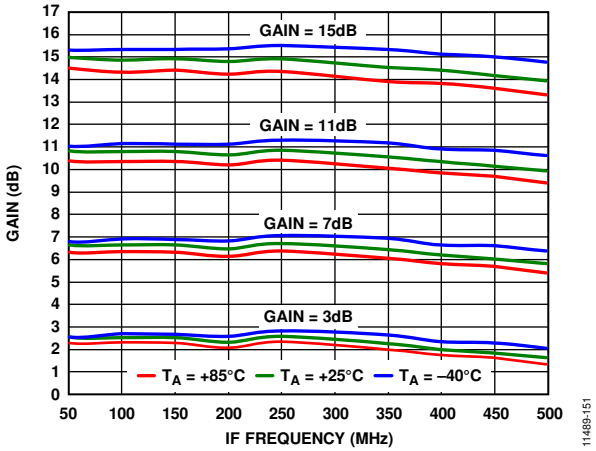

Figure 54. DGA Gain vs. IF Frequency and Temperature

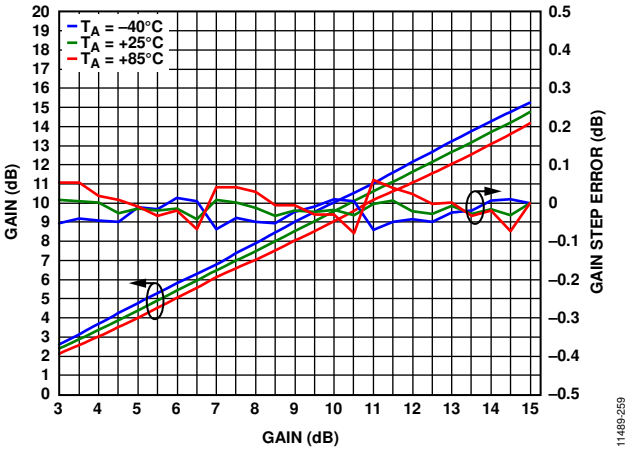

Figure 57. DGA Gain and Gain Step Error vs. Gain Setting and Temperature

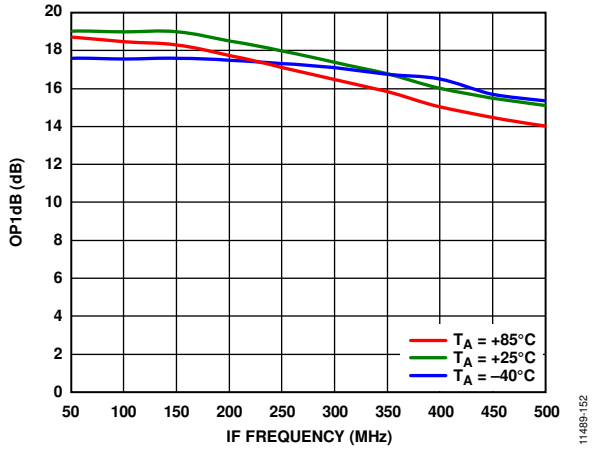

Figure 55. DGA OP1dB vs. Frequency and Temperature; Maximum Gain

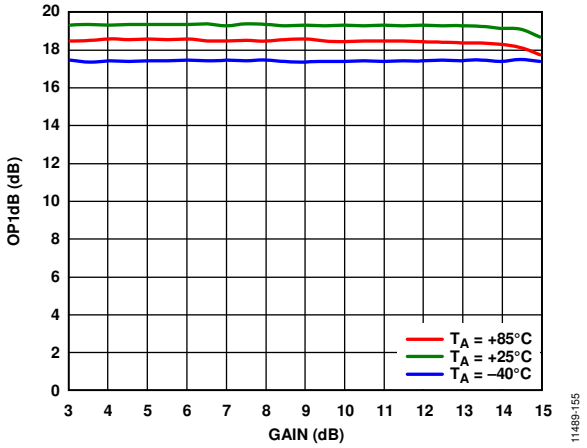

Figure 58. DGA OP1dB vs. Gain Setting and Temperature

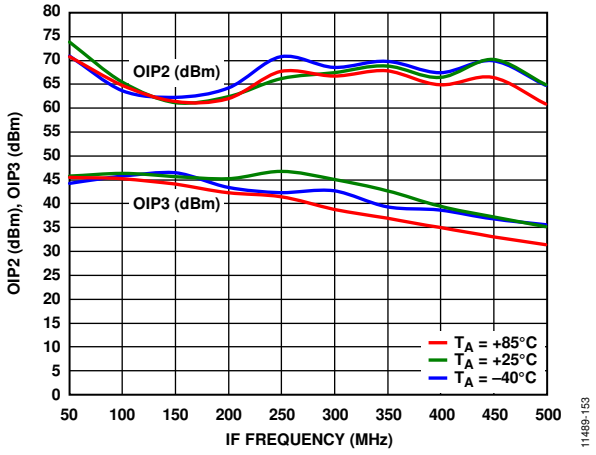

Figure 56. DGA OIP2/OIP3 vs. IF Frequency and Temperature; Maximum Gain

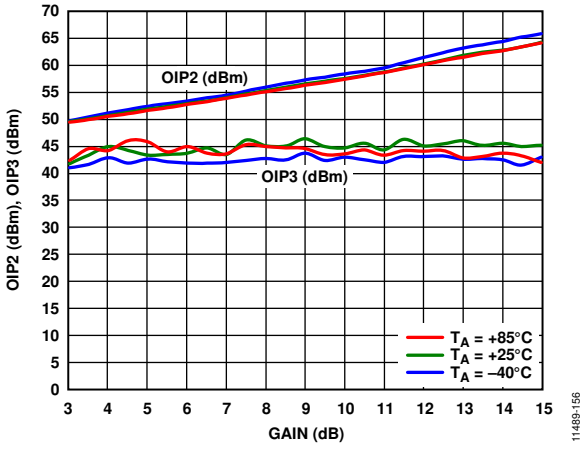

Figure 59. DGA OIP2/OIP3 vs. Gain Setting and Temperature

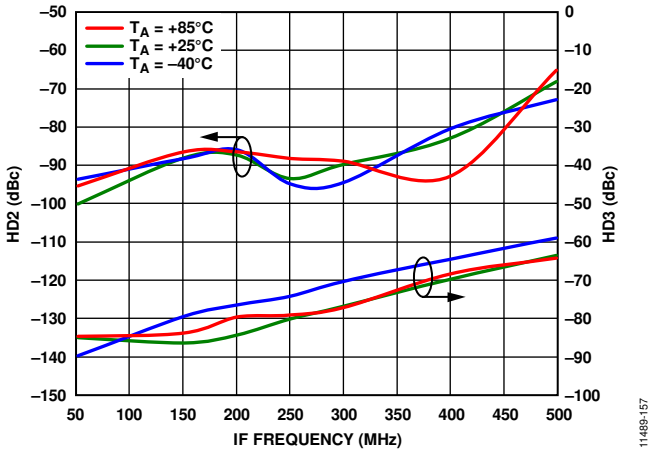

Figure 60. DGA HD2/HD3 vs. IF Frequency and Temperature; Maximum Gain

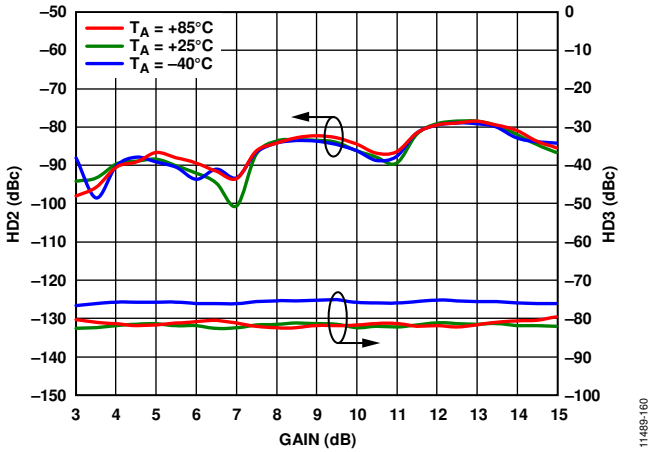

Figure 63. DGA HD2/HD3 vs. Gain Setting and Temperature

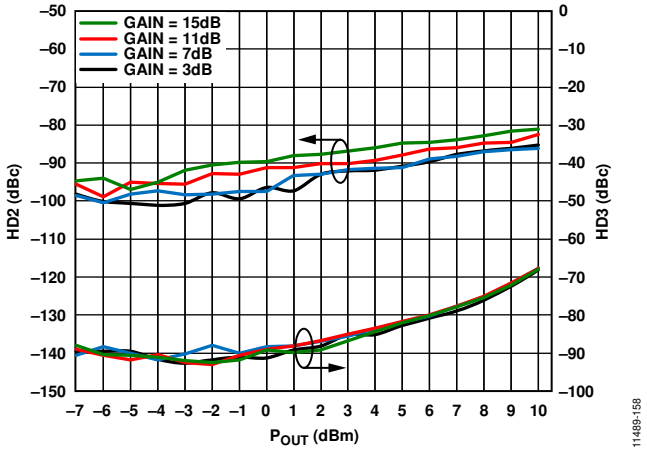

Figure 61. DGA HD2/HD3 vs. Output Power (P_{OUT}) and Gain Setting

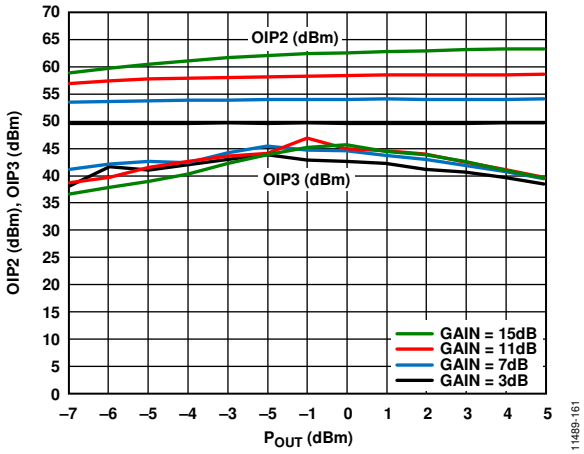

Figure 64. DGA OIP2/OIP3 vs. Output Power (P_{OUT}) and Gain Setting

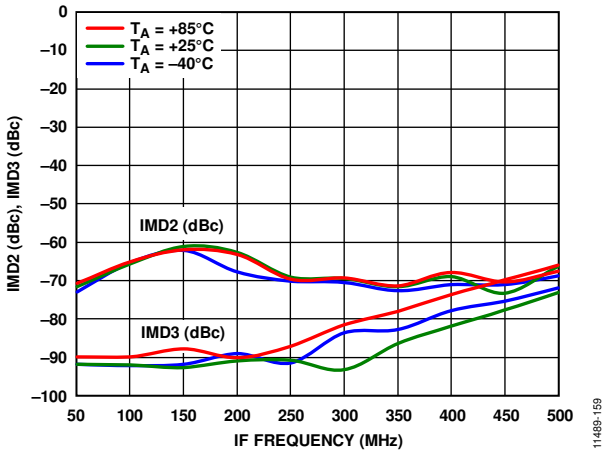

Figure 62. DGA IMD2/IMD3 vs. IF Frequency and Temperature; Maximum Gain

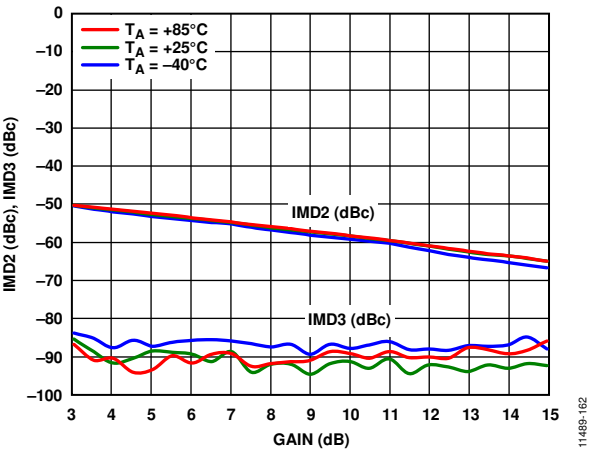

Figure 65. DGA IMD2/IMD3 vs. Gain Setting

SPURIOUS PERFORMANCE

$(N \times f_{RF}) - (M \times f_{LO})$ spur measurements were made using the standard evaluation board. Mixer spurious products were measured in decibels (dB) relative to the carrier (dBc) from the IF output power level. Data is shown for all spurious components greater than −115 dBc and frequencies of less than 3 GHz.

915 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 914 MHz, f_{LO} = 1114 MHz

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−34	−35				
	1	−43	0	−52	−16			
	2	−72	−60	−72	−67	−74		
	3	−102	−73	−103	−78	<−115	−80	
	4		−102	<−115	<−115	<−115	<−115	
	5			<−115	−105	<−115	<−115	<−115
	6				<−115	<−115	<−115	<−115

1910 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 1910 MHz, f_{LO} = 2110 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−38.208					
	1	−40.462	−0.001	−50.9				
	2		−59.208	−69.655	−62.35			
	3			−106.741	−74.322	−106.429		
	4				<−115	<−115	<−115	
	5				<−115	<−115	−110.954	
	6						<−115	<−115

2140 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 2140 MHz, f_{LO} = 2340 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−40					
	1	−36	0	−45				
	2		−58	−67	−59			
	3			<−115	−74	<−115		
	4				<−115	<−115	<−115	
	5					<−115	<−115	<−115
	6						<−115	<−115

2700 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 2700 MHz, f_{LO} = 2500 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−38.613					
	1	−40.126	−0.001	−43.84				
	2		−58.299	−67.06	−62.116			
	3				−73.603	<−115		
	4					<−115	<−115	
	5						<−115	<−115
	6							<−115

THEORY OF OPERATION

The ADRF6620 integrates the essential elements of a multi-channel loopback receiver that is typically used in digital predistortion systems. The main features of the ADRF6620 include a single-pole four throw (SP4T) RF input switch with tunable balun, variable attenuation, a wideband active mixer, and digitally programmable variable gain amplifier (DGA). In addition, the ADRF6620 integrates a local oscillator (LO) generation block consisting of a synthesizer and a multicore voltage controlled oscillator (VCO) with an octave range and low phase noise. The synthesizer uses a fractional-N phase-locked loop (PLL) to enable continuous LO coverage from 350 MHz to 2850 MHz.

Putting all the building blocks of the ADRF6620 together, the signal path through the device starts at the RF input, where one of four single-ended RF inputs is selected by the input mux and converted to a differential signal via a tunable balun. The differential RF signal is attenuated to an optimal input level via the digital step attenuator with 15 dB of attenuation range in steps of 1 dB. The RF signal is then mixed via a Gilbert cell mixer with the LO signal down to an IF frequency. The 255 Ω terminated differential output of the mixer is brought off chip to a pair of inductors and passed through an IF filter. The output of the IF filter is ac-coupled off chip and fed to an on-chip digital attenuator and IF DGA. The output of the IF DGA is then passed to an off-chip analog-to-digital converter (ADC).

RF INPUT SWITCHES

The ADRF6620 integrates a SP4T switch where one of four RF inputs is selected. The desired RF input can be selected using either pin control or register writes via the SPI. Compared to the serial write approach, pin control allows faster control over the switch. When the RFSW0 pin (Pin 38) and the RFSW1 pin (Pin 39) are used, the RF switches can switch at speeds of up to 100 ns. When serial port control is used, the switch time is 100 ns, plus the latency of the SPI programming.

The RFSW_MUX bit (Register 0x23, Bit 11) selects whether the RF input switch is controlled via the external pins or the SPI port. By default at power-up, the device is configured for serial control. Writing to the RFSW_SEL bits (Register 0x23, Bits[10:9]) allows selection of one of the four RF inputs. Alternatively, by setting the RFSW_MUX bit high, the RFSW0 and RFSW1 pins can be used to select the RF input. Table 10 summarizes the different control options for the RF inputs.

To maintain good channel-to-channel isolation, ensure that unused RF inputs are properly terminated. The RFINx ports are internally terminated with 50 Ω resistors and have a dc bias level of 2.5 V. To avoid disrupting the dc level, the recommended termination is a dc blocking capacitor to GND. Figure 66 shows the recommended configuration when only RFIN0 is used, and the other RF input ports are properly terminated.

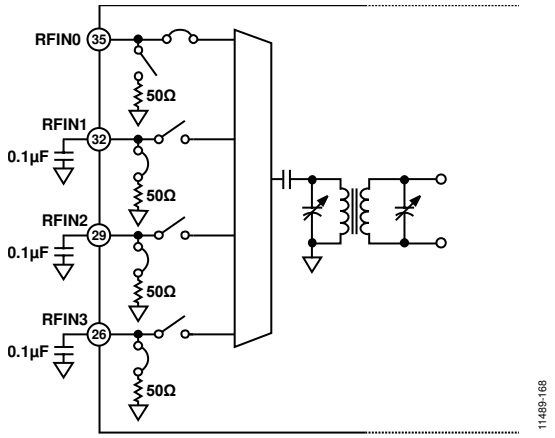

Figure 66. Terminating Unused RF Input Ports

Table 10. RF Input Selection Table

RFSW_MUX (Register Address 0x23[11])	SPI Control, RFSW_SEL (Register Address 0x23[10:9])		Pin Control		
Bit 11	**Bit 10**	**Bit 9**	**RFSW1, Pin 39**	**RFSW0, Pin 38**	**RF Input**
0	0	0	X[1]	X[1]	RFIN0
0	0	1	X[1]	X[1]	RFIN1
0	1	0	X[1]	X[1]	RFIN2
0	1	1	X[1]	X[1]	RFIN3
1	X[1]	X[1]	0	0	RFIN0
1	X[1]	X[1]	0	1	RFIN1
1	X[1]	X[1]	1	0	RFIN2
1	X[1]	X[1]	1	1	RFIN3

[1] X = don't care.