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Wideband Quadrature Modulator with Integrated Fractional-N PLL and VCOs

Data Sheet

ADRF6720

FEATURES

I/Q modulator with integrated fractional-N PLL
RF output frequency range: 700 MHz to 3000 MHz
Internal LO frequency range: 356.25 MHz to 2855 MHz
Output P1dB: 12.2 dBm at 2140 MHz
Output IP3: 32.6 dBm at 2140 MHz
Carrier feedthrough: −40.3 dBm at 2140 MHz
Sideband suppression: −37.6 dBc at 2140 MHz
Noise floor: −157.9 dBm/Hz at 2140 MHz
Baseband 1 dB modulation bandwidth: >1000 MHz
Baseband input bias level: 0.5 V
Power supply: 3.3 V/425 mA
Integrated RF tunable balun allowing single-ended RF output
Multicore integrated VCOs
HD3/IP3 optimization
Sideband suppression and carrier feedthrough optimization
High-side/low-side LO injection
Programmable via 3-wire serial port interface (SPI)
40-lead 6 mm × 6 mm LFCSP

APPLICATIONS

2G/3G/4G/LTE broadband communication systems
Microwave point-to-point radios
Satellite modems
Military/aerospace
Instrumentation

GENERAL DESCRIPTION

The ADRF6720 is a wideband quadrature modulator with an integrated synthesizer ideally suited for 3G and 4G communication systems. The ADRF6720 consists of a high linearity broadband modulator, an integrated fractional-N phase-locked loop (PLL), and four low phase noise multicore voltage controlled oscillators (VCOs).

The ADRF6720 local oscillator (LO) signal can be generated internally via the on-chip integer-N and fractional-N synthesizers, or externally via a high frequency, low phase noise LO signal. The internal integrated synthesizer enables LO coverage from 356.25 MHz to 2855 MHz using the multicore VCOs. In the case of internal LO generation or external LO input, quadrature signals are generated with a divide-by-2 phase splitter. When the ADRF6720 is operated with an external 1 × LO input, a polyphase filter generates the quadrature inputs to the mixer.

The ADRF6720 offers digital programmability for carrier feedthrough optimization, sideband suppression, HD3/IP3 optimization, and high-side or low-side LO injection.

The ADRF6720 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, RoHS-compliant, 6 mm × 6 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

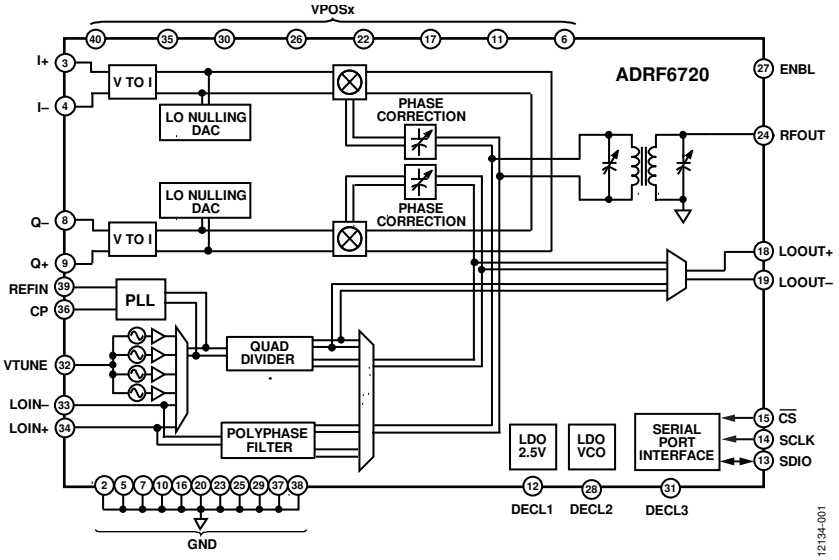

Figure 1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

4/14—Revision 0: Initial Version

SPECIFICATIONS

VPOSx = 3.3 V, T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE	RF output range	700		3000	MHz
	Internal LO range	356.25		2855	MHz
	External LO range	700		3000	MHz
RF OUTPUT = 940 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		5.8		dBm
Modulator Voltage Gain			1.82		dB
Output P1dB			13.1		dBm
Carrier Feedthrough			−44.0		dBm
Sideband Suppression			−47.1		dBc
Quadrature Error			−0.15		Degrees
I/Q Amplitude Balance			−0.01		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−66.1		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−60.6		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		66.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		36.2		dBm
Noise Floor	I/Q input with 500 mV dc bias and no RF output, 20 MHz carrier offset		−157.6		dBm/Hz
	I/Q input with 500 mV dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.3		dBm/Hz
RF OUTPUT = 1900 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		5.6		dBm
Modulator Voltage Gain			1.62		dB
Output P1dB			13.1		dBm
Carrier Feedthrough			−39.2		dBm
Sideband Suppression			−41.2		dBc
Quadrature Error			1.15		Degrees
I/Q Amplitude Balance			−0.0175		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−66.2		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−57.2		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		62.2		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		35.7		dBm
Noise Floor	I/Q input with 500 mV dc bias and no RF output, 20 MHz carrier offset		−158.8		dBm/Hz
	I/Q input with 500 mV dc bias and −10 dBm RF output, 20 MHz carrier offset		−158.1		dBm/Hz
RF OUTPUT = 2140 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		5		dBm
Modulator Voltage Gain			1.12		dB
Output P1dB			12.2		dBm
Carrier Feedthrough			−40.3		dBm
Sideband Suppression			−37.6		dBc
Quadrature Error			−1.15		Degrees
I/Q Amplitude Balance			−0.022		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−57.9		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−58.1		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		57.7		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		32.6		dBm
Noise Floor	I/Q input with 500 mV dc bias and no RF output, 20 MHz carrier offset		−157.9		dBm/Hz
	I/Q input with 500 mV dc bias and −10 dBm RF output, 20 MHz carrier offset		−156.3		dBm/Hz
RF OUTPUT = 2300 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		4.6		dBm
Modulator Voltage Gain			0.62		dB
Output P1dB			11.8		dBm
Carrier Feedthrough			−37.6		dBm
Sideband Suppression			−36.6		dBc
Quadrature Error			−1.5		Degrees
I/Q Amplitude Balance			−0.0285		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−54.8		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−56.6		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		57.6		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		30.4		dBm
Noise Floor	I/Q input with 500 mV dc bias and no RF output, 20 MHz carrier offset		−159.2		dBm/Hz
	I/Q input with 500 mV dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.5		dBm/Hz
RF OUTPUT = 2600 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		3.9		dBm
Modulator Voltage Gain			−0.08		dB
Output P1dB			11.3		dBm
Carrier Feedthrough			−36.5		dBm
Sideband Suppression			−42.3		dBc
Quadrature Error			−0.55		Degrees
I/Q Amplitude Balance			−0.021		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−60.3		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−54.7		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		56.6		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.45 V p-p differential		29.9		dBm
Noise Floor	I/Q input with 500 mV dc bias and no RF output, 20 MHz carrier offset		−159.2		dBm/Hz
	I/Q input with 500 mV dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.3		dBm/Hz
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to the modulator output				
Figure of Merit (FOM)[1]			−218.5		dBc/Hz/Hz
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
REFIN Input Frequency		5.7		320	MHz
REFIN Input Amplitude			4		dBm
Phase Detector Frequency		11.4		40	MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MUXOUT Output Level	Low (lock detect output selected)		0.25		V
	High (lock detect output selected)		2.7		V
MUXOUT Duty Cycle			50		%
CHARGE PUMP					
Charge Pump Current	Programmable to 250 µA, 500 µA, 750 µA, or 1000 µA		1000		µA
Output Compliance Range		1		2.8	V
PHASE NOISE, FREQUENCY = 940 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−97.8		dBc/Hz
	100 kHz offset		−120.8		dBc/Hz
	1 MHz offset		−144.4		dBc/Hz
	5 MHz offset		−154.4		dBc/Hz
	10 MHz offset		−154.9		dBc/Hz
	20 MHz offset		−155.3		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.175		° rms
Reference Spurs	f_{PFD}		−104.8		dBc
	$f_{PFD} \times 2$		−97.8		dBc
	$f_{PFD} \times 3$		−98.8		dBc
	$f_{PFD} \times 4$		−103		dBc
PHASE NOISE, FREQUENCY = 1900 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−91.5		dBc/Hz
	100 kHz offset		−114.5		dBc/Hz
	1 MHz offset		−139.9		dBc/Hz
	5 MHz offset		−151.4		dBc/Hz
	10 MHz offset		−153		dBc/Hz
	20 MHz offset		−153.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.332		° rms
Reference Spurs	f_{PFD}		−102		dBc
	$f_{PFD} \times 2$		−90.8		dBc
	$f_{PFD} \times 3$		−93.6		dBc
	$f_{PFD} \times 4$		−100.5		dBc
PHASE NOISE, FREQUENCY = 2140 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−92		dBc/Hz
	100 kHz offset		−115.7		dBc/Hz
	1 MHz offset		−140.3		dBc/Hz
	5 MHz offset		−151.3		dBc/Hz
	10 MHz offset		−152.1		dBc/Hz
	20 MHz offset		−152.9		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.305		° rms
Reference Spurs	f_{PFD}		−95.9		dBc
	$f_{PFD} \times 2$		−93.1		dBc
	$f_{PFD} \times 3$		−87.4		dBc
	$f_{PFD} \times 4$		−91.5		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PHASE NOISE, FREQUENCY = 2300 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−94.1		dBc/Hz
	100 kHz offset		−114.6		dBc/Hz
	1 MHz offset		−138.7		dBc/Hz
	5 MHz offset		−150.1		dBc/Hz
	10 MHz offset		−151.4		dBc/Hz
	20 MHz offset		−152.6		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.270		° rms
Reference Spurs	f_{PFD}		−100.8		dBc
	$f_{PFD} \times 2$		−95.6		dBc
	$f_{PFD} \times 3$		−89.4		dBc
	$f_{PFD} \times 4$		−93.1		dBc
PHASE NOISE, FREQUENCY = 2600 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−91.5		dBc/Hz
	100 kHz offset		−111.3		dBc/Hz
	1 MHz offset		−136.8		dBc/Hz
	5 MHz offset		−148.3		dBc/Hz
	10 MHz offset		−150		dBc/Hz
	20 MHz offset		−150.7		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.378		°rms
Reference Spurs	f_{PFD}		−97.4		dBc
	$f_{PFD} \times 2$		−89.3		dBc
	$f_{PFD} \times 3$		−95.2		dBc
	$f_{PFD} \times 4$		−91.4		dBc
LO INPUT/OUTPUT					
LO Output Frequency Range	LO output	700		2855	MHz
LO Output Level	2 × LO or 1 × LO mode, into a 50 Ω load, LO buffer enabled at 2140 MHz				
	LO_DRV_LVL = 0		−5.1		dBm
	LO_DRV_LVL = 1		−0.5		dBm
	LO_DRV_LVL = 2		3		dBm
LO Input Level	Externally applied LO, PLL disabled	−6	0	+6	dBm
LO Input Impedance	Externally applied LO, PLL disabled		50		Ω
BASEBAND INPUTS	I± and Q± pins				
I and Q Input DC Bias Level			0.5		V
Bandwidth	1 dB		>1000		MHz
Differential Input Impedance	Frequency = 10 MHz[2]		465		Ω
Differential Input Capacitance	Frequency = 10 MHz[2]		1.84		pF
OUT ENABLE	ENBL pin				
Turn-On Settling Time	ENBL high to low (90% of envelope), when Register 0x01[10] = 1, Register 0x10[10] = 1		190		ns
Turn-Off Settling Time	ENBL low to high (10% of envelope), when Register 0x01[10] = 1, Register 0x10[10] = 1		20		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL LOGIC	SCLK, SDIO, $\overline{CS}$, and ENBL				
Input Voltage High (V_{IH})		1.4			V
Input Voltage Low (V_{IL})				0.7	V
Input Current (I_{IH}/I_{IL})		−1		1	µA
Input Capacitance (C_{IN})			5		pF
Output Voltage High (V_{OH})	I_{OH} = −100 uA	2.3			V
Output Voltage Low (V_{OL})	I_{OL} = 100 uA			0.2	V
POWER SUPPLIES					
Voltage Range	VPOSx		3.3		V
Supply Current	Tx mode at internal LO mode (PLL, internal VCO , and modulator enabled, LO output driver disabled)		425		mA
	Tx mode at external 1× LO mode (PLL, internal VCO disabled, modulator enabled, LO output driver disabled)		228		mA
	LO output driver; LO_DRV_LVL bits (Register 0x22[7:6]) = 10		50		mA
	Power-down mode		14.5		mA

[1] The figure of merit (FOM) is computed as phase noise (dBc/Hz) − 10log10(f_{PFD}) − 20log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm with a 38.4 MHz f_{PFD}. The FOM was computed at a 50 kHz offset.
[2] Refer to Figure 47 for a plot of input impedance over frequency.

TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Typ	Max	Units
t_{SCLK}	Serial clock period	38			ns
t_{DS}	Setup time between data and rising edge of SCLK	8			ns
t_{DH}	Hold time between data and rising edge of SCLK	8			ns
t_S	Setup time between falling edge of $\overline{CS}$ and SCLK	10			ns
t_H	Hold time between rising edge of $\overline{CS}$ and SCLK	10			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation			231	ns
t_z	Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance			5	ns

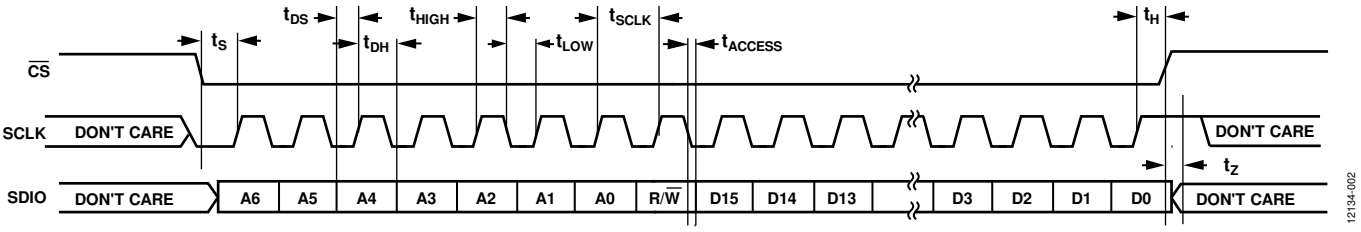


Figure 2. Serial Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
I+, I−, Q+, Q−	−0.5 V to +1.5 V
LOIN+, LOIN−	16 dBm differential
REFIN	−0.3 V to +3.6 V
ENBL	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
$\overline{CS}$, SCLK, SDIO	−0.3 V to +3.6 V
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
40-Lead LFCSP	30.23	0.44	°C/W

[1] See JEDEC standard JESD51-2 for information on optimizing thermal impedance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

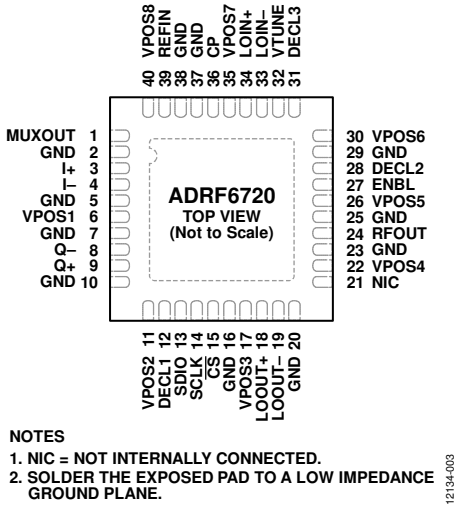


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MUXOUT	Multiplexer Output. This output allows a digital lock detect signal, a voltage proportional to absolute temperature (VPTAT), or a buffered, frequency-scaled reference signal to be accessed externally. The output is selected by programming Bits[6:4] in Register 0x21.
2, 10	GND	Baseband Ground.
3, 4	I+, I–	Differential In-Phase Baseband Inputs.
5, 7	GND	Mixer Core (I and Q) Ground.
6	VPOS1	3.3 V Supply Voltage for Baseband. Decouple VPOS1 with 100 pF and 0.1 µF capacitors located close to the pin.
8, 9	Q–, Q+	Differential Quadrature Baseband Inputs.
11	VPOS2	3.3 V Supply Voltage for 2.5 V LDO. Decouple VPOS2 with 100 pF and 0.1 µF capacitors located close to the pin.
12	DECL1	Decoupling Pin for 2.5 V LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
13	SDIO	Serial Data Input/Output for SPI.
14	SCLK	Serial Clock Input/Output for SPI.
15	$\overline{CS}$	Chip Select Input/Output for SPI.
16	GND	Digital Ground.
17	VPOS3	3.3 V Supply Voltage for LO. Decouple VPOS3 with 100 pF and 0.1 µF capacitors located close to the pin.
18, 19	LOOUT+, LOOUT–	Differential LO Outputs. Either the internally generated LO or external 1 × LO/2 × LO is available at 1 × LO or 2 × LO on these pins.
20	GND	LO Ground.
21	NIC	Not Internally Connected. This pin can be left open or tied to RF ground.
22	VPOS4	3.3 V Supply Voltage for RF. Decouple VPOS4 with 100 pF and 0.1 µF capacitors located close to the pin.
23, 25	GND	RF Ground.
24	RFOUT	Single-Ended 0 V DC RF Output.
26	VPOS5	3.3 V Supply Voltage for RF. Decouple VPOS5 with 100 pF and 0.1 µF capacitors located close to the pin.
27	ENBL	Enables/Disables the Circuit Blocks. References the settings at Register 0x01 and Register 0x10. Refer to the ENBL section for more information.
28	DECL2	Decoupling Pin for VCO LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
29	GND	VCO Ground.

Pin No.	Mnemonic	Description
30	VPOS6	3.3 V Supply Voltage for VCO LDO. Decouple VPOS6 with 100 pF and 0.1 µF capacitors located close to the pin.
31	DECL3	Decoupling Pin for VCO LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
32	VTUNE	VCO Tuning Voltage.
33, 34	LOIN–, LOIN+	Differential External LO Inputs.
35	VPOS7	3.3 V Supply Voltage for Charge Pump. Decouple VPOS7 with 100 pF and 0.1 µF capacitors located close to the pin.
36	CP	Charge Pump Output.
37	GND	Charge Pump Ground.
38	GND	PLL Reference Ground.
39	REFIN	PLL Reference Input.
40	VPOS8	3.3 V Supply Voltage for PLL Reference. Decouple VPOS8 with 100 pF and 0.1 µF capacitors located close to the pin.
	EP	Exposed Pad. Solder the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VPOSx = 3.3 V; T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz; f_{PFD} = 38.4 MHz; f_{REF} = 153.6 MHz at 4 dBm referred to 50 Ω (1 V p-p); 20 kHz loop filter, unless otherwise noted.

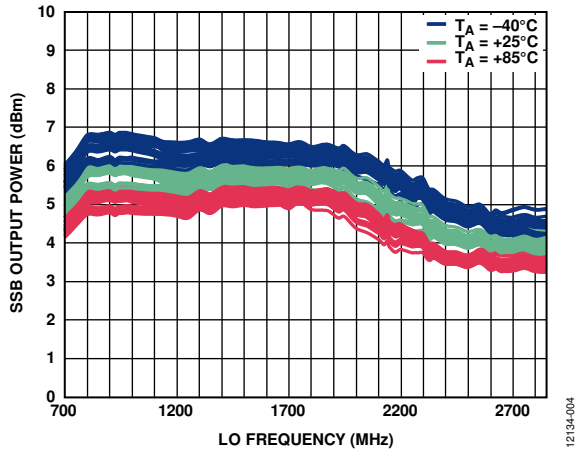


Figure 4. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

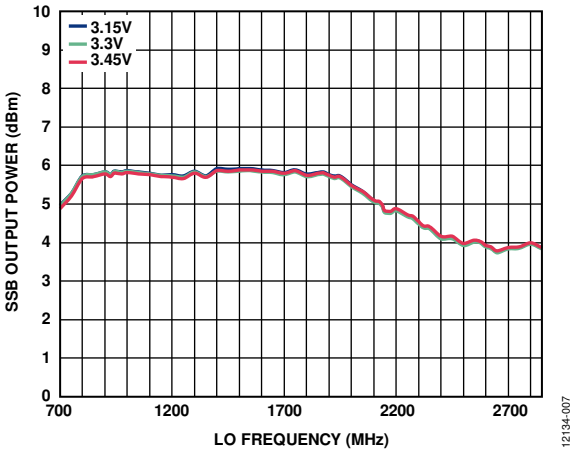


Figure 7. SSB Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Supply

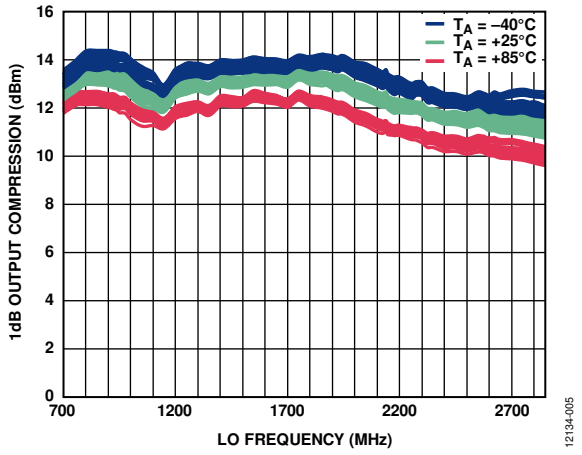


Figure 5. SSB 1 dB Output Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

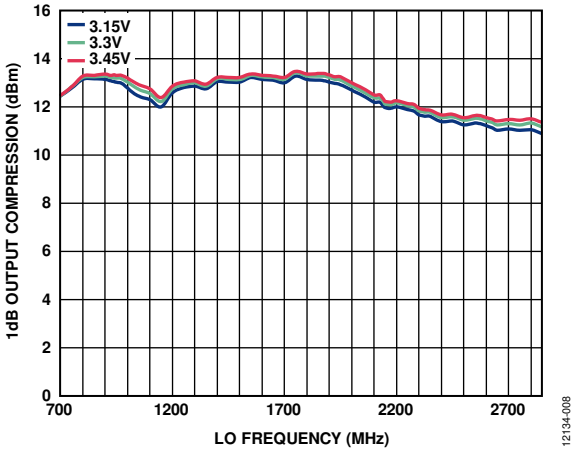


Figure 8. SSB 1 dB Output Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Supply

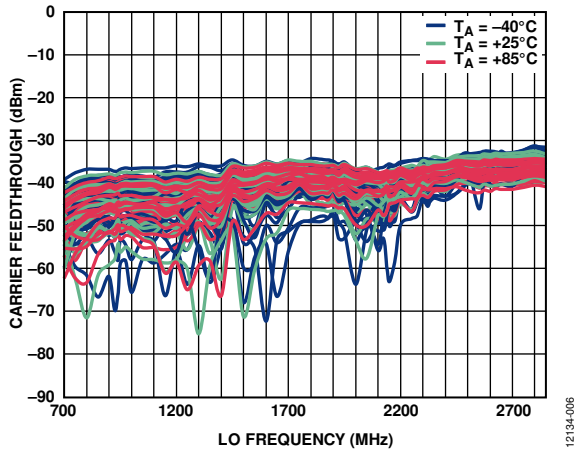


Figure 6. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature Before Nulling; Multiple Devices Shown

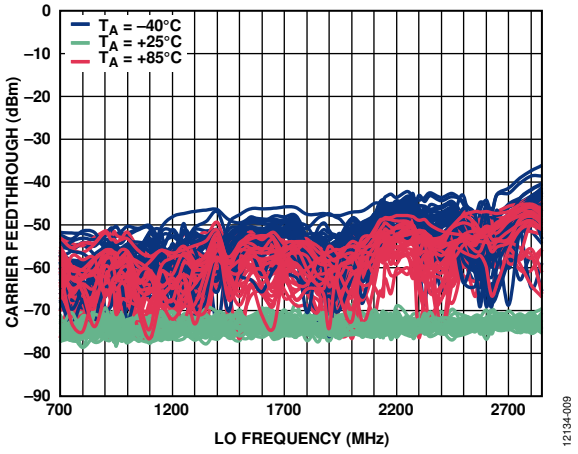


Figure 9. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature After Nulling Using DCOFF_I and DCOFF_Q at 25°C; Multiple Devices Shown

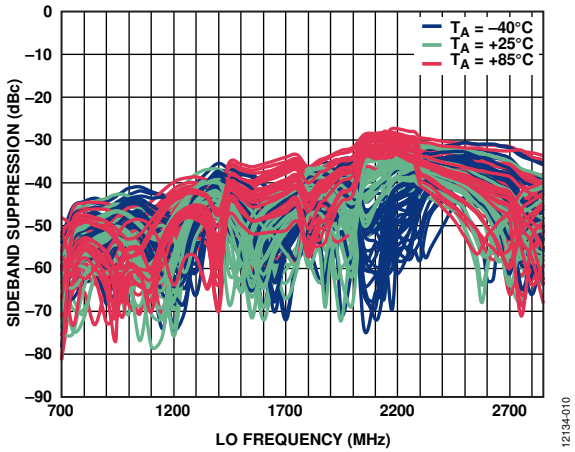


Figure 10. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature Before Nulling; Multiple Devices Shown

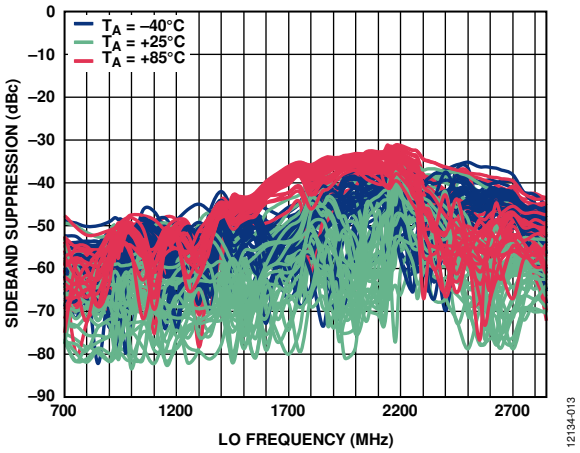


Figure 13. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature After Nulling Using I_LO and Q_LO at 25°C; Multiple Devices Shown

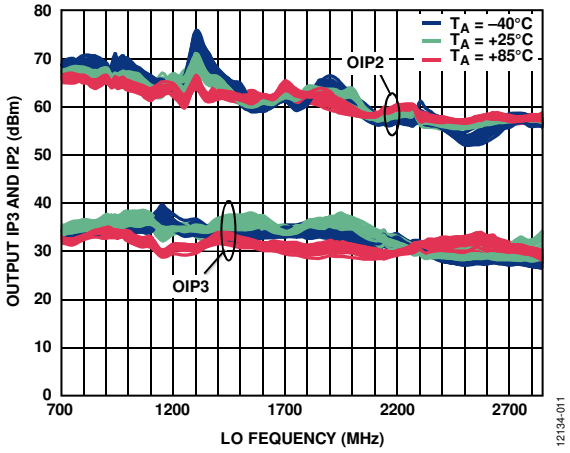


Figure 11. OIP3 and OIP2 vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ −5 dBm per Tone); Multiple Devices Shown

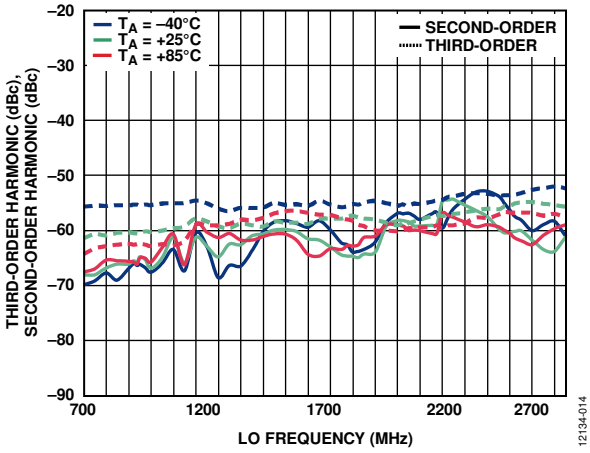


Figure 14. Second- and Third-Order Harmonics vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ 5 dBm)

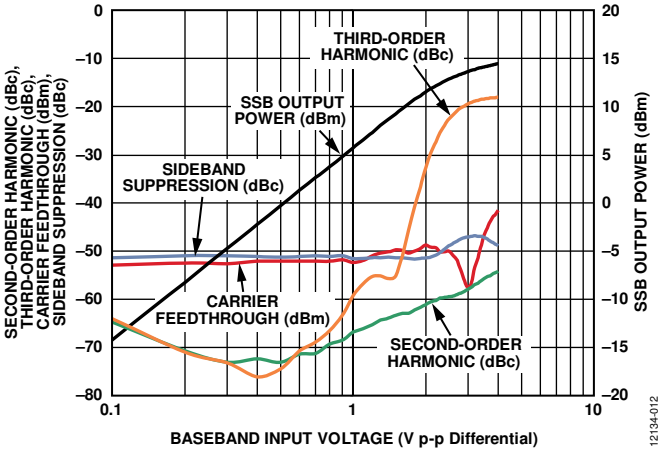


Figure 12. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 940 MHz)

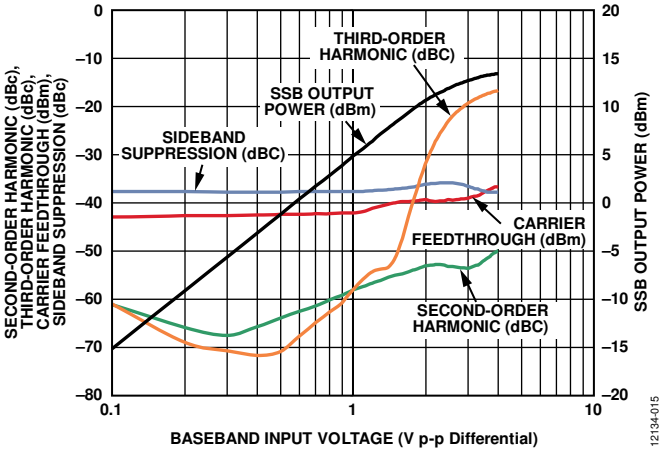


Figure 15. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2140 MHz)

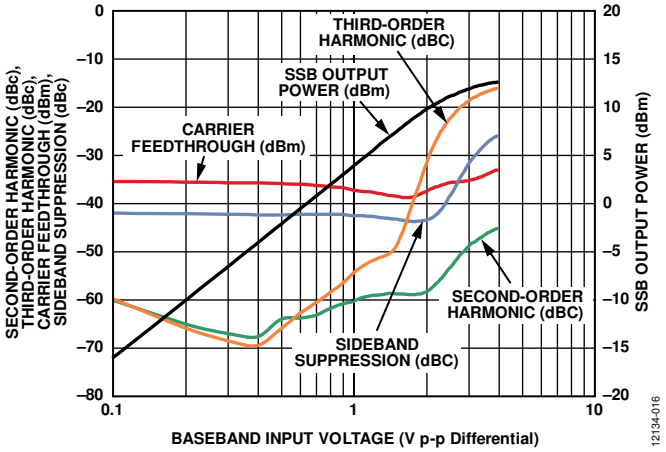


Figure 16. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2600 MHz)

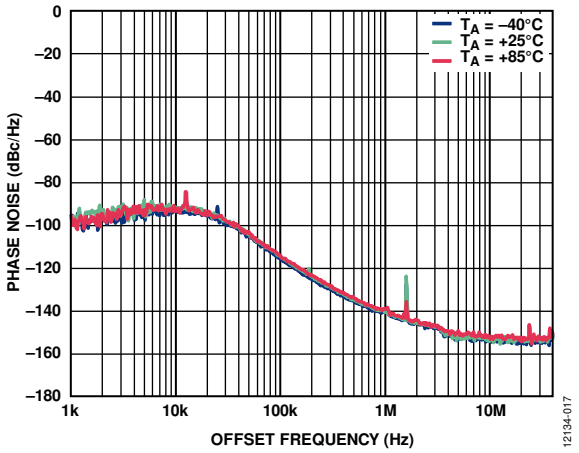


Figure 17. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 1900 MHz; 20 kHz Loop Filter

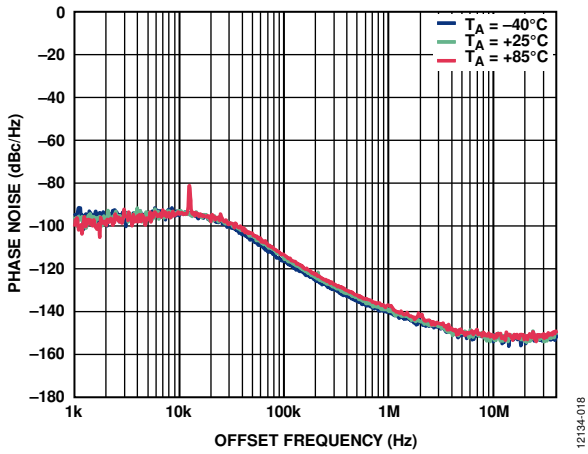


Figure 18. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2300 MHz; 20 kHz Loop Filter

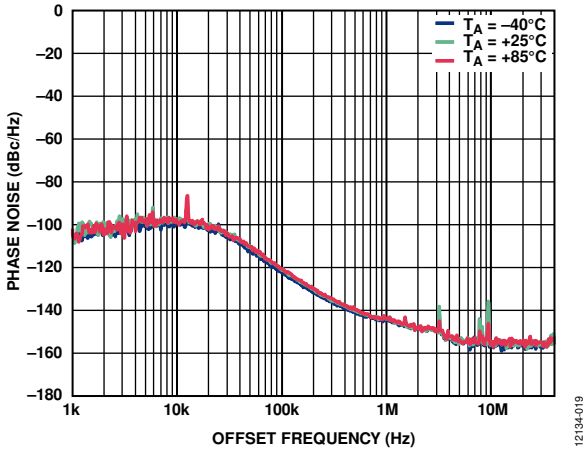


Figure 19. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 940 MHz; 20 kHz Loop Filter

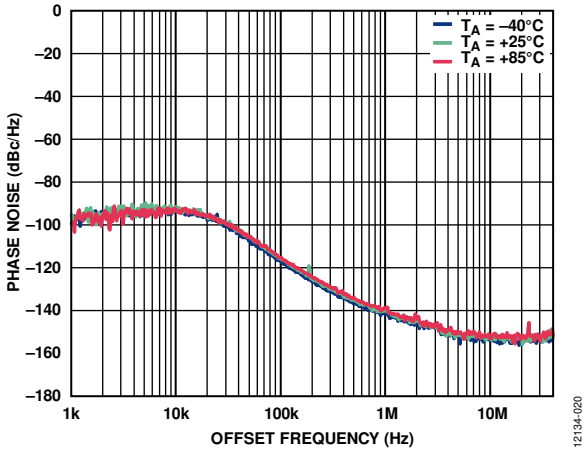


Figure 20. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2140 MHz; 20 kHz Loop Filter

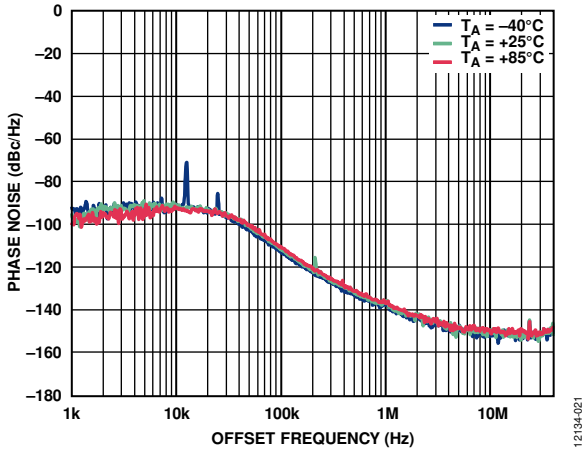


Figure 21. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2600 MHz; 20 kHz Loop Filter

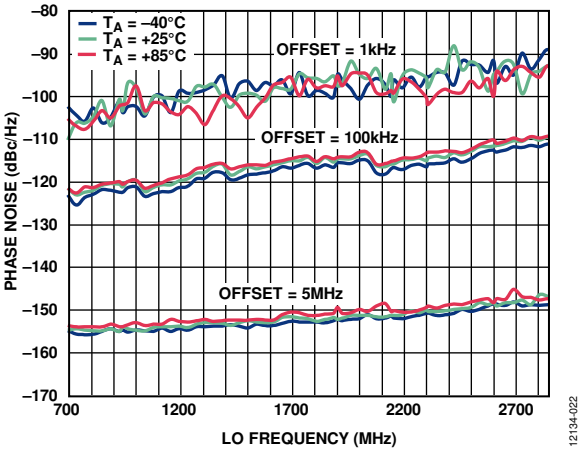


Figure 22. Closed-Loop Phase Noise vs. LO Frequency at 1 kHz, 100 kHz, and 5 MHz Offsets

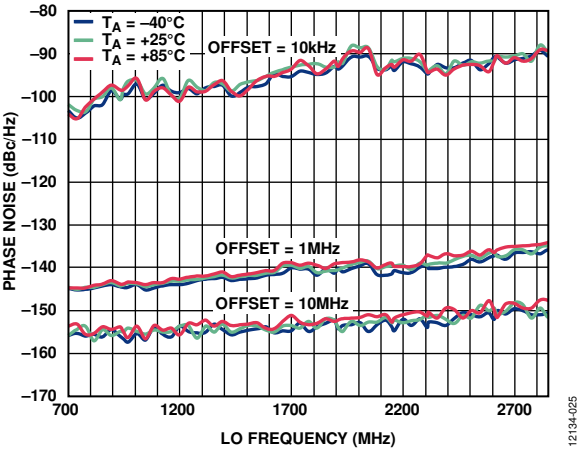


Figure 25. Closed-Loop Phase Noise vs. LO Frequency at 10 kHz, 1 MHz, and 10 MHz Offsets

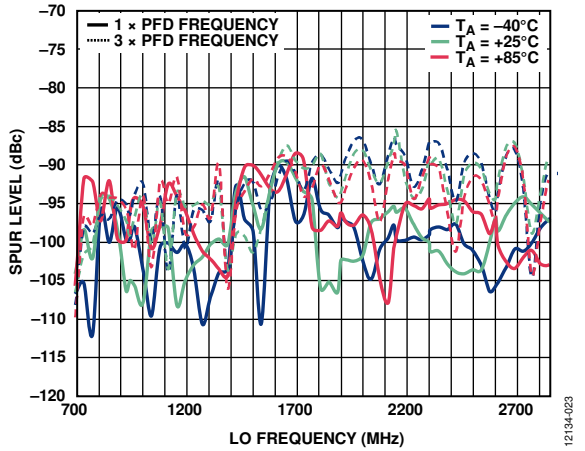


Figure 23. PLL Reference Spurs vs. LO Frequency (1 × PFD and 3 × PFD) at Modulator Output

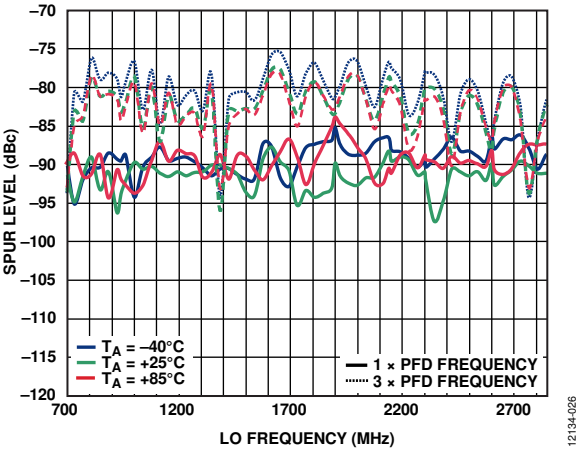


Figure 26. PLL Reference Spurs vs. LO Frequency (1 × PFD and 3 × PFD) at LO Output

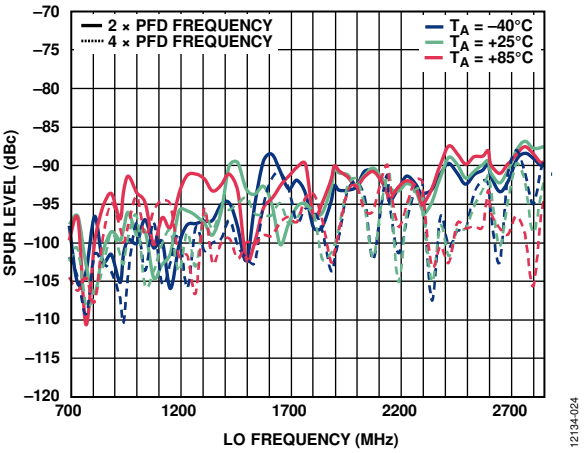


Figure 24. PLL Reference Spurs vs. LO Frequency (2 × PFD and 4 × PFD) at Modulator Output

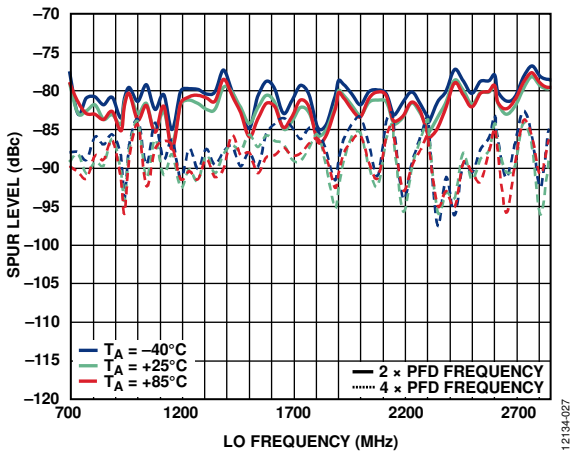


Figure 27. PLL Reference Spurs vs. LO Frequency (2 × PFD and 4 × PFD) at LO Output

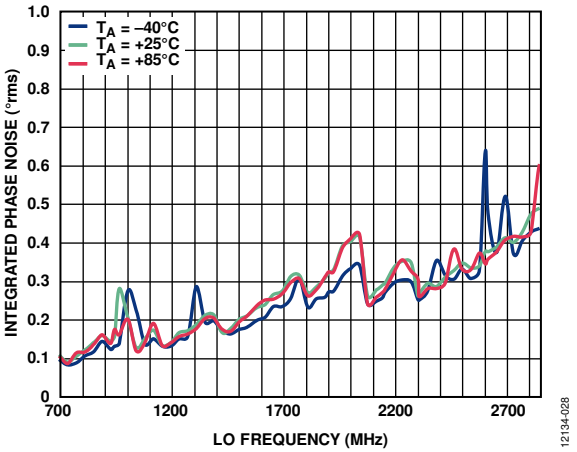


Figure 28. Integrated Phase Noise with Spurs vs. LO Frequency and Temperature

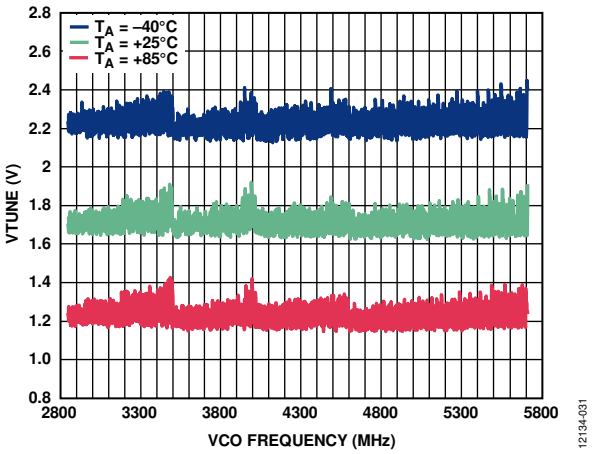


Figure 31. VTUNE vs. VCO Frequency and Temperature

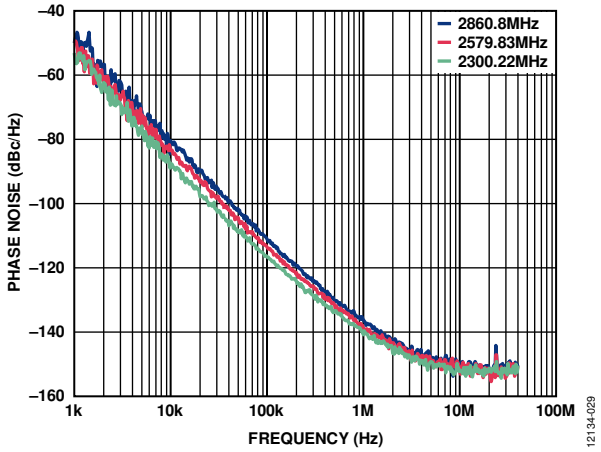


Figure 29. Open-Loop VCO Phase Noise for VCO 0 Measured at 2300.22 MHz, 2579.83 MHz, and 2860.8 MHz (VCO ÷ 2)

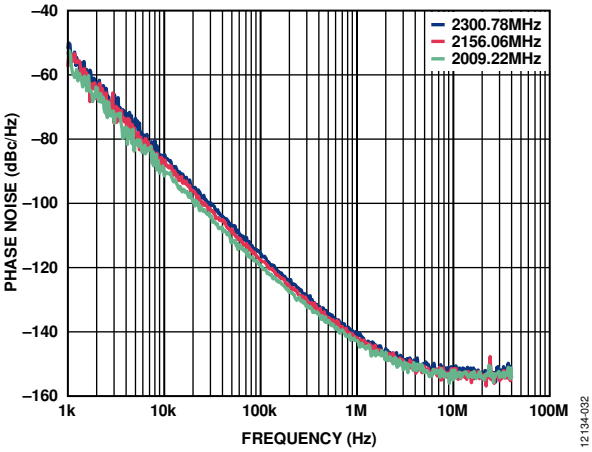


Figure 32. Open-Loop VCO Phase Noise for VCO 1 Measured at 2009.22 MHz, 2156.06 MHz, and 2300.78 MHz (VCO ÷ 2)

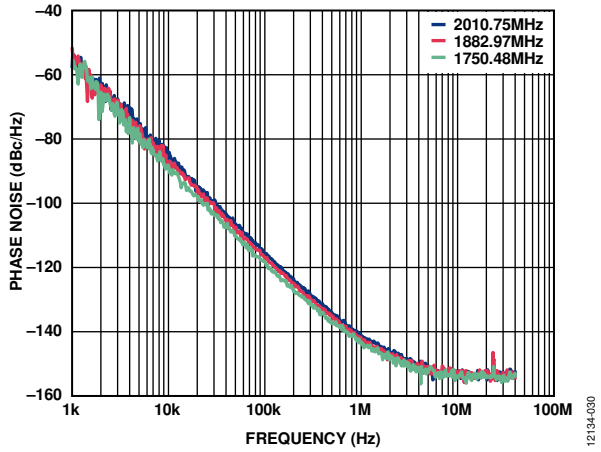


Figure 30. Open-Loop VCO Phase Noise for VCO 2 Measured at 1750.48 MHz, 1882.97 MHz, and 2010.75 MHz (VCO ÷ 2)

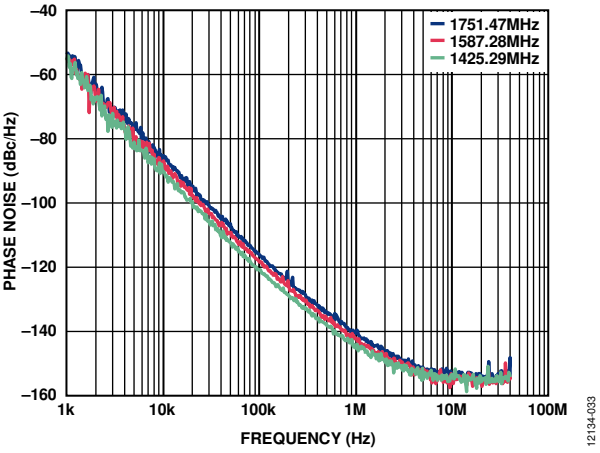


Figure 33. Open-Loop VCO Phase Noise for VCO 3 Measured at 1425.29 MHz, 1587.28 MHz, and 1751.47 MHz (VCO ÷ 2)

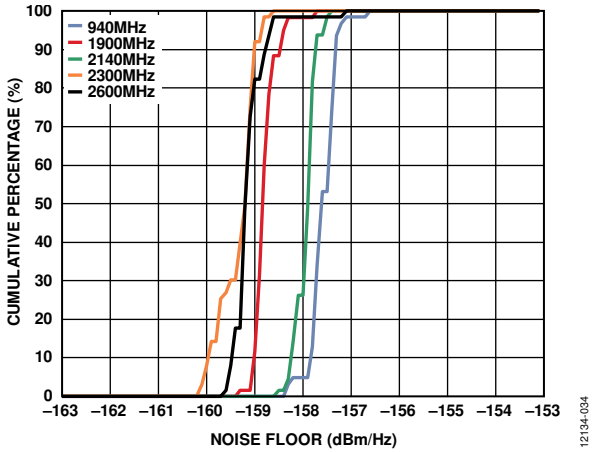


Figure 34. Noise Floor Cumulative Distribution at Various LO Frequencies Using Internal LO; I/Q Input with 500 mV DC Bias and No RF Output

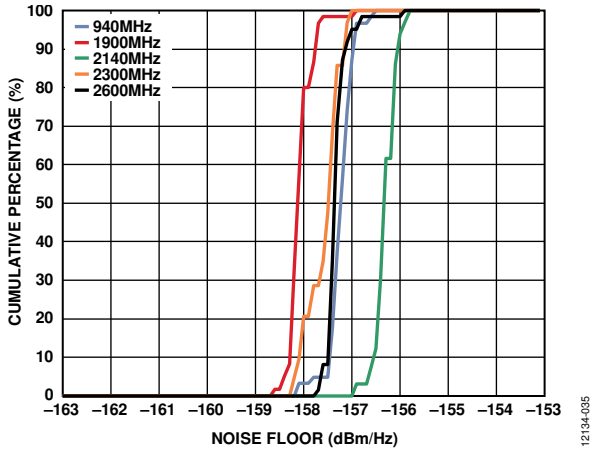


Figure 35. Noise Floor Cumulative Distribution at Various LO Frequencies Using Internal LO; I/Q Input with 500 mV DC Bias and RF Output = −10 dBm

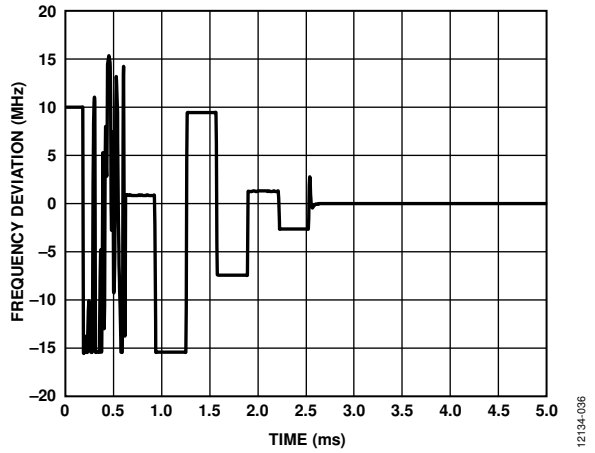


Figure 36. Frequency Deviation from LO Frequency at LO = 1.91 GHz to 1.9 GHz vs. Lock Time

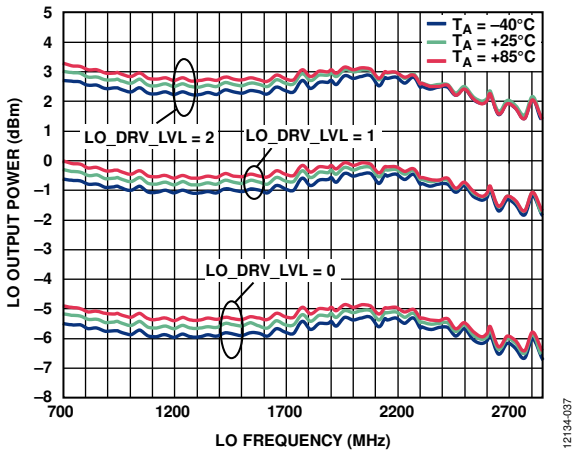


Figure 37. LO Output Power vs. LO Frequency at Various LO_DRV_LVL Settings

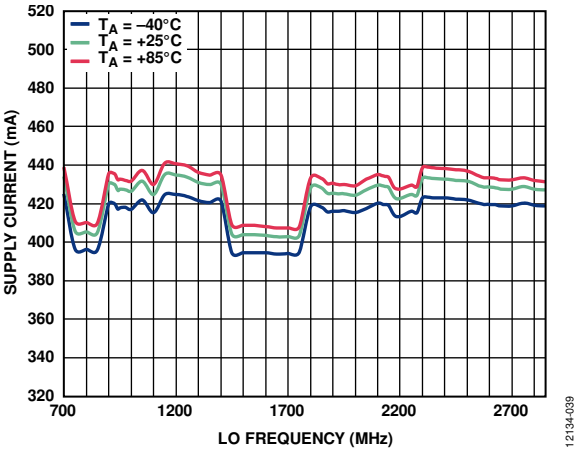


Figure 38. Supply Current vs. LO Frequency and Temperature (PLL and I/Q Modulator Enabled, LO Buffer Disabled)

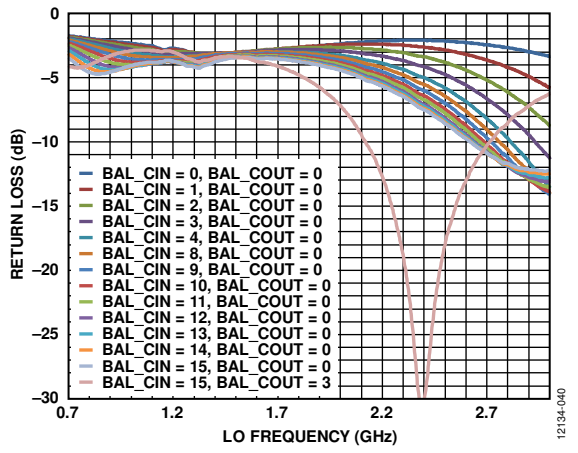


Figure 39. RF Output Return Loss vs. LO Frequency (f_{LO}) for Multiple BAL_CIN and BAL_COUT Combinations

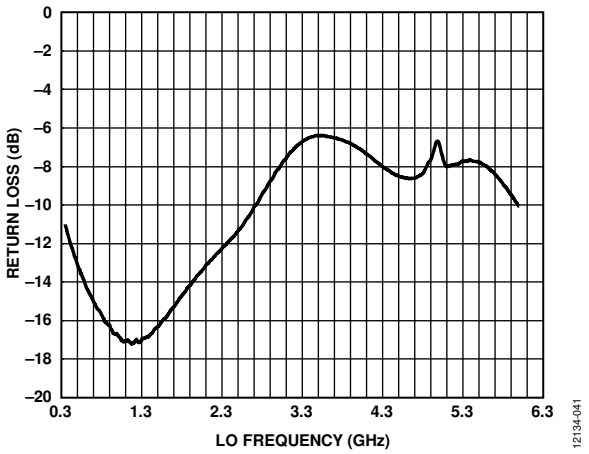


Figure 40. LO Input Return Loss vs. LO Frequency (f_{LO})

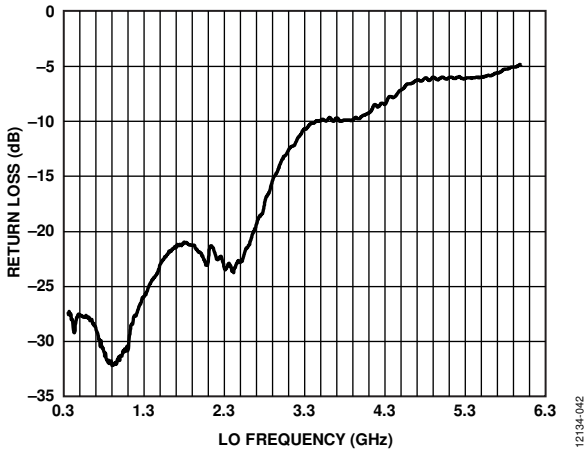


Figure 41. LO Output Return Loss vs. LO Frequency (f_{LO})

THEORY OF OPERATION

The ADRF6720 integrates a high performance broadband I/Q modulator with a fractional-N PLL and low noise multicore VCOs. The baseband inputs mix with the LO generated internally or provided externally, and convert it to a single-ended RF using an integrated RF balun. A block diagram of the device is shown in Figure 1. The ADRF6720 is programmed via an SPI.

LO GENERATION BLOCK

The ADRF6720 supports the use of both internal and external LO signals for the mixers. The internal LO is generated by an on-chip VCO, which is tunable over an octave frequency range of 2850 MHz to 5710 MHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce in-phase and quadrature phase LO signals over the 356.25 MHz to 2855 MHz frequency range to drive the mixers, steer the VCO outputs through a combination of frequency dividers, as shown in Figure 42.

Alternatively, an external signal can be used with the dividers or a polyphase phase splitter to generate the LO signals in quadrature to the mixers. In demanding applications that require the lowest possible phase noise performance, it may be necessary to source the LO signal externally. The different methods of quadrature LO generation and the control register programming needed are listed in Table 6.

Internal LO Mode

For internal LO mode, the ADRF6720 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 42, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and divides it down by a factor of 2, 4, or 8, or multiplies it by a factor of 1 or 2, and then passes it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends either an up or down signal to the charge pump if the VCO signal is either slow or fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (V_{TUNE}).

The ADRF6720 integrates four VCO cores, covering an octave range of 2850 MHz to 5710 MHz.

Table 6 lists the frequency range covered by each VCO. The desired VCO can be selected by addressing the VCO_SEL bits at Register 0x22[2:0].

The LO source and quadrature generation path can be selected by setting the QUAD_DIV_EN bit (Register 0x01[9]) and the LO_1XVCO_EN bit (Register 0x01[11]). The mode of the VCO signal through a polyphase filter is intended to extend the operating frequency with an internal VCO and is only useful for baseband input frequencies high enough to prevent the RF output from pulling the VCO.

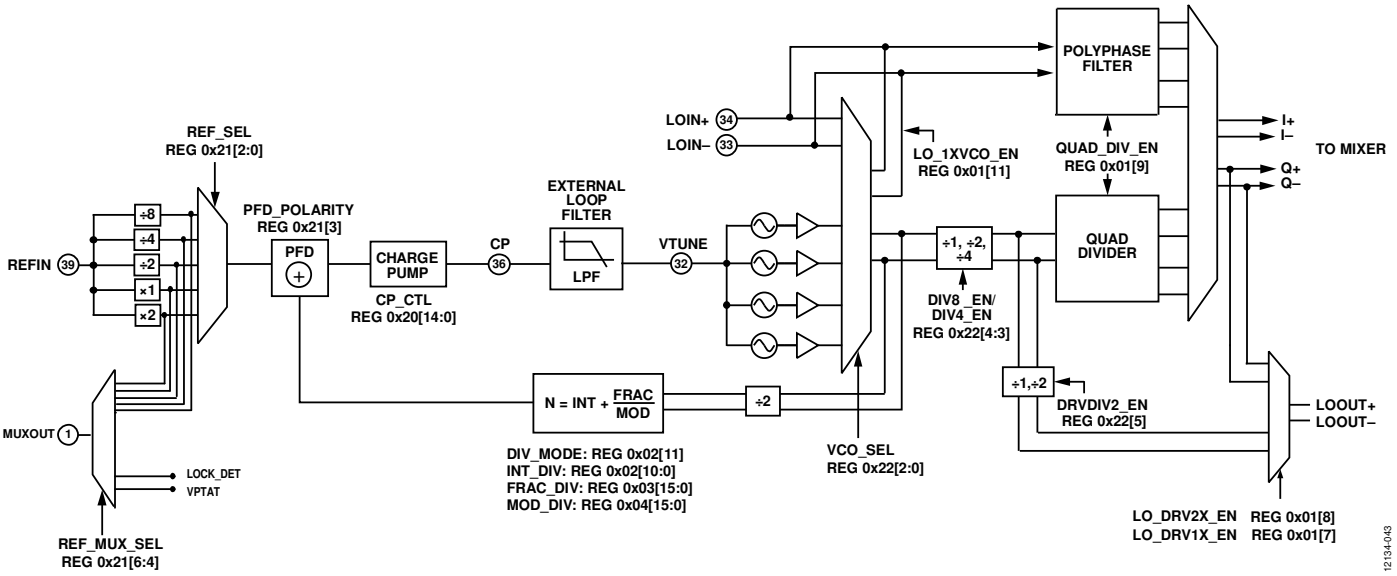


Figure 42. LO Block Diagram

Table 6. LO Mode Selection

LO Selection	f_{VCO} or f_{EXT} (MHz)	Quadrature Generation	QUAD_DIV_EN (Register 0x01[9])	LO_1XVCO_EN (Register 0x1 [11])	Enables (Register 0x01[6:0])	VCO_SEL (Register 0x22[2:0])
Internal (VCO)	2850 to 3500	Divide by 2	1	0	111 111X[1]	011
	3500 to 4020	Divide by 2	1	0	111 111X[1]	010
	4020 to 4600	Divide by 2	1	0	111 111X[1]	001
	4600 to 5710	Divide by 2	1	0	111 111X[1]	000
	2855 to 3000	Polyphase	0	0	111 111X[1]	011
External	700 to 6000	Divide by 2	1	0	101 000X[1]	1XX[1]
	700 to 3000	Polyphase	0	0	000 000X[1]	XXX[1]

[1] X = don't care.

LO Frequency and Dividers

The signal coming from the VCO or the external LO inputs goes through a series of dividers before it is buffered to drive the active mixers. Two programmable divide-by-2 stages divide the frequency of the incoming signal by 1, 2, or 4 before reaching the quadrature divider that further divides the signal frequency by 2 to generate the in-phase and quadrature phase LO signals for the mixers. The control bits (Register 0x22[4:3]) needed to select the different LO frequency ranges are listed in Table 7.

Table 7. LO Frequency and Dividers

LO Frequency Range (MHz)	f_{VCO}/f_{LO} or $f_{EXT\,LO}/f_{LO}$	DIV8_EN (Register 0x22[4])	DIV4_EN (Register 0x22[3])
1425 to 2855	2	0	0
712.5 to 1425	4	0	1
356.25 to 712.5	8	1	1

PLL Frequency Programming

The N divider with divide-by-2 divides down the VCO signal to the PFD frequency. The N divider can be configured for fractional or integer mode by addressing the DIV_MODE bit (Register 0x02[11]). The default configuration is set for fractional mode. Use the following equations to determine the N value and PLL frequency:

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{fvco}{LO\_DIVIDER} = \frac{f_{PFD} \times 2 \times N}{LO\_DIVIDER}$$

where:
f_{PFD} is the phase frequency detector frequency.
f_{VCO} is the VCO frequency.
N is the fractional divide ratio ($INT + FRAC/MOD$).
INT is the integer divide ratio programmed in Register 0x02.
$FRAC$ is the fractional divider programmed in Register 0x03.
MOD is the modulus divide ratio programmed in Register 0x04.
f_{LO} is the LO frequency going to the mixer core when the loop is locked.
$LO\_DIVIDER$ is the final frequency divider ratio that divides the frequency of the VCO or the external LO signal down by 2, 4, or 8 before it reaches the mixer, as shown in Table 7.

Loop Filter

The loop filter is connected between the CP and VTUNE pins. The recommended components for 20 kHz filter designs are shown in Table 8 and referenced in Figure 44.

The ADRF6720 closed-loop phase noise is characterized using a 20 kHz loop filter. Operation with an external VCO is possible. In this case, the output of the loop filter is connected to the tuning pin of the external VCO. The output of the VCO is brought back into the device on the LOIN+ and LOIN− pins. For assistance in designing loop filters with other characteristics, download the most recent revision of ADIsimPLL™ from http://www.analog.com/adisimpll.

Table 8. Recommended Loop Filter Components

Component	20 kHz Loop Filter
C57	2700 pF
R12	300 Ω
C58	100 nF
R23	5.6 Ω
C59	2700 pF
R26	820 Ω
C60	1500 pF

PLL Lock Time

It takes time to lock the PLL after the last register is written. VCO band calibration time and loop settling time are used to determine the PLL lock time.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration takes approximately 94,208 PFD cycles. For a 40 MHz f_{PFD}, this corresponds to 2.36 ms. After a band calibration completes, the feedback action of the PLL results in the VCO locking to the correct frequency. The speed to be locked depends on the nonlinear cycle slipping behavior, as well as the small signal settling of the loop. For an accurate estimation of the lock time, download the ADIsimPLL tool to

capture these effects correctly. In general, higher bandwidth loops tend to lock more quickly than lower bandwidth loops.

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with a logic high signifying that the loop is locked. The control bits for the MUXOUT pin are the REF_MUX_SEL bits (Register 0x21[6:4]), and the default configuration is for PLL lock detect.

Required PLL/VCO Settings and Register Write Sequence

In addition to writing to the necessary registers to configure the PLL and VCO for the desired LO frequency and phase noise performance, the registers listed in Table 9 are the required registers to write.

To ensure that the PLL locks to the desired frequency, follow the proper write sequence of the PLL registers. Configure the PLL registers accordingly to achieve the desired frequency, and the last writes must be to Register 0x02 (INT_DIV), Register 0x03 (FRAC_DIV), or Register 0x04 (MOD_DIV). When Register 0x02, Register 0x03, and Register 0x04 are programmed, an internal VCO calibration initiates, which is the last step to locking the PLL.

Table 9. Required PLL/VCO Register Writes

Address	Bit Name	Setting	Description
0x21[3]	PFD_POLARITY	0x01	Negative polarity
0x49[13:0]	SET_1[13:9], SET_0[8:0]	0x14B4	Internal settings

External LO Mode

Use the VCO_SEL bits (Register 0x22[2:0]) to select external or internal LO mode. To configure for external LO mode, set Register 0x22[2:0] to 4 decimal and apply the differential LO signals to Pin 33 (LOIN−) and Pin 34 (LOIN+). The external LO frequency range is 700 MHz to 3 GHz. When the polyphase phase splitter is selected, a 1 × LO signal is required for the active mixer, or a 2 × LO can be used with the internal quadrature divider, as shown in Table 6.

There is also the option of using an external VCO with the internal PLL. In this case, the PLL is enabled, but the VCO blocks are turned off.

The LOIN+ and LOIN− input pins must be ac-coupled. When not in use, leave the LOIN+ and LOIN− pins unconnected.

LO Polarity

The ADRF6720 offers the flexibility of specifying the quadrature polarity on LO to the I channel or Q channel mixers. This specification determines whether the LO is injected above or below the RF frequency. RF frequency can place either above or below the LO depending on the Register 0x32[11:8] setting as well as the phase relationship between the baseband I and Q. For normal operation and characterization, the Register 0x32 settings are 2 decimal for POL_I (Register 0x32[9:8]) and 1 decimal for POL_Q (Register 0x32, Bits[11:10]). Setting Register 0x32 as such places the RF frequency below the LO ($f_{RF} < f_{LO}$) when Q leads I and places the RF frequency above the LO ($f_{RF} > f_{LO}$) when I leads Q.

Table 10. LO Polarity Setting

Address	Bit Name	Settings	Description
0x32[11:10]	POL_Q		Quadrature polarity switch, Q channel
		01	Inverted Q channel polarity
		10	Normal polarity
0x32[9:8]	POL_I		Quadrature polarity switch, I channel.
		01	Normal polarity
		10	Inverted I channel polarity

LO Outputs

The ADRF6720 can provide either a differential 1 × or 2 × LO output signal at the LOOUT+ and LOOUT− pins (Pin 18 and Pin 19, respectively). The availability of the LO signal makes it possible to daisy-chain many devices. One ADRF6720 device can serve as the master where the LO signal is sourced, and the subsequent slave devices can share the same LO output signal from the master.

When the quadrature LO signals are generated using the quadrature divider, the output signal is available at either 2× or 1× the frequency of the LO signal at the mixer by setting LO_DRV2X_EN bit(Register 0x1[8]) and DRVDIV2_EN bit (Register 0x22[5]). However, 1× the frequency of the LO signal in this case has a phase ambiguity of 180° relative to the LO signal that drives the mixer core. Because of this phase ambiguity, the utility of this 1 × LO output signal as a system daisy-chained LO signal is compromised. To avoid this ambiguity, a second 1× the frequency of the LO signal output is made available after the quadrature divider. This second 1 × LO output path is enabled by setting the LO_DRV1X_EN bit (Register 0x01[7]) high.

When the quadrature LO signals are generated using the polyphase phase splitter, the output signal is also available at 1× the frequency of the LO signal by setting LO_DRV1X_EN bit (Register 0x10[7]) high.

Set the output to different drive levels by accessing the LO_DRV_LVL bits (Register 0x22[7:6]), as shown in Table 11.

Table 11. LO Output Level at 2140 MHz

LO_DRV_LVL (Register 0x22[7:6])	Amplitude (dBm)
00	−5.1
01	−0.5
10	3

BASEBAND

The input impedance of the baseband inputs is a 500 Ω differential. These inputs are designed to work with a 0.5 V common-mode voltage. To match the 100 Ω impedance of the DAC, place a shunt 125 Ω external resistor across the I and Q inputs.

The voltages applied to the differential baseband inputs (I+, I−, Q+, and Q−) drive the V-to-I stage that converts baseband voltages into currents. The converted modulated signal current feeds the modulator mixer core.

A programmable dc current can be added to both the I and Q channels to null any carrier feedthrough at the RF output. Refer to the Carrier Feedthrough Nulling section for more information

The linearity can be optimized by adding the amplitude and phase correction signals to the current output via the MOD_RSEL (Register 0x31[12:6]) and MOD_CSEL (Register 0x31[5:0]) adjustment. Refer to the Linearity section for more information.

ACTIVE MIXERS

The ADRF6720 has two double balanced mixers: one for the in-phase channel (I channel) and the other for the quadrature channel (Q channel). They upconvert the modulated baseband signal currents by the LO signals to the RF.

Tunable RF_{OUT} Balun

The ADRF6720 integrates a programmable balun operating over a frequency range from 700 MHz to 3000 MHz. It offers single-ended-to-differential conversion and provides additional common-mode noise rejection.

The capacitors at the input and output of the balun in parallel with the inductive windings of the balun change the resonant frequency of the inductor capacitor (LC) tank. Therefore, selecting the proper combination of BAL_CIN (Register 0x30[3:0]) and BAL_COUT (Register 0x30[7:4]) sets the desired frequency and optimizes gain. Under most circumstances, it is suggested to set BAL_CIN and BAL_COUT over the frequency profile given in Table 12. However, for matching reasons, it is advantageous to tune the registers independently.

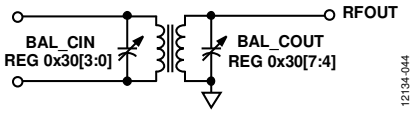


Figure 43. Integrated Tunable Balun

Table 12. Optimum Balun Setting For Desired Frequency Range

BAL_CIN	BAL_COUT	Frequency Range (MHz)
0	0	$f_{RF} > 1730$
1	0	$1550 < f_{RF} < 1730$
2	0	$1380 < f_{RF} < 1550$
3	0	$1250 < f_{RF} < 1380$
4	0	$1170 < f_{RF} < 1250$
8	0	$1100 < f_{RF} < 1170$
9	0	$1020 < f_{RF} < 1100$
10	0	$970 < f_{RF} < 1020$
11	0	$930 < f_{RF} < 970$
12	0	$890 < f_{RF} < 930$
13	0	$840 < f_{RF} < 890$
14	0	$820 < f_{RF} < 840$
15	0	$740 < f_{RF} < 820$
15	3	$680 < f_{RF} < 740$

ENBL

The ENBL pin quickly enables/disables the RF output. The circuit blocks that are enabled/disabled with the ENBL pin can be programmed by setting the appropriate bits in the enables register (Register 0x01) and the ENBL_MASK register (Register 0x10). When the bits in the enables and the ENBL_MASK register are 1, pulling the ENBL pin low disables and pulling high enables the internal blocks more quickly than possible with an SPI write operation.

Table 13. Enable/Disable Settings

Register 0x01 Enables Bit[1]	Register 0x10 ENBL_MASK Bit[1]	ENBL Pin Voltage	State
0	X[2]	X[2]	Block controlled by Register 0x01, enables bit [A] disabled. No effect by ENBL.
1	0	X[2]	Block controlled by Register 0x01, enables bit [A] disabled. No effect by ENBL.
1	1	>1.8 V	Block controlled by Register 0x01, enables bit [A] enabled.
1	1	<0.5 V	Block controlled by Register 0x01, enables bit [A] disabled

[1] This bit refers to any of the 11 bits in the register.
[2] X = don't care.

SERIAL PORT INTERFACE

The SPI of the ADRF6720 allows the user to configure the device for specific functions or operations via a 3-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of three control lines: SCLK, SDIO, and $\overline{CS}$. The timing requirements for the SPI port are shown in Table 2.

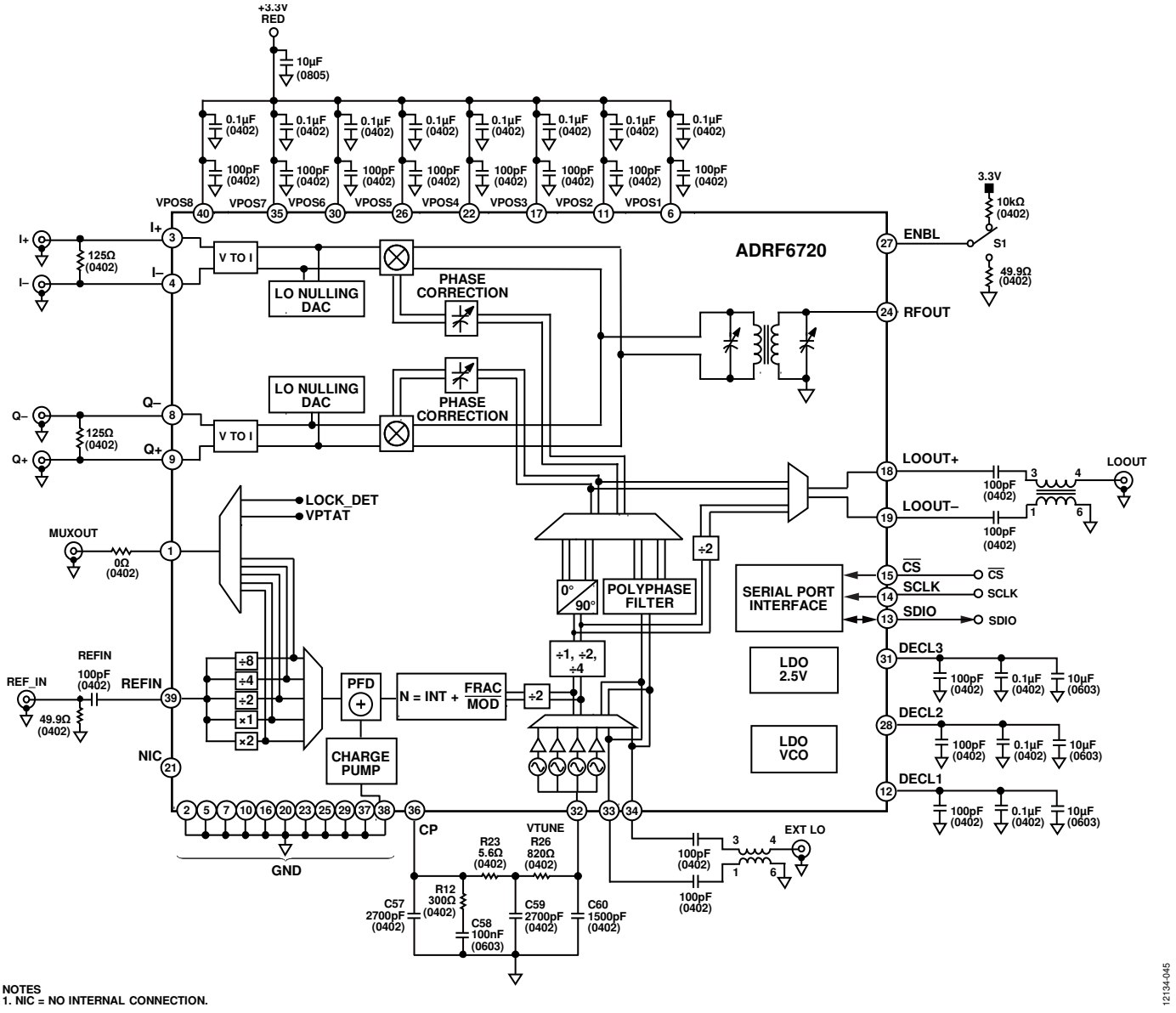
The ADRF6720 protocol consists of seven register address bits, followed by a read/write and 16 data bits. Both the address and data fields are organized with the most significant bit (MSB) first, and end with the least significant bit (LSB).

On a write cycle, up to 16 bits of serial write data are shifted in, MSB to LSB. If the rising edge of $\overline{CS}$ occurs before the LSB of the serial data is latched, only the bits that were latched are written to the device. If more than 16 data bits are shifted in, the 16 most recent bits are written to the device. The ADRF6720 input logic level for the write cycle supports an interface as low as 1.4 V.

On a read cycle, up to 16 bits of serial read data are shifted out, MSB first. Data shifted out beyond 16 bits is undefined. Readback content at a given register address does not necessarily correspond with the write data of the same address. The output logic level for a read cycle is 2.3 V.

BASIC CONNECTIONS FOR OPERATION

Figure 44 shows the basic connections for operating the ADRF6720 as they are implemented on the evaluation board of the device.



NOTES
1. NIC = NO INTERNAL CONNECTION.

12134-045

Figure 44. Basic Connections for Operation (Loop Filter Set to 20 kHz)

POWER SUPPLY AND GROUNDING

Connect the power supply pins to a 3.3 V source; the pins can range between 3.15 V and 3.45 V. Individually decouple the pins using 100 pF and 0.1 µF capacitors located as close as possible to the pins. Individually decouple the three internal decoupling nodes (labeled DECL3, DECL2, and DECL1) with capacitors as shown in Figure 44.

Tie the 11 GND pins to the same ground plane through low impedance paths.

Solder the exposed pad on the underside of the package to a ground plane with low thermal and electrical impedance. If the ground plane spans multiple layers on the circuit board, stitch them together under the exposed pad. The AN-772 Application Note discusses the thermal and electrical grounding of the LFCSP package in detail.

BASEBAND INPUTS

Drive the four I and Q inputs with an external bias level of 500 mV. These inputs are generally dc-coupled to the outputs of a dual DAC. The nominal drive level used in the characterization of the ADRF6720 is 1 V p-p differential (or 500 mV p-p on each pin).

The I and Q input resistances are 500 Ω, differential. As a result, the external shunt resistors at the I and Q inputs may be required to interface a DAC or a filter. The effective value of the resistance is 500 Ω in parallel with the shunt resistor (see the DAC to I/Q Modulator Interfacing section for more information).

LO INPUT

The external LO input is designed to be driven differentially. AC couple both sides of the differential LO source through a pair of series capacitors to the LOIN+ and LOIN− pins.

The typical LO drive level, used for the characterization of the ADRF6720, is 0 dBm.

Apply the reference frequency for the PLL (between 5.7 MHz and 320 MHz) to the REFIN pin, which is ac-coupled. If the REFIN pin is being driven from a 50 Ω source, terminate the pin with 50 Ω as shown in Figure 44. Apply a drive level of about 4 dBm to 14 dBm; 4 dBm is used at characterization.

LOOP FILTER

The loop filter in Figure 44 is connected between the CP and VTUNE pins. The recommended components for 20 kHz filter designs are shown in Table 8.

RF OUTPUT

The RF output is available at the RFOUT pin (Pin 24), which can drive a 50 Ω load.

APPLICATIONS INFORMATION

DAC TO I/Q MODULATOR INTERFACING

The ADRF6720 is designed to interface with minimal components to members of the Analog Devices, Inc., family of TxDAC® converters. These dual-channel differential current output DACs provide an output current swing from 0 mA to 20 mA. The interface described in this section can be used with any DAC that has a similar output.

An example of an interface using the AD9142A TxDAC is shown in Figure 45. The baseband inputs of the ADRF6720 require a dc bias of 500 mV. The nominal midscale output current on each of the outputs of the AD9142A is 10 mA. Therefore, an average current of 10 mA flowing through a single 50 Ω resistor to ground from each of the DAC outputs produces the desired 500 mV dc bias for the inputs to the ADRF6720. Place a shunt 125 Ω external resistor across the I and Q inputs to match the 100 Ω impedance of the DAC. The external resistor reduces the voltage swing for a given DAC output current. The AD9142A output currents have a swing ranging from 0 mA to 20 mA. With the 50 Ω termination resistors to ground in the DAC outputs and the 125 Ω shunt resistors in place, the resulting drive signal from each differential pair is 1 V p-p differential (with the DAC running at 0 dBFS) with a 500 mV dc bias.

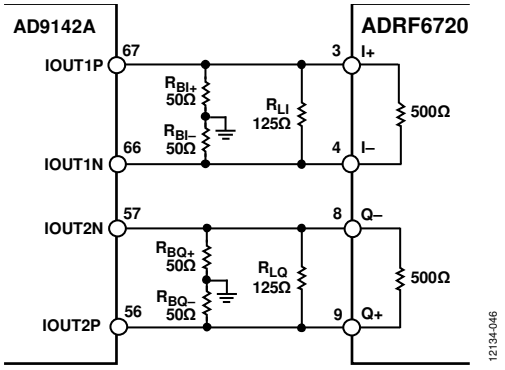


Figure 45. Interface Between the AD9142A and ADRF6720 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADRF6720 Baseband Inputs

Adjust the voltage swing for a given DAC output current by placing a different resistance value on R_{LI} and R_{LQ} to the interface (see Figure 45). This adjustment has the effect of varying the ac swing without changing the dc bias already established by the 50 Ω resistors. A higher resistance value increases the output power of the ADRF6720 and signal-to-noise ratio (SNR) at the cost of higher intermodulation distortion.

When setting the size of resistor to adjust swing level, take the input impedance of the I and Q inputs into account. The I and Q inputs have a differential input resistance of 500 Ω. As a result, the effective value of the resistance is 500 Ω in parallel with the chosen shunt resistor. For example, if a 100 Ω resistance is desired (based on Figure 45), the value of R_{LI} or R_{LQ} must be set such that

$$100\ \Omega = (500 \times R_{LI})/(500 + R_{LI})$$

$$100\ \Omega = (500 \times R_{LQ})/(500 + R_{LQ})$$

resulting in a value for R_{LI} and R_{LQ} of 125 Ω.

Figure 47 shows the differential input resistance and capacitance over baseband input frequencies.

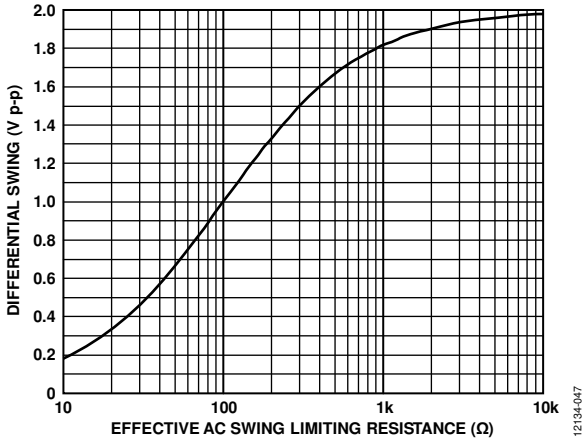


Figure 46. Relationship Between the Effective AC Swing Limiting Resistance and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

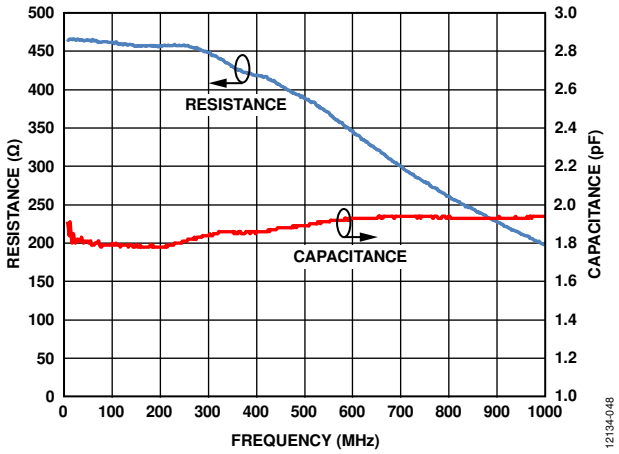


Figure 47. Differential Baseband Input Resistance and Input Capacitance Equivalents (Shunt R, Shunt C)

I/Q Filtering

An antialiasing filter between the DAC and modulator is necessary to filter out Nyquist images, common-mode noise, and broadband DAC noise. The interface for setting up the biasing and ac swing described in the DAC to I/Q Modulator Interfacing section lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing limiting resistor. With this configuration, the dc bias setting resistors set the source impedance, and the ac swing limiting resistor sets the load impedance with a 500 Ω differential I and Q input impedance in parallel for the filter.

BASEBAND BANDWIDTH

The ADRF6720 can be used with a DAC generating a complex IF (CIF), as well as a zero IF signal (ZIF). The 1 dB bandwidth of the ADRF6720 is more than 1000 MHz. Figure 48 shows the