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100 MHz to 2400 MHz I/Q Modulator with Integrated Fractional-N PLL and VCO

Data Sheet

ADRF6755

FEATURES

I/Q modulator with integrated fractional-N PLL and VCO
Gain control span: 47 dB in 1 dB steps
Output frequency range: 100 MHz to 2400 MHz
Output 1 dB compression: 8 dBm at LO = 1800 MHz
Output IP3: 20.5 dBm at LO = 1800 MHz
Noise floor: −161 dBm/Hz at LO = 1800 MHz
Baseband modulation bandwidth: 600 MHz (3 dB)
Output frequency resolution: 1 Hz
SPI and I²C-compatible serial interfaces
Power supply: 5 V/380 mA

GENERAL DESCRIPTION

The ADRF6755 is a highly integrated quadrature modulator, frequency synthesizer, and programmable attenuator. The device covers an operating frequency range from 100 MHz to 2400 MHz for use in satellite, cellular, and broadband communications.

The ADRF6755 modulator includes a high modulus, fractional-N frequency synthesizer with integrated VCO, providing less than 1 Hz frequency resolution, and a 47 dB digitally controlled output attenuator with 1 dB steps.

Control of all the on-chip registers is through a user-selected SPI interface or I²C interface. The device operates from a single power supply ranging from 4.75 V to 5.25 V.

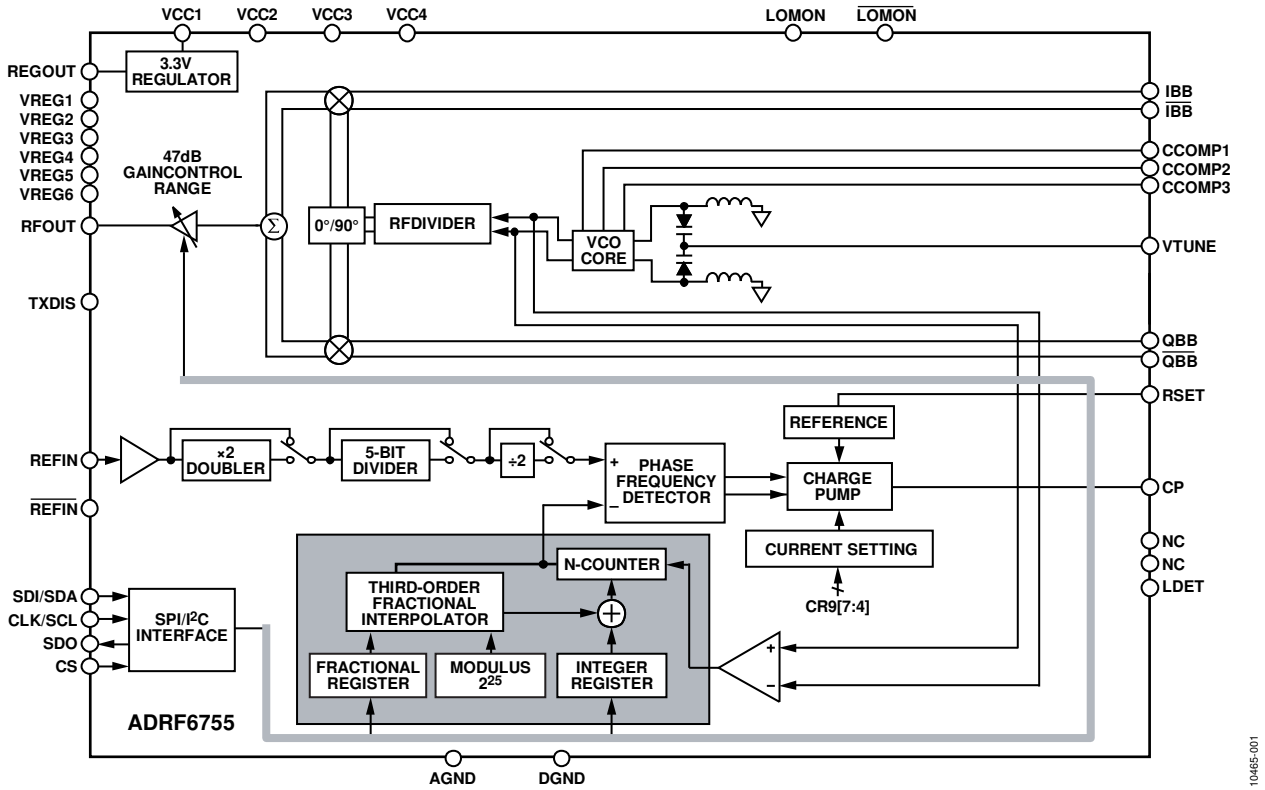

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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- ADIsimRF

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Product Selection Guide

- RF Source Booklet

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- ADRF6755 Material Declaration
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7/12—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 5%, operating temperature range = −40°C to +85°C, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, REFIN = 80 MHz, PFD = 40 MHz, baseband frequency = 1 MHz, LOMON off, loop bandwidth (LBW) = 100 kHz, I_{CP} = 5 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE		100		2400	MHz
RF OUTPUT = 100 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.2		dBm
Gain Flatness	Any 40 MHz		±2.0		dB
Output P1dB			9.0		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		21.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−12		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−55		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−80		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−153		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−85		dBc
	>10 MHz offset from carrier		−90		dBc
Phase Noise	100 Hz offset		−106		dBc/Hz
	1 kHz offset		−116		dBc/Hz
	10 kHz offset		−127		dBc/Hz
	100 kHz offset		−131		dBc/Hz
	1 MHz offset		−146		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.02		° rms
RF OUTPUT = 300 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.2		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.3		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		23.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−20		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−50		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−75		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−85		dBc
	>10 MHz offset from carrier		−85		dBc
Phase Noise	100 Hz offset		−105		dBc/Hz
	1 kHz offset		−113		dBc/Hz
	10 kHz offset		−117		dBc/Hz
	100 kHz offset		−122		dBc/Hz
	1 MHz offset		−145		dBc/Hz
	10 MHz offset		−150		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.04		° rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT = 700 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.2		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		23.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−16		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−48		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−70		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−85		dBc
Phase Noise	100 Hz offset		−97		dBc/Hz
	1 kHz offset		−106		dBc/Hz
	10 kHz offset		−112		dBc/Hz
	100 kHz offset		−115		dBc/Hz
	1 MHz offset		−139		dBc/Hz
	10 MHz offset		−154		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.07		° rms
RF OUTPUT = 900 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.0		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.2		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		22.8		dBm
Output Return Loss	Attenuator setting = 0 dB		−15		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−48		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−68		dBm
Sideband Suppression			−60		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158.5		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−152		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−171		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−80		dBc
Phase Noise	100 Hz offset		−94		dBc/Hz
	1 kHz offset		−104		dBc/Hz
	10 kHz offset		−109		dBc/Hz
	100 kHz offset		−114		dBc/Hz
	1 MHz offset		−139		dBc/Hz
	10 MHz offset		−154		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.11		° rms
RF OUTPUT = 1800 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.4		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			8.0		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		20.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−13		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−45		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−53		dBm
Sideband Suppression			−45		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−161		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−150		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−58		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−75		dBc
Phase Noise	100 Hz offset		−89		dBc/Hz
	1 kHz offset		−99		dBc/Hz
	10 kHz offset		−103		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−133		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.17		° rms
RF OUTPUT = 1875 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.6		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			7.8		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		20.2		dBm
Output Return Loss	Attenuator setting = 0 dB		−13		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−45		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−52		dBm
Sideband Suppression			−50		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−160		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−150		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−73		dBc
Phase Noise	100 Hz offset		−89		dBc/Hz
	1 kHz offset		−97		dBc/Hz
	10 kHz offset		−103		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−133		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.18		° rms
RF OUTPUT = 2100 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−1.0		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			7.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		19.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−12		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−44		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−51		dBm
Sideband Suppression			−45		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−161		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−149		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−67		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Phase Noise	100 Hz offset		−88		dBc/Hz
	1 kHz offset		−98		dBc/Hz
	10 kHz offset		−101		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−134		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.25		° rms
RF OUTPUT = 2400 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−1.7		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			6.5		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		18.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−11		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−43		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−60		dBm
Sideband Suppression			−40		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−160.5		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−148		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−55		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−55		dBc
	>10 MHz offset from carrier		−64		dBc
Phase Noise	100 Hz offset		−85		dBc/Hz
	1 kHz offset		−96		dBc/Hz
	10 kHz offset		−100		dBc/Hz
	100 kHz offset		−107		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.25		° rms
REFERENCE CHARACTERISTICS	REFIN pin				
Input Frequency	With reference divide-by-2 enabled	10		300	MHz
	With reference divide-by-2 disabled	10		165	MHz
	With reference doubler enabled	10		80	MHz
Input Sensitivity	AC-coupled	0.4		VREG	V p-p
Input Capacitance				10	pF
Input Current				±100	µA
CHARGE PUMP					
I_{CP} Sink/Source	Programmable, RSET = 4.7 kΩ				
High Value			5		mA
Low Value			312.5		µA
Absolute Accuracy			4.0		%
VCO					
Gain	K_{VCO}		25		MHz/V
SYNTHESIZER	LO = 100 MHz to 2400 MHz				
Frequency Resolution				1	Hz
Frequency Settling	Any step size, maximum frequency error = 100 Hz		0.17		ms
Maximum Frequency Step for No Autocalibration	Frequency step with no autocalibration routine; Register CR24, Bit 0 = 1			$100/2^{RFDIV}$	kHz
Phase Detector Frequency		10		40	MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN CONTROL					
Gain Range			47		dB
Step Size			1		dB
Relative Step Accuracy	Fixed frequency, adjacent steps, all attenuation steps, LO > 300 MHz[2]		±0.3		dB
	Over full frequency range, adjacent steps, all attenuation steps, LO > 300 MHz[3]		±1.5		dB
Absolute Step Accuracy[4]	47 dB attenuation step, LO > 300 MHz[5]		−2.0		dB
Output Settling Time	Any step; output power settled to ±0.2 dB		15		µs
OUTPUT DISABLE	TXDIS pin				
Off Isolation	RFOUT, attenuator setting = 0 dB to 47 dB, TXDIS high		−100		dBm
	LO, attenuator setting = 0 dB to 47 dB, TXDIS high		−75		dBm
	2× LO, attenuator setting = 0 dB to 47 dB, TXDIS high		−50		dBm
Turn-On Settling Time	TXDIS high to low: output power to 90% of envelope		180		ns
	Frequency settling to 100 Hz		20		µs
Turn-Off Settling Time	TXDIS low to high (to −55 dBm)		350		ns
MONITOR OUTPUT	LOMON, $\overline{\text{LOMON}}$ pins				
Nominal Output Power			−24		dBm
BASEBAND INPUTS	IBB, $\overline{\text{IBB}}$, QBB, $\overline{\text{QBB}}$ pins				
I and Q Input Bias Level			500		mV
3 dB Bandwidth			600		MHz
LOGIC INPUTS					
Input High Voltage, V_{INH}	CS, TXDIS pins	1.4			V
Input Low Voltage, V_{INL}	CS, TXDIS pins			0.6	V
Input High Voltage, V_{INH}	SDI/SDA, CLK/SCL pins	2.1			V
Input Low Voltage, V_{INL}	SDI/SDA, CLK/SCL pins			1.1	V
Input Current, I_{INH}/I_{INL}	CS, TXDIS, SDI/SDA, CLK/SCL pins			±1	µA
Input Capacitance, C_{IN}	CS, TXDIS, SDI/SDA, CLK/SCL pins			10	pF
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	SDO, LDET pins; I_{OH} = 500 µA	2.8			V
Output Low Voltage, V_{OL}	SDO, LDET pins; I_{OL} = 500 µA			0.4	V
	SDA (SDI/SDA); I_{OL} = 3 mA			0.4	V
POWER SUPPLIES	VCC1, VCC2, VCC3, VCC4, VREG1, VREG2, VREG3, VREG4, VREG5, VREG6, and REGOUT pins; REGOUT normally connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6				
Voltage Range	VCC1, VCC2, VCC3, and VCC4	4.75	5	5.25	V
	REGOUT, VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		3.3		V
Supply Current	VCC1, VCC2, VCC3, and VCC4 combined; REGOUT connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		380	420	mA
Power-Down Current	CR29[0] = 0, power down modulator, CR12[2] = 1, power down PLL, CR28[4] = 1, power down RFDIVIDER, CR27[2] = 0, power down LOMON		7		mA
Operating Temperature		−40		+85	°C

[1] LO carrier feedthrough is expressed in dBc relative to the RF output power changing as the attenuator is stepped. LO carrier feedthrough is constant as the RF output is altered due to a change in the I/Q input amplitude.
[2] For relative step accuracy at LO < 300 MHz, refer to Figure 37.
[3] For relative step accuracy over frequency range at LO < 300 MHz, refer to Figure 39.
[4] All other attenuation steps have an absolute error of <±2.0 dB.
[5] For absolute step accuracy at LO < 300 MHz, refer to Figure 40.

TIMING CHARACTERISTICS

I²C Interface Timing

Table 2.

Parameter[1]	Symbol	Limit	Unit
SCL Clock Frequency	f_{SCL}	400	kHz max
SCL Pulse Width High	t_{HIGH}	600	ns min
SCL Pulse Width Low	t_{LOW}	1300	ns min
Start Condition Hold Time	$t_{HD;STA}$	600	ns min
Start Condition Setup Time	$t_{SU;STA}$	600	ns min
Data Setup Time	$t_{SU;DAT}$	100	ns min
Data Hold Time	$t_{HD;DAT}$	300	ns min
Stop Condition Setup Time	$t_{SU;STO}$	600	ns min
Data Valid Time	$t_{VD;DAT}$	900	ns max
Data Valid Acknowledge Time	$t_{VD;ACK}$	900	ns max
Bus Free Time	t_{BUF}	1300	ns min

[1] See Figure 2.

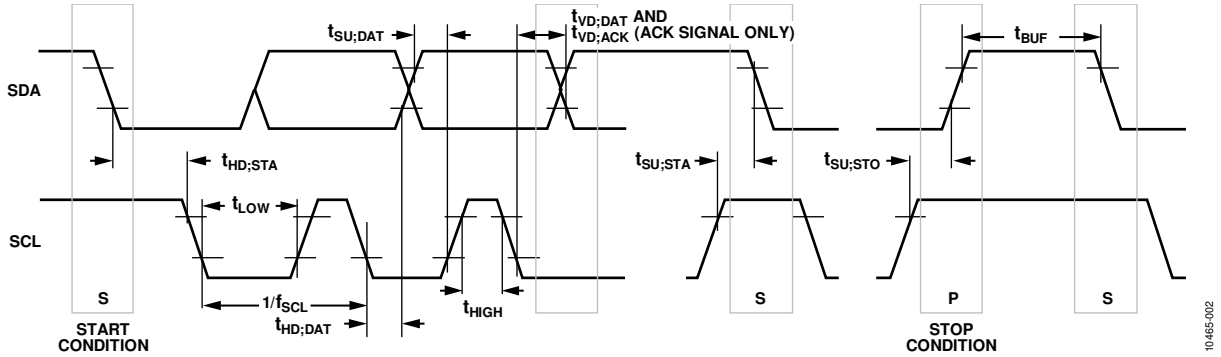

Figure 2. I²C Port Timing Diagram

SPI Interface Timing

Table 3.

Parameter[1]	Symbol	Limit	Unit
CLK Frequency	f_{CLK}	20	MHz max
CLK Pulse Width High	t_1	15	ns min
CLK Pulse Width Low	t_2	15	ns min
Start Condition Hold Time	t_3	5	ns min
Data Setup Time	t_4	10	ns min
Data Hold Time	t_5	5	ns min
Stop Condition Setup Time	t_6	5	ns min
SDO Access Time	t_7	15	ns min
CS to SDO High Impedance	t_8	25	ns max

[1] See Figure 3.

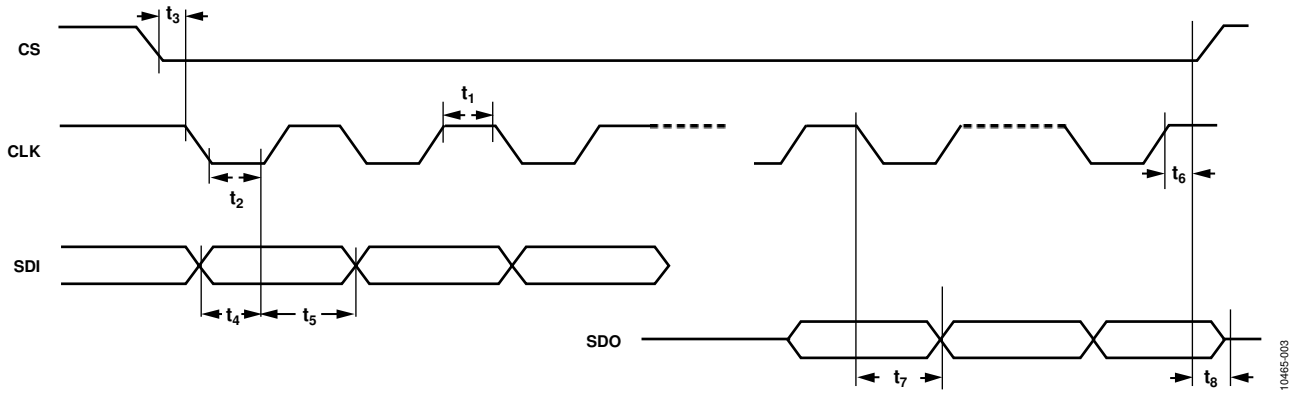

Figure 3. SPI Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VCC1, VCC2, VCC3, and VCC4 Supply Voltage	−0.3 V to +6 V
VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6 Supply Voltage	−0.3 V to +4 V
IBB, $\overline{\text{IBB}}$, QBB, and $\overline{\text{QBB}}$	0 V to 2.5 V
Digital I/O	−0.3 V to +4 V
Analog I/O (Other Than IBB, $\overline{\text{IBB}}$, QBB, and $\overline{\text{QBB}}$)	−0.3 V to +4 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

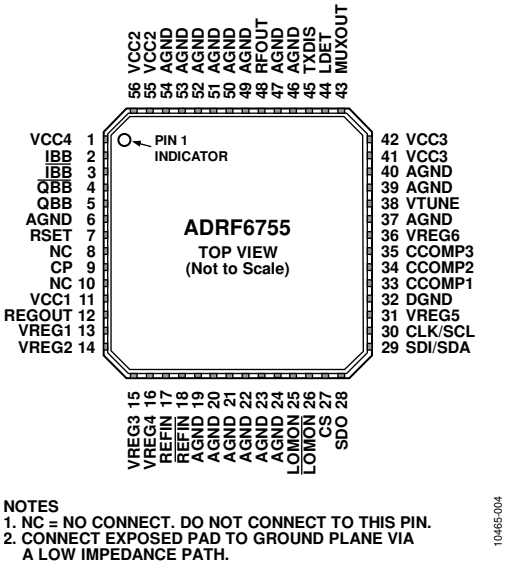

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
11, 55, 56, 41, 42, 1	VCC1 to VCC4	Positive Power Supplies for I/Q Modulator. Apply a 5 V power supply to VCC1, which should be decoupled with power supply decoupling capacitors. Connect VCC2, VCC3, and VCC4 to the same 5 V power supply.
12	REGOUT	3.3 V Output Supply. Drives VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6.
13, 14, 15, 16, 31, 36	VREG1 to VREG6	Positive Power Supplies for PLL Synthesizer, VCO, and Serial Port. Connect these pins to REGOUT (3.3 V) and decouple them separately.
6, 19, 20, 21, 22, 23, 24, 37, 39, 40, 46, 47, 49, 50, 51, 52, 53, 54	AGND	Analog Ground. Connect to a low impedance ground plane.
32	DGND	Digital Ground. Connect to the same low impedance ground plane as the AGND pins.
2, 3	IBB, $\overline{\text{IBB}}$	Differential In-Phase Baseband Inputs. These high impedance inputs must be dc biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. These inputs are not self-biased and must be externally biased.
4, 5	$\overline{\text{QBB}}$, QBB	Differential Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. These inputs are not self-biased and must be externally biased.
33, 34, 35	CCOMP1 to CCOMP3	Internal Compensation Nodes. These pins must be decoupled to ground with a 100 nF capacitor.
38	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
7	RSET	Charge Pump Current Set. Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is as follows: $I_{CPmax} = \frac{23.5}{R_{SET}}$ where R_{SET} = 4.7 kΩ and $I_{CP\,max}$ = 5 mA.
9	CP	Charge Pump Output. When enabled, this output provides ±I_{CP} to the external loop filter, which, in turn, drives the internal VCO.
27	CS	Chip Select, CMOS Input. When CS is high, the data stored in the shift registers is loaded into one of 31 latches. In I^2C mode, when CS is high, the slave address of the device is 0x60, and, when CS is low, the slave address is 0x40.

Pin No.	Mnemonic	Description
29	SDI/SDA	Serial Data Input for SPI Port/Serial Data Input/Output for I²C Port. In SPI mode, this pin is a high impedance CMOS data input, and data is loaded in an 8-bit word. In I²C mode, this pin is a bidirectional port.
30	CLK/SCL	Serial Clock Input for SPI/I²C Port. This serial clock is used to clock in the serial data to the registers. This input is a high impedance CMOS input.
28	SDO	Serial Data Output for SPI Port. Register states can be read back on the SDO data output line.
17	REFIN	Reference Input. This high impedance CMOS input should be ac-coupled.
18	$\overline{\text{REFIN}}$	Reference Input Bar. This pin should be either grounded or ac-coupled to ground.
48	RFOUT	RF Output. Single-ended, 50 Ω, internally biased RF output. This pin must be ac-coupled to the load.
45	TXDIS	Output Disable. This pin can be used to disable the RF output. Connect to a high logic level to disable the output. Connect to a low logic level for normal operation.
25, 26	LOMON, $\overline{\text{LOMON}}$	Differential Monitor Outputs. These pins provide a replica of the internal local oscillator frequency (1× LO) at four different power levels: −6 dBm, −12 dBm, −18 dBm, and −24 dBm, approximately. These open-collector outputs must be terminated with external resistors to REGOUT. These outputs can be disabled through serial port programming and should be tied to REGOUT if not used.
8, 10	NC	No Connect. Do not connect to these pins.
44	LDET	Lock Detect. This output pin indicates the state of the PLL: a high level indicates a locked condition, whereas a low level indicates a loss of lock condition.
43	MUXOUT	Mux Output. This pin is a test output for diagnostic use only. Do not connect to this pin.
Exposed Paddle	EP	Exposed Paddle. Connect to ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5 V ± 5%, operating temperature range = −40°C to +85°C, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, REFIN = 80 MHz, PFD = 40 MHz, baseband frequency = 1 MHz, LOMON is off, loop bandwidth (LBW) = 100 kHz, I_{CP} = 5 mA, unless otherwise noted. A nominal condition is defined as 25°C, 5.00 V, and an LO frequency of 1800 MHz. A worst-case condition is defined as having the worst-case temperature, supply voltage, and LO frequency.

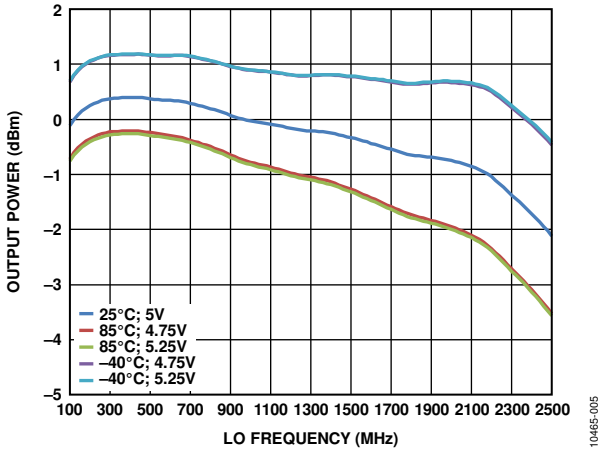

Figure 5. Output Power vs. LO Frequency, Supply, and Temperature

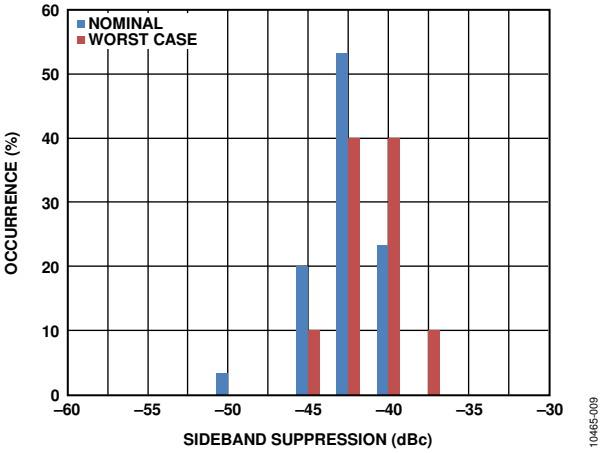

Figure 8. Sideband Suppression Distribution at Nominal and Worst-Case Conditions

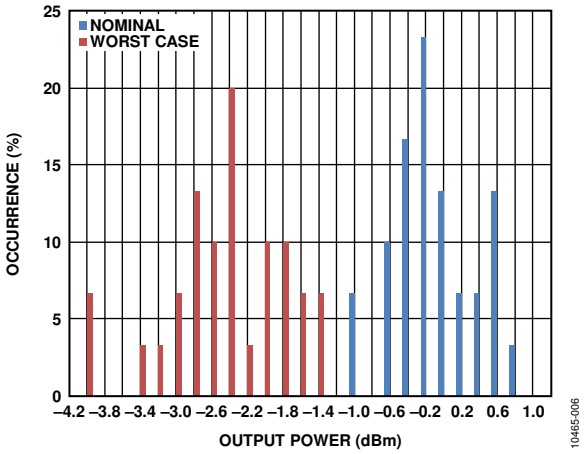

Figure 6. Output Power Distribution at Nominal and Worst-Case Conditions

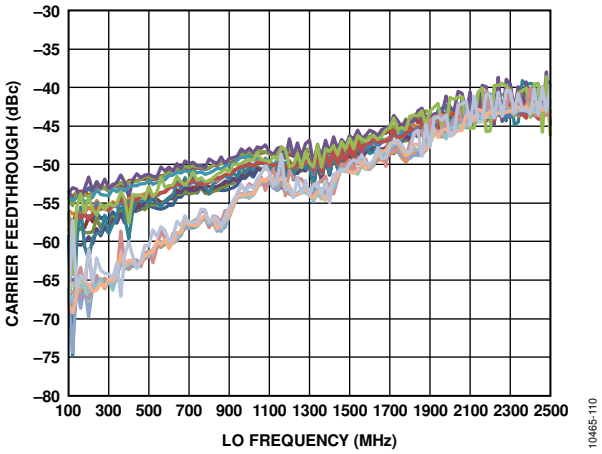

Figure 9. LO Carrier Feedthrough vs. LO Frequency, Attenuation, Supply, and Temperature

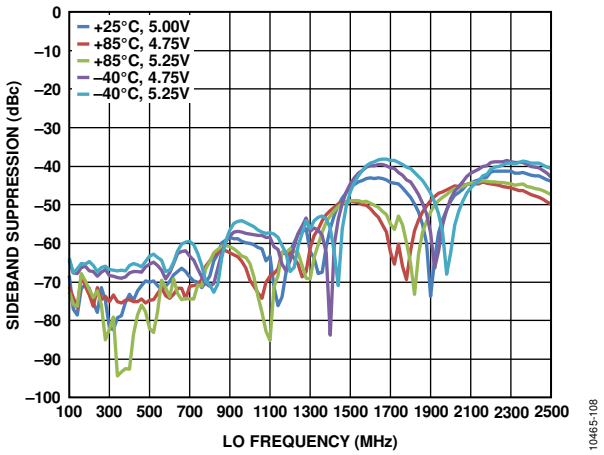

Figure 7. Sideband Suppression vs. LO Frequency, Supply, and Temperature

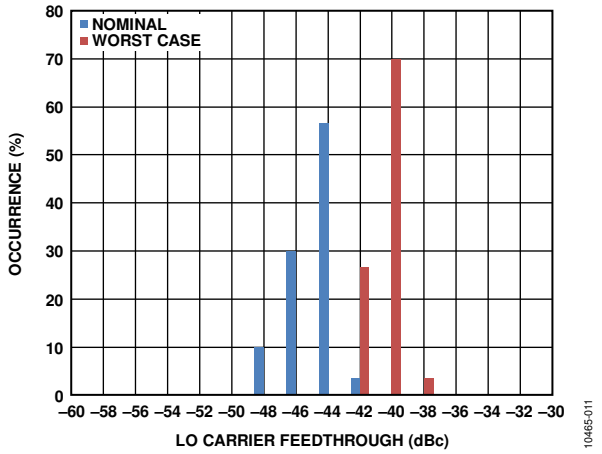

Figure 10. LO Carrier Feedthrough Distribution at Nominal and Worst-Case Conditions and Attenuation Setting

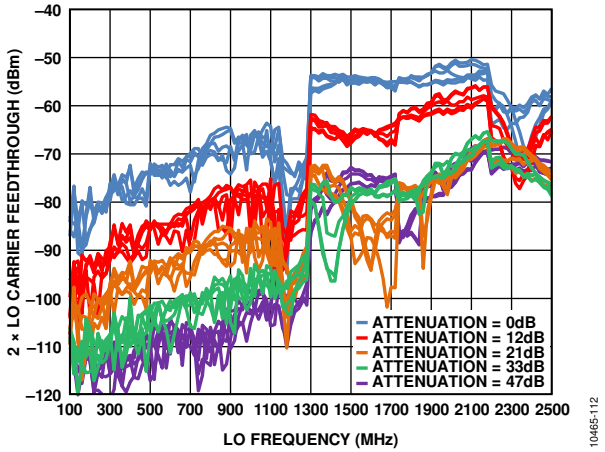

Figure 11. 2× LO Carrier Feedthrough vs. LO Frequency, Attenuation, Supply, and Temperature

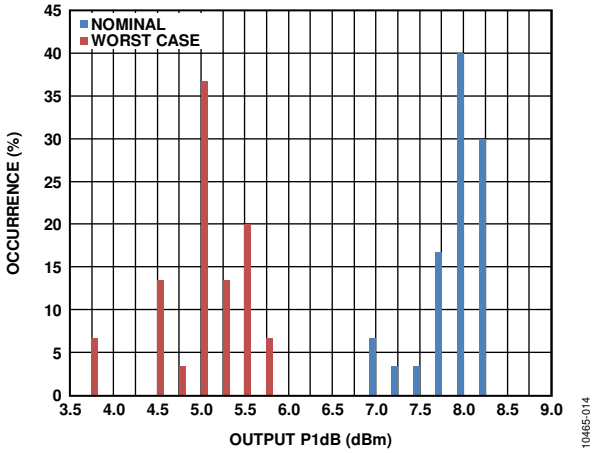

Figure 14. Output P1dB Compression Point Distribution at Nominal and Worst-Case Conditions

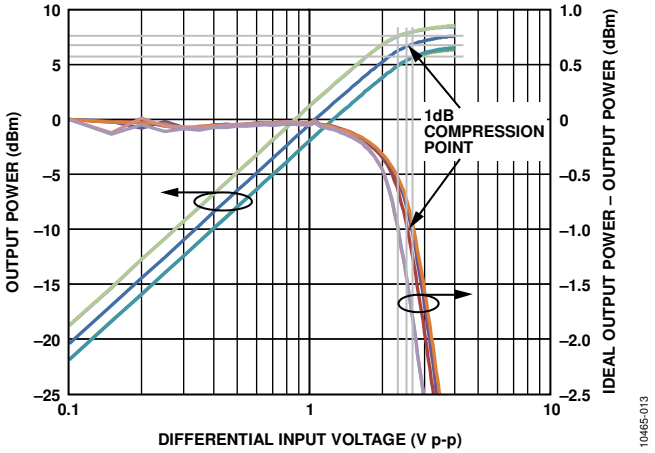

Figure 12. Output P1dB Compression Point at Worst-Case LO Frequency vs. Supply and Temperature

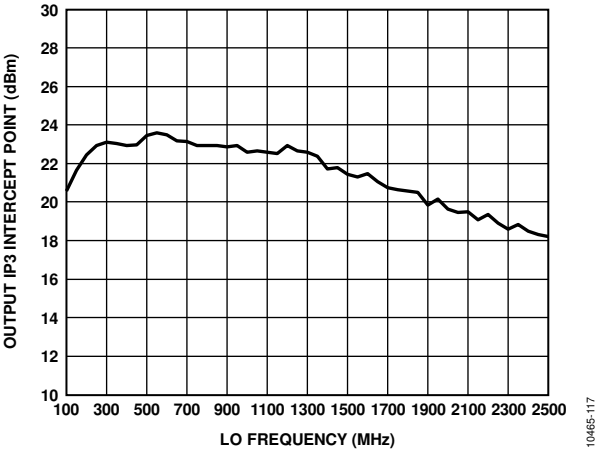

Figure 15. Output IP3 vs. LO Frequency at Nominal Conditions

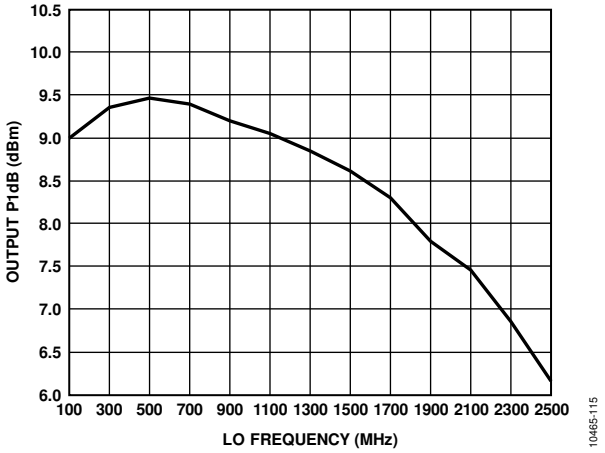

Figure 13. Output P1dB Compression Point vs. LO Frequency at Nominal Conditions

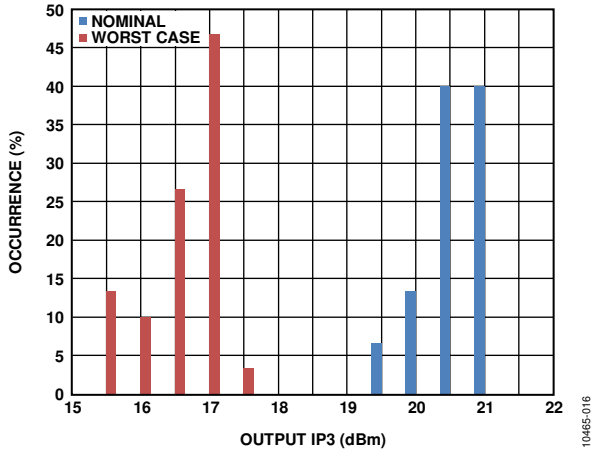

Figure 16. Output IP3 Distribution at Nominal and Worst-Case Conditions

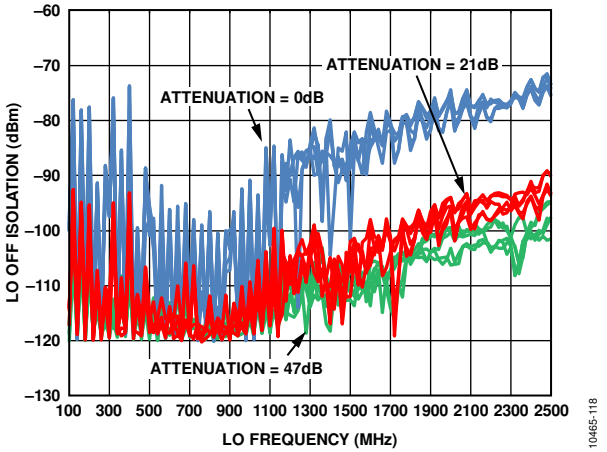

Figure 17. LO Off Isolation vs. LO Frequency, Attenuation, Supply, and Temperature

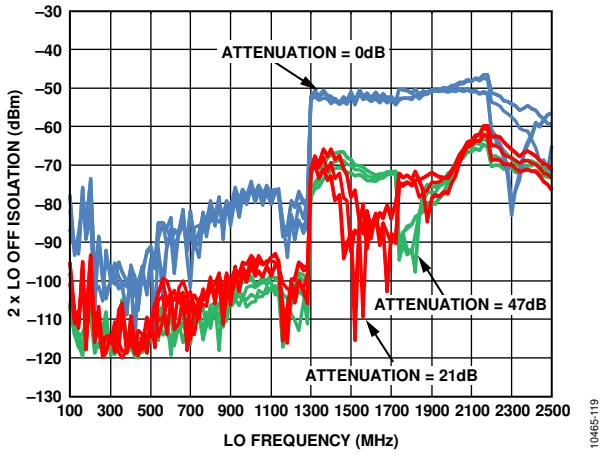

Figure 18. 2 × LO Off Isolation vs. LO Frequency, Attenuation, Supply, and Temperature

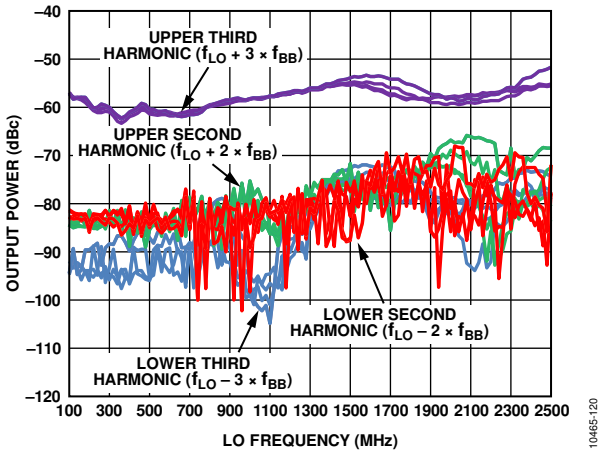

Figure 19. Second-Order and Third-Order Harmonic Distortion vs. LO Frequency, Supply, and Temperature

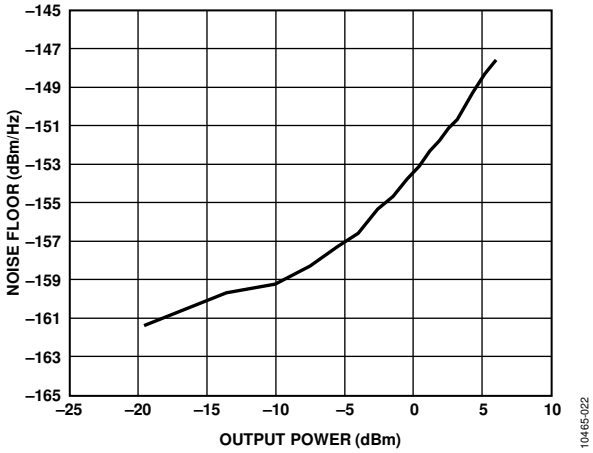

Figure 20. Noise Floor at 0 dB Attenuation vs. Output Power at Nominal Conditions

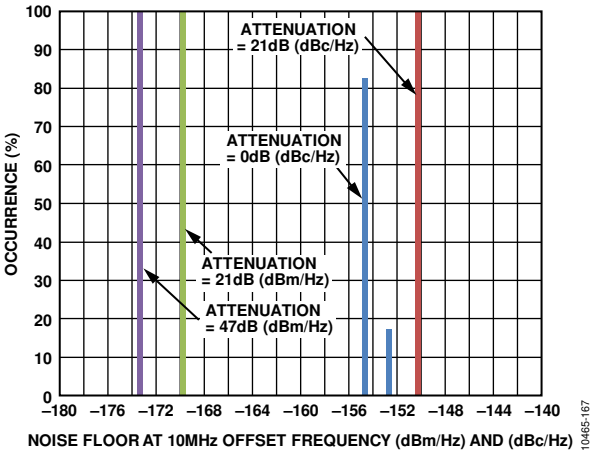

Figure 21. Noise Floor at 10 MHz Offset Frequency Distribution at Worst-Case Conditions and Different Attenuation Settings

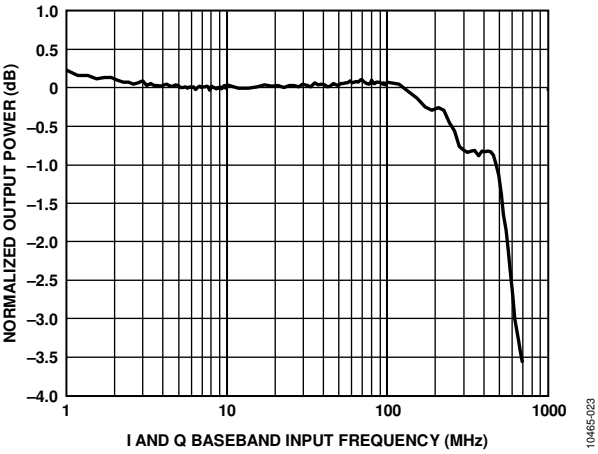

Figure 22. Normalized I and Q Input Bandwidth

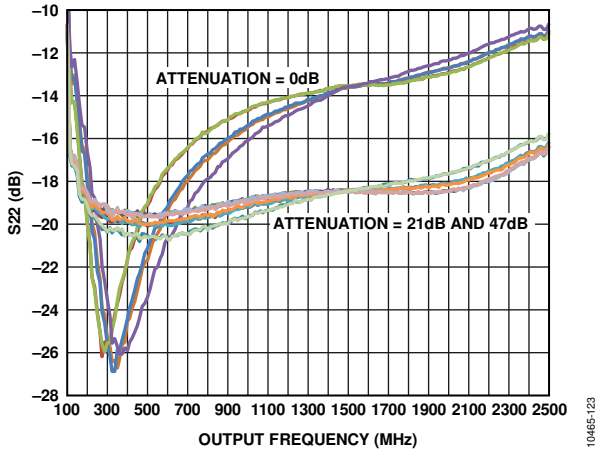

Figure 23. Output Return Loss at Different Attenuation Settings vs. Output Frequency, Supply, and Temperature

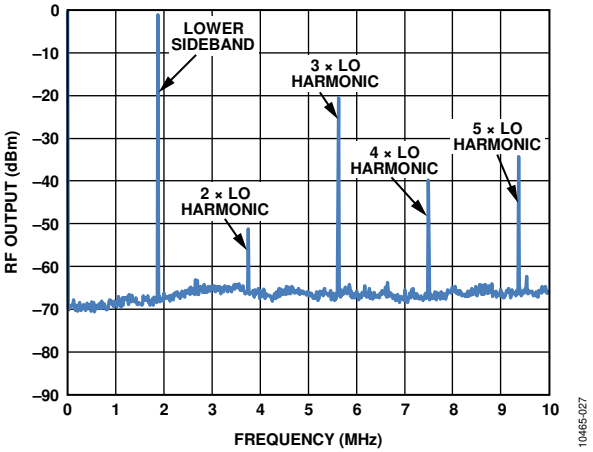

Figure 26. RF Output Spectral Plot over a Wide Span

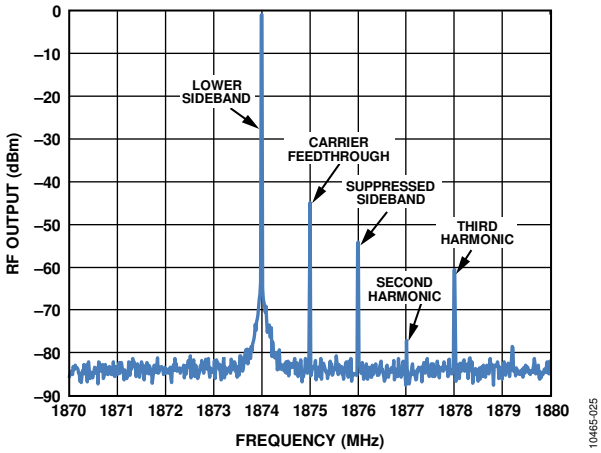

Figure 24. RF Output Spectral Plot over a 10 MHz Span

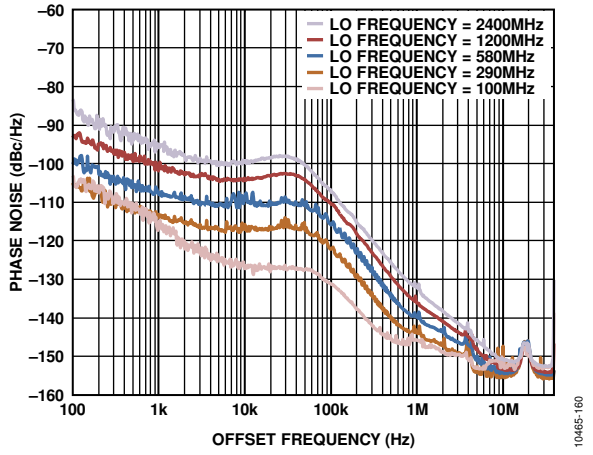

Figure 27. Phase Noise Performance vs. LO Frequency, Nominal Conditions

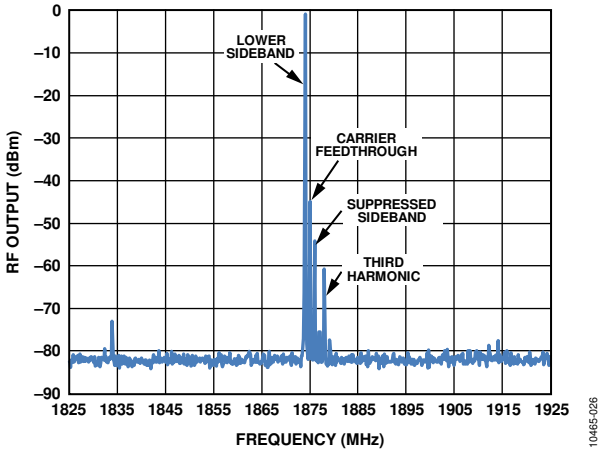

Figure 25. RF Output Spectral Plot over a 100 MHz Span

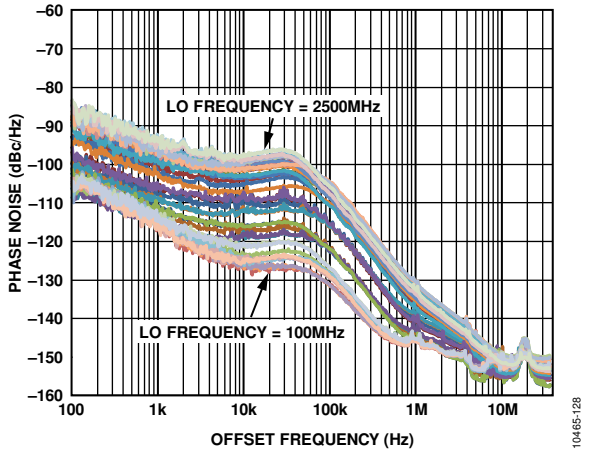

Figure 28. Phase Noise Performance vs. LO Frequency, Supply, and Temperature

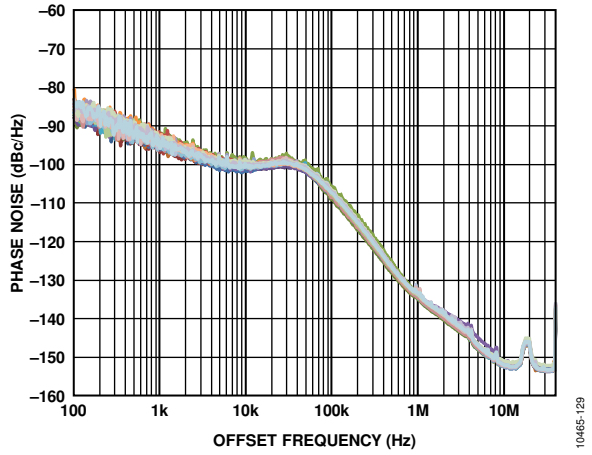

Figure 29. Phase Noise Performance Distribution at Worst-Case Conditions

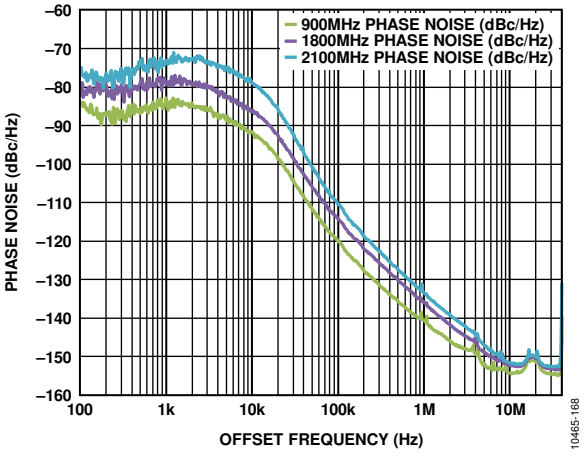

Figure 32. Phase Noise Performance vs. LO Frequency, Nominal Conditions with Narrow Loop Bandwidth

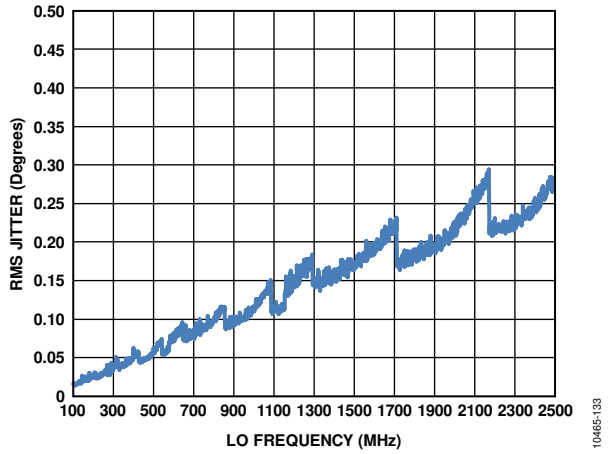

Figure 30. Integrated Phase Noise over an Integration Bandwidth of 1 kHz to 8 MHz vs. LO Frequency at Nominal Conditions

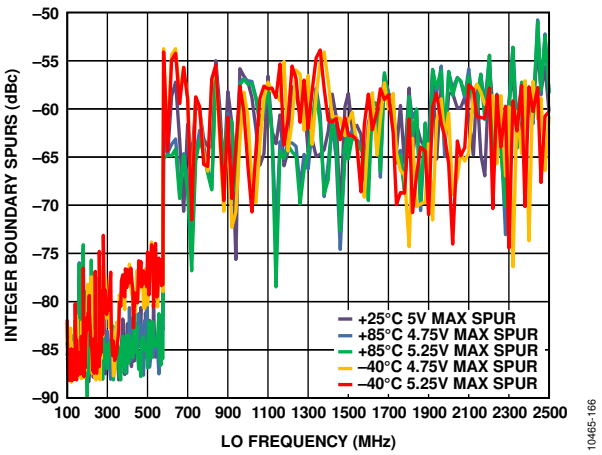

Figure 33. Integer Boundary Spur Performance vs. LO Frequency, Supply, and Temperature

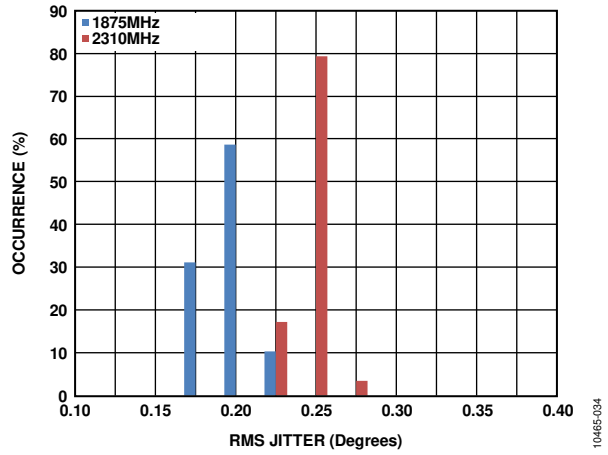

Figure 31. Integrated Phase Noise Distribution over an Integration Bandwidth of 1 kHz to 8 MHz at 1875 MHz and 2310 MHz

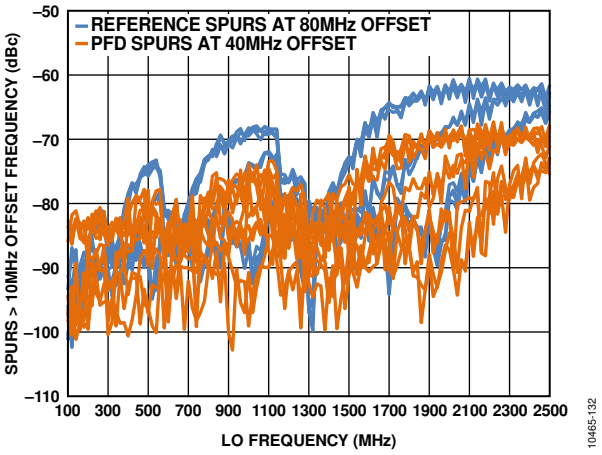

Figure 34. Spurs > 10 MHz from Carrier vs. LO Frequency, Supply, and Temperature

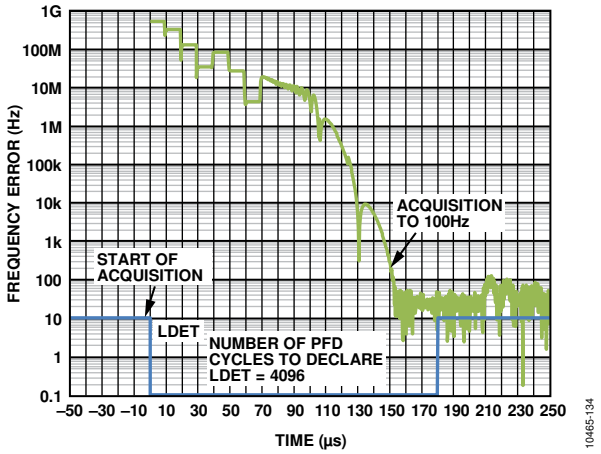

Figure 35. PLL Frequency Settling Time at Worst-Case LO Frequency with Lock Detect Shown

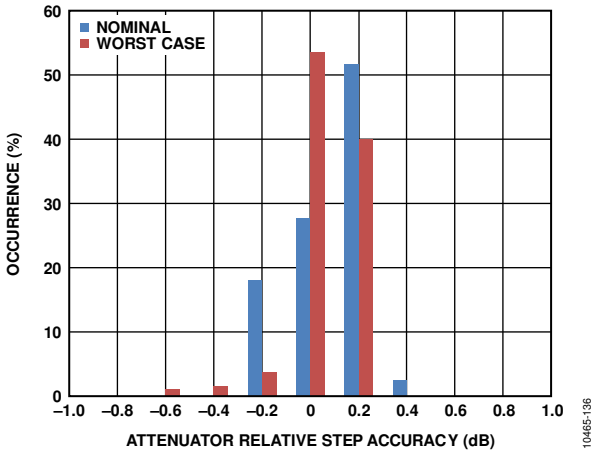

Figure 38. Attenuator Relative Step Accuracy Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

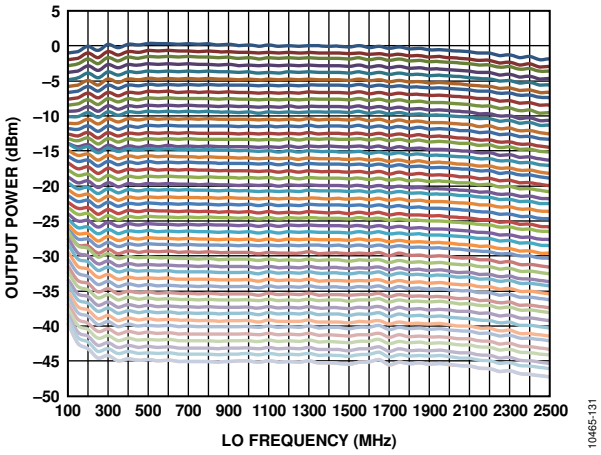

Figure 36. Attenuator Gain vs. LO Frequency by Gain Code, All Attenuator Code Steps

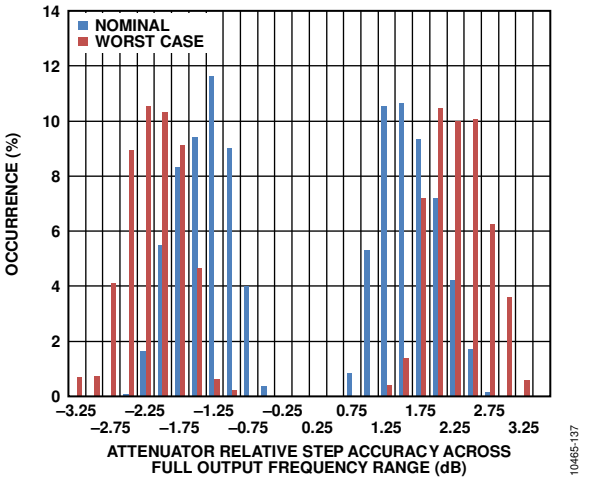

Figure 39. Attenuator Relative Step Accuracy Across Full Output Frequency Range Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

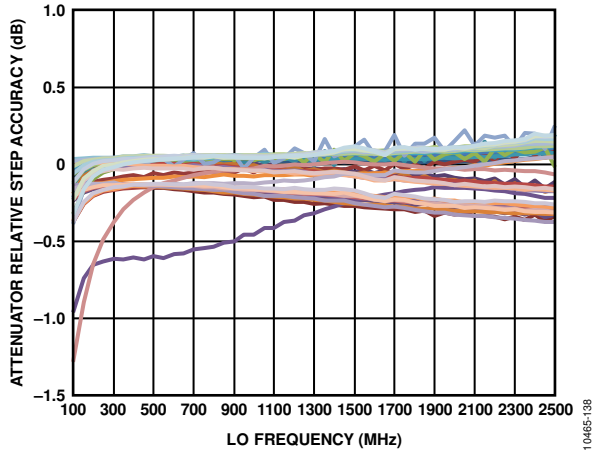

Figure 37. Attenuator Relative Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

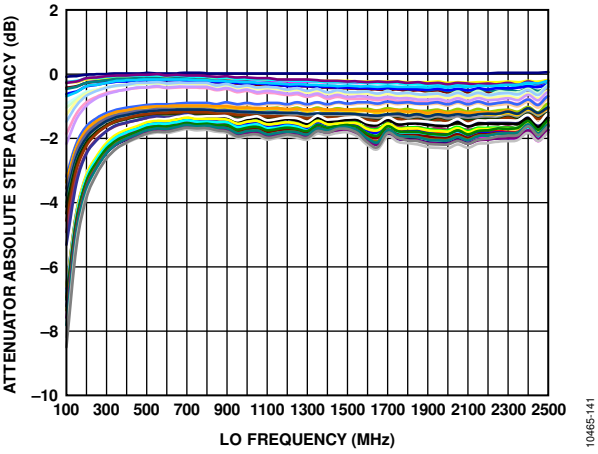

Figure 40. Attenuator Absolute Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

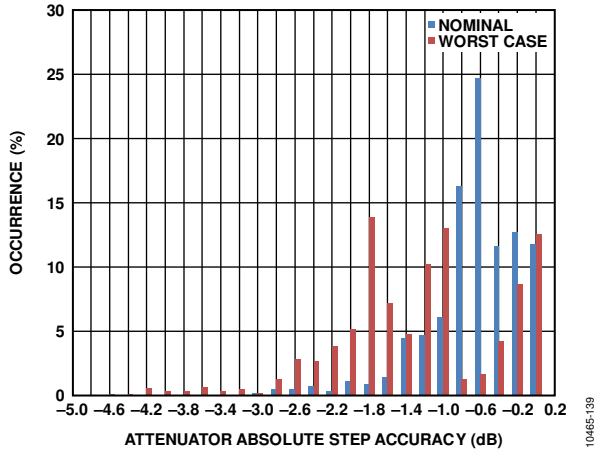

Figure 41. Attenuator Absolute Step Accuracy Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

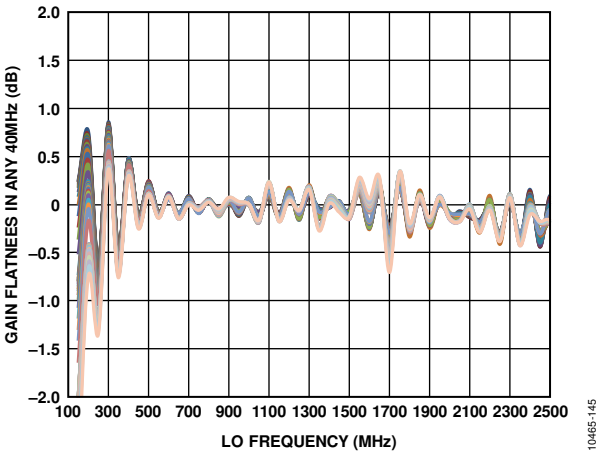

Figure 42. Gain Flatness in any 40 MHz for all Attenuation Steps vs. LO Frequency at Nominal Conditions

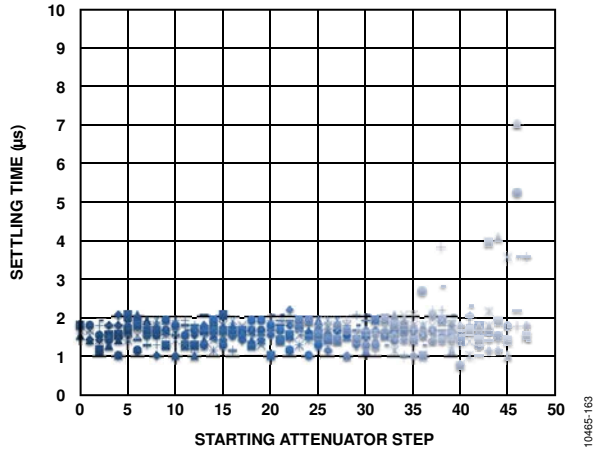

Figure 43. Attenuator Setting Time to 0.2 dB for Small Steps (1 dB to 6 dB) at Nominal Conditions

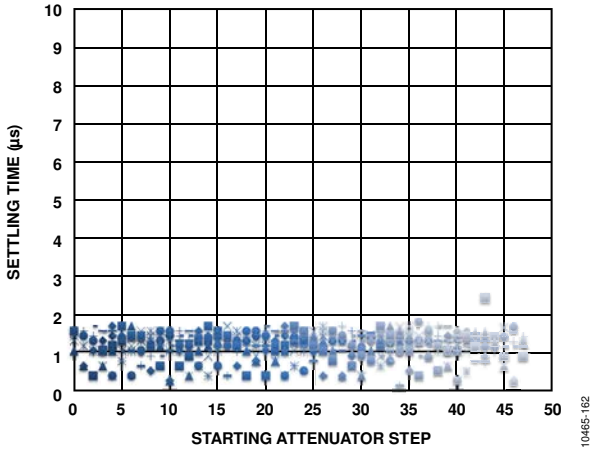

Figure 44. Attenuator Settling Time to 0.5 dB for Small Steps (1 dB to 6 dB) at Nominal Conditions

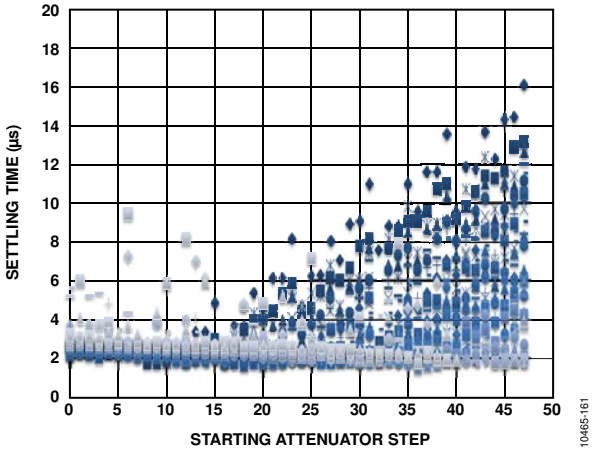

Figure 45. Attenuator Settling Time to 0.2 dB for Large Steps (7 dB to 47 dB) at Nominal Conditions

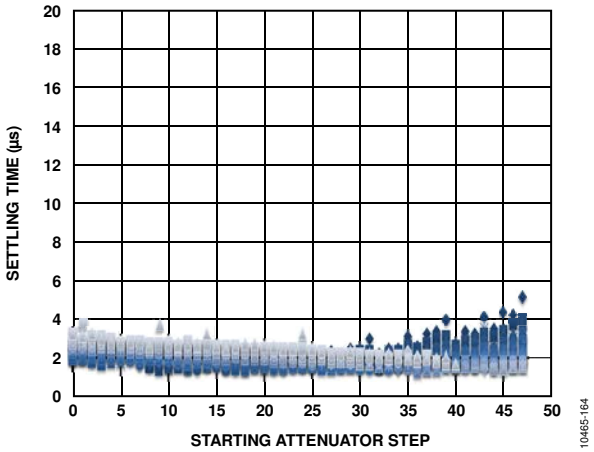

Figure 46. Attenuator Settling Time to 0.5 dB for Large Steps (7 dB to 47 dB) at Nominal Conditions

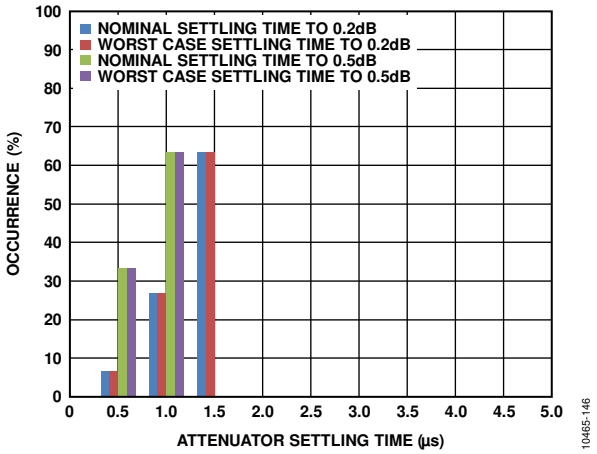

Figure 47. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Small Step

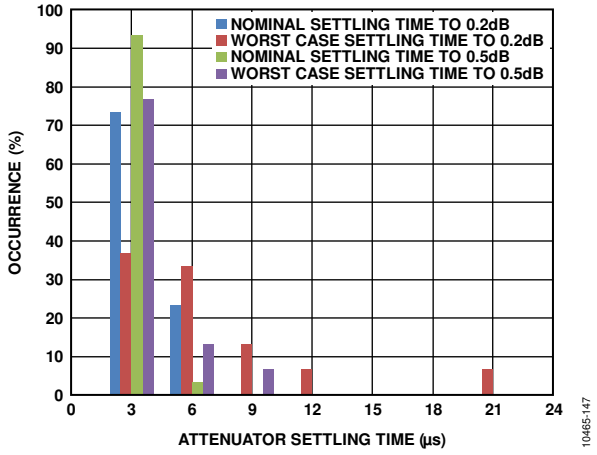

Figure 48. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Small Step (36 dB to 42 dB)

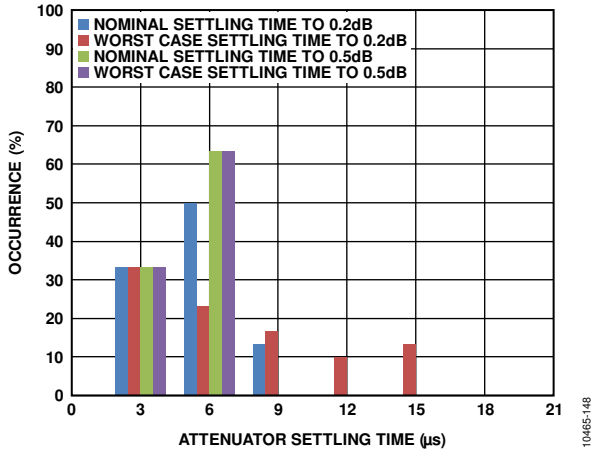

Figure 49. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Large Step

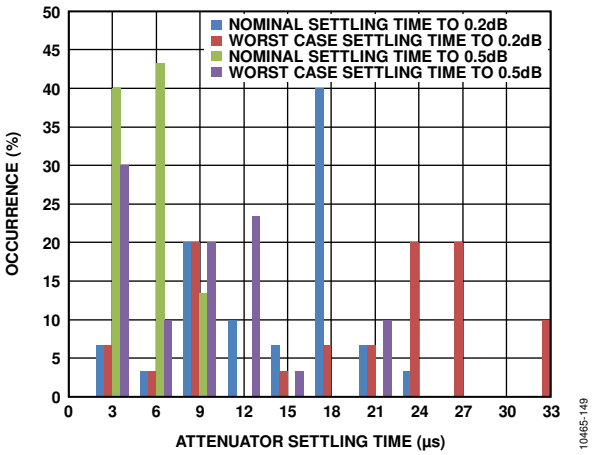

Figure 50. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Large Step (47 dB to 0 dB)

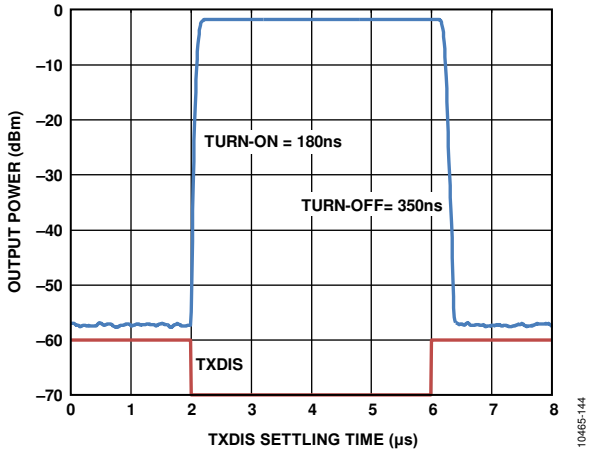

Figure 51. TXDIS Settling Time at Worst-Case Supply and Temperature

THEORY OF OPERATION

OVERVIEW

The ADRF6755 device can be divided into the following basic building blocks:

- PLL synthesizer and VCO
- Quadrature modulator
- Attenuator
- Voltage regulator
- I²C/SPI interface

Each of these building blocks is described in detail in the sections that follow.

PLL SYNTHESIZER AND VCO

Overview

The phase-locked loop (PLL) consists of a fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing a frequency resolution of less than 1 Hz over the entire frequency range. It also has an integrated voltage-controlled oscillator (VCO) with a fundamental output frequency ranging from 2310 MHz to 4800 MHz. An RF divider, controlled by Register CR28, Bits[2:0], extends the lower limit of the local oscillator (LO) frequency range to 100 MHz. See Table 6 for more details on Register CR28.

Reference Input Section

The reference input stage is shown Figure 52. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are open. This ensures that there is no loading of the REFIN pin at power-down.

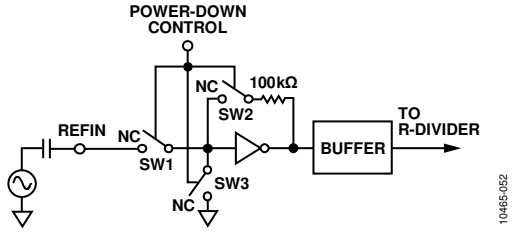

Figure 52. Reference Input Stage

Reference Input Path

The on-chip reference frequency doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves the in-band phase noise performance by up to 3 dBc/Hz.

The 5-bit R-divider allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

An additional divide-by-2 (÷2) function in the reference input path allows for a greater division range.

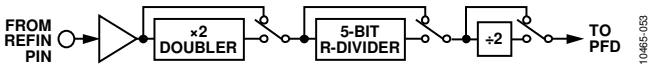

Figure 53. Reference Input Path

The PFD frequency equation is

$$f_{PFD} = f_{REFIN} \times [(1 + D)/(R \times (1 + T))] \quad (1)$$

where:
f_{REFIN} is the reference input frequency.
D is the doubler bit.
R is the programmed divide ratio of the binary 5-bit programmable reference divider (1 to 32).
T is the R/2 divider setting bit (CR10[6] = 0 or 1).

If no division is required, it is recommended that the 5-bit R-divider and the divide-by-2 be disabled by setting CR5[4] = 0. If an even numbered division is required, enable the divide-by-2 by setting CR5[4] = 1 and CR10[6] = 1 and implement the remainder of the division in the 5-bit R-divider. If an odd number division is required, set CR5[4] = 1 and implement all of the division in the 5-bit R-divider.

RF Fractional-N Divider

The RF fractional-N divider allows a division ratio in the PLL feedback path that can range from 23 to 4095. The relationship between the fractional-N divider and the LO frequency is described in the INT and FRAC Relationship section.

INT and FRAC Relationship

The integer (INT) and fractional (FRAC) values make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD) frequency. See the Example—Changing the LO Frequency section for more information.

The LO frequency equation is

$$LO = f_{PFD} \times (INT + (FRAC/2^{25}))/2^{RFDIV} \quad (2)$$

where:
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.
INT is the integer component of the required division factor and is controlled by the CR6 and CR7 registers.
$FRAC$ is the fractional component of the required division factor and is controlled by the CR0 to CR3 registers.
$RFDIV$ is set in Register CR28, Bits[2:0], and controls the setting of the divider at the output of the PLL.

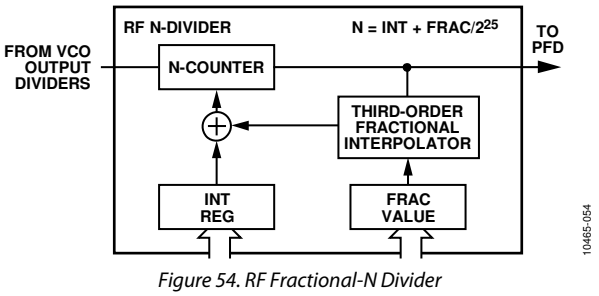

Figure 54. RF Fractional-N Divider

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the R-divider and the N-counter and produces an output proportional to the phase and frequency difference between them (see Figure 55 for a simplified schematic). The PFD includes a fixed delay element that sets the width of the antibacklash pulse, ensuring that there is no dead zone in the PFD transfer function.

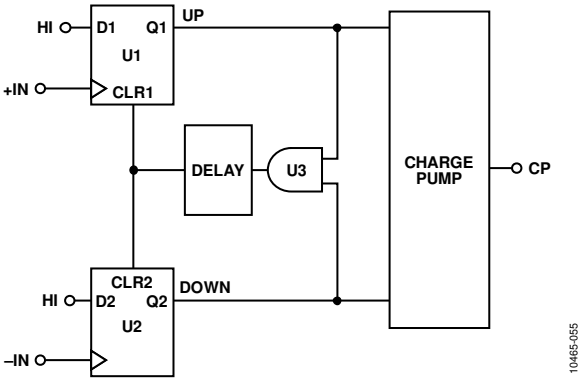

Figure 55. PFD Simplified Schematic

Lock Detect (LDET)

LDET (Pin 44) signals when the PLL has achieved lock to an error frequency of less than 100 Hz. On a write to Register CR0, a new PLL acquisition cycle starts, and the LDET signal goes low. When lock has been achieved, this signal returns high.

Voltage-Controlled Oscillator (VCO)

The VCO core in the ADRF6755 consists of three separate VCOs, each with 16 overlapping bands. This configuration of 48 bands allows the VCO frequency range to extend from 2310 MHz to 4800 MHz. The three VCOs are divided by a programmable divider, RFDIV, controlled by Register CR28, Bits[2:0]. This divider provides divisions of 1, 2, 4, 8, and 16 to ensure that the frequency range is extended from 144.375 MHz (2310 MHz/16) to 4800 MHz (4800 MHz/1). A divide-by-2 quadrature circuit in the path to the modulator then provides the full LO frequency range from 100 MHz to 2400 MHz.

Figure 56 shows a sweep of V_{TUNE} vs. LO frequency demonstrating the three VCOs overlapping and the multiple overlapping bands within each VCO at the LO frequency range of 100 MHz to 2400 MHz. Note that Figure 56 includes the RFDIV being incorporated to provide further divisions of the fundamental VCO frequency; thus, each VCO is used on multiple different occasions throughout the full LO frequency range. The choice of three 16-band VCOs and an RFDIV allows the wide frequency range to be covered without large VCO sensitivity (K_{VCO}) or resultant poor phase noise and spurious performance.

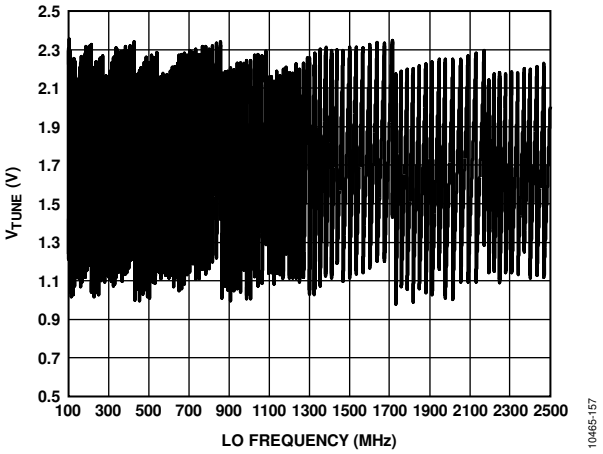

Figure 56. V_{TUNE} vs. LO Frequency

The VCO displays a variation of K_{VCO} as V_{TUNE} varies within the band and from band to band. Figure 57 shows how K_{VCO} varies across the full frequency range. Figure 57 is useful when calculating the loop filter bandwidth and individual loop filter components using ADISimPLL™. ADISimPLL is an Analog Devices, Inc., simulator that aids in PLL design, particularly with respect to the loop filter. It reports parameters such as phase noise, integrated phase noise, and acquisition time for a particular set of input conditions. ADISimPLL can be downloaded from www.analog.com/adisimpll.

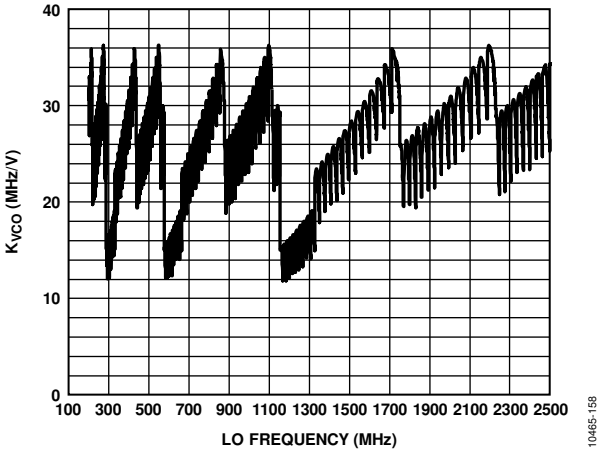

Figure 57. K_{VCO} vs. LO Frequency

Autocalibration

The correct VCO and band are chosen automatically by the VCO and band select circuitry when Register CR0 is updated. This is referred to as autocalibration. The autocalibration time is set by Register CR25.

$$Autocalibration\ Time = (BSCDIV \times 28)/PFD \quad (3)$$

where:
BSCDIV = Register CR25, Bits[7:0].
PFD = PFD frequency.

For a PFD frequency of 40 MHz, set BSCDIV = 100 to set an autocalibration time of 70 µs.

Note that BSCDIV must be recalculated if the PFD frequency is changed. The recommended autocalibration setting is 70 µs. During this time, the VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage. A typical frequency acquisition is shown in Figure 58.

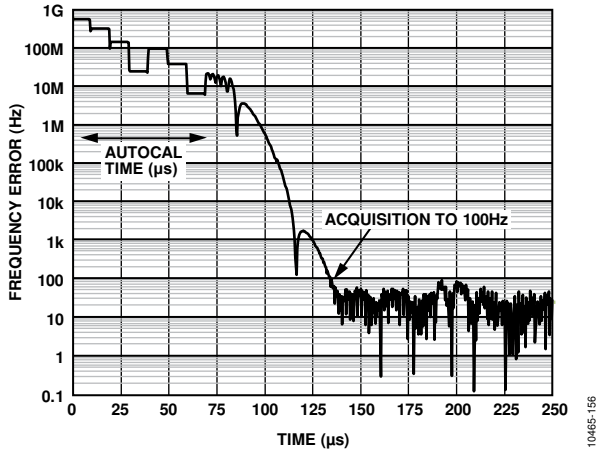

Figure 58. PLL Acquisition

After autocalibration, normal PLL action resumes, and the correct frequency is acquired to within a frequency error of 100 Hz in 170 µs typically. For a maximum cumulative step of 100 kHz/2^{RFDIV}, autocalibration can be turned off by setting Register CR24, Bit 0 = 1. This enables cumulative PLL acquisitions of ≤100 kHz (for RFDIV = ÷1, 50 kHz for RFDIV = ÷2, and so on) to occur without the autocalibration procedure, which improves acquisition times significantly (see Figure 59).

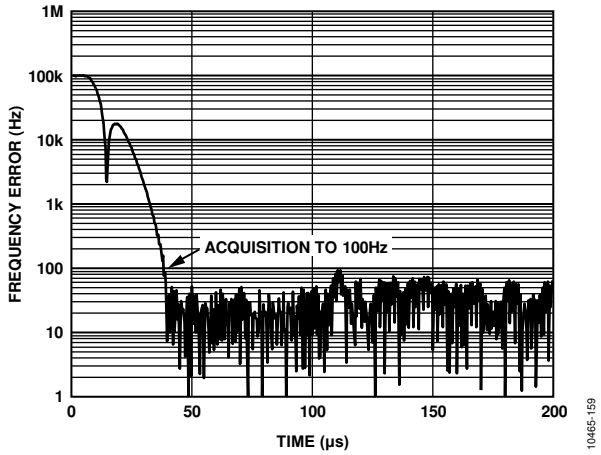

Figure 59. PLL Acquisition Without Autocalibration for a 100 kHz Step

Programming the Correct LO Frequency

There are two steps to programming the correct LO frequency. The user must calculate the RFDIV value based on the required LO frequency and PFD frequency, and the N-divider ratio that is required in the PLL.

1. Calculate the value of RFDIV, which is used to program Register CR28, Bits[2:0] and CR27, Bit 4 from the following lookup table, Table 6.

Table 6. RFDIV Lookup Table

LO Frequency (MHz)	RFDIVIDER	CR28[2:0] = RFDIV	CR27[4]
1155 < LO < 2400	Divide-by-1	000	1
577.5 < LO ≤ 1155	Divide-by-2	001	0
288.75 < LO ≤ 577.5	Divide-by-4	010	0
144.375 < LO ≤ 288.75	Divide-by-8	011	0
100 < LO ≤ 144.375	Divide-by-16	100	0

2. Using the following equation, calculate the value of the N-divider:

$$N = (2^{RFDIV} \times LO)/f_{PFD} \quad (4)$$

where:
N is the N-divider value.
$RFDIV$ is the setting in Register CR28, Bits[2:0].
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.

This equation is a different representation of Equation 2.

Example to Program the Correct LO Frequency

Assume that the PFD frequency is 40 MHz and that the required LO frequency is 1875 MHz.

From Table 6, $2^{RFDIV} = 1$ (RFDIV = 0)

$$N = (1 \times 1875 \times 10^6)/(40 \times 10^6) = 46.875$$

The N-divider value is composed of integer (INT) and fractional (FRAC) components according to the following equation:

$$N = INT + FRAC/2^{25} \quad (5)$$

INT = 46 and FRAC = 29,360,128

The appropriate registers must then be programmed according to the register map. The order in which the registers are programmed is important. Writing to CR0 initiates a PLL acquisition cycle. If the programmed LO frequency requires a change in the value of CR27[4] (see Table 6), CR27 should be the last register programmed, preceded by CR0. If the programmed LO frequency does not require a change in the value of CR27[4], it is optional to omit the write to CR27 and, in that case, CR0 should be the last register programmed.

QUADRATURE MODULATOR

Overview

A basic block diagram of the ADRF6755 quadrature modulator circuit is shown in Figure 60. The VCO/RFDIVIDER generates a signal at the 2× LO frequency, which is then divided down to give a signal at the LO frequency. This signal is then split into in-phase and quadrature components to provide the LO signals that drive the mixers.

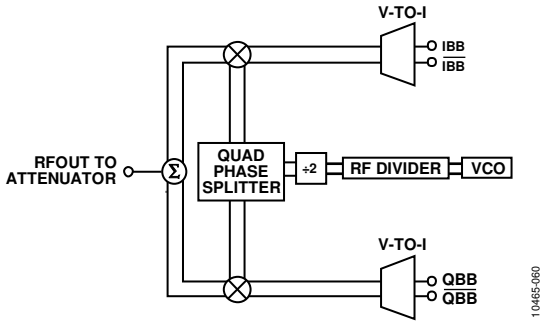

Figure 60. Block Diagram of the Quadrature Modulator

The I and Q baseband input signals are converted to currents by the V-to-I stages, which then drive the two mixers. The outputs of these mixers combine to feed the single-ended output. This single-ended output is then fed to the attenuator and, finally, to the external RFOUT signal pin.

Baseband Inputs

The baseband inputs, QBB, $\overline{\text{QBB}}$, IBB, and $\overline{\text{IBB}}$, must be driven from a differential source. The nominal drive level of 0.9 V p-p differential (450 mV p-p on each pin) should be biased to a common-mode level of 500 mV dc.

To set the dc bias level at the baseband inputs, refer to Figure 61. The average output current on each of the AD9779 outputs is 10 mA. A current of 10 mA flowing through each of the 50 Ω resistors to ground produces the desired dc bias of 500 mV at each of the baseband inputs.

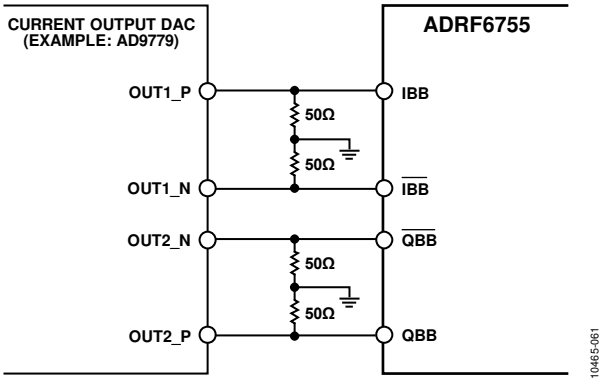

Figure 61. Establishing DC Bias Level on Baseband Inputs

The differential baseband inputs (QBB, $\overline{\text{QBB}}$, $\overline{\text{IBB}}$, and IBB) consist of the bases of PNP transistors, which present a high impedance of about 30 kΩ in parallel with approximately 2 pF of capacitance. The impedance is approximately 30 kΩ below 1 MHz and starts to roll off at higher frequency. A 100 Ω differential termination is recommended at the baseband inputs, and this dominates the input impedance as seen by the input baseband signal. This ensures that the input impedance, as seen by the input circuit, remains flat across the baseband bandwidth. See Figure 62 for a typical configuration.

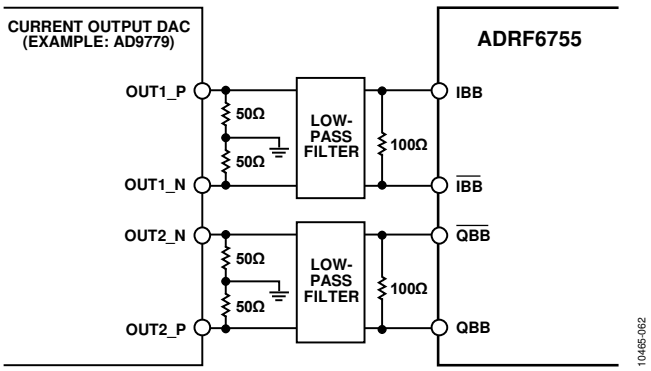

Figure 62. Typical Baseband Input Configuration

The swing of the AD9779 output currents ranges from 0 mA to 20 mA. The ac voltage swing is 1 V p-p single-ended or 2 V p-p differential with the 50 Ω resistors in place. The 100 Ω differential termination resistors at the baseband inputs have the effect of limiting this swing without changing the dc bias condition of 500 mV. The low-pass filter is used to filter the DAC outputs and remove images when driving a modulator.

Another consideration is that the baseband inputs actually source a current of 240 µA out of each of the four inputs. This current must be taken into account when setting up the dc bias of 500 mV. In the initial example based on Figure 61, an error of 12 mV occurs due to the 240 µA current flowing through the 50 Ω resistor. Analog Devices recommends that the accuracy of the dc bias should be 500 mV ± 25 mV. It is also important that this 240 µA current have a dc path to ground.

Optimization

The carrier feedthrough and the sideband suppression performance of the ADRF6755 can be improved over the specifications in Table 1 by using the following optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from dc offsets that occur between the P and N inputs of each of the differential baseband inputs. Normally these inputs are set to a dc bias of approximately 500 mV.

However, if a dc offset is introduced between the P and N inputs of either or both I and Q inputs, the carrier feedthrough is affected in either a positive or a negative fashion. Note that the dc bias level remains at 500 mV (average P and N level). The I channel offset is often held constant while the Q channel offset is varied until a minimum carrier feedthrough level is obtained. Then, while retaining the new Q channel offset, the I channel offset is adjusted until a new minimum is reached. This is usually performed at a single frequency and, thus, is not optimized over the complete frequency range. Multiple optimizations at different