
Chipsmall
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采购部

ANALOG DEVICES

5.9 GHz to 23.6 GHz, Wideband, Microwave Upconverter

Data Sheet

ADRF6780

FEATURES

Wideband RF output frequency range: 5.9 GHz to 23.6 GHz
Two upconversion modes
  Direct conversion from baseband I/Q to RF
  Single sideband upconversion from real IF
LO input frequency range: 5.4 GHz to 14 GHz
LO doubler for up to 28 GHz
Matched 100 Ω balanced RF output, LO input, and IF input
High impedance baseband inputs
Sideband suppression and carrier feedthrough optimization
Variable attenuator and power detector for Tx power control
Programmable via 4-wire SPI interface
32-lead, 5 mm × 5 mm LFCSP microwave packaging

APPLICATIONS

Point to point microwave radios
Radar, electronic warfare systems
Instrumentation, automatic test equipment (ATE)

GENERAL DESCRIPTION

The ADRF6780 is a silicon germanium (SiGe) design, wideband, microwave upconverter optimized for point to point microwave radio designs operating in the 5.9 GHz to 23.6 GHz frequency range.

The upconverter offers two modes of frequency translation. The device is capable of direct conversion to radio frequency (RF) from baseband I/Q input signals, as well as single sideband (SSB) upconversion from a real intermediate frequency (IF) input carrier frequency. The baseband inputs are high impedance and are generally terminated off chip with 100 Ω differential back terminations. The baseband I/Q input path can be disabled and a modulated real IF signal anywhere from 0.8 GHz to 3.5 GHz can fed into the IF input path and upconverted to 5.9 GHz to 23.6 GHz while suppressing the unwanted sideband by typically better than 25 dBc. The serial port interface (SPI) allows tweaking of the quadrature phase adjustment to allow optimum sideband suppression. In addition, the SPI interface allows powering down the output power detector to reduce power consumption when power monitoring is not necessary.

The ADRF6780 upconverter comes in a compact, thermally enhanced, 5 mm × 5 mm LFCSP package. The ADRF6780 operates over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

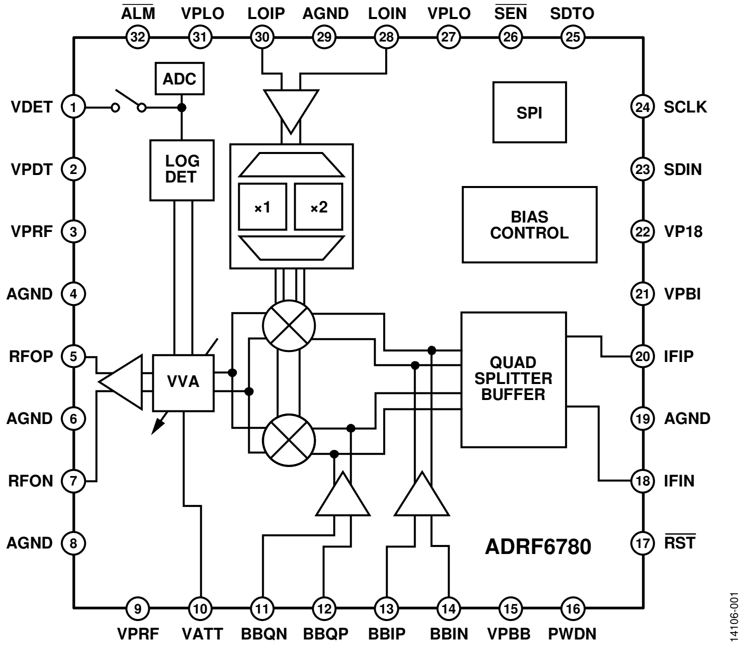

Figure 1.

Rev. A

Document Feedback

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Technical Support
www.analog.com

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Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6780 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6780: 5.9 GHz to 23.6 GHz, Wideband, Microwave Upconverter Data Sheet

User Guides

- UG-920: Evaluating the ADRF6780 5.9 GHz to 23.6 GHz, Wideband Upconverter

TOOLS AND SIMULATIONS

- ADRF6780 S-Parameter

REFERENCE MATERIALS

Technical Articles

- The Changing Landscape of Frequency Mixing Components

DESIGN RESOURCES

- ADRF6780 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6780 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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REVISION HISTORY

5/2016—Rev. 0 to Rev. A

Change to Table 4 ... 7
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3/2016—Revision 0: Initial Version

SPECIFICATIONS

VPBB = VPBI = VPLO = 3.3 V, VP18 = 1.8 V, VPDT = VPRF = 5 V, T_A = 25°C, LO = 0 dBm differential drive; baseband I/Q amplitude = −15 dBm differential sine waves in quadrature with a 500 mV dc bias, baseband input termination with 100 Ω externally, IF amplitude = −12 dBm differential sine waves, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT FREQUENCY RANGE		5.9		23.6	GHz
LOCAL OSCILLATOR (LO) INPUT FREQUENCY RANGE		5.4		14	GHz
LO AMPLITUDE RANGE		−6	0	+6	dBm
IF INPUT FREQUENCY RANGE		0.8		3.5	GHz
BASEBAND (BB) I/Q INPUT FREQUENCY RANGE		DC		750	MHz
I/Q MODULATOR PERFORMANCE					
Modulator Voltage Gain	Maximum gain at maximum gain setting	10	13		dB
	Minimum gain at minimum gain setting		−12		dB
Output Noise Density	Output carrier > −5 dBm		−147		dBc/Hz
	Output carrier > −14 dBm		−145		dBc/Hz
	Output carrier > −22.5 dBm		−136		dBc/Hz
Output Third-Order Intercept (OIP3)	f_{1BB} = 10 MHz, f_{2BB} = 12 MHz, BB I/Q amplitude per tone = −15 dBm sine waves in quadrature with a 500 mV dc bias, 10 dB gain setting				
5.9 GHz to 10 GHz			24		dBm
10 GHz to 14 GHz			25		dBm
14 GHz to 20 GHz			27		dBm
20 GHz to 23.6 GHz			27		dBm
Fifth-Order Intermodulation Distortion (IMD5)	f_1 BB = 10 MHz, f_2 BB = 12 MHz, baseband I/Q amplitude per tone = −15 dBm sine waves in quadrature with a 500 mV dc bias, 10 dB gain setting		65		dBm
Output Second-Order Intercept (OIP2)	f_1 BB = 10 MHz, f_2 BB = 12 MHz, baseband I/Q amplitude per tone = −15 dBm sine waves in quadrature with a 500 mV dc bias, 10 dB gain setting				
5.9 GHz to 10 GHz			65		dBm
10 GHz to 14 GHz			65		dBm
14 GHz to 20 GHz			66		dBm
20 GHz to 23.6 GHz			50		dBm
Output 1 dB Compression Point (P1dB)					
5.9 GHz to 10 GHz	At 10 dB gain setting		10.5		dBm
	At maximum gain setting		11		dBm
10 GHz to 14 GHz	At 10 dB gain setting		11		dBm
	At maximum gain setting		12		dBm
14 GHz to 20 GHz	At 10 dB gain setting		10		dBm
	At maximum gain setting		12		dBm
20 GHz to 23.6 GHz	At 10 dB gain setting		10		dBm
	At maximum gain setting		11		dBm
LO Feedthrough	At 10 dB gain setting (can be improved baseband dc offset adjustment)		−25		dBm
Sideband Suppression	At 10 dB gain setting		25		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IF UPCONVERTER PERFORMANCE					
Upconversion Voltage Gain	Maximum gain at maximum gain setting	7	11		dB
	Minimum gain at minimum gain setting		−14		dB
Output Noise Density	Output carrier > −5 dBm		−147		dBc/Hz
	Output carrier > −14 dBm		−145		dBc/Hz
	Output carrier > −22.5 dBm		−136		dBc/Hz
OIP3	f_1 IF = 1810 MHz, f_2 IF = 1812 MHz, amplitude per tone = −15 dBm sine waves in quadrature with ac bias, 7 dB gain setting		23.5		
5.9 GHz to 10 GHz			27		dBm
10 GHz to 14 GHz			24		dBm
14 GHz to 20 GHz			22.5		dBm
20 GHz to 23.6 GHz			22.5		dBm
IMD5	f_1 IF = 1810 MHz, f_2 IF = 1812 MHz, amplitude per tone = −15 dBm sine waves in quadrature with ac bias, 7 dB gain setting		80		dBm
Output P1dB					
5.9 GHz to 10 GHz	At 7 dB gain setting		10.5		dBm
	At maximum gain setting		11.5		dBm
10 GHz to 14 GHz	At 7 dB gain setting		10		dBm
	At maximum gain setting		12		dBm
14 GHz to 20 GHz	At 7 dB gain setting		9.5		dBm
	At maximum gain setting		12		dBm
20 GHz to 23.6 GHz	At 7 dB gain setting		9.5		dBm
	At maximum gain setting		11.5		dBm
LO Feedthrough	At 7 dB gain setting (can be improved by baseband dc offset adjustment)		−35		dBm
Sideband Suppression	At 7 dB gain setting		25		dBc
Tx POWER DETECTOR PERFORMANCE					
Output Level					
Maximum			2		dBm
Minimum			−30		dBm
±1 dB Dynamic Range			34		dB
Output Voltage					
Maximum			1		V
Minimum			0.2		V
Log Slope			25		mV/dB
Time					
Rise	P_{IN} = off to −10 dBm, 10% to 90%, C7 = 10 pF (see Figure 83)		134		ns
Fall	P_{IN} = −10 dBm to off, 10% to 90%, C7 = 10 pF (see Figure 83)		190		ns
Response	C7 = 10 pF (see Figure 83)		30		ns
RETURN LOSS					
RF Output	100 Ω differential		12		dB
LO Input	100 Ω differential		12		dB
IF Input	100 Ω differential		17		dB
Baseband I/Q Input Impedance			1		MΩ
LOGIC INPUTS					
Input High Voltage Range, V_{INH}		VP18 − 0.4		1.8	V
Input Low Voltage Range, V_{INL}		0		0.4	V
Input Current, I_{INH}/I_{INL}			100		µA
Input Capacitance, C_{IN}			3		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC OUTPUTS					
Output High Voltage Range, V_{OH}		VP18 − 0.4		1.8	V
Output Low Voltage Range, V_{OL}		0		0.4	V
Output High Current, I_{OH}				500	µA
POWER INTERFACE					
VPBB, VPLO, VPBI		3.15	3.3	3.45	V
VPBB, VPLO, VPBI Supply Current	×1 LO path enabled, IF path disabled		340		mA
	×2 LO path enabled, IF path disabled		390		mA
	×1 LO path enabled, IF path enabled		490		mA
	×2 LO path enabled, IF path enabled		540		mA
VP18		1.7	1.8	1.9	V
VP18 Supply Current			1		mA
VPDT, VPRF		4.75	5	5.25	V
VPDT, VPRF Supply Current	×1/×2 LO path enabled, IF path disabled		180		mA
	×1/×2 LO path enabled, IF path enabled		160		mA
Total Power Consumption	×2 LO path enabled, IF path enabled		2.58		W
	Power down		35	50	mW

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
VPDT, VPRF	6.5 V
VPBB, VPLO, VPBI	4.3 V
VP18	2.3 V
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 3. Thermal Resistance

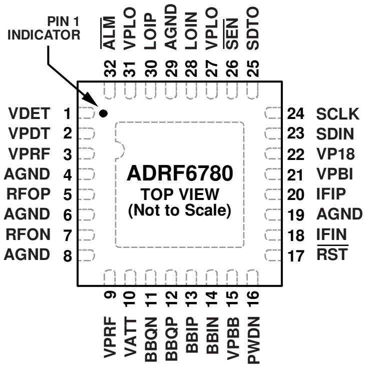
Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
32-Lead LFCSP	32.95	1.14	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (printed circuit board (PCB) with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. SOLDER THE EXPOSED PAD TO A LOW IMPEDANCE GROUND PLANE.
2. THE DEVICE NUMBER ON THE FIGURE DOES NOT INDICATE THE LABEL ON THE PACKAGE. PLEASE REFER TO PIN 1 INDICATOR FOR PIN LOCATIONS.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDET	RF Detector Output. The voltage output is proportional to the decibel RF output power. The detector slope is nominally 50 mV/dB.
2	VPDT	Power Supply Connection for the RF Detector. Decouple the VPDT pin with 100 pF and 0.1 μF capacitors as close as possible to the pin.
3, 9	VPRF	Power Supply Connections for the RF Path. Decouple the VPRF pin with 100 pF and 0.1 μF capacitors as close as possible to the pins.
4, 6, 8, 19, 29	AGND	Analog Grounds. Connect these pins to a low impedance ground plane.
5, 7	RFOP, RFON	RF Outputs. These outputs are 100 Ω differential outputs for the RF path. Frequency range is 5.9 GHz to 23.6 GHz.
10	VATT	Modulator Output Attenuator Control Input. The RF voltage variable attenuator is controlled by applying a 0 V to 2.6 V control voltage to the VATT pin. Increase the gain when VATT voltage increases. This pin is linear in dB over central gain range.
11 to 14	BBQN, BBQP, BBIP, BBIN	I Channel and Q Channel Baseband Inputs. These inputs are high input impedance and are typically differentially terminated to a 100 Ω resistor using an off chip termination. The nominal common-mode bias level on these pins must be 0.5 V.
15	VPBB	Power Supply Connection for Baseband Path. Decouple the VPBB pin with 100 pF and 0.1 μF capacitors as close as possible to the pin.
16	PWDN	Power Down. The ADRF6780 powers up when the PWDN pin is at a low logic level (<0.5 V). To power down the ADRF6780, apply a logic high level (>1.2 V). When the ADRF6780 is powered up, the SPI can also be used as a power-down capability. The PWDN pin has an internal 18 kΩ pull-down resistor.
17	$\overline{\text{RST}}$	Reset. This pin provides the ability to reset the SPI to the default register settings. Pull the $\overline{\text{RST}}$ pin to a logic high level in normal operation. Driving the $\overline{\text{RST}}$ pin to a logic low level loads the default SPI register settings. The $\overline{\text{RST}}$ pin has an internal 7.75 kΩ pull-up resistor.
18, 20	IFIN, IFIP	IF Inputs. These inputs are 100 Ω differential inputs for IF upconversion, and they must be ac-coupled. When the IF mode is set, remove the 0 Ω R10 to R13 resistors from the I/Q lines.
21	VPBI	Power Supply Connection. Decouple the VPBI pin with 100 pF and 0.1 μF capacitors as close as possible to the pin.
22	VP18	1.8 V Power Supply. Decouple the VP18 pin with 100 pF and 0.1 μF capacitors as close as possible to the pin.
23	SDIN	Serial Data Input. Serial data applied to the SDIN pin is loaded into the SPI register upon a successful write command as indicated in the timing diagrams (see Figure 68 to Figure 70). The first most significant bit (MSB) is a control bit and it determines whether data is written to the register (logic high) or read from the serial data output pin (logic low). The SDIN pin has an internal 18 kΩ pull-down resistor.
24	SCLK	Serial Clock. This pin is the clock input for the SPI interface. The SCLK pin has an internal 18 kΩ pull-down resistor.
25	SDTO	Serial Data Output. The SDTO pin provides a SPI readback capability. See the timing diagrams for normal operation (see Figure 68 to Figure 70). The SDTO pin has an internal 18 kΩ pull-down resistor.
26	$\overline{\text{SEN}}$	Serial Enable. When the $\overline{\text{SEN}}$ input pin goes high, the data stored in the shift registers is loaded into the register. The $\overline{\text{SEN}}$ pin has an internal 7.75 kΩ pull-up resistor.

Pin No.	Mnemonic	Description
27, 31	VPLO	Power Supply Connections for the LO Path. Decouple the VPLO pin with 100 pF and 0.1 µF capacitors as close as possible to the pin.
28, 30	LOIN, LOIP	LO Inputs. These inputs are 100 Ω differential inputs for the LO path. The LO input frequency range is 5.4 GHz to 14 GHz. The on-chip LO frequency doubler can be enabled via a SPI command.
32	$\overline{\text{ALM}}$	Alarm. The $\overline{\text{ALM}}$ pin indicates internal alarm conditions. The $\overline{\text{ALM}}$ pin is logic low when an alarm condition is detected.
	EP	Exposed Pad. Solder the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VPBB = VPBI = VPLO = 3.3 V, VP18 = 1.8 V, VPDT = VPRF = 5 V, T_A = 25°C, LO = 0 dBm differential drive, polyphase filter (PPF, ×1) mode below 14 GHz and differential drive doubler (×2) mode above 14 GHz, VATT = 2.6 V, unless otherwise noted.

I/Q MODE

Baseband (BB) I/Q amplitude = −15 dBm, differential sine waves in quadrature with a 500 mV dc bias, BB I/Q frequency (f_x BB) = 10 MHz, BB input termination with 100 Ω externally, unless otherwise noted.

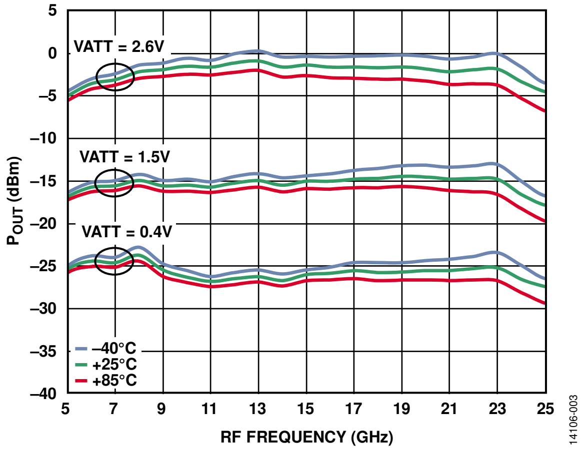


Figure 3. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various Temperatures, BB I/Q Amplitude = −15 dBm

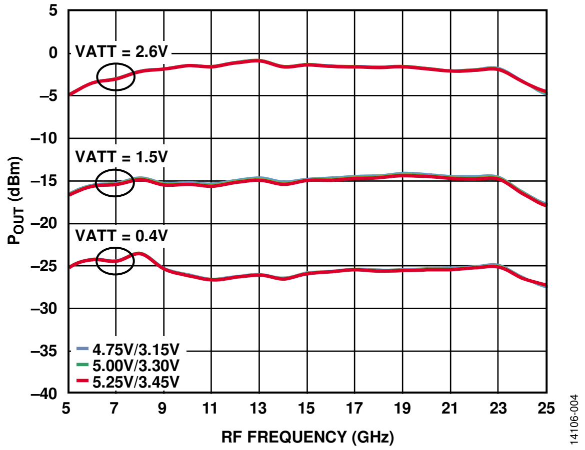


Figure 4. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various Supply Voltages, BB I/Q Amplitude = −15 dBm

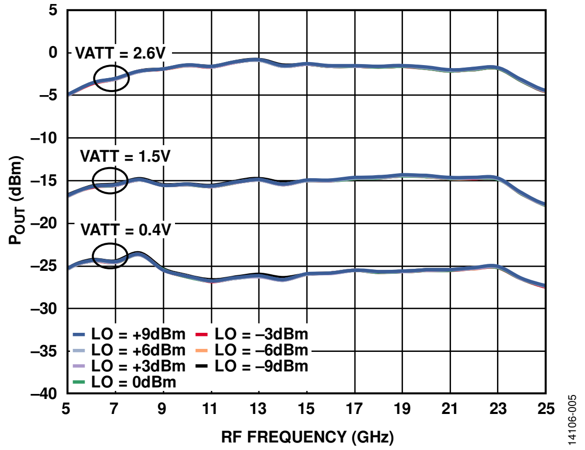


Figure 5. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various LO Inputs, BB I/Q Amplitude = −15 dBm

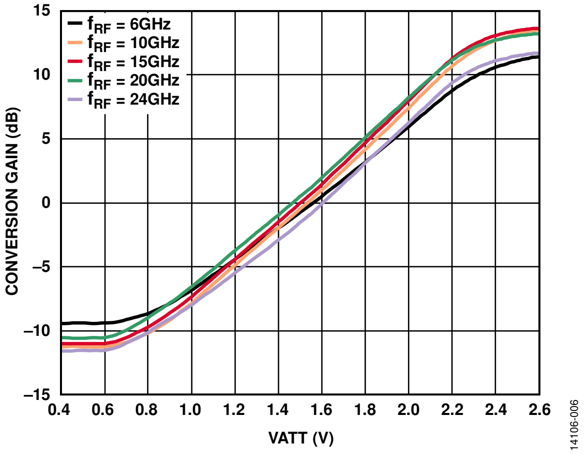


Figure 6. Conversion Gain vs. VATT for Various RF Frequencies (f_{RF})

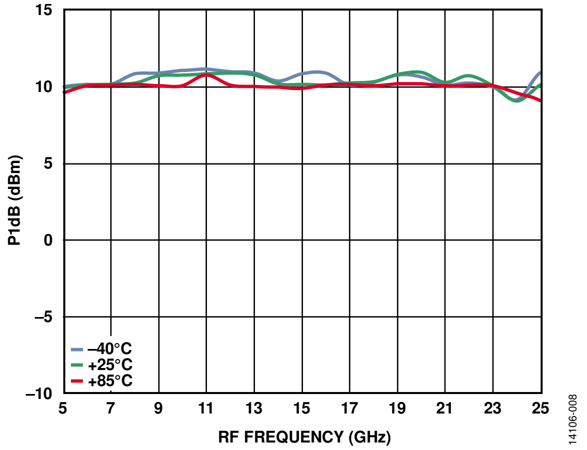


Figure 7. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Temperatures

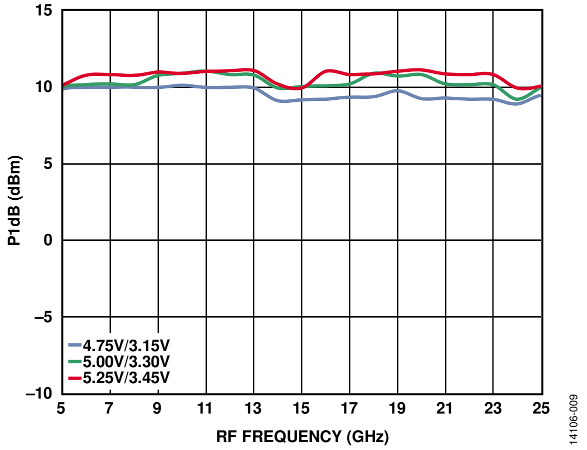


Figure 8. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Supply Voltages

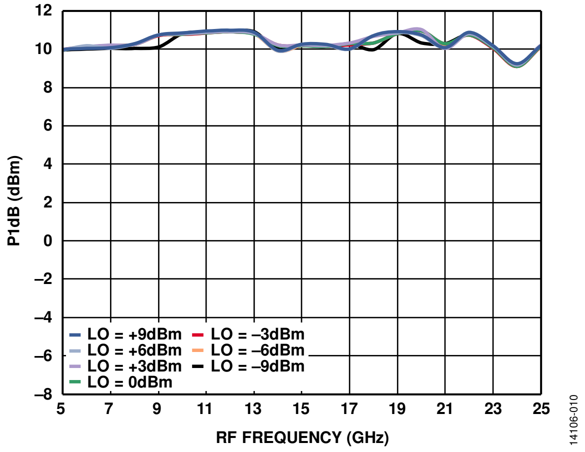


Figure 9. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various LO Inputs

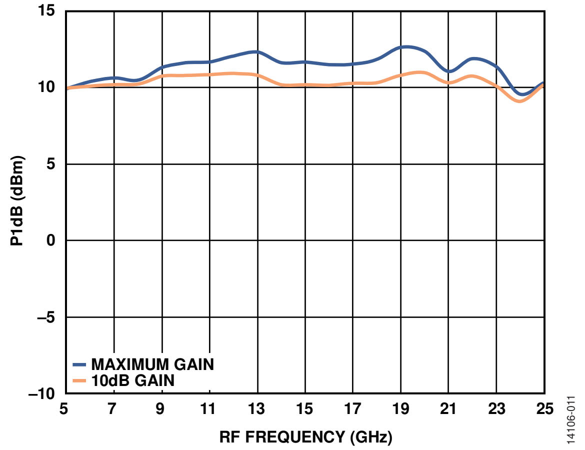


Figure 10. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting and the Maximum Gain Setting

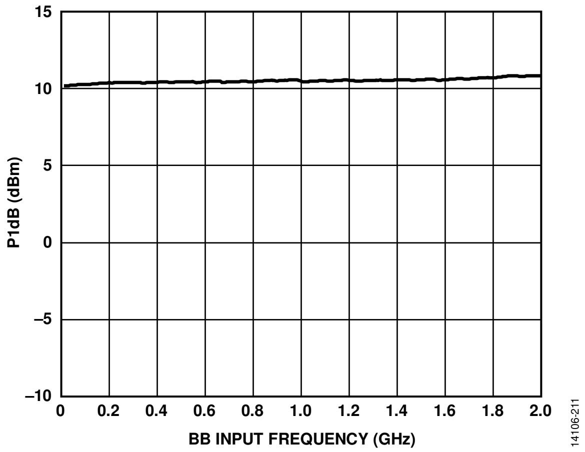


Figure 11. Output 1 dB Compression Point (P1dB) vs. BB Input Frequency at a 10 dB Gain Setting

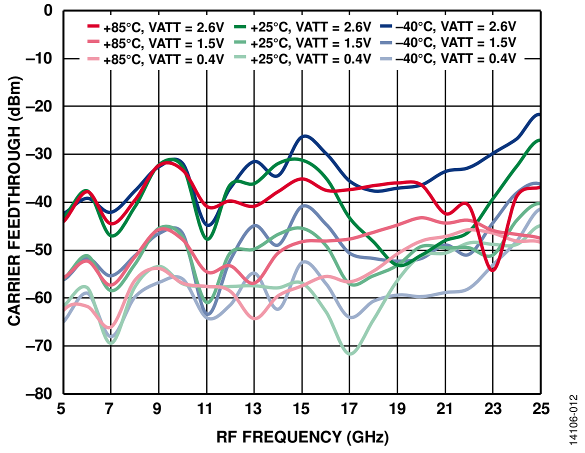


Figure 12. Carrier Feedthrough vs. RF Frequency (f_{RF}) at Three Gain Settings and Temperatures Before Nulling

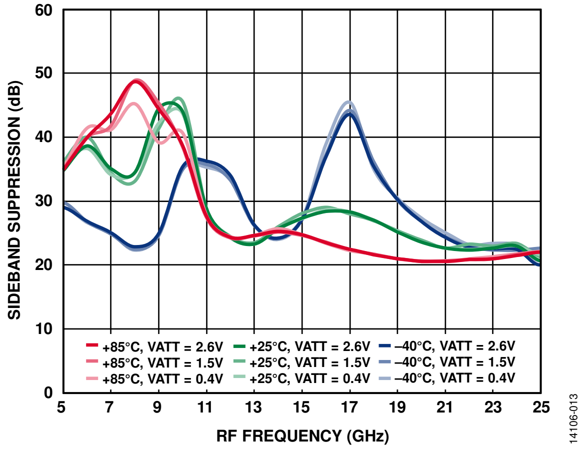


Figure 13. Sideband Suppression vs. RF Frequency (f_{RF}) at Three Gain Settings and Temperatures Before Nulling

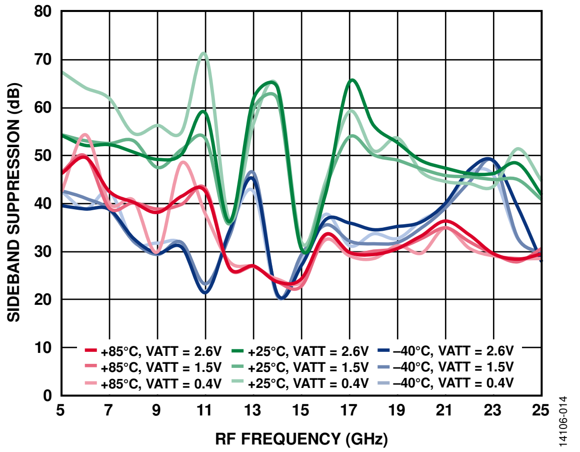


Figure 14. Sideband Suppression vs. RF Frequency (f_{RF}) at Three Gain Settings and Temperatures after Nulling Using I_PATH_PHASE_ACCURACY and Q_PATH_PHASE_ACCURACY at 25°C

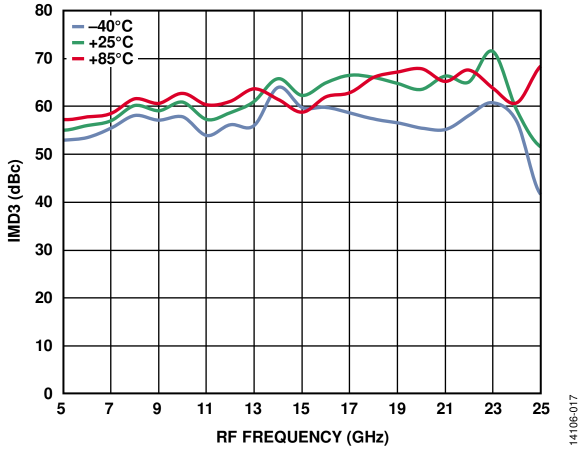


Figure 15. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Temperatures, BB I/Q Amplitude = −15 dBm per Tone

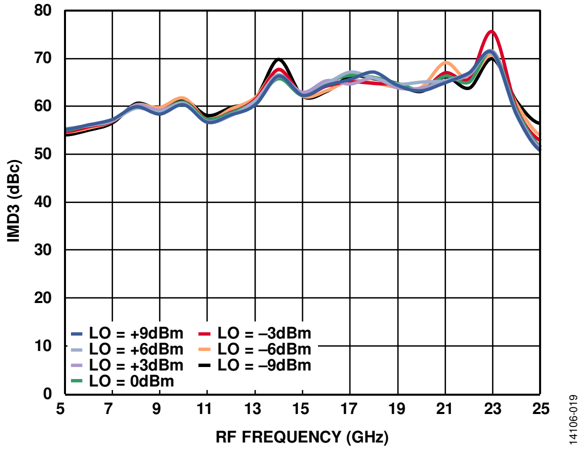


Figure 18. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various LO Inputs, BB I/Q Amplitude = −15 dBm per Tone

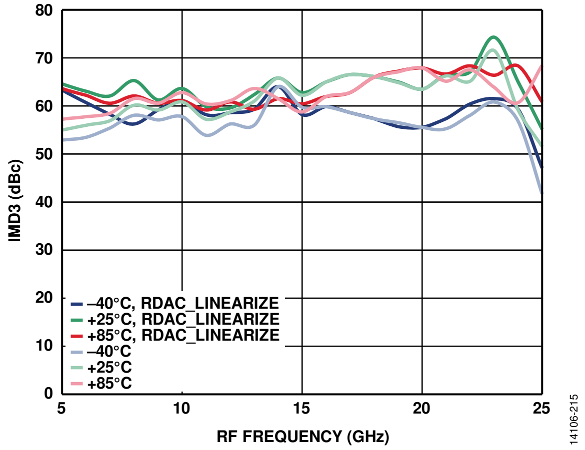


Figure 16. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various RDAC_LINEARIZE Settings and Various Temperatures, BB I/Q Amplitude = −15 dBm per Tone

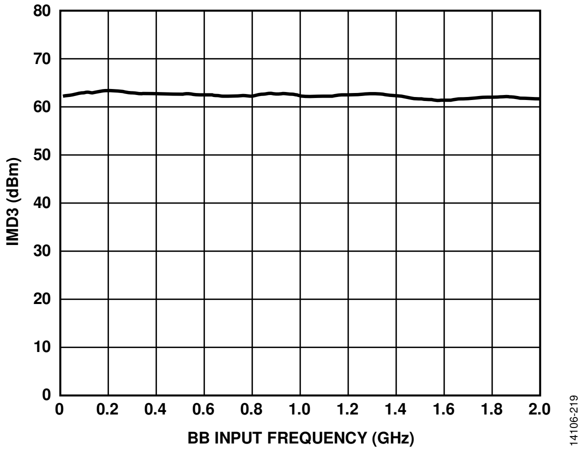


Figure 19. Third-Order Intermodulation Distortion (IMD3) vs. BB Input Frequency at a 10 dB Gain Setting, BB I/Q Amplitude = −15 dBm per Tone

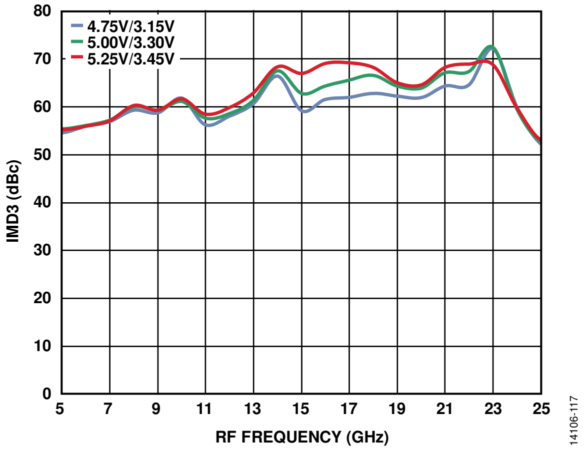


Figure 17. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) for Various Supply Voltages, BB I/Q Amplitude = −15 dBm per Tone

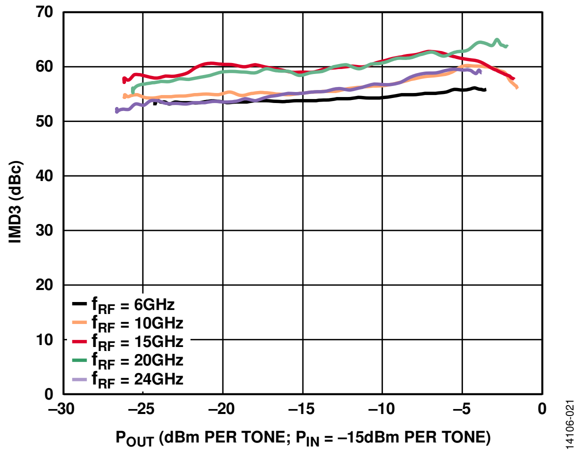


Figure 20. Third-Order Intermodulation Distortion (IMD3) vs. Output Power (P_{OUT}) for Various RF Frequencies (f_{RF}), BB I/Q Amplitude = −15 dBm per Tone

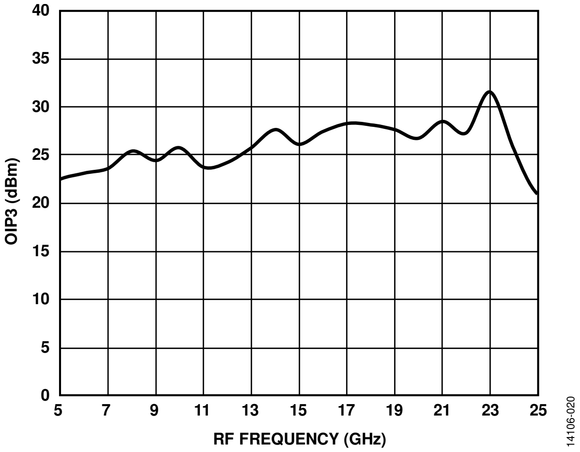


Figure 21. Output Third-Order Intercept (OIP3) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting, BB I/Q Amplitude = −15 dBm per Tone

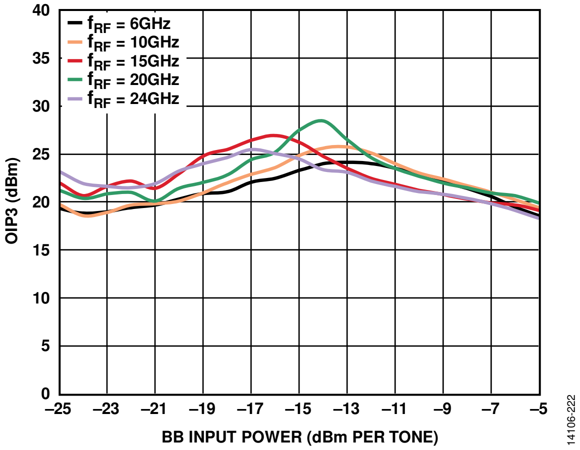


Figure 22. Output Third-Order Intercept (OIP3) vs. BB Input Power at a 10 dB Gain Setting for Various RF Frequencies (f_{RF})

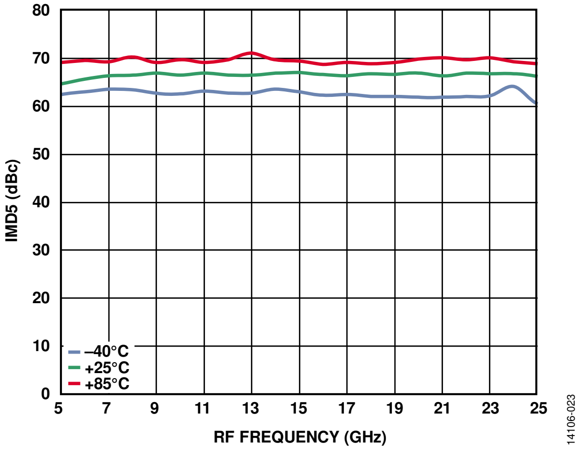


Figure 23. Fifth-Order Intermodulation Distortion (IMD5) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Temperatures, BB I/Q Amplitude = −15 dBm per Tone

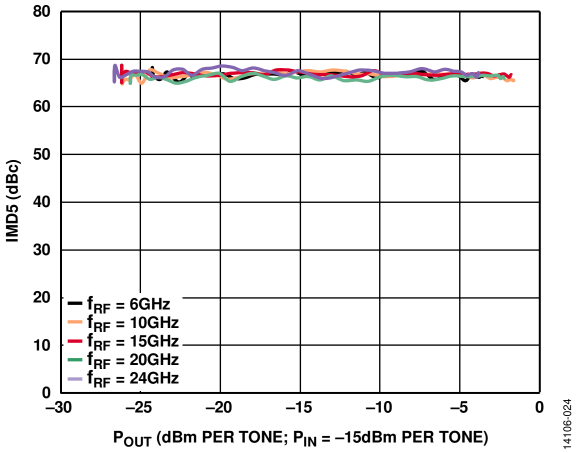


Figure 24. Fifth-Order Intermodulation Distortion (IMD5) vs. Output Power (P_{OUT}) for Various RF Frequencies, BB I/Q Amplitude = −15 dBm per Tone

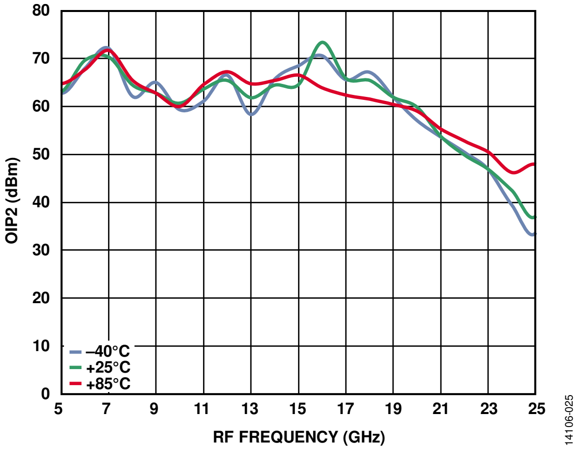


Figure 25. Output Second-Order Intercept (OIP2) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Temperatures, BB I/Q Amplitude = −15 dBm per Tone

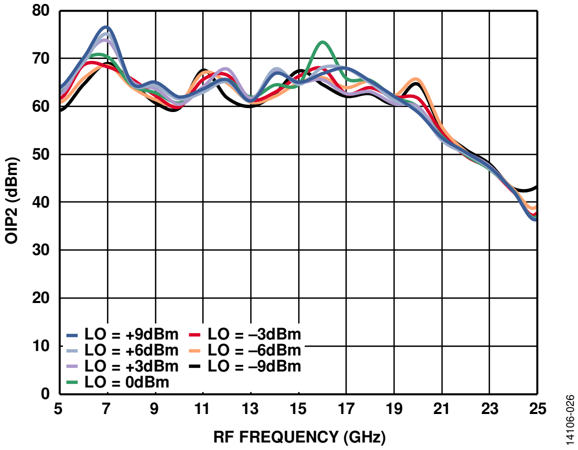


Figure 26. Output Second-Order Intercept (OIP2) vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various LO Inputs, BB I/Q Amplitude = −15 dBm per Tone

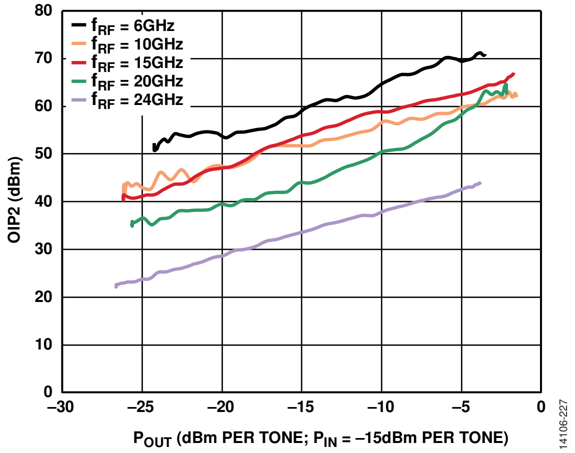


Figure 27. Output Second-Order Intercept (OIP2) vs. Output Power (P_{OUT}) for Various RF Frequencies (f_{RF}), BB I/Q Amplitude = −15 dBm per Tone

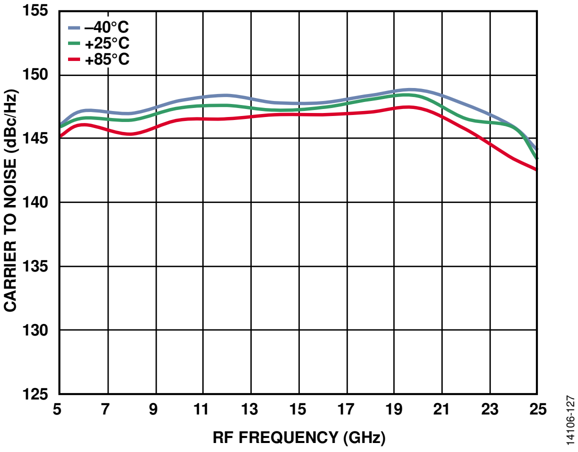


Figure 28. Output Noise Density vs. RF Frequency (f_{RF}) at a 10 dB Gain Setting for Various Temperatures with an Output Carrier of −5 dBm

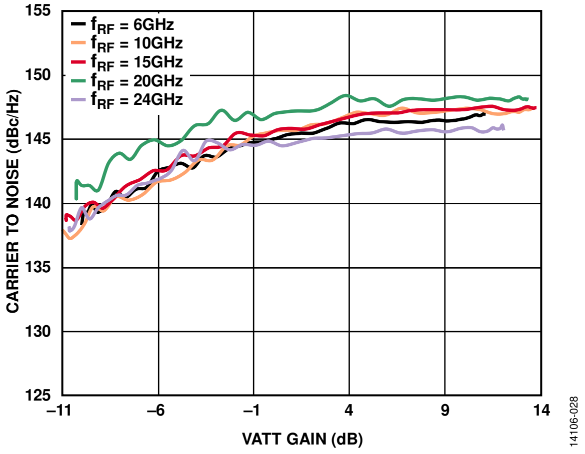


Figure 29. Output Noise Density vs. VATT Gain for Various RF Frequencies (f_{RF}) with an Input Carrier of −15 dBm

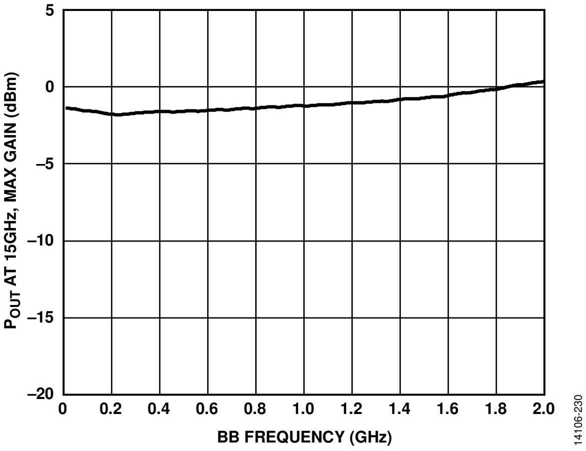


Figure 30. Bandwidth, P_{OUT} at 15 GHz and the Maximum Gain Setting vs. BB Input Frequency

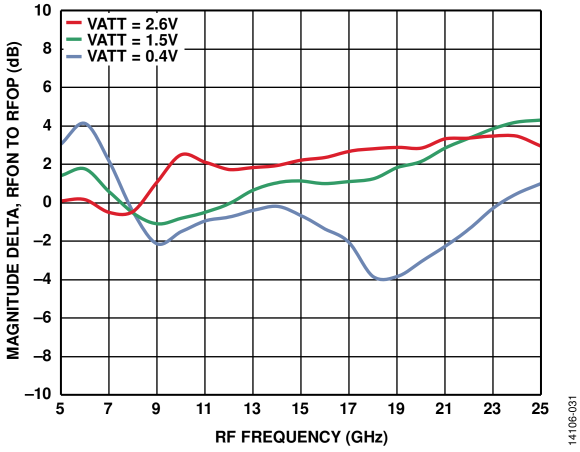


Figure 31. Magnitude Delta, RFON to RFOP vs. RF Frequency (f_{RF}) at Three Different Gain Settings

IF MODE

IF frequency (IF mode) = 1900 MHz, IF amplitude = −12 dBm, input ac-coupled, unless otherwise noted.

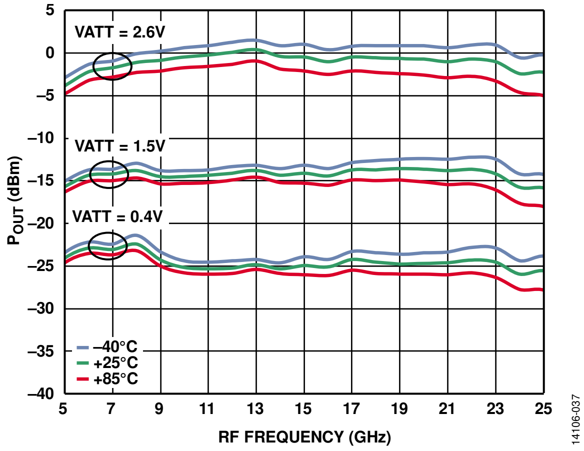


Figure 32. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various Temperatures, IF Amplitude = −12 dBm

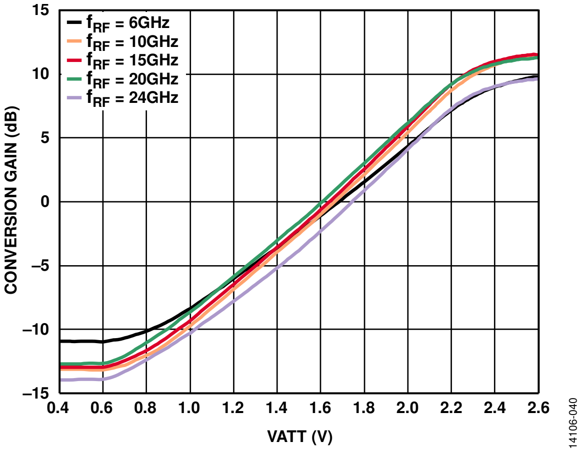


Figure 35. Conversion Gain vs. VATT at Various RF Frequencies (f_{RF})

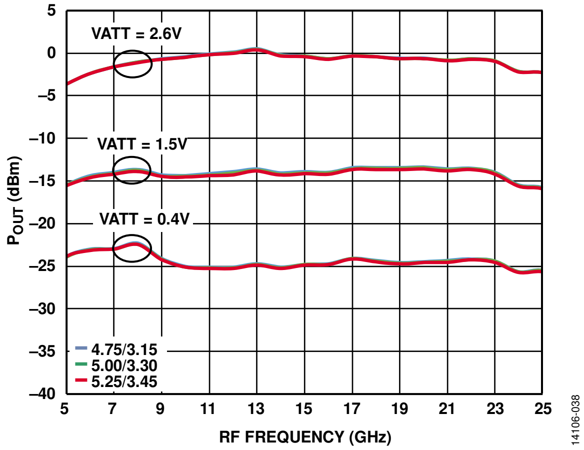


Figure 33. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various Supply Voltages, IF Amplitude = −12 dBm

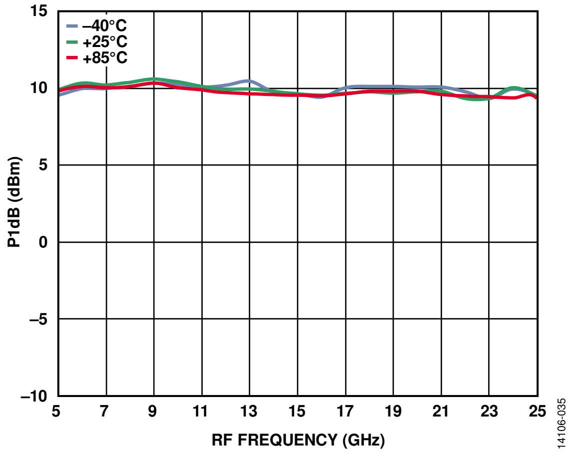


Figure 36. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Temperatures

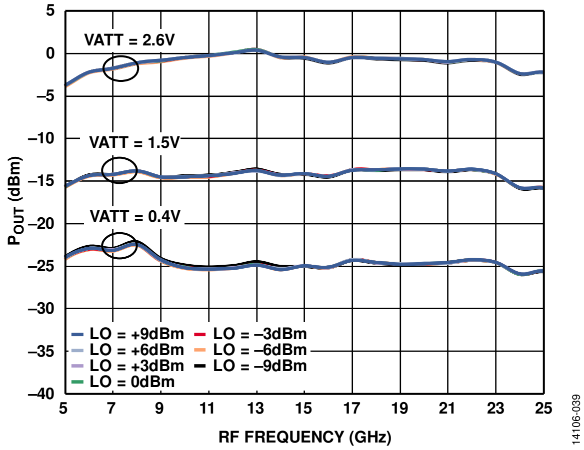


Figure 34. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) at Three Gain Settings for Various LO Inputs, IF Amplitude = −12 dBm

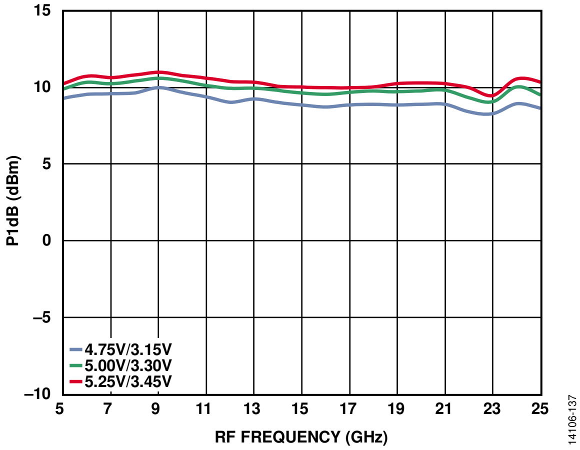


Figure 37. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Supply Voltages

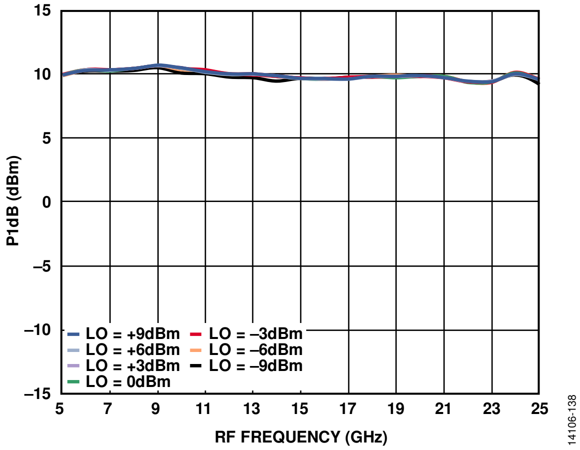


Figure 38. Output 1 dB Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various LO Inputs

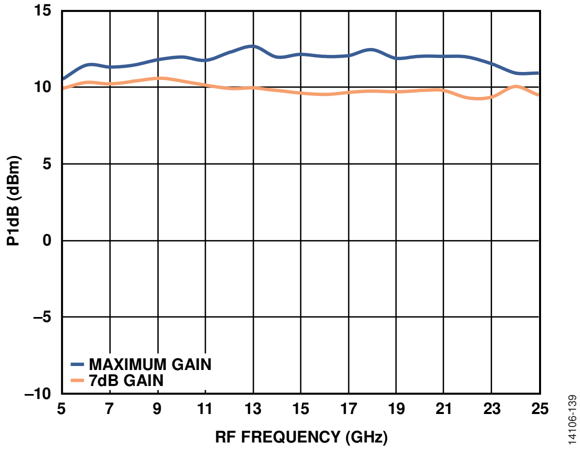


Figure 39. 1 dB Output Compression Point (P1dB) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting and the Maximum Gain Setting

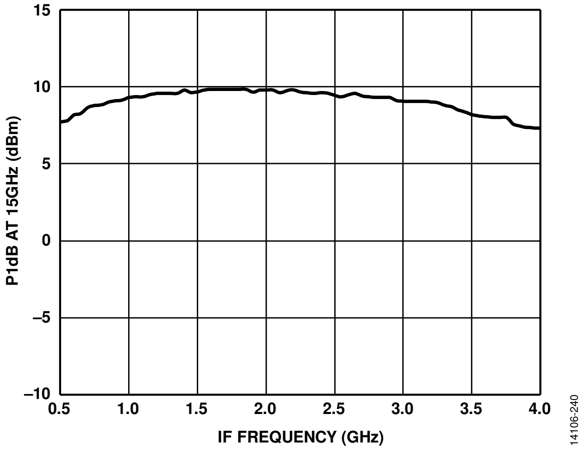


Figure 40. Output 1 dB Compression Point (P1dB) at 15 GHz vs. IF Frequency at a 7 dB Gain Setting

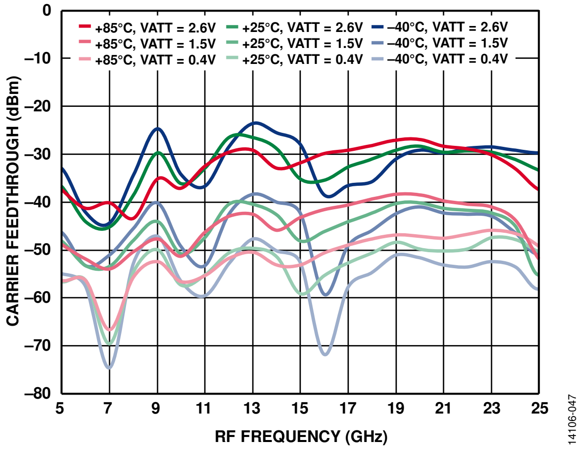


Figure 41. Carrier Feedthrough vs. RF Frequency (f_{RF}) at Three Gain Settings for Various Temperatures Before Nulling

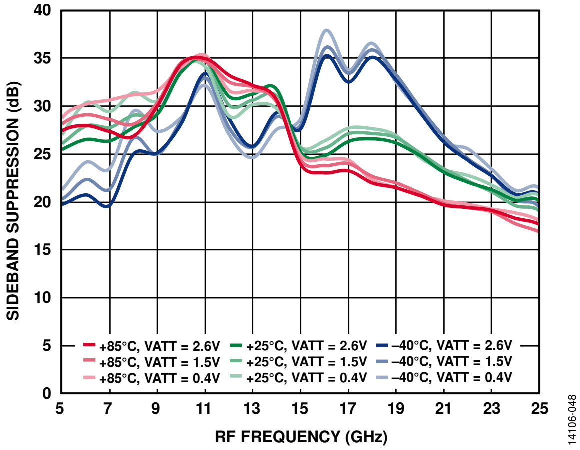


Figure 42. Sideband Suppression vs. RF Frequency (f_{RF}) at Three Different Gain Settings for Various Temperatures Before Nulling

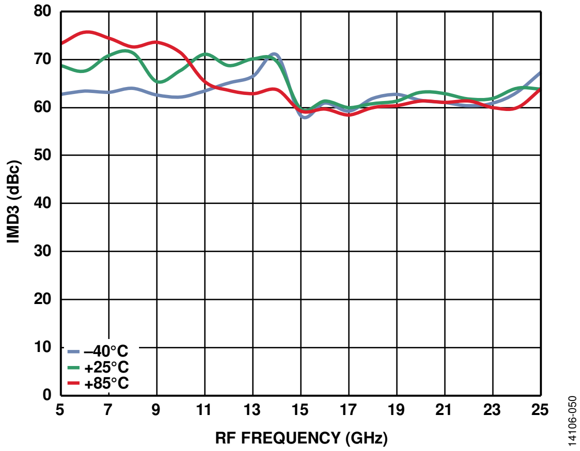


Figure 43. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Temperatures, IF Amplitude = −15 dBm per Tone

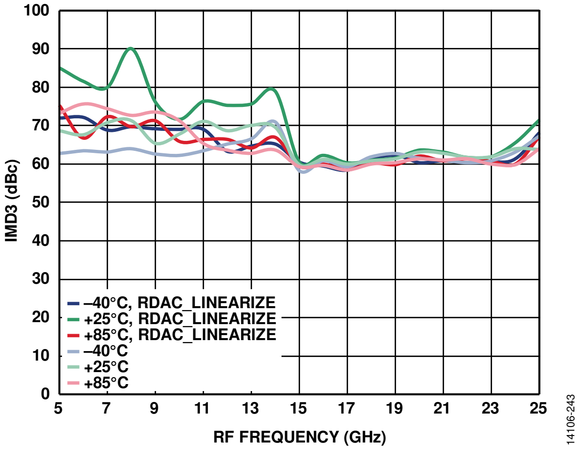


Figure 44. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at 7 dB Gain Setting for Various RDAC_LINEARIZE Settings and Various Temperatures, IF Amplitude = −15 dBm per Tone

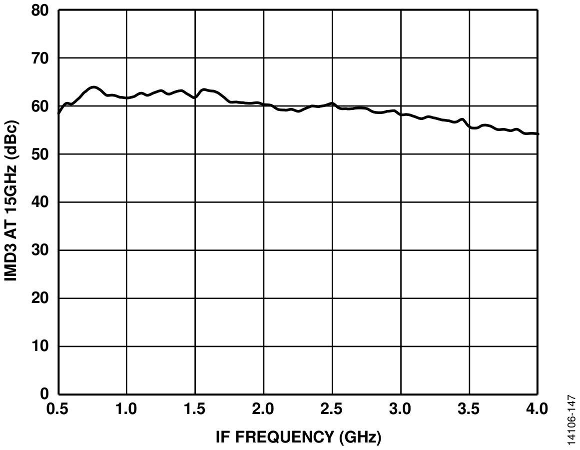


Figure 47. Third-Order Intermodulation Distortion (IMD3) at 15 GHz vs. IF Frequency at a 7 dB Gain Setting

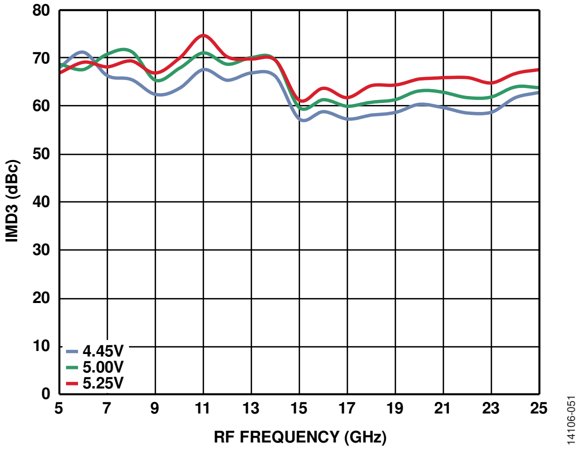


Figure 45. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting and for Various Supply Voltages, IF Amplitude = −15 dBm per Tone

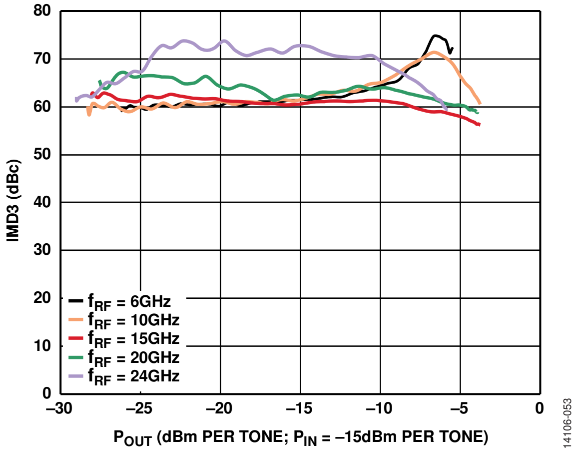


Figure 48. Third-Order Intermodulation Distortion (IMD3) vs. Output Power (P_{OUT}) for Various RF Frequencies (f_{RF}), IF Amplitude = −15 dBm per Tone

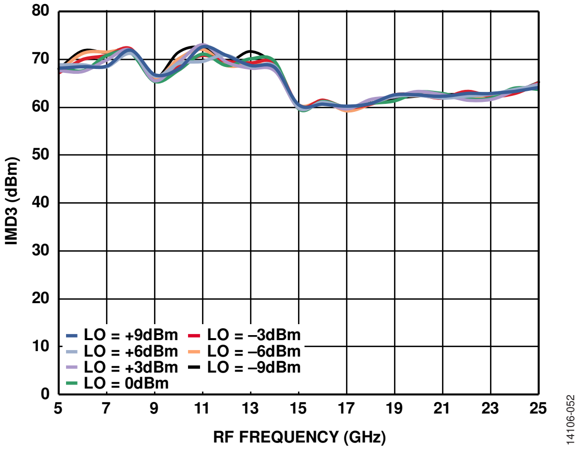


Figure 46. Third-Order Intermodulation Distortion (IMD3) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various LO Inputs, IF Amplitude = −15 dBm per Tone

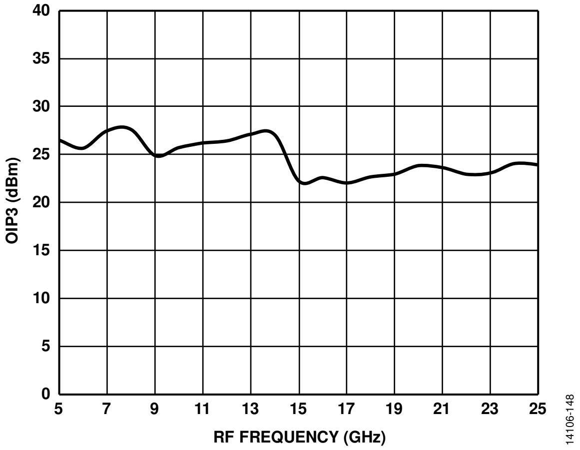


Figure 49. Output Third-Order Intercept (OIP3) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting, IF Amplitude = −15 dBm per Tone

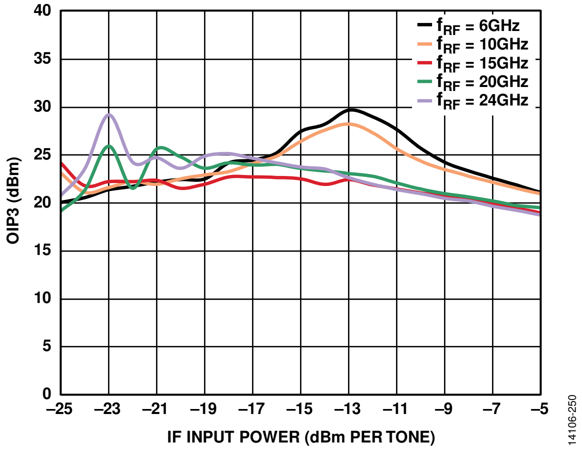


Figure 50. Output Third-Order Intercept (OIP3) vs. IF Input Power at a 7 dB Gain Setting for Various RF Frequencies (f_{RF})

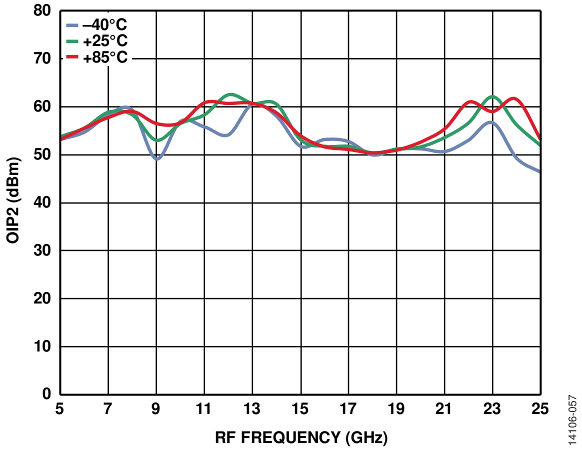


Figure 53. Output Second-Order Intercept (OIP2) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Temperatures, IF Amplitude = −15 dBm per Tone

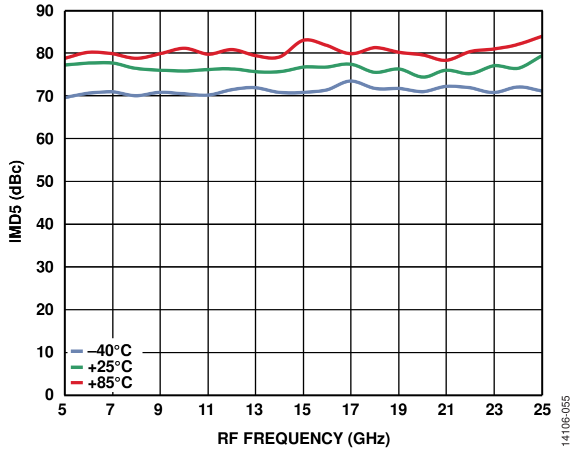


Figure 51. Fifth-Order Intermodulation Distortion (IMD5) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Temperatures, IF Amplitude = −15 dBm per Tone

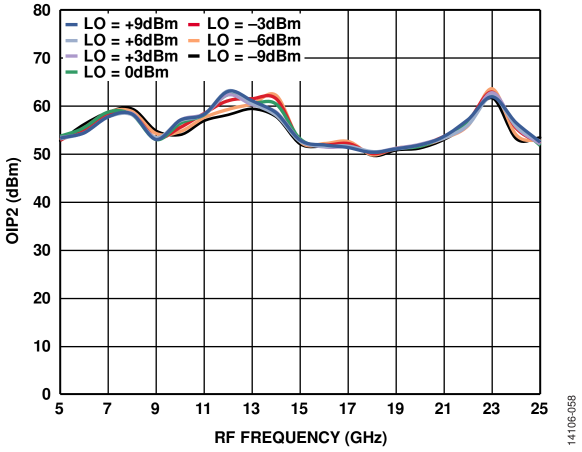


Figure 54. Output Second-Order Intercept (OIP2) vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various LO Inputs, IF Amplitude = −15 dBm per Tone

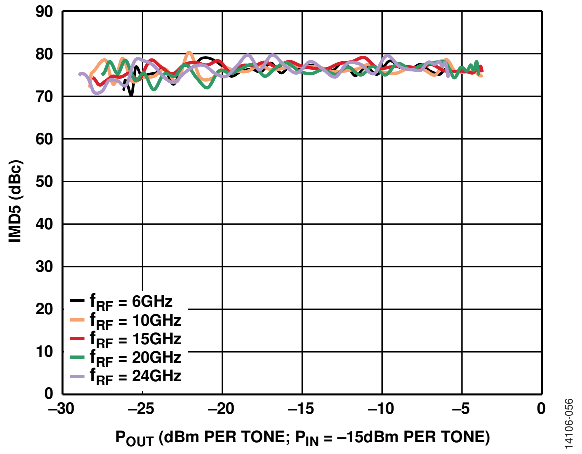


Figure 52. Fifth-Order Intermodulation Distortion (IMD5) vs. Output Power (P_{OUT}) for Various RF Frequencies (f_{RF}), IF Amplitude = −15 dBm per Tone

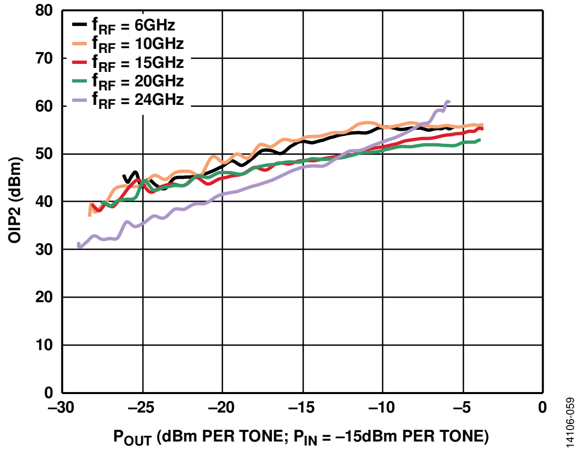


Figure 55. Output Second-Order Intercept (OIP2) vs. Output Power (P_{OUT}) for Various RF Frequencies (f_{RF}), IF Amplitude = −15 dBm per Tone

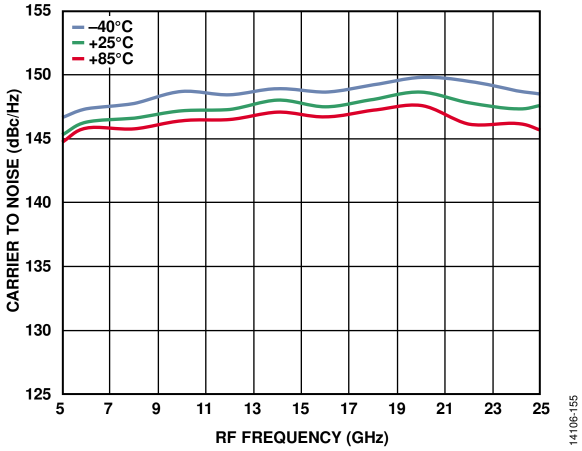


Figure 56. Output Noise Density vs. RF Frequency (f_{RF}) at a 7 dB Gain Setting for Various Temperatures with an Output Carrier of −5 dBm

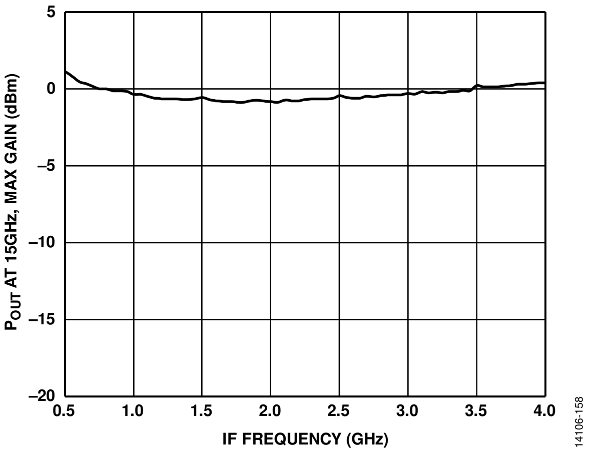


Figure 58. Bandwidth, P_{OUT} at 15 GHz and Maximum Gain Setting vs. IF Frequency (f_{IF})

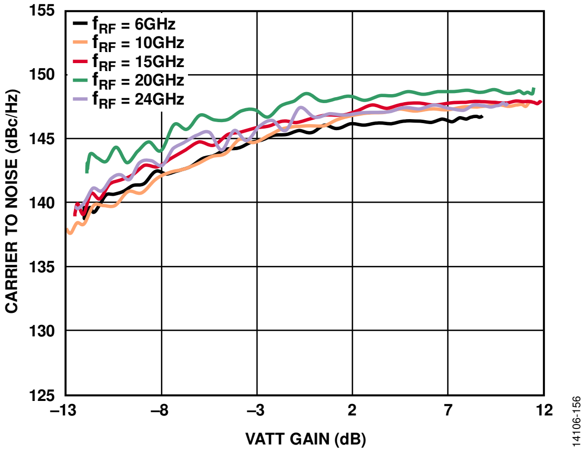


Figure 57. Output Noise Density vs. VATT Gain for Various RF Frequencies (f_{RF}) with an Input Carrier of −12 dBm

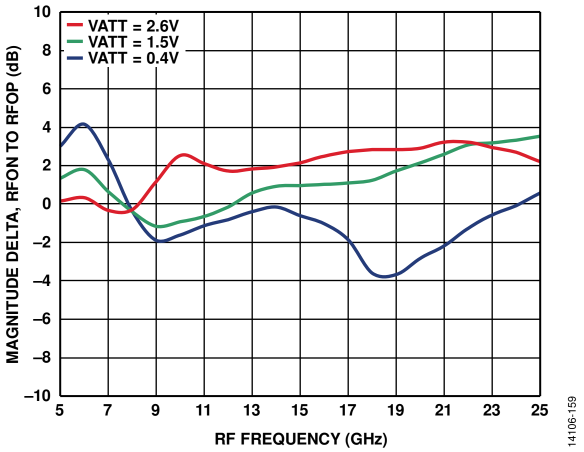


Figure 59. Magnitude Delta, RFON to RFOP vs. RF Frequency (f_{RF}) at Three Different Gain Settings

OUTPUT DETECTOR PERFORMANCE

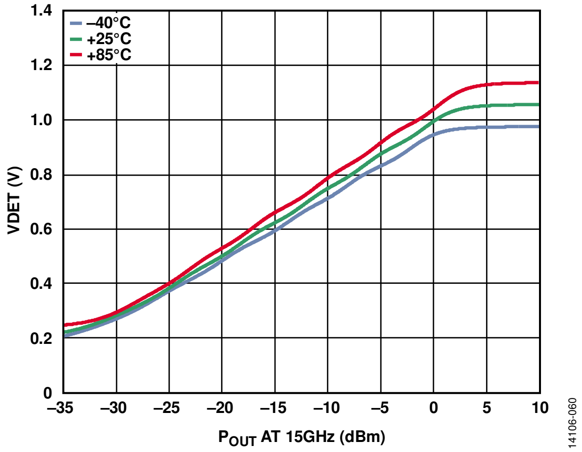


Figure 60. Detector Output (VDET) vs. Output Power (P_{OUT}) at 15 GHz for Various Temperatures

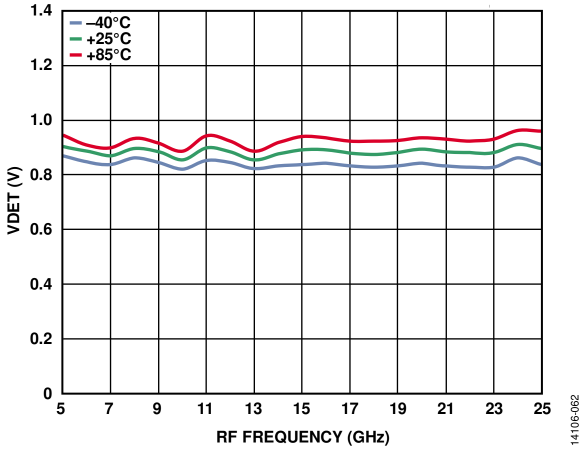


Figure 62. Detector Output (VDET) vs. RF Frequency (f_{RF}), –5 dBm Output Power (P_{OUT}) for Various Temperatures

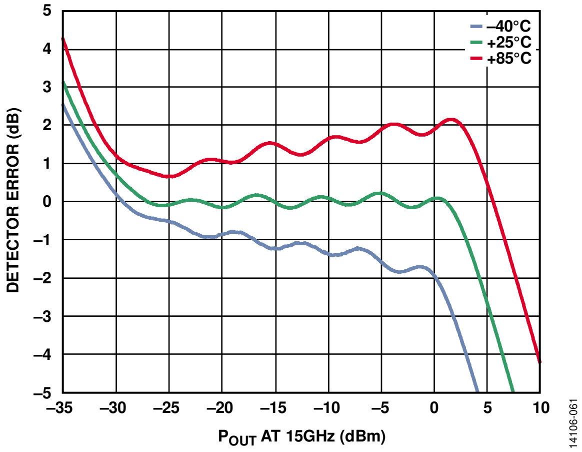


Figure 61. Detector Error vs. Output Power (P_{OUT}) at 15 GHz for Various Temperatures

RETURN LOSS

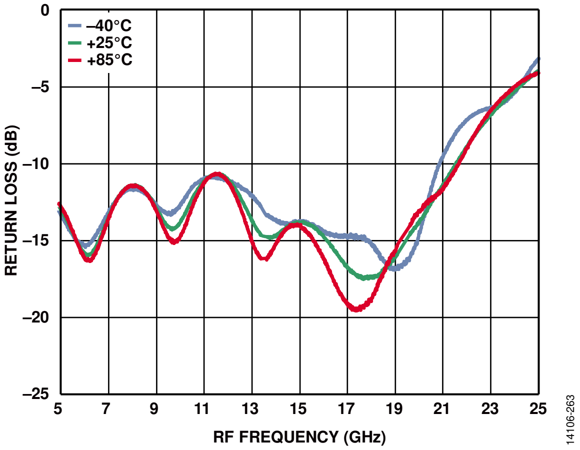


Figure 63. RF Output Return Loss S11 vs. RF Frequency for Various Temperatures

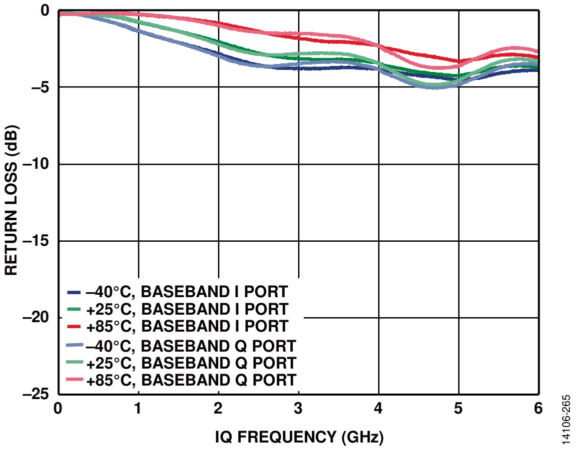


Figure 65. I/Q Input Return Loss S11 vs. I/Q Frequency for Various Temperatures

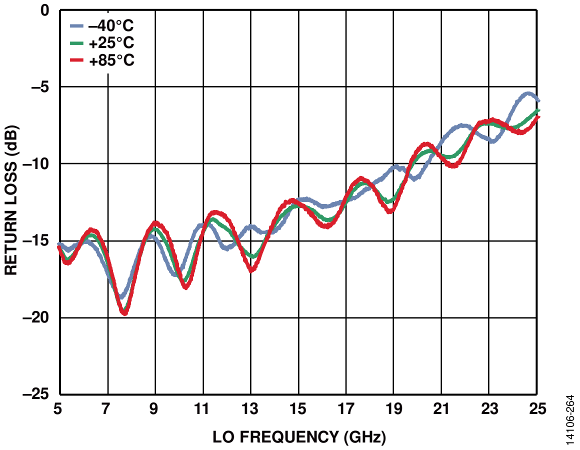


Figure 64. LO Input Return Loss S11 vs. LO Frequency for Various Temperatures

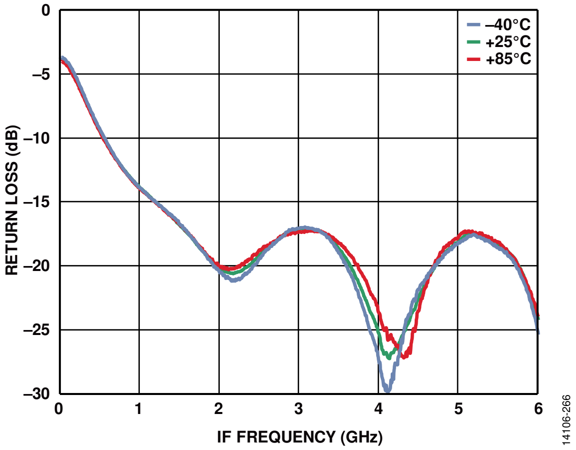


Figure 66. IF Input Return Loss S11 vs. IF Frequency for Various Temperatures

THEORY OF OPERATION

The ADRF6780 is a wideband microwave upconverter optimized for point to point microwave radio designs operating in the 5.9 GHz to 23.6 GHz frequency range. A functional block diagram of the device is shown in Figure 1. The ADRF6780 is programmed via an SPI.

BASEBAND

The input impedance of the basebands are high input impedance. These inputs are designed to operate with a 0.5 V common-mode voltage. These inputs are differentially terminated to a 100 Ω resistor using an off chip termination.

The linearity can be optimized by adding phase correction signals to the current output via adjusting the I_PATH_PHASE_ACCURACY register (Register 0x05, Bits[3:0]) and the Q_PATH_PHASE_ACCURACY (Register 0x05, Bits[7:4]) register.

SINGLE SIDEBAND (SSB) UPCONVERSION

The IF input path can be fed anywhere from 0.8 GHz to 3.5 GHz. The IF inputs path can be upconverted to 5.9 GHz to 23.6 GHz, while suppressing the unwanted sideband by typically better than 25 dBc. The IF upconversion inputs are 100 Ω differential and must be ac-coupled. In addition, the I/Q baseband input must stay floating without any termination on their inputs.

LO INPUT PATH

The LO input path operates from 5.4 GHz to 14 GHz with a LO amplitude range of −6 dBm to +6 dBm. It is built from two modes: ×1 mode (Register 0x03, Bit 2), which provides an LO output frequency equal to the LO input frequency, and ×2 mode (Register 0x03, Bit 3), which doubles the LO output frequency from the LO input frequency. Note that, when enabling the LO ×2 mode (Register 0x03, Bit 3), the LO ×1 mode (Register 0x03, Bit 2) must be disabled.

The LO path is designed to operate differentially. LOIP and LOIN are the inputs to the LO path. It is recommended to use the ADRF6780 with a LO differential input to acheive the best performance.

Figure 67 shows a block diagram of the LO path.

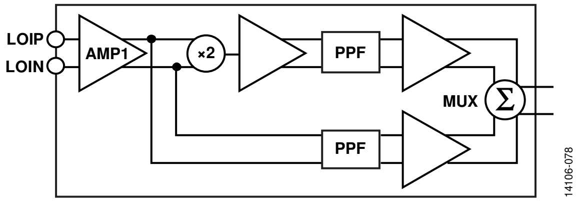


Figure 67. LO Path Block Diagram

SERIAL PORT INTERFACE (SPI)

The SPI of the ADRF6780 allows the user to configure the device for specific functions or operations via a 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDIN, SDTO, and $\overline{\text{SEN}}$.

The ADRF6780 protocol consists of a write/read bit followed by six register address bits, 16 data bits, and a parity bit. Both the address and data fields are organized MSB first and end with the least significant bit (LSB). For a write, set the first bit to 0, and for a read, set this bit to 1.

The write cycle sampling must be done on the rising edge. The 16 bits of the serial write data are shifted in, MSB to LSB. The ADRF6780 input logic level for the write cycle supports an 1.8 V interface.

For a read cycle, up to 16 bits of serial read data are shifted out, MSB first. After the 16 bits of data shift out, the parity bit shifts out. The output logic level for a read cycle is 1.8 V.

The parity bit always follows the direction of the data. If parity is not used, the transmitting end transmits zero instead of parity. The parity is odd, which means that the total number of ones transmitted during a command, including the read/write bit, the address bit, the data bit, and the parity bit, must be odd.

Table 5. Serial Port Register Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{DI, SETUP}$	Data to clock setup time	10			ns
$t_{DI, HOLD}$	Data to clock hold time	10			ns
$t_{CLK, HIGH}$	Clock high duration	40 to 60			%
$t_{CLK, LOW}$	Clock low duration	40 to 60			%
$t_{CLK, \overline{SEN}\_SETUP}$	Clock to $\overline{\text{SEN}}$ setup time	30			ns
$t_{CLK, DOT}$	Clock to data out transition time			10	ns
$t_{CLK, DOV}$	Clock to data out valid time			10	ns
$t_{CLK, \overline{SEN}\_INACTIVE}$	Clock to $\overline{\text{SEN}}$ inactive	20			ns
$t_{\overline{SEN}\_INACTIVE}$	Inactive $\overline{\text{SEN}}$ (between two operations)	80			ns

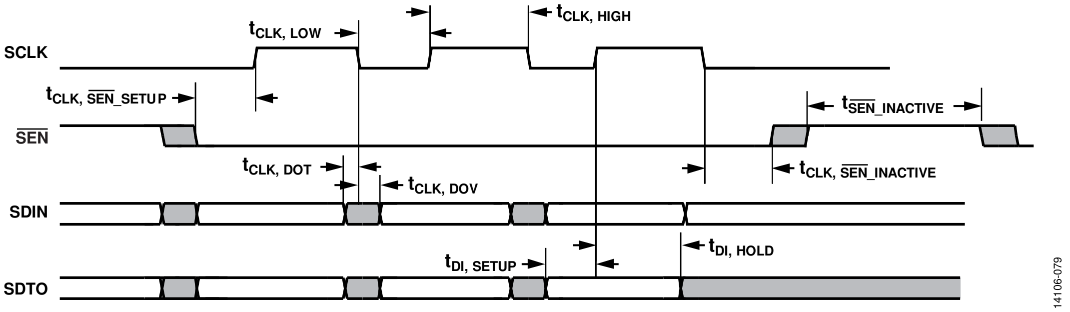


Figure 68. Serial Port Register Timing Diagram

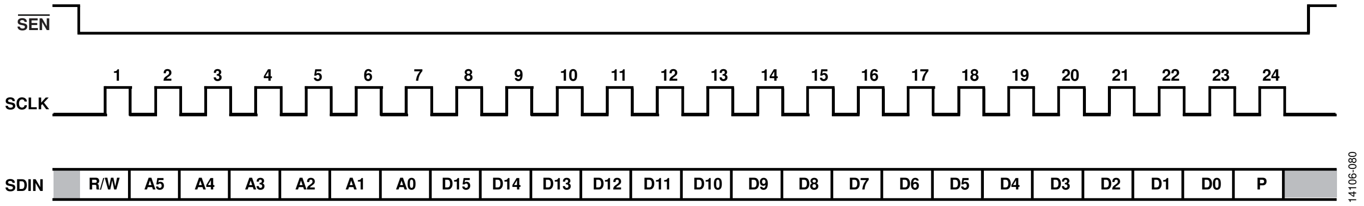


Figure 69. Write Serial Port Timing Diagram

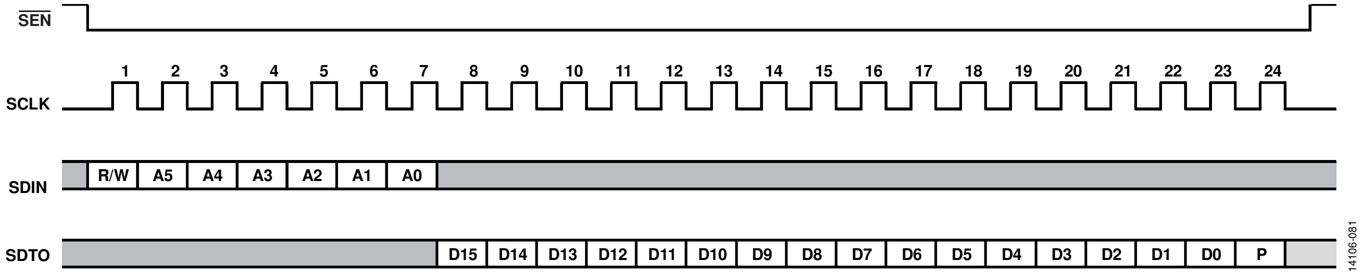


Figure 70. Read Serial Port Timing Diagram

APPLICATIONS INFORMATION

CARRIER FEEDTHROUGH NULLING

Carrier feedthrough results from minute dc offsets that occur on the differential baseband inputs. In an I/Q modulator, nonzero differential offsets mix with the LO and result in carrier feedthrough to the RF output. In addition to this effect, some of the signal power at the LO input couples directly to the RF output (this may be because of the bond wire to bond wire coupling or coupling through the silicon substrate). The net carrier feedthrough at the RF output is the vector combination of the signals that appear at the output because of these two effects. A TxDAC can externally accomplish carrier feedthrough nulling.

SIDEBAND SUPPRESSION OPTIMIZATION

Sideband results from gain and phase imperfections between the I and Q channels. Sideband also results from the quadrature error in generating the quadrature LO signals. Quadrature I and Q signals are constructed in the LO path, and the vector combination of these signals at the RF output results in suppression of the unwanted sideband. Deviation from perfect quadrature on these signals limits the amount of achievable sideband suppression.

The ADRF6780 offers quadrature phase adjustment in the LO path quadrature signals. Make these adjustments through the I_PATH_PHASE_ACCURACY bits (Register 0x05, Bits[3:0]) and Q_PATH_PHASE_ACCURACY (Register 0x05, Bits[7:4]) bits to reject the unwanted sideband signal.

Figure 14 shows the level of unwanted sideband signal achievable from the ADRF6780 across the I_PATH_PHASE_ACCURACY bits (Register 0x05, Bits[3:0]) and Q_PATH_PHASE_ACCURACY (Register 0x05, Bits[7:4]) bits.

If further optimization is needed, adjust the amplitude and phase externally through a TxDAC.

LINEARITY

The linearity in the ADRF6780 can be optimized through the distortion cancellation circuit that is set up by the RDAC_LINEARIZE bits (Register 0x04, Bits[7:0]) SPI settings. The distortion cancellation circuit connects in parallel with the baseband signal path in such a way that the fundamental is minimally affected whereas the third-order portions cancel to some degree. Adjusting the value of the RDAC_LINEARIZE bits (Register 0x04, Bits[7:0]) changes the resistance value in the cancellation path by fine tuning the amount of third-order destructively added to the main signal path. It also serves as a form or predistortion for third-order impedance generated further down in the signal path.

Figure 16 and Figure 44 show the level of linearity improvement achievable across the ADRF6780 RDAC_LINEARIZE bits.

ADC

The ADRF6780 includes an ADC that connects to a detector. The user has an option to read the detector output from the detector output pin (VDET, Pin 1) or using the ADC from the SPI. Figure 71 shows normal operation at I/Q mode, an RF output of 6.7 GHz, an I/Q input of 1 MHz, and a maximum gain. Figure 72 shows normal operation at IF mode and an RF output of 6.7 GHz, an IF input of 800 MHz, and a maximum gain.

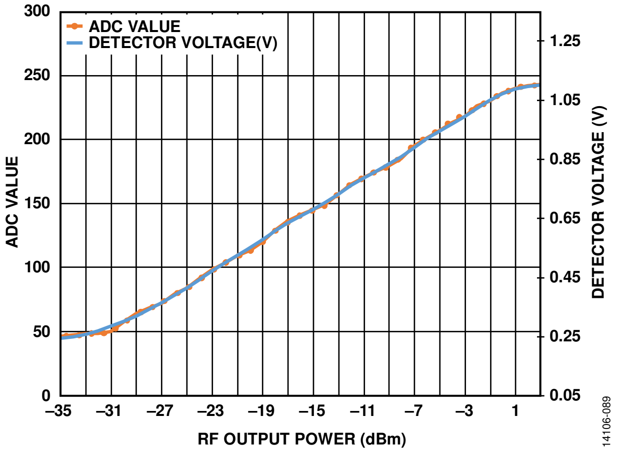


Figure 71. ADC Detector Output and Detector Output Power, I/Q Mode

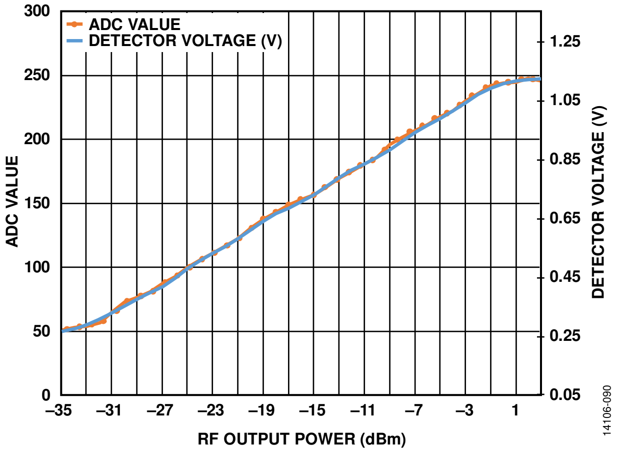


Figure 72. ADC Detector Output and Detector Output Power, IF Mode

To read back from the detector using the ADC, take the following steps.

1. Set Bit 7 of Register 0x03 to 1 (DETECTOR_ENABLE).
2. Set Bit 1 of Register 0x06 to 1 (ADC_ENABLE).
3. Set Bit 0 of Register 0x06 to 1 (ADC_CLOCK_ENABLE).
4. Set Bit 2 of Register 0x06 to 1 (ADC_START).
5. Wait 200 μs for the ADC to be ready.
6. Set Bit 8 of Register 0x0C to 1 (ADC_STATUS).
7. Set Bit 2 of Register 0x06 to 0 (ADC_START).
8. Set Bits[7:0] of Register 0x0C to read back the ADC value (ADC_VALUE). To read the ADC value, the ADC_CLOCK_ENABLE, ADC_ENABLE, and ADC_START bits must be enabled.

To disable the ADC, disable the ADC_CLOCK_ENABLE, ADC_ENABLE, and ADC_START bits.

WIDE FREQUENCY PERFORMANCE

Figure 73 and Figure 74 show the typical performance of the ADRF6780 when using values outside of the RF output frequency range. It is important to understand that this performance is typical and not guaranteed.

Figure 73 was tested in I/Q mode with an RF output frequency of 1 GHz to 31 GHz. The LO input frequency was switched to LO ×2 doubler mode above 14 GHz.

Figure 74 was tested in IF mode with an RF output frequency of 1 GHz to 31 GHz. The LO input frequency was switched to LO ×2 doubler mode above 14 GHz.

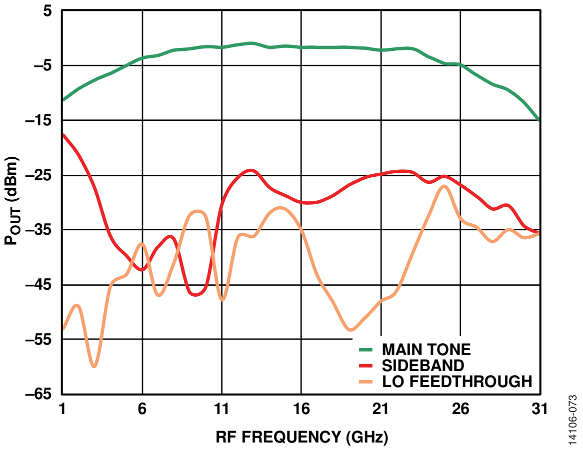


Figure 73. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) in I/Q Mode at the Maximum Gain Setting, BB I/Q Amplitude = −15 dBm

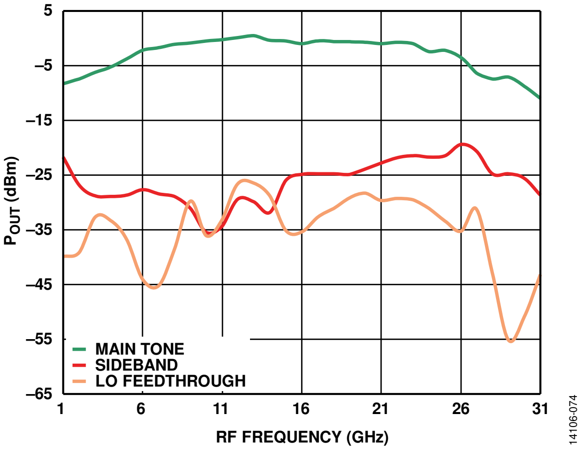


Figure 74. Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) in IF Mode at the Maximum Gain Setting, IF Amplitude = −12 dBm

LO Path ×1, ×2 Full Range

Figure 75 shows the typical performance of the ADRF6780 when the LO input frequency is used within the full frequency range. It is important to understand that this performance is typical and not guaranteed.

Figure 75 was tested with the LO path set to ×1 mode and ×2 mode with a 5.9 GHz to 23.6 GHz frequency range in I/Q mode. It is recommended to switch to LO ×2 doubler mode above 14 GHz to achieve better performance out of the device.

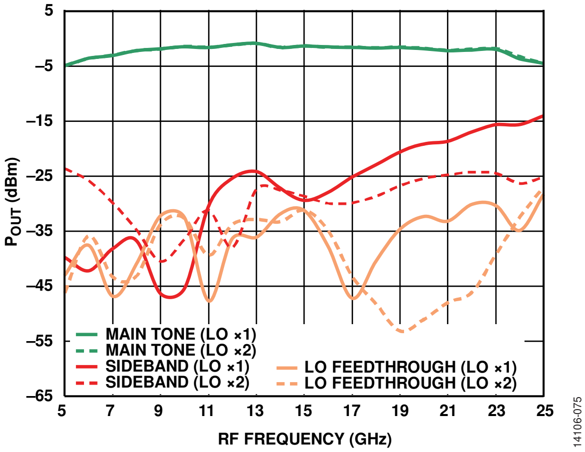


Figure 75. LO ×1 Mode and LO ×2 Mode, Output Power (P_{OUT}) vs. RF Frequency (f_{RF}) in I/Q Mode at the Maximum Gain Setting, BB I/Q Amplitude = −15 dBm

LAYOUT

Solder the exposed pad on the underside of the ADRF6780 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package.

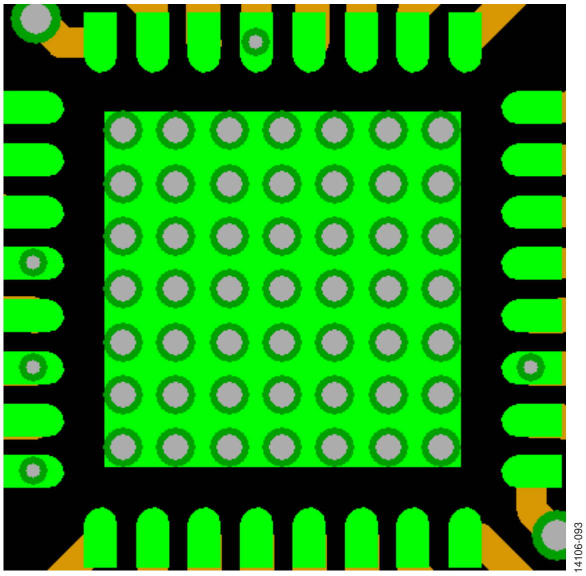


Figure 76. Evaluation Board Layout for the ADRF6780 Package