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750 MHz to 1150 MHz Quadrature Demodulator with Fractional-N PLL and VCO

ADRF6801

FEATURES

IQ demodulator with integrated fractional-N PLL
LO frequency range: 750 MHz to 1150 MHz
Input P1dB: 12.5 dBm
Input IP3: 25 dBm
Noise figure (DSB): 14.3 dB
Voltage conversion gain: 5.1 dB
Quadrature demodulation accuracy
Phase accuracy: 0.3°
Amplitude accuracy: 0.05 dB
Baseband demodulation: 275 MHz, 3 dB bandwidth
SPI serial interface for PLL programming
40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

QAM/QPSK RF/IF demodulators
Cellular W-CDMA/CDMA/CDMA2000
Microwave point-to-(multi)point radios
Broadband wireless and WiMAX

GENERAL DESCRIPTION

The ADRF6801 is a high dynamic range IQ demodulator with integrated PLL and VCO. The fractional-N PLL/synthesizer generates a frequency in the range of 3.0 GHz to 4.6 GHz. A divide-by-4 quadrature divider divides the output frequency of the VCO down to the required local oscillator (LO) frequency to drive the mixers in quadrature. Additionally, an output buffer can be enabled that generates an $f_{VCO}/2$ signal for external use.

The PLL reference input is supported from 10 MHz to 160 MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop filter. The loop filter output is then applied to an integrated VCO.

The IQ demodulator mixes the differential RF input with the complex LO derived from the quadrature divider. The differential I and Q output paths have excellent quadrature accuracy and can handle baseband signaling or complex IF up to 120 MHz.

The ADRF6801 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, exposed-paddle, RoHS-compliant, 6 mm × 6 mm LFCSP package. Performance is specified over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

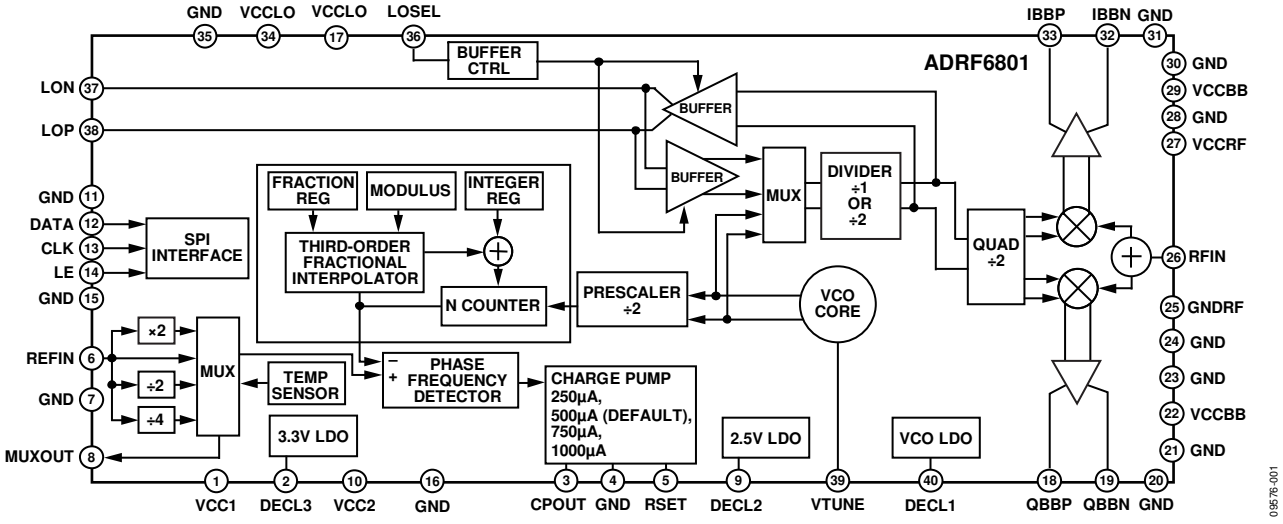

Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

ADRF6801* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6801 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6801: 750 MHz to 1150 MHz Quadrature Demodulator with Fractional-N PLL and VCO

SOFTWARE AND SYSTEMS REQUIREMENTS

- Windows 7 Drivers for the SPI Software

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE DESIGNS

- CN0320

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADRF6801 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6801 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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TABLE OF CONTENTS

REVISION HISTORY

1/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; ambient temperature (T_A) = 25°C; f_{REF} = 26 MHz, f_{LO} = 900 MHz, f_{BB} = 4.5 MHz, R_{LOAD} = 450 Ω differential, all register and PLL settings use the recommended values shown in the Register Structure section, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT AT 900 MHz	RFIN pins				
Internal LO Frequency Range	With VCO amplitude = 63 (R6 [DB15 to DB10])	750		1125	MHz
	With VCO amplitude = 24 (R6 [DB15 to DB10])	750		1150	MHz
Input Return Loss	Measured at 900 MHz		<−20		dB
Input P1dB			12.5		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each tone		>65		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each tone		25		dBm
Noise Figure	Double sideband from RF to either I or Q output		14.3		dB
	With a −10 dBm interferer 5 MHz away		18.9		dB
LO-to-RF Leakage	At 1×LO frequency, 50 Ω termination at the RF port		−75		dBm
I/Q BASEBAND OUTPUTS	IBBP, IBBN, QBBP, QBBN pins				
Voltage Conversion Gain	450 Ω differential load across IBBP, IBBN (or QBBP, QBBN)		5.1		dB
Demodulation Bandwidth	1 V p-p signal 3 dB bandwidth		275		MHz
Quadrature Phase Error			0.3		Degrees
I/Q Amplitude Imbalance			0.05		dB
Output DC Offset (Differential)			±5		mV
Output Common-Mode Voltage			V_{POS} − 2.4		V
Gain Flatness	Any 5 MHz (<100 MHz)		0.2		dB p-p
Maximum Output Swing	Differential 450 Ω load		4		V p-p
	Differential 200 Ω load		2.4		V p-p
Maximum Output Current	Each pin		12		mA p-p
LO INPUT/OUTPUT	LOP, LON				
Output Level	Into a differential 50 Ω load, LO buffer enabled (LO frequency = 900 MHz, output frequency = 1800 MHz)		−2.5		dBm
Input Level	Externally applied 2×LO, PLL disabled		0		dBm
Input Impedance	Externally applied 2×LO, PLL disabled		50		Ω
VCO Operating Frequency	With VCO amplitude = 63 (R6 [DB15 to DB10])	3000		4500	MHz
	With VCO amplitude = 24 (R6 [DB15 to DB10])	3000		4600	MHz
SYNTHESIZER SPECIFICATIONS	All synthesizer specifications measured with recommended settings provided in Figure 33 through Figure 39				
Channel Spacing	f_{PFD} = 26 MHz; modulus = 2047		25		kHz
PLL Bandwidth	Can be adjusted with off-chip loop filter component values and R_{SET}		130		kHz
SPURS	f_{LO} = 900 MHz, f_{REF} = 26 MHz, f_{PFD} = 26 MHz, measured at BB outputs with f_{BB} = 50 MHz				
Reference Spurs	f_{REF} = 26 MHz, f_{PFD} = 26 MHz		−91.6		dBc
	$f_{PFD}/2$		−107.8		dBc
	$f_{PFD} \times 2$		−89.1		dBc
	$f_{PFD} \times 3$		−94.2		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PHASE NOISE (USING 130 kHz LOOP FILTER)	f_{LO} = 900 MHz, f_{REF} = 26 MHz, f_{PFD} = 26 MHz, measured at BB outputs with f_{BB} = 50 MHz				
	1 kHz offset		−99.5		dBc/Hz
	10 kHz offset		−107.8		dBc/Hz
	100 kHz offset		−106.6		dBc/Hz
	500 kHz offset		−126.7		dBc/Hz
	1 MHz offset		−131.7		dBc/Hz
	5 MHz offset		−143.5		dBc/Hz
	10 MHz offset		−150.5		dBc/Hz
Integrated Phase Noise	1 kHz to 10 MHz integration bandwidth		0.16		°rms
PHASE NOISE (USING 2.5 kHz LOOP FILTER)	f_{LO} = 900 MHz, f_{REF} = 26 MHz, f_{PFD} = 26 MHz, measured at BB outputs with f_{BB} = 50 MHz				
	1 kHz offset		−71.3		dBc/Hz
	10 kHz offset		−88.3		dBc/Hz
	100 kHz offset		−114.1		dBc/Hz
	500 kHz offset		−129.5		dBc/Hz
	1 MHz offset		−138.6		dBc/Hz
	5 MHz offset		−150.2		dBc/Hz
	10 MHz offset		−150.3		dBc/Hz
PLL FIGURE OF MERIT (FOM)	Measured with f_{REF} = 26 MHz, f_{PFD} = 26 MHz		−215.4		dBc/Hz/Hz
	Measured with f_{REF} = 104 MHz, f_{PFD} = 26 MHz		−220.9		dBc/Hz/Hz
Phase Detector Frequency		20	26	40	MHz
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
REFIN Input Frequency	Usable range	10		160	MHz
REFIN Input Capacitance			4		pF
MUXOUT Output Level	V_{OL} (lock detect output selected)			0.25	V
	V_{OH} (lock detect output selected)	2.7			V
REFOUT Duty Cycle			50		%
CHARGE PUMP					
Pump Current			500		µA
Output Compliance Range		1		2.8	V
LOGIC INPUTS	CLK, DATA, LE pins				
Input High Voltage, V_{INH}		1.4		3.3	V
Input Low Voltage, V_{INL}		0		0.7	V
Input Current, I_{INH}/I_{INL}			0.1		µA
Input Capacitance, C_{IN}			5		pF
POWER SUPPLIES	VCC1, VCC2, VCCLO, VCCBB, VCCRF pins				
Voltage Range (5 V)		4.75	5	5.25	V
Supply Current (5 V)	Normal Rx mode, internal LO		262		mA
	Rx mode, internal LO with LO buffer enabled		288		mA
	Rx mode, using external LO input (internal VCO, PLL shut down)		157		mA
Supply Current (5 V)	Power-down mode		20		mA

TIMING CHARACTERISTICS

V_S = 5 V, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

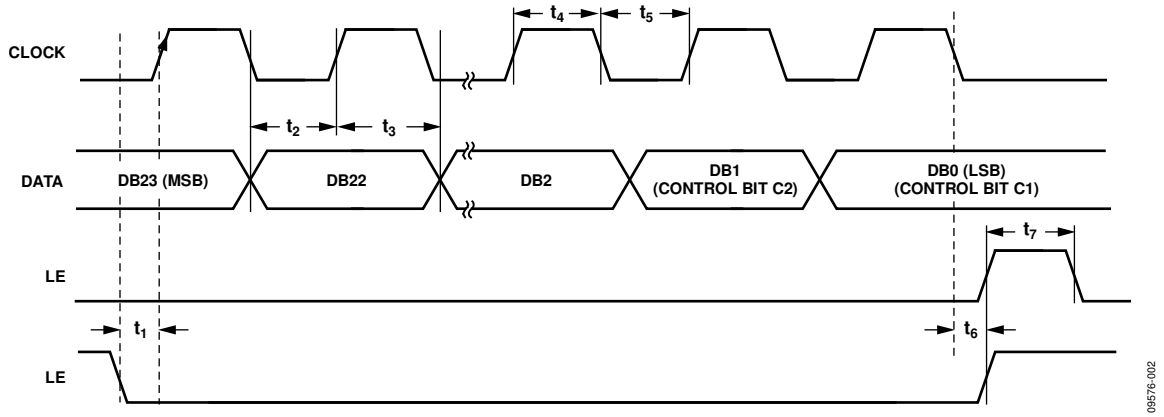

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VCC1, VCC2, VCCLO, VCCBB, and VCCRF (V_{S1})	−0.5 V to +5.5 V
Digital I/O, CLK, DATA, and LE	−0.3 V to +3.6 V
RFIN	16 dBm
θ_{JA} (Exposed Paddle Soldered Down)	30°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

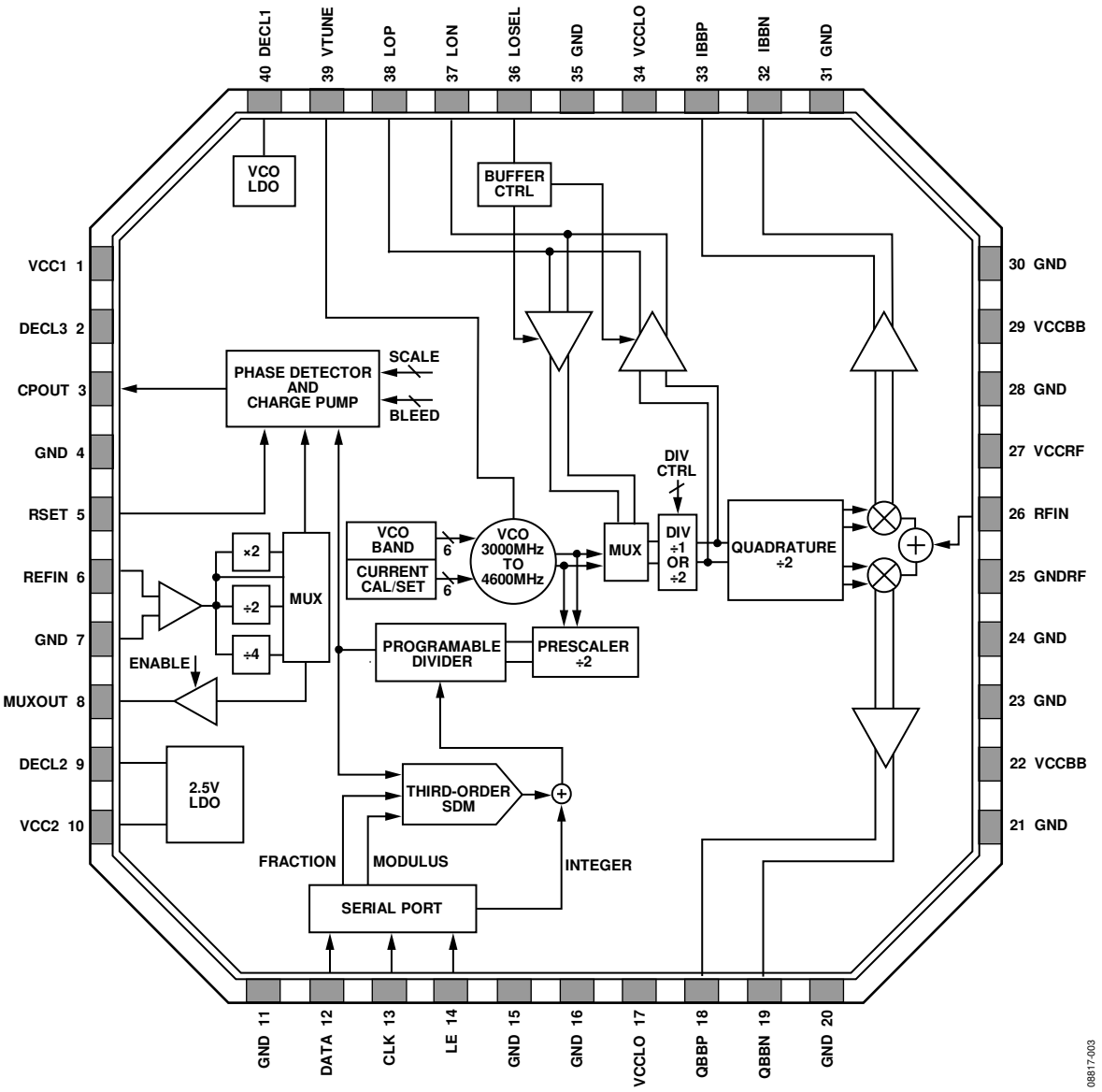

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC1	The 5 V Power Supply Pin for VCO and PLL (VCC1).
2	DECL3	Decoupling Node for the 3.3 V LDO. Connect a 0.1 µF capacitor between this pin and ground.
3	CPOUT	Charge Pump Output Pin. Connect this pin to VTUNE through the loop filter.
4, 7, 11, 15, 16, 20, 21, 23, 24, 28, 30, 31, 35	GND	Connect these pins to a low impedance ground plane.

Pin No.	Mnemonic	Description
5	RSET	Charge Pump Current. The nominal charge pump current can be set to 250 µA, 500 µA, 750 µA, or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (internal reference current). In this mode, no external R_{SET} is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the following equation where the resulting value is in units of ohms. $$R_{SET} = \left[\frac{217.4 \times I_{CP}}{I_{NOMINAL}} \right] - 37.8$$
6	REFIN	Reference Input. Nominal input level is 1 V p-p. Input range is 10 MHz to 160 MHz.
8	MUXOUT	Multiplexer Output. This output can be programmed to provide the reference output signal or the lock detect signal. The output is selected by programming the appropriate register.
9	DECL2	Decoupling Node for 2.5 V LDO. Connect a 0.1 µF capacitor between this pin and ground.
10	VCC2	The 5 V power supply pin for the 2.5 V LDO.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits.
13	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.
14	LE	Load Enable. When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word.
17, 34	VCCLO	The 5 V Power Supply for the LO Path Blocks.
18, 19	QBBP, QBBN	Demodulator Q-Channel Differential Baseband Outputs; Differential Output Impedance of 24 Ω.
22, 29	VCCBB	The 5 V Power Supply for the Baseband Output Section of the Demodulator Blocks.
25	GNDRF	Ground Return for RF Input Balun.
26	RFIN	Single-Ended, Ground Referenced 50 Ω, RF Input.
27	VCCRF	The 5 V Power Supply for the RF Input Section of the Demodulator Blocks.
32, 33	IBBN, IBBP	Demodulator I-Channel Differential Baseband Outputs; Differential Output Impedance of 24 Ω.
36	LOSEL	LO Select. Connect this pin to ground for the simplest operation and to completely control the LO path and input/output direction from the register SPI programming. For additional control without register reprogramming, this input pin can determine whether the LOP and LON pins operate as inputs or outputs. LOP and LON become inputs if the LOSEL pin is set low, the LDRV bit of Register 5 is set low, and the LXL bit of Register 5 is set high. The externally applied LO drive must be at 2×LO frequency (and the LDIV bit of Register 5 (DB5) set low). LON and LOP become outputs when LOSEL is high or if the LDRV bit of Register 5 (DB3) is set high and the LXL bit of Register 5 (DB4) is set low. The output frequency is 2×LO frequency (and the LDIV bit of Register 5 (DB5) must be set high). This pin should not be left floating.
37, 38	LON, LOP	Local Oscillator Input/Output. When these pins are used as output pins, a differential frequency divided version of the internal VCO is available on these pins. When the internal LO generation is disabled, an external M×LO frequency signal can be applied to these pins (where M corresponds to the LO path divider setting). (Differential Input/Output Impedance of 50 Ω)
39	VTUNE	VCO Control Voltage Input. This pin is driven by the output of the loop filter. The nominal input voltage range on this pin is 1.0 V to 2.8 V.
40	DECL1	Connect a 10 µF capacitor between this pin and ground as close to the device as possible because this pin serves as the VCO supply and loop filter reference.
	EP	Exposed Paddle. The exposed paddle should be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, unless otherwise noted. LO = 750 MHz to 1150 MHz.

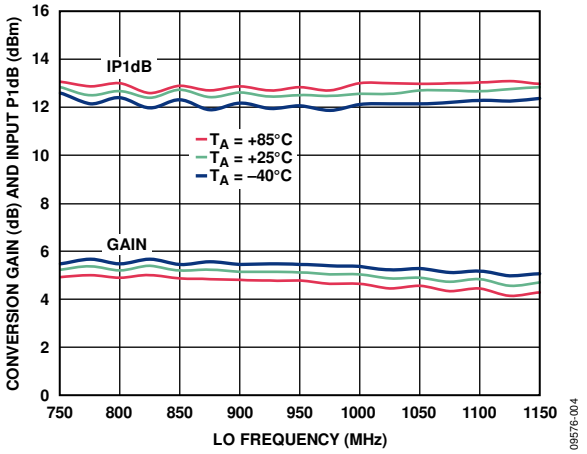

Figure 4. Conversion Gain and Input P1dB vs. LO Frequency

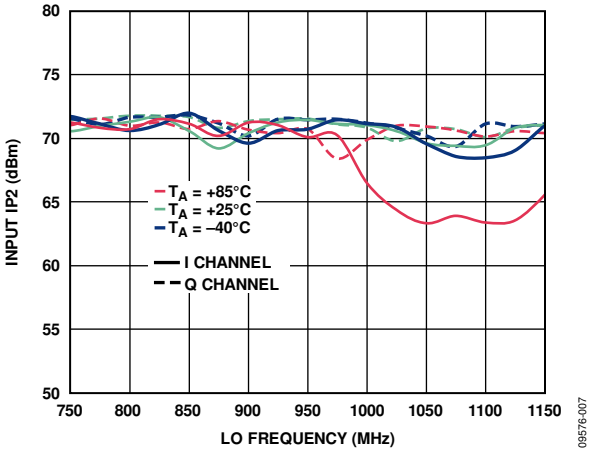

Figure 7. Input IP2 vs. LO Frequency

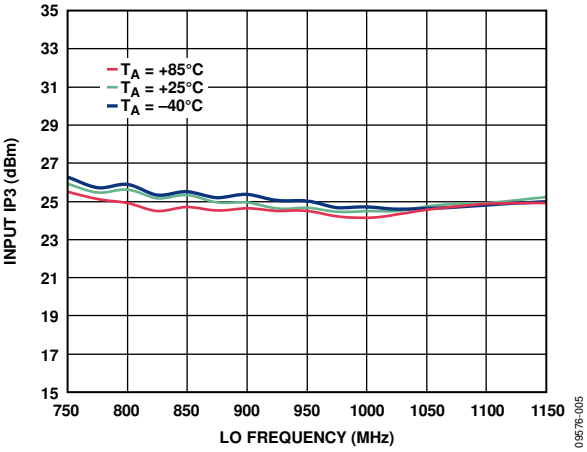

Figure 5. Input IP3 vs. LO Frequency

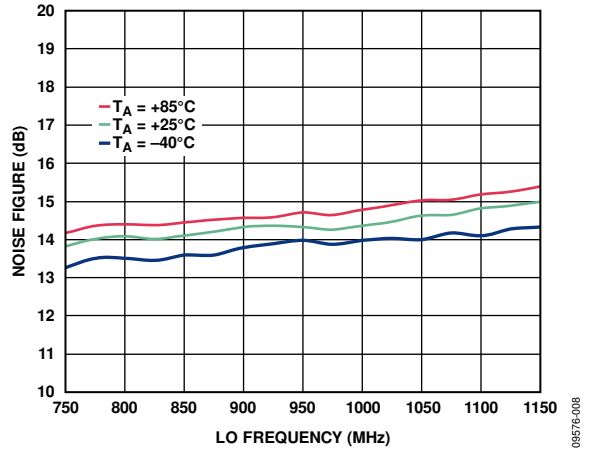

Figure 8. Noise Figure vs. LO Frequency

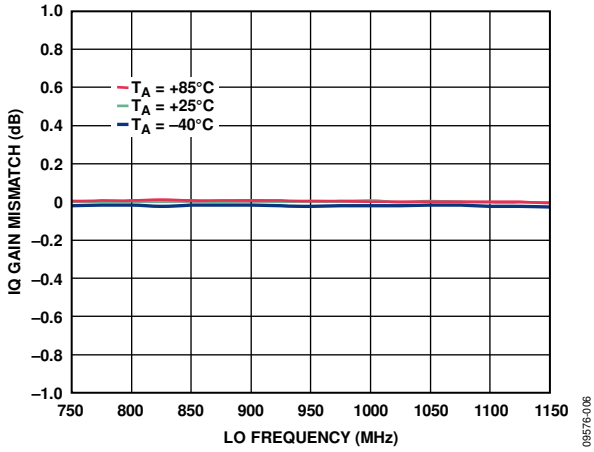

Figure 6. IQ Gain Mismatch vs. LO Frequency

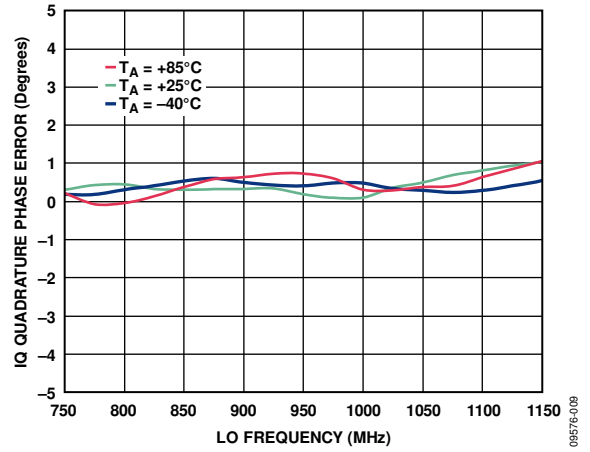

Figure 9. IQ Quadrature Phase Error vs. LO Frequency

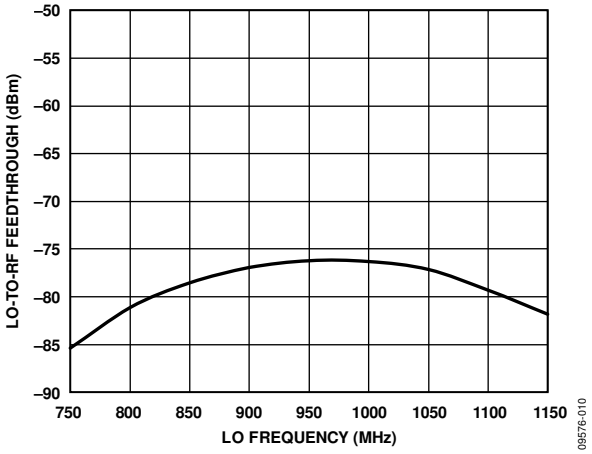

Figure 10. LO-to-RF Feedthrough vs. LO Frequency, LO Output Turned Off

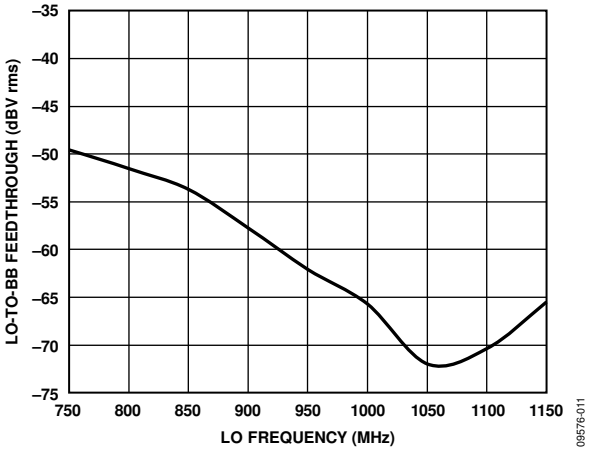

Figure 11. LO-to-BB Feedthrough vs. LO Frequency, LO Output Turned Off

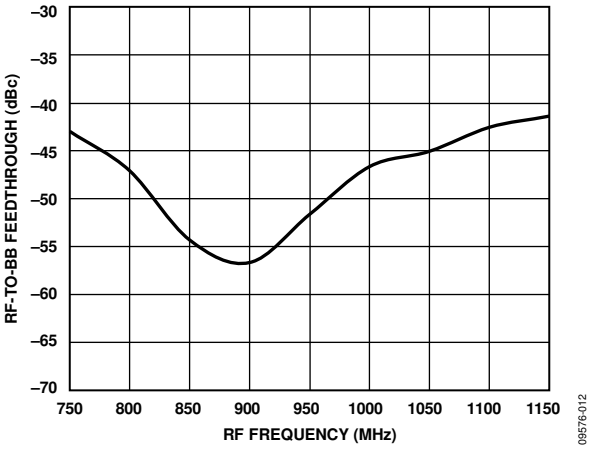

Figure 12. RF-to-BB Feedthrough vs. RF Frequency

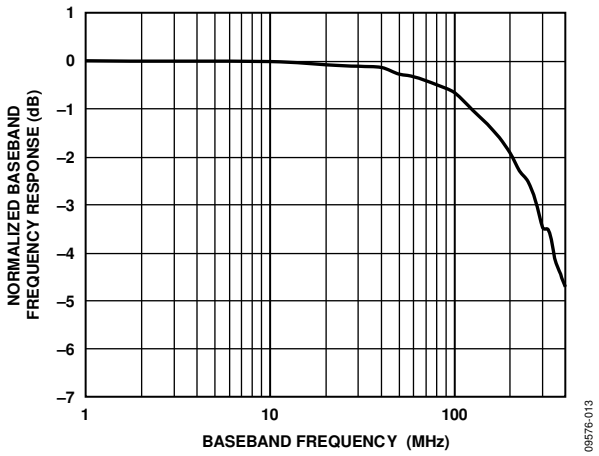

Figure 13. Normalized Baseband Frequency Response vs. Baseband Frequency

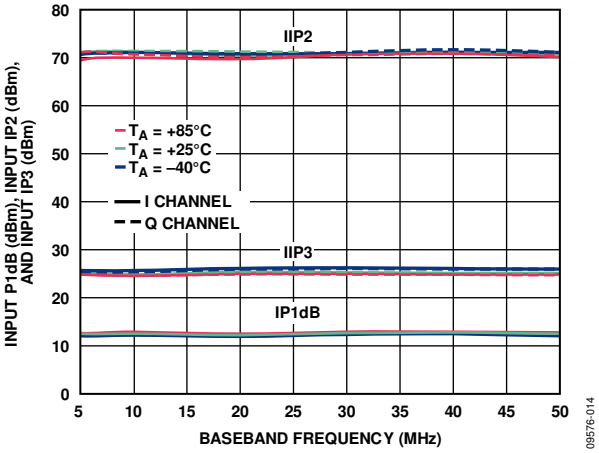

Figure 14. Input P1dB, Input IP2, and Input IP3 vs. Baseband Frequency

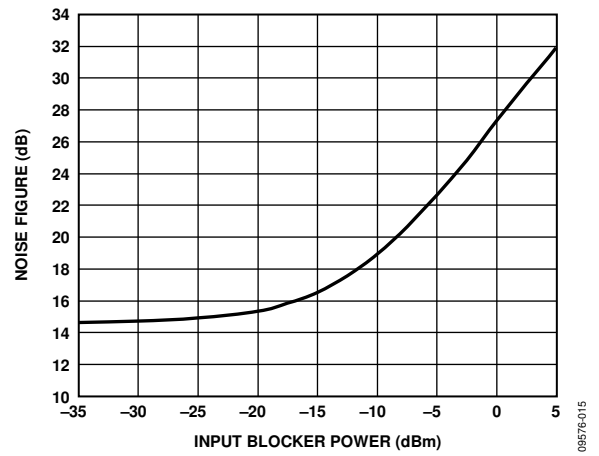

Figure 15. Noise Figure vs. Input Blocker Level, f_{LO} = 900 MHz (RF Blocker 5 MHz Offset)

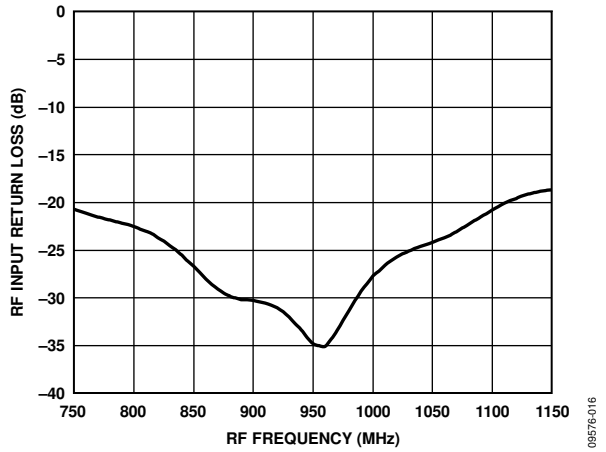

Figure 16. RF Input Return Loss vs. RF Frequency

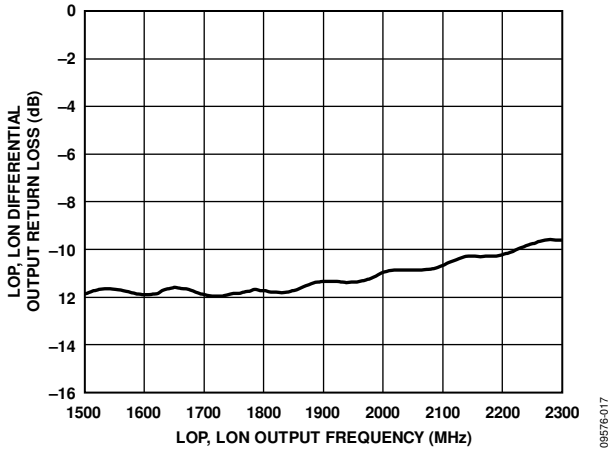

Figure 17. LO Output Return Loss vs. LO Output Frequency, LO Output Enabled (1500 MHz to 2300 MHz), Measured through TC1-1-13 Balun

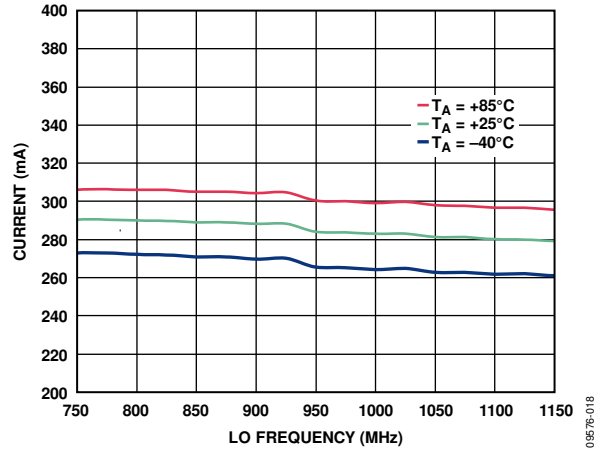

Figure 18. 5 V Supply Currents vs. LO Frequency, LO Output Enabled

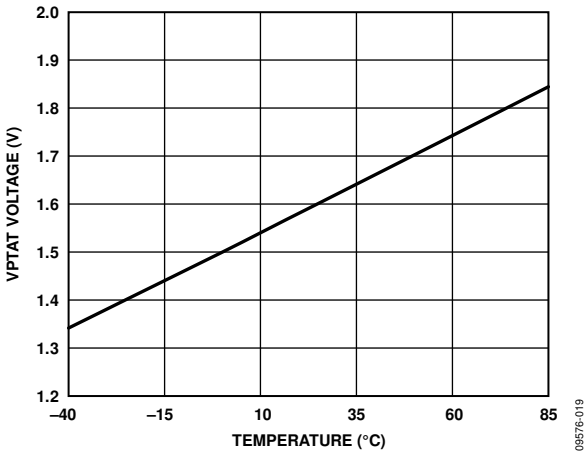

Figure 19. VPTAT vs. Temperature

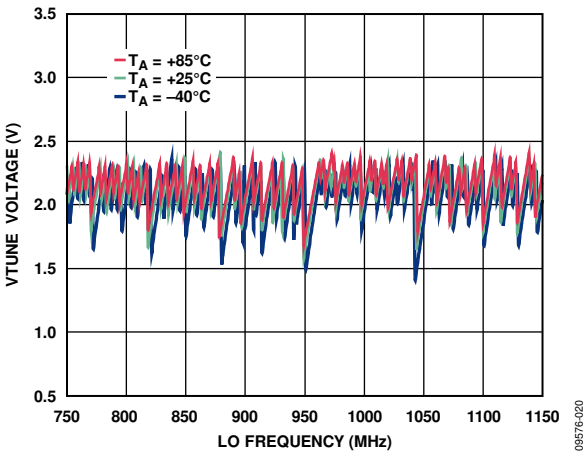

Figure 20. VTUNE vs. LO Frequency

SYNTHESIZER/PLL

V_S = 5 V. See the Register Structure section for recommended settings used. External loop filter bandwidths of ~130 kHz and 2.5 kHz used (see plots within this section for annotations), $f_{REF} = f_{PFD}$ = 26 MHz, measured at BB output, f_{BB} = 50 MHz, unless otherwise noted.

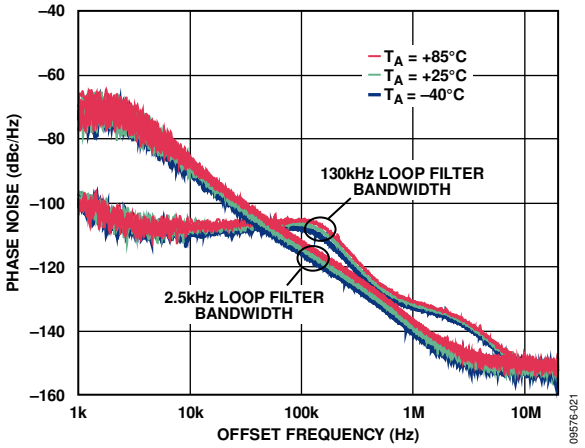

Figure 21. Phase Noise vs. Offset Frequency, f_{LO} = 900 MHz, Shown for Loop Filter Bandwidths of 2.5 kHz and 130 kHz

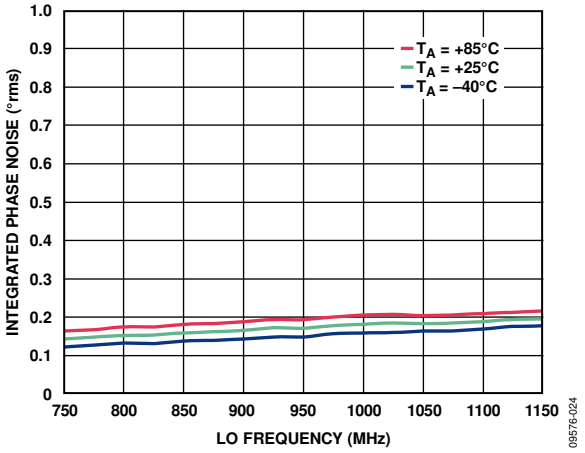

Figure 24. Integrated Phase Noise vs. LO Frequency (Spurs Omitted), Using Loop Filter Bandwidth of 130 kHz

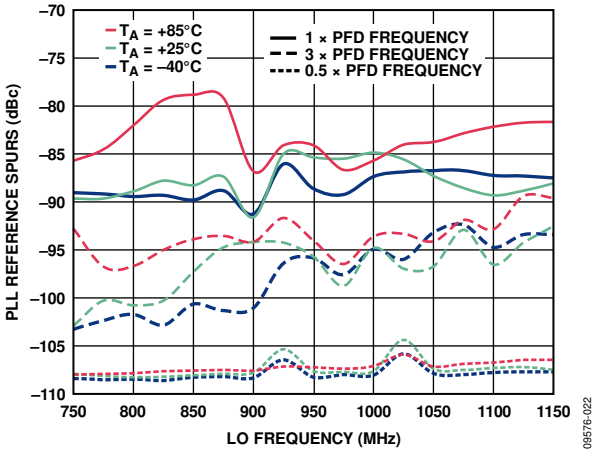

Figure 22. PLL Reference Spurs vs. LO Frequency, Using Loop Filter Bandwidth of 130 kHz

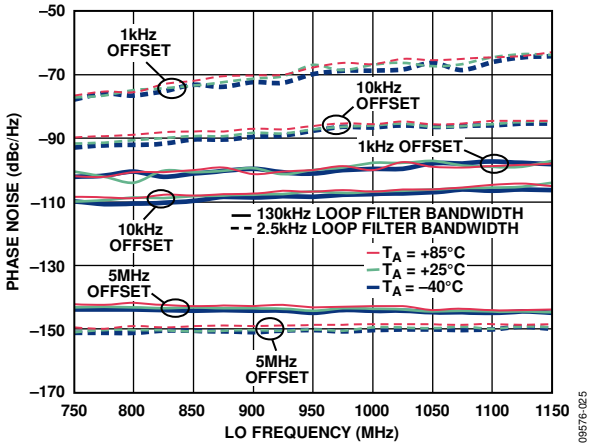

Figure 25. Phase Noise vs. LO Frequency (1 kHz, 10 kHz, and 5 MHz Offsets), Shown for Loop Filter Bandwidths of 2.5 kHz and 130 kHz

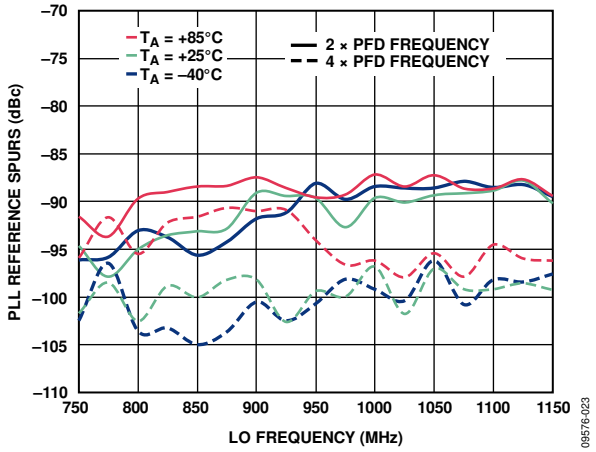

Figure 23. PLL Reference Spurs vs. LO Frequency, Using Loop Filter Bandwidth of 130 kHz

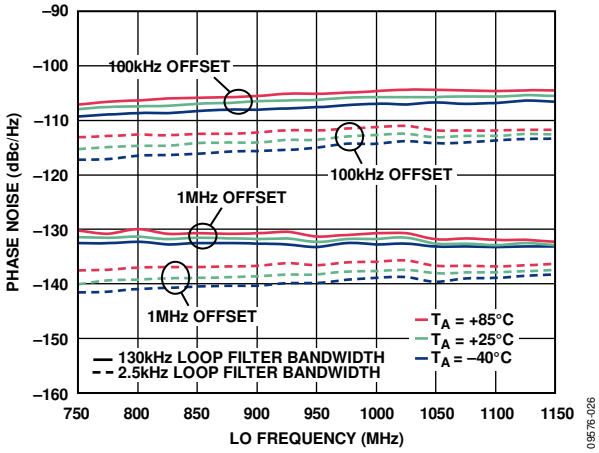

Figure 26. Phase Noise vs. LO Frequency (100 kHz and 1 MHz Offsets), Shown for Loop Filter Bandwidths of 2.5 kHz and 130 kHz

COMPLEMENTARY CUMULATIVE DISTRIBUTION FUNCTIONS (CCDF)

V_S = 5 V, f_{LO} = 900 MHz, f_{BB} = 4.5 MHz.

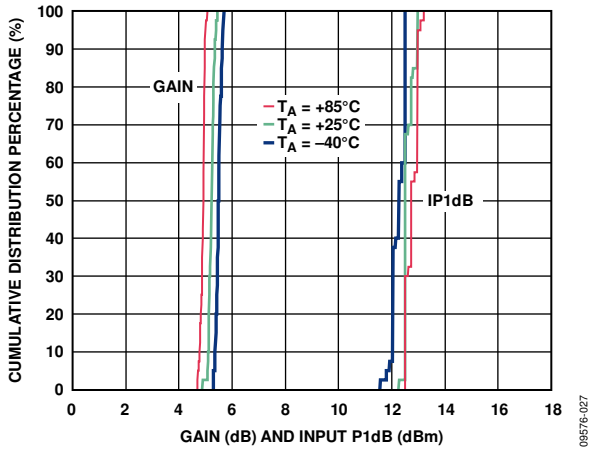

Figure 27. Gain and Input P1dB

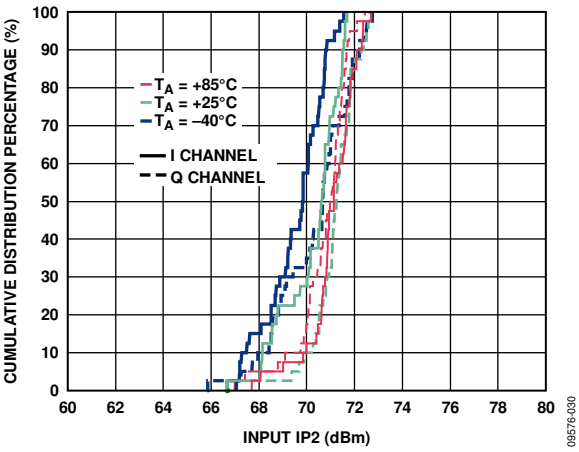

Figure 30. Input IP2

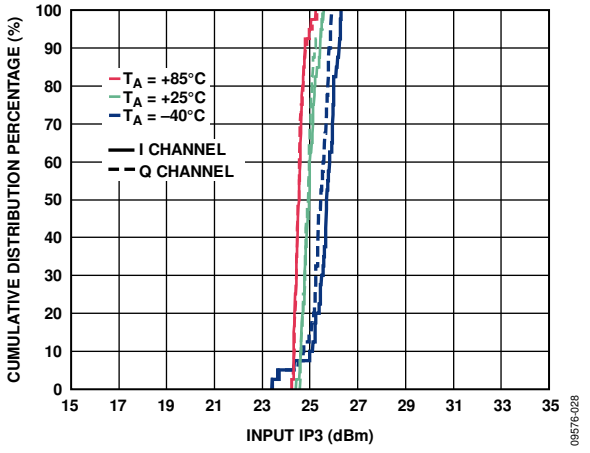

Figure 28. Input IP3

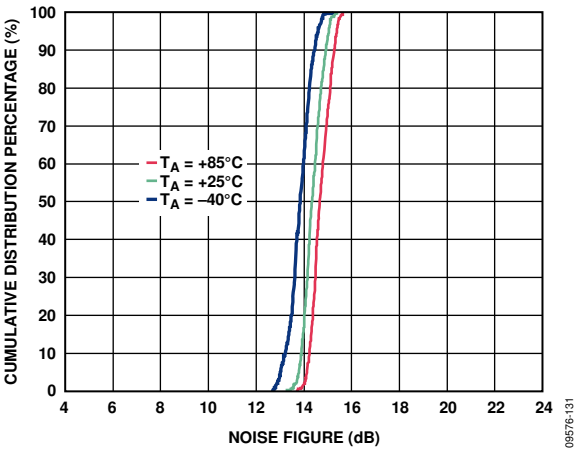

Figure 31. Noise Figure

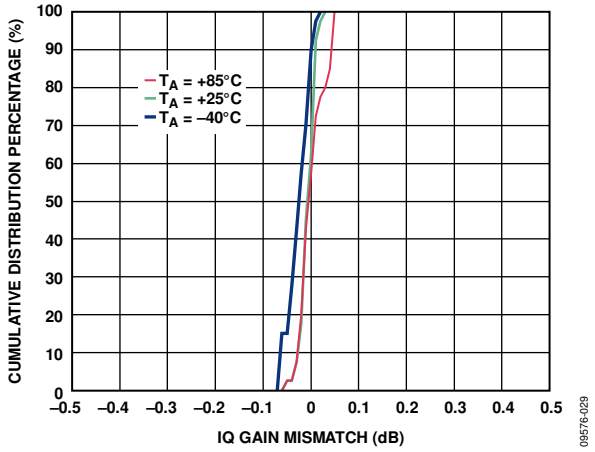

Figure 29. IQ Gain Mismatch

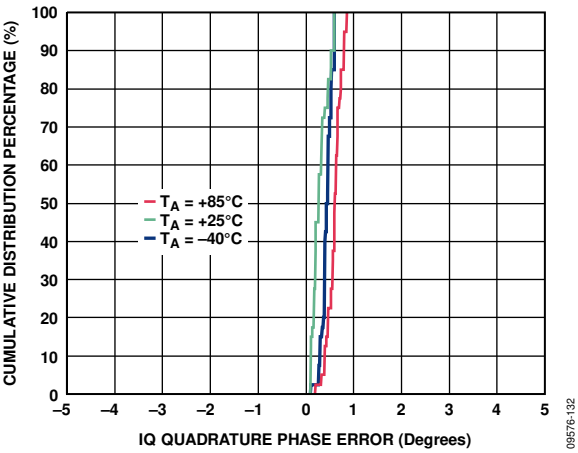

Figure 32. IQ Quadrature Phase Error

CIRCUIT DESCRIPTION

The ADRF6801 integrates a high performance IQ demodulator with a state-of-the-art fractional-N PLL. The PLL also integrates a low noise VCO. The SPI port allows the user to control the fractional-N PLL functions, the demodulator LO divider functions, and optimization functions, as well as allowing for an externally applied LO.

The ADRF6801 uses a high performance mixer core that results in an exceptional input IP3 and input P1dB, with a very low output noise floor for excellent dynamic range.

LO QUADRATURE DRIVE

A signal at 2× the desired mixer LO frequency is delivered to a divide-by-2 quadrature phase splitter followed by limiting amplifiers which then drive the I and Q mixers, respectively.

V-TO-I CONVERTER

The RF input signal is applied to an on-chip balun which then provides both a ground referenced, 50 Ω single-ended input impedance and a differential voltage output to a V-to-I converter that converts the differential voltages to differential output currents. These currents are then applied to the emitters of the Gilbert cell mixers.

MIXERS

The ADRF6801 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off chip. The output impedance is set by on-chip 12 Ω series resistors that yield a 24 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has ~0.5 dB lower effective gain than with a high (10 kΩ) differential load impedance.

The common-mode dc output levels of the emitter followers are set from VCCBB via the voltage drop across the mixer load resistors, the V_{BE} of the output emitter follower, and the voltage drop across the 12 Ω series resistor.

BIAS CIRCUITRY

There are several band gap reference circuits and three low dropout regulators (LDOs) in the ADRF6801 that generate the reference currents and voltages used by different sections. The first of the LDOs is the 2.5 V LDO, which is always active and provides the 2.5 V supply rail used by the internal digital logic blocks. The 2.5 V LDO output is connected to DECL2 (Pin 9) for the user to provide external decoupling.

The second LDO is the VCO LDO, which acts as the positive supply rail for the internal VCO. The VCO LDO output is connected to DECL2 (Pin 40) for the user to provide external decoupling. The VCO LDO can be powered down by setting Register 6, DB18 = 0, which allows the user to save power when not using the VCO.

The third LDO is the 3.3 V LDO, which acts as the 3.3 V positive supply rail for the reference input, phase frequency detector, and charge pump circuitry. The 3.3 V LDO output is connected to DECL3 (Pin 2) for the user to provide external decoupling. The 3.3 V LDO can be powered down by setting Register 6, DB19 = 0, which allows the user to save power when not using the VCO. The demodulator also has a bias circuit that supplies bias current for the mixer V-to-I stage, which then sets the bias for the mixer core. The demodulator bias cell can also be shut down by setting Register 5, DB7 = 0.

REGISTER STRUCTURE

The ADRF6801 provides access to its many programmable features through a 3-wire SPI control interface that is used to program the seven internal registers. The minimum delay and hold times are shown in the timing diagram (see Figure 2). The SPI provides digital control of the internal PLL/VCO as well as several other features related to the demodulator core, on-chip referencing, and available system monitoring functions. The MUXOUT pin provides a convenient, single-pin monitor output signal that can be used to deliver a PLL lock-detect signal or an internal voltage proportional to the local junction temperature.

Note that internal calibration for the PLL must run when the ADRF6801 is initialized at a given frequency. This calibration is run automatically whenever Register 0, Register 1, or Register 2 is programmed. Because the other registers affect PLL performance, Register 0, Register 1, and Register 2 must always be programmed last. For ease of use, starting the initial programming with Register 7 and then programming the registers in descending order, ending with Register 0, is recommended. Once the PLL and other settings are programmed, the user can change the PLL frequency simply by programming Register 0, Register 1, or Register 2 as necessary.

													DIVIDE MODE	INTEGER DIVIDE RATIO							CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

DM	DIVIDE MODE
0	FRACTIONAL (DEFAULT)
1	INTEGER

ID6	ID5	ID4	ID3	ID2	ID1	ID0	DIVIDE RATIO
0	0	1	0	1	0	1	21 (INTEGER MODE ONLY)
0	0	1	0	1	1	0	22 (INTEGER MODE ONLY)
0	0	1	0	1	1	1	23 (INTEGER MODE ONLY)
0	0	1	1	0	0	0	24
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
0	1	1	1	0	0	0	56 (DEFAULT)
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
1	1	1	0	1	1	1	119
1	1	1	1	0	0	0	120 (INTEGER MODE ONLY)
1	1	1	1	0	0	1	121 (INTEGER MODE ONLY)
1	1	1	1	0	1	0	122 (INTEGER MODE ONLY)
1	1	1	1	0	1	1	123 (INTEGER MODE ONLY)

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Figure 33. Integer Divide Control Register (R0)

Register 0—Integer Divide Control

With R0[2:0] set to 000, the on-chip integer divide control register is programmed as shown in Figure 33. The internal VCO frequency (f_{VCO}) equation is

$$f_{VCO} = f_{PFD} \times (INT + (FRAC/MOD)) \times 2 \quad (1)$$

where:
f_{VCO} is the output frequency of the internal VCO.
INT is the preset integer divide ratio value (21 to 123 for integer mode, 24 to 119 for fractional mode).
MOD is the preset fractional modulus (1 to 2047).
FRAC is the preset fractional divider ratio value (0 to MOD − 1).

The integer divide ratio sets the INT value in Equation 1. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency.

Note that the demodulator LO frequency is given by $f_{LO} = f_{VCO}/4$.

Divide Mode

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the VCO output frequency, f_{VCO}, is calculated by

$$f_{VCO} = f_{PFD} \times (INT) \times 2 \quad (2)$$

Register 1—Modulus Divide Control

With R1[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in Figure 34. The MOD value is the preset fractional modulus ranging from 1 to 2047.

										MODULUS DIVIDE RATIO											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	MODULUS VALUE
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	0	0	0	0	0	0	0	0	0	1536 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	2047

09576-032

Figure 34. Modulus Divide Control Register (R1)

Register 2—Fractional Divide Control

With R2[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in Figure 35. The FRAC value is the preset fractional modulus ranging from 0 to MOD − 1.

										FRACTIONAL DIVIDE RATIO											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	FRACTIONAL VALUE
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
0	1	1	0	0	0	0	0	0	0	0	768 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
FRACTIONAL VALUE MUST BE LESS THAN MODULUS											<MOD

09576-033

Figure 35. Fractional Divide Control Register (R2)

Register 3—Σ-Δ Modulator Dither Control

With R3[2:0] set to 011, the on-chip Σ-Δ modulator dither control register is programmed as shown in Figure 36. The dither restart value can be programmed from 0 to 217 to 1, though a value of 1 is typically recommended.

	DITHER MAGNITUDE		DITHER ENABLE	DITHER RESTART VALUE																	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DEN	DITHER ENABLE
0	DISABLE
1	ENABLE (DEFAULT, RECOMMENDED)

DITH1	DITH0	DITHER MAGNITUDE
0	0	15 (DEFAULT)
0	1	7
1	0	3
1	1	1 (RECOMMENDED)

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	DITHER RESTART VALUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

09576-034

Figure 36. Σ-Δ Modulator Dither Control Register (R3)

Register 4—Charge Pump, PFD, and Reference Path Control

With R4[2:0] set to 100, the on-chip charge pump, PFD, and reference path control register is programmed as shown in Figure 37.

The charge pump current is controlled by the base charge pump current ($I_{CP, BASE}$) and the value of the charge pump current multiplier ($I_{CP, MULT}$).

The base charge pump current can be set using an internal or external resistor (according to Bit DB18 of Register 4). When using an external resistor, the value of $I_{CP, BASE}$ can be varied according to

$$R_{SET}\ [\Omega] = \left[\frac{217.4 \times I_{CP, BASE}}{250}\right] - 37.8$$

The actual charge pump current can be programmed to be a multiple (1, 2, 3, or 4) of the charge pump base current. The multiplying value ($I_{CP, MULT}$) is equal to 1 plus the value of the DB11 and DB10 bits in Register 4.

The PFD phase offset multiplier ($\theta_{PFD, OFS}$), which is set by Bit DB16 to Bit DB12 of Register 4, causes the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by

$$|\Delta\Phi|[\text{deg}] = 22.5\frac{\theta_{PFD, OFS}}{I_{CP, MULT}}$$

Finally, the phase offset can be either positive or negative depending on the value of the DB17 bit in Register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2×, 1×, 0.5×, or 0.25×. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The ADRF6801 also provides a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode provides a lock-detect output that allows users to verify when the PLL has locked to the target frequency. In addition, several other internal signals can be routed to the MUXOUT pin as described in Figure 37.

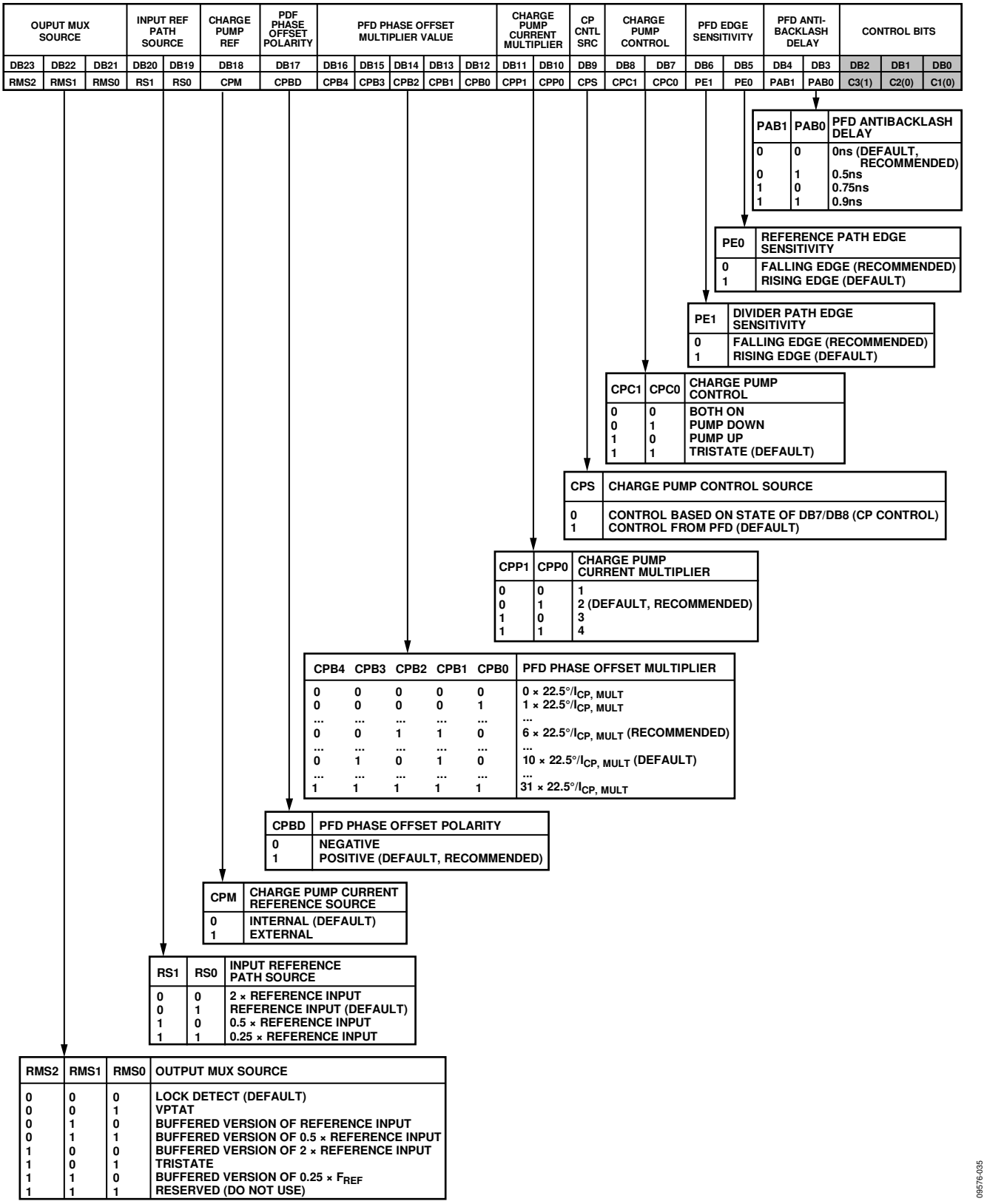

Figure 37. Charge Pump, PFD, and Reference Path Control Register (R4)

Register 5—LO Path and Demodulator Control

Register 5 controls whether the LOIP and LOIN pins act as an input or output, whether the divider before the polyphase divider is in divide-by-1 or divide-by-2, and whether the demodulator bias circuitry is enabled as detailed in Figure 38.

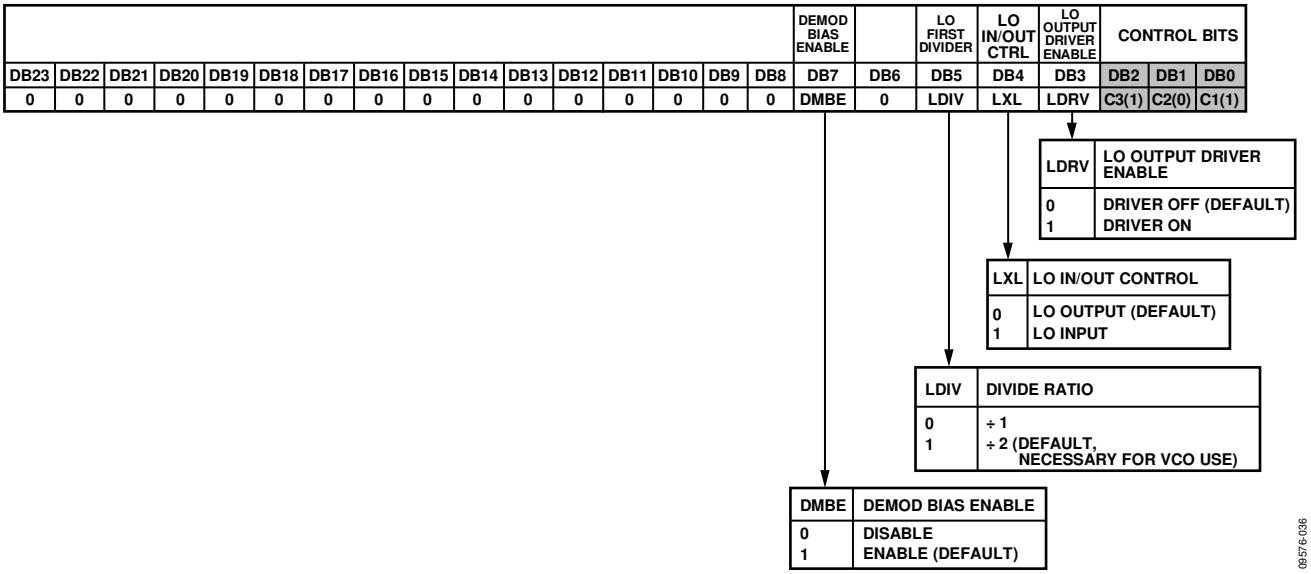

Figure 38. LO Path and Demodulator Control Register (R5)

Register 6—VCO Control and Enables

With R6[2:0] set to 110, the VCO control and enables register is programmed as shown in Figure 39.

VCO band selection is normally selected based on BANDCAL calibration; however, the VCO band can be selected directly using Register 6. The VCO BS SRC determines whether the BANDCAL calibration determines the optimum VCO tuning band or if the external SPI interface is used to select the VCO tuning band based on the value of the VCO band select.

The VCO amplitude can be controlled through Register 6. The VCO amplitude setting can be controlled between 0 and 31 decimal, with a default value of 24.

The internal VCO can be disabled using Register 6. The internal VCO LDO can be disabled if an external clean 3.0 V supply is available.

The internal charge pump can be disabled through Register 6. Normally, the charge pump is enabled.

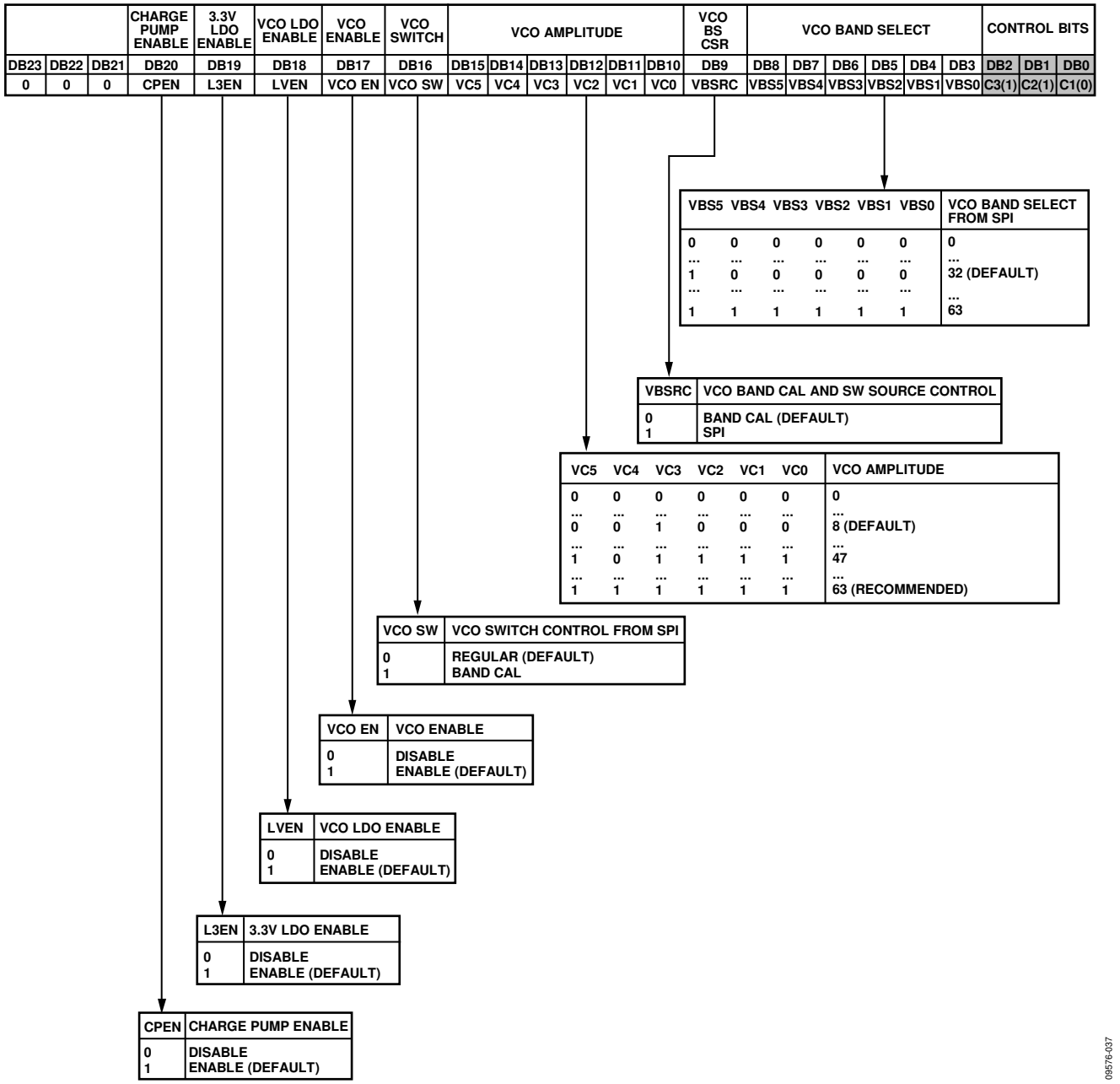

Figure 39. VCO Control and Enables (R6)

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic circuit connections for a typical ADRF6801 application are shown in Figure 40.

SUPPLY CONNECTIONS

The ADRF6801 has several supply connections and on-board regulated reference voltages that should be bypassed to ground using low inductance bypass capacitors located in close proximity to the supply and reference pins of the ADRF6801. Specifically Pin 1, Pin 2, Pin 9, Pin 10, Pin 17, Pin 22, Pin 27, Pin 29, Pin 34, and Pin 40 should be bypassed to ground using individual bypass capacitors. Pin 40 is the decoupling pin for the on-board VCO LDO, and for best phase noise performance, several bypass capacitors ranging from 100 pF to 10 µF may help to improve phase noise performance. For additional details on bypassing the supply nodes, see the evaluation board schematic in Figure 42.

SYNTHESIZER CONNECTIONS

The ADRF6801 includes an on-board VCO and PLL for LO synthesis. An external reference must be applied for the PLL to operate. A 1 V p-p nominal external reference must be applied to Pin 6 through an ac coupling capacitor. The reference is compared to an internally divided version of the VCO output frequency to create a charge pump error current to control and lock the VCO. The charge pump output current is filtered and converted to a control voltage through the external loop filter that is then applied to the VTUNE pin (Pin 39). ADIsimPLL™ can be a helpful tool when designing the external charge pump loop filter. The typical Kv of the VCO, the charge pump output current magnitude, and PFD frequency should all be considered when designing the loop filter. The charge pump current magnitude can be set internally or with an external RSET resistor connected to Pin 5 and ground, along with the internal digital settings applied to the PLL (see the Register 4—Charge Pump, PFD, and Reference Path Control section for more details).

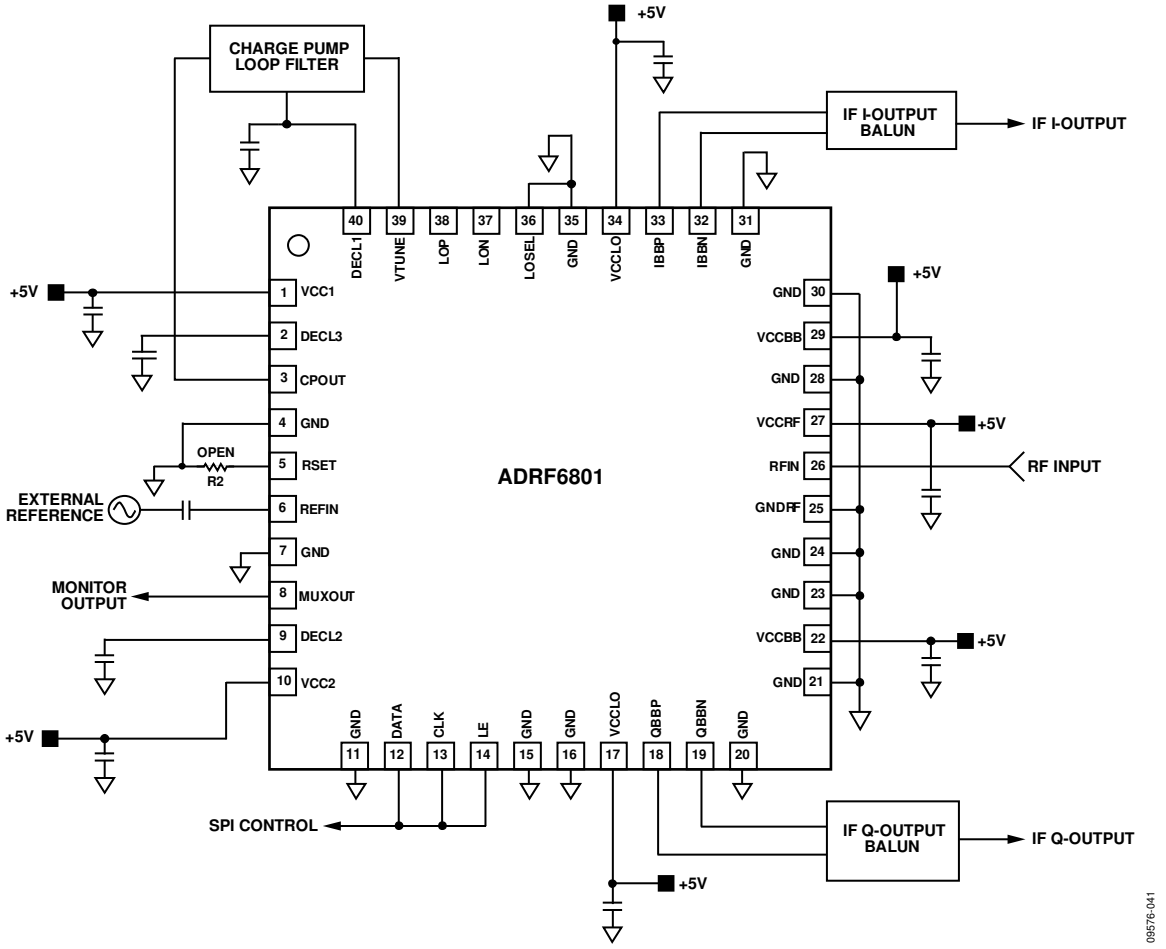

Figure 40. Basic Connections

I/Q OUTPUT CONNECTIONS

The ADRF6801 has I and Q baseband outputs. Each output stage consists of emitter follower output transistors with a low differential impedance of 24 Ω and can source up to 12 mA p-p differentially. A Mini-Circuits TCM9-1+ balun is used to transform a single-ended 50 Ω load impedance into a nominal 450 Ω differential impedance.

RF INPUT CONNECTIONS

The ADRF6801 is to be driven single-ended and can be either dc coupled or ac coupled. There is an on-chip ground referenced balun that converts the applied single-ended signal to a differential signal that is then input to the RF V-to-I converter.

CHARGE PUMP/VTUNE CONNECTIONS

The ADRF6801 uses a loop filter to create the VTUNE voltage for the internal VCO. The loop filter in its simplest form is an integrating capacitor. It converts the current mode error signal coming out of the CPOUT pin into a voltage to control the VCO via the VTUNE voltage. The stock filter on the evaluation board has a bandwidth of 130 kHz. The loop filter contains seven components, four capacitors, and three resistors. Changing the values of these components changes the bandwidth of the loop filter. Note that to obtain the approximately 2.5 kHz loop bandwidth, the user can change the values of the following components on the evaluation board to as follows: C14 = 0.1 µF, R10 = 68 Ω, C15 = 4.7 µF, R9 = 270 Ω, C13 = 47 nF, R60 = 0 Ω, C4 = open.

LO SELECT INTERFACE

The ADRF6801 has the option of either monitoring a scaled version of the internally generated LO (LOSEL pin driven high at 3.3 V) or providing an external LO source (LOSEL pin driven low to ground, the LDRV bit in Register 5 set low, and the LXL bit in Register 5 set high). See the Pin Configuration and Function Descriptions section for full operation details.

EXTERNAL LO INTERFACE

The ADRF6801 provides the option to use an external signal source for the LO into the IQ demodulating mixer core. It is important to note that the applied LO signal is divided down by either 2 or 4 depending on the LO path divider bit, LDIV, in Register 5, prior to the actual IQ demodulating mixer core. The divider is determined by the register settings in the LO path and mixer control register (see the Register 5—LO Path and Demodulator Control section). The LO input pins (Pin 37 and Pin 38) present a broadband differential 50 Ω input impedance. The LOP and LON input pins must be ac-coupled. This is achieved on the evaluation board via a Mini-Circuits TC1-1-13+ balun with a 1:1 impedance ratio. When not in use, the LOP and LON pins can be left unconnected.

SETTING THE FREQUENCY OF THE PLL

The frequency of the VCO/PLL, once locked, is governed by the values programmed into the PLL registers, as follows:

$$f_{PLL} = f_{PFD} \times 2 \times (INT + FRAC/MOD)$$

where:
f_{PLL} is the frequency at the VCO when the loop is locked.
f_{PFD} is the frequency at the input of the phase frequency detector.
INT is the integer divide ratio programmed into Register 0.
MOD is the modulus divide ratio programmed into Register 1.
FRAC is the fractional value programmed into Register 2.

The practical lower limit of the reference input frequency is determined by the combination of the desired f_{PLL} and the maximum programmable integer divide ratio of 119 and reference input frequency multiplier of 2. For a maximum f_{PLL} of 4600 MHz,

$$f_{REF} > \sim f_{PLL}/(119 \times 2 \times 2), \text{ or } 9.7 \text{ MHz}.$$

A lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with logic high signifying that the loop is locked.

When the internal VCO is used, the actual LO frequency is

$$f_{LO} = f_{PLL}/4$$

REGISTER PROGRAMMING

Because Register 6 controls the powering of the VCO and charge pump, it must be programmed once before programming the PLL frequency (Register 0, Register 1, and Register 2).

The registers should be programmed starting with the highest register (Register 7) first and then sequentially down to Register 0 last. When Register 0, Register 1, or Register 2 is programmed, an internal VCO calibration is initiated that must execute when the other registers are set. Therefore, the order must be Register 7, Register 6, Register 5, Register 4, Register 3, Register 2, Register 1, and then Register 0. Whenever Register 0, Register 1, or Register 2 is written to, it initializes the VCO calibration (even if the value in these registers does not change). After the device has been powered up and the registers configured for the desired mode of operation, only Register 0, Register 1, or Register 2 must be programmed to change the LO frequency.

If none of the register values is changing from their defaults, there is no need to program them.

EVM MEASUREMENTS

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver has all constellation points at their ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from their ideal locations.

In general, a demodulator exhibits three distinct EVM limitations vs. received input signal power. As signal power increases, the distortion components increase. At large enough signal levels, where the distortion components due to the harmonic non-linearities in the device are falling in-band, EVM degrades as signal levels increase. At medium signal levels, where the demodulator behaves in a linear manner and the signal is well above any notable noise contributions, the EVM has a tendency to reach an optimal level determined dominantly by either quadrature accuracy and I/Q gain match of the demodulator or the precision of the test equipment. As signal levels decrease, such that the noise is the major contribution, the EVM performance vs. the signal level exhibits a decibel-for-decibel degradation with decreasing signal level. At lower signal levels, where noise proves to be the dominant limitation, the decibel EVM proves to be directly proportional to the SNR.

The basic test setup to test EVM for the ADRF6801 consisted of an Agilent E4438C, which was used as a signal source. The 900 MHz modulated signal was driven single ended into the RFIN SMA connector of the ADRF6801 evaluation board. The IQ baseband outputs were taken differentially into two AD8130 difference amplifiers to convert the differential signals into single-ended signals. A Hewlett Packard 89410A VSA was used to sample and calculate the EVM of the signal. The ADRF6801 IQ baseband output pins were presented with a 450 Ω differential load impedance.

The ADRF6801 shows excellent EVM performance for 16 QAM. Figure 41 shows the EVM of the ADRF6801 being better than −40 dB over a RF input range of about +35 dB for the 16 QAM modulated signal at a 10 MHz symbol rate. The pulse shaping filter's roll-off (alpha) was set to 0.35.

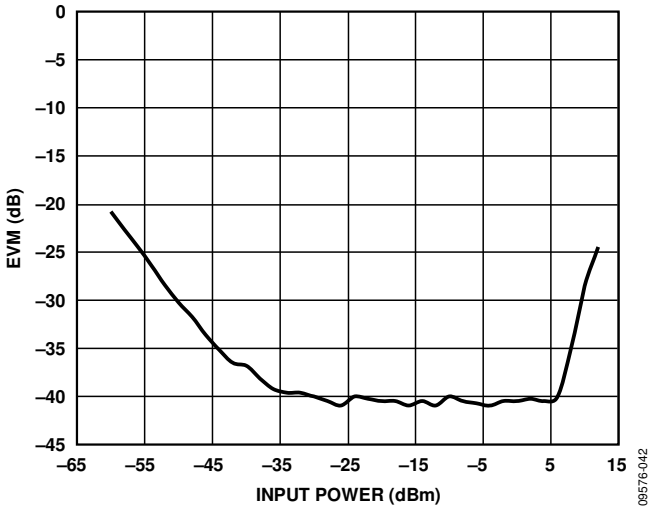

Figure 41. EVM vs. Input Power, EVM Measurements at f_{RF} = 900 MHz; f_{IF} = 0 MHz (that is, Direct Down Conversion); 16 QAM; Symbol Rate = 10 MHz

EVALUATION BOARD LAYOUT AND THERMAL GROUNDING

An evaluation board is available for testing the ADRF6801. The evaluation board schematic is shown in Figure 42. Table 5 provides the component values and suggestions for modifying the component values for the various modes of operation.

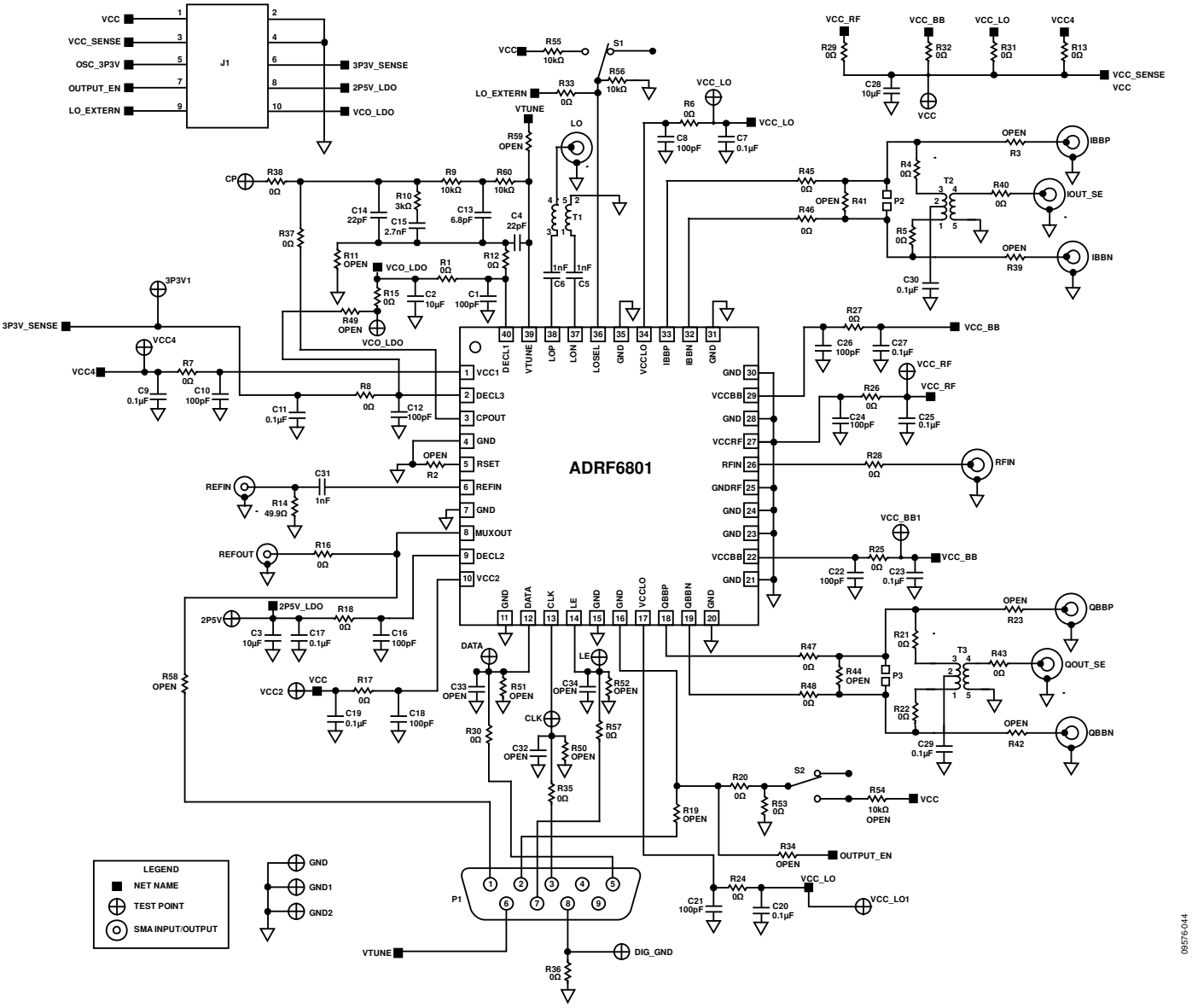

Figure 42. Evaluation Board Schematic