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450 MHz to 2800 MHz, DPD RFIC with Integrated Fractional-N PLL and VCO

Data Sheet **ADRF6821**

FEATURES

DPD receiver with integrated fractional-N PLL
RF input frequency range: 450 MHz to 2800 MHz
Internal LO input frequency range: 450 MHz to 2800 MHz
Dual RF inputs with SPDT absorptive RF switches
Integrated RF balun for single-ended 50 Ω input
Integrated VCO to cover complete RF input range
Digital programmable LO phase offset and dc nulling
Programmable via 4-wire SPI
56-lead, 8 mm × 8 mm LFCSP

APPLICATIONS

Cellular W-CDMA/GSM/LTE
DPD receivers
Microwave, point to point radios

GENERAL DESCRIPTION

The ADRF6821 is a highly integrated, dual radio frequency (RF) input, zero intermediate frequency (IF)/low IF RFIC receiver with a quadrature demodulator, digital step attenuator (DSA), IF linear amplifiers, an integrated, fractional-N phase-locked loop (PLL), and a low phase noise, multicore, voltage controlled oscillator (VCO). The RFIC is ideally suited for communication digital predistortion (DPD) systems.

The high isolation 2:1 RF switch and on-chip wideband RF balun enable the ADRF6821 to support two single-ended, 50 Ω terminated RF inputs. A programmable attenuator ensures an optimal differential RF input level to the high linearity demodulator core. The integrated attenuator offers an attenuation range of 15 dB with a step size of 1 dB. High linearity IF amplifiers follow the demodulator and provide an interface to the next component in the chain, typically an analog-to-digital converter (ADC).

The ADRF6821 offers two alternatives for generating the differential local oscillator (LO) input signal: internally via the on-chip fractional-N synthesizer with low phase noise VCOs or externally via a low phase noise LO signal. The integrated synthesizer enables continuous LO coverage from 450 MHz to 2800 MHz. The PLL reference input supports a wide frequency range and includes integrated reference dividers before the phase frequency detector (PFD).

When selected, the output of the internal fractional-N synthesizer is applied to a divide by 2, quadrature phase splitter. From the external LO path, a 2× LO signal can be used with the divide by 2, quadrature phase splitter to generate the quadrature LO inputs to the mixers.

The ADRF6821 is fabricated using an advanced silicon germanium (SiGe), bipolar complementary metal oxide semiconductor (BiCMOS) process. It is available in a 56-lead, RoHS compliant, 8 mm × 8 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +105°C case temperature range.

FUNCTIONAL BLOCK DIAGRAM

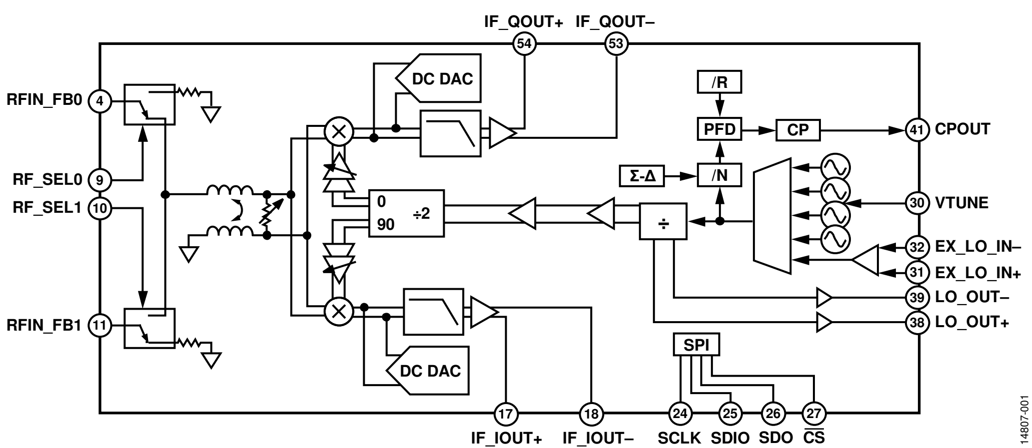

Figure 1.

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Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Changed VCC_AMP_I Pin and VCC_MIX_I Pin to VCC_IFMIX_I Pin ... Throughout
Changed VCC_MIX_Q Pin and VCC_AMP_Q Pin to VCC_IFMIX_Q Pin ... Throughout
Changes to Figure 3 ... 10
Changes to Figure 62 ... 32
Updated Outline Dimensions ... 62

5/2017—Revision 0: Initial Version

SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, low-side LO injection, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, common-mode voltage (V_{CM}) = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Input Impedance			50		Ω
RF Frequency Range		450		2800	MHz
I/Q OUTPUT INTERFACE					
Return Loss	IF_IOUT± and IF_QOUT± terminated with 100 Ω differential loads (25 Ω external resistors are required on each differential output pin)		−10		dB
Output Impedance			10		Ω
Output DC Offset	No correction		40		mV
	Correction applied		2		mV
DC Offset Correction Range			55		mV
Output V_{CM}		1.2	1.6	1.8	V
V_{CM} Ripple		−5		+5	mV
LO INPUT	External LO operation, differential				
Required Power		−6		+6	dBm
Input Impedance			100		Ω
Return Loss			−10		dB
Frequency Range	Low-side or high-side LO	450		2800	MHz
LO OUTPUT	2× LO output, differential, observation purposes only				
Power[1, 2]	TRM_XLODRV_DRV_POUT = 1				
2× f_{LO} = 1800 MHz			0		dBm
2× f_{LO} = 3600 MHz			−1		dBm
2× f_{LO} = 5400 MHz			0		dBm
Output Impedance	Differential		50		Ω
Return Loss			−10		dB
Frequency Range	2× f_{LO}	900		5600	MHz
POWER SUPPLY					
PLL/VCO Supplies[3]		3.2	3.3	3.4	V
RF/IF Supplies		3.1	3.3	3.5	V
POWER CONSUMPTION					
RF/IF Supplies			0.9		W
PLL/VCO Supplies					
f_{LO} = 1000 MHz	Internal LO		1.0		W
f_{LO} = 2000 MHz	Internal LO		0.9		W
f_{LO} = 2800 MHz	Internal LO		0.8		W

[1] For LO output power setting, see the LO Generation Block section.
[2] f_{LO} means LO frequency.
[3] See the Applications Information section for the supply circuit design.

SYSTEM SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DEMODULATION BANDWIDTH			500		MHz
GROUP DELAY RIPPLE	Fixed LO frequency, any 75 MHz bandwidth (BW)		0.1		ns
	Fixed LO frequency, any 280 MHz BW		0.2		ns
DYNAMIC PERFORMANCE AT f_{LO} = 1000 MHz	High-side LO, IF frequency (f_{IF}) = 100 MHz, RF frequency (f_{RF}) = 900 MHz, low-pass filter (LPF) set to lowest BW				
Power Gain			12		dB
Gain Flatness	Over any 75 MHz bandwidth, LPF set to maximum BW		0.12		dB
	Over any 280 MHz bandwidth, LPF set to maximum BW		0.35		dB
Output 1 dB Power Compression (OP1dB)	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
Output Third-Order Intercept (OIP3)	Over all DSA settings, output power (P_{OUT}) = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		33		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		35		dBm
Output Second-Order Intercept (OIP2)	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		75		dBm
Second-Order Harmonic Distortion (HD2)	P_{OUT} = −7 dBm continuous wave (CW) signal		−85		dBc
Third-Order Harmonic Distortion (HD3)	P_{OUT} = −7 dBm CW signal		−85		dBc
Noise Figure	Double-side band (DSB)		14		dB
Image Rejection			−41		dB
LO to IF Leakage	See Figure 26		−40		dBm
LO to RF Leakage	See Figure 27		−62		dBm
RF to IF Leakage	See Figure 25		−47		dBc
Isolation	Channel to channel		−58		dBc
DYNAMIC PERFORMANCE AT f_{LO} = 2000 MHz	Low-side LO, f_{IF} = 100 MHz, f_{RF} = 2100 MHz				
Power Gain			11		dB
Gain Flatness	Over any 75 MHz bandwidth		0.16		dB
	Over any 280 MHz bandwidth		0.55		dB
OP1dB	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
OIP3	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} =1 MHz to 75 MHz separation		32		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		33		dBm
OIP2	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		74		dBm
HD2	P_{OUT} = −7 dBm CW signal		−81		dBc
HD3	P_{OUT} = −7 dBm CW signal		−86		dBc
Noise Figure	DSB		15		dB
Image Rejection			−41		dB
LO to IF Leakage	See Figure 26		−48		dBm
LO to RF Leakage	See Figure 27		−61		dBm
RF to IF Leakage	See Figure 25		−52		dBc
Isolation	Channel to channel		−43		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT f_{LO} = 2800 MHz	High-side LO, f_{IF} = 100 MHz, f_{RF} = 2700 MHz				
Power Gain			10		dB
Gain Flatness	Over any 75 MHz bandwidth		0.08		dB
	Over any 280 MHz bandwidth		0.25		dB
OP1dB	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
OIP3	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} =1 MHz to 75 MHz separation		33		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		34		dBm
OIP2	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		70		dBm
HD2	P_{OUT} = −7 dBm CW signal		−80		dBc
HD3	P_{OUT} = −7 dBm CW signal		−82		dBc
Noise Figure	DSB		17		dB
Image Rejection			−32		dB
LO to IF Leakage	See Figure 26		−54		dBm
LO to RF Leakage	See Figure 27		−59		dBm
RF to IF Leakage	See Figure 25		−61		dBc
Isolation	Channel to channel		−46		dBc

DSA AND RF INPUT SWITCH SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL STEP ATTENUATOR					
Attenuation Range			15		dB
Step Size			1		dB
Step Error			±(0.3 + attenuation × 5%)		dB
Settling Time	Between any two different attenuation settings		100		ns
DSA Phase Shift	Between any two different attenuation settings		5		Degrees
RF INPUT SWITCH					
Switch Settling Time	50% control signal to 99% or1% RF signal final value		2		µs

PLL/VCO SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, reference frequency (f_{REF}) = 122.88 MHz, f_{REF} power = 10 dBm, PFD frequency (f_{PFD}) = 30.72 MHz, and loop filter BW = 20 kHz, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
Frequency		10	30.72	250	MHz
Level	For PLL lock condition, 50 Ω to ground required close to REF_IN pin	0.7		3.3	V p-p
Step Size			240		kHz
Lock Time	For PLL lock condition		0.4		ms
PFD FREQUENCY, f_{PFD}			30.72	61.44	MHz
INTERNAL VCO RANGE		4000		8000	MHz
OPEN-LOOP VCO PHASE NOISE					
VCO Frequency (f_{VCO}) = 5440 MHz					
	10 kHz offset		−83		dBc/Hz
	100 kHz offset		−110		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	10 MHz offset		−152		dBc/Hz
f_{VCO} = 7060 MHz					
	10 kHz offset		−80		dBc/Hz
	100 kHz offset		−106		dBc/Hz
	1 MHz offset		−127		dBc/Hz
	10 MHz offset		−147		dBc/Hz
SYNTHESIZER SPECIFICATIONS					
Fractional Figure of Merit (FOM)			−227		dBc/Hz
Flicker FOM			−262		dBc/Hz
f_{PFD} Spurs[1]	Output to internal mixer and daisy-chain of another ADRF6821				
f_{PFD} × 1			−90		dBc
f_{PFD} × 2			−95		dBc
f_{PFD} × 3 and Higher			−95		dBc
Unwanted Spurs (Other Than PFD and Harmonics)[1]	Output to internal mixer and daisy-chain of another ADRF6821		−70		dBc
f_{LO} = 1765 MHz, f_{VCO} = 7060 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−97		dBc/Hz
	100 kHz offset		−117		dBc/Hz
	950 kHz offset		−138		dBc/Hz
	2.1 MHz offset		−145		dBc/Hz
	3.5 MHz offset		−149		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−156		dBc/Hz
	85 MHz offset		−158		dBc/Hz
Integrated Phase Noise	100 Hz to 10 MHz integration BW		0.2		°rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{LO} = 2720 MHz, f_{VCO} = 5440 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−99		dBc/Hz
	100 kHz offset		−114		dBc/Hz
	950 kHz offset		−137		dBc/Hz
	2.1 MHz offset		−144		dBc/Hz
	3.5 MHz offset		−148		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−155		dBc/Hz
	85 MHz offset		−156		dBc/Hz
Integrated Phase Noise	100 Hz to 10 MHz integration BW		0.2		°rms

[1] Auxiliary LO output measurements are performed under a daisy-chain configuration with another ADRF6821 device. Measurements are taken from the auxiliary LO output of the daisy chained ADRF6821.

DIGITAL LOGIC SPECIFICATIONS

The following specifications are for all digital inputs.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUT VOLTAGE						
Low	V_{IL}		0		0.5	V
High	V_{IH}		1.2		3.6	V
LOGIC INPUT CURRENT						
High	I_{IH}		−100		+100	µA
Low	I_{IL}		−100		+100	µA
LOGIC OUTPUT VOLTAGE						
Low	V_{OL}		0		0.4	V
High	V_{OH}	When driving loads with complementary metal oxide semiconductor (CMOS) 1.8 V interface	1.4		1.8	V
		When driving loads with CMOS 3.3 V interface	2.4		3.3	V
LOGIC OUTPUT CURRENT						
High Driving	I_{OH}			1	2	mA
Low Driving	I_{OL}			1	2	mA

SERIAL PERIPHERAL INTERFACE (SPI) TIMING SPECIFICATIONS

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit
TIMING REQUIREMENTS					
SDI to SCLK Rising Edge Setup	t_{DS}	8			ns
SCLK Rising Edge to SDI Hold	t_{DH}	8			ns
Period of SCLK	t_{CLK}	50			ns
$\overline{CS}$ Falling Edge to SCLK Rising Edge, Setup Time	t_S	10			ns
SCLK Rising Edge to $\overline{CS}$ Rising Edge, Hold Time	t_C	30			ns
SCLK Falling Edge to Valid Readback Data, SDIO or SDO (Not Shown in Figure 2)	t_{DV}	18			ns
SCLK					
Period of SCLK for a Logic High State	t_{HIGH}	25			ns
Period of SCLK for a Logic Low State	t_{LOW}	25			ns

SPI Timing Diagram

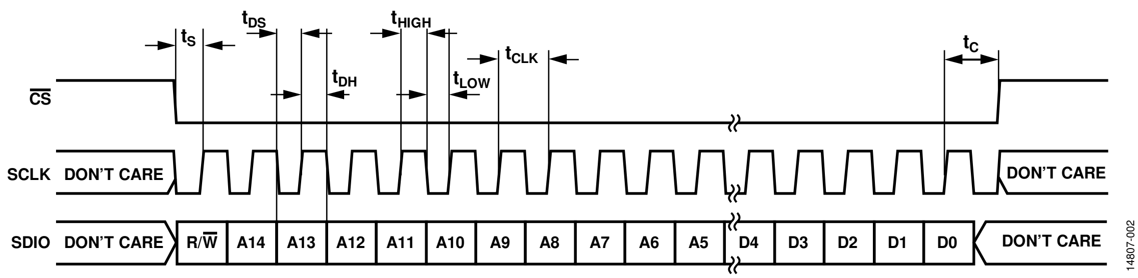


Figure 2. SPI Write (MSB First), 16-Bit Instruction, Timing Measurements

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCC_LO1, VCC_LO2, VCC_3V3_I, VCC_3V3_Q, VCC_IFMIX_I, VCC_IFMIX_Q, VCCVCO_3V3, VCCDIV_3V3, VCCFBDIV_3V3, VCCLO_MIX_3V3, VCCLO_AUX_3V3, VCCCP_3V3, VCCPFD_3V3, VCCREF_3V3, VBAT_DIG_3V3	−0.3 V to +3.6 V
VCM_I, VCM_Q	−0.3 V to +3.3 V
$\overline{CS}$, SCLK, SDIO, SDO	−0.3 V to +3.6 V
RF_SEL0, RF_SEL1, RFBT_FB	−0.3 V to +3.6 V
RFIN_FB0, RFIN_FB1	2.5 V peak, ac-coupled
$\overline{RST}$, SLEEP	−0.3 V to +3.6 V
VTUNE, CPOUT, REF_IN, DCL_BIAS	−0.3 V to +3.6 V
RF Input Power RFIN	20 dBm
EXT_LO_IN−, EXT_LO_IN+	10 dBm, differential
Maximum Junction Temperature	125°C
Operating Temperature Range (Measured at Paddle)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

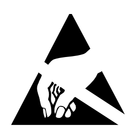
Typical θ_{JA} and θ_{JC} are specified vs. the number of PCB layers. The use of appropriate thermal management techniques is recommended to ensure the maximum junction temperature does not exceed the limits shown in Table 8.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-56-16[1]			
JEDEC 1s0p Board[2]	Not applicable	3.3	°C/W
Cold Plate Only, No PCB[3]	Not applicable	2.8	°C/W
JEDEC 2s2p Board[2]	29.3	Not applicable	°C/W

[1] The maximum junction temperature of 125°C cannot be exceeded.
[2] Per JEDEC JESD51-12.
[3] For nonstandardized testing where the paddle of the device is directly connected to a cold plate. This approach can be useful to estimate junction temperature when the exact paddle temperature is known in the application.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

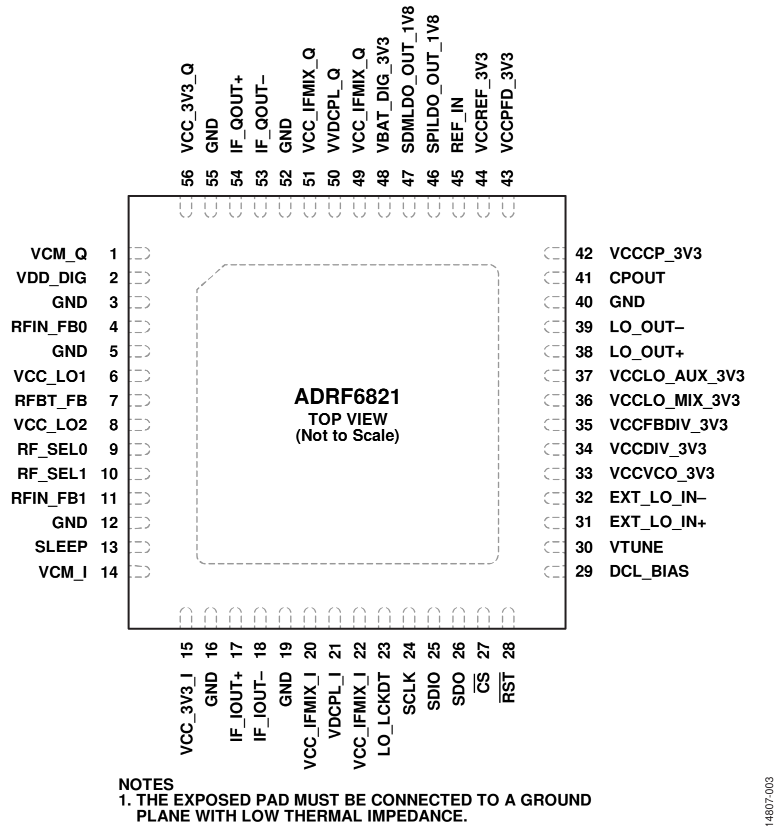


Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCM_Q	Q Channel VCM Input.
2	VDD_DIG	Digital VDD (1.8 V) Pin from On-Chip LDO.
3, 5, 12, 16, 19, 52, 55	GND	Ground.
4	RFIN_FB0	RF Input 0 Single-Pole, Double-Throw (SPDT), 50 Ω Single-Ended.
6	VCC_LO1	LO Path VCC.
7	RFBT_FB	RF Input Low Frequency Balun Connection. This pin requires a dc block to an external inductor.
8	VCC_LO2	LO Path VCC.
9	RF_SEL0	RF Input 0 Select.
10	RF_SEL1	RF Input 1 Select.
11	RFIN_FB1	RF Input 1 SPDT, 50 Ω Single-Ended.
13	SLEEP	Pin Controllable Fast Turn On/Off (1.8 V and 3.3 V Compatible).
14	VCM_I	I Channel VCM Input.
15	VCC_3V3_I	I Channel 3.3 V Supply.
17	IF_IOUT+	I Channel IF Positive Output.
18	IF_IOUT–	I Channel IF Negative Output.
20	VCC_IFMIX_I	I Channel IF Amplifier VCC Supply.
21	VDCPL_I	I Channel Mixer Decoupling.
22	VCC_IFMIX_I	I Channel Mixer VCC Supply.
23	LO_LCKDT	LO Lock Detect.
24	SCLK	SPI Clock.
25	SDIO	SPI Data Input/Output in 3-Wire Mode. SPI data input in 4-wire mode.
26	SDO	SPI Data Output. SDO used in 4-wire mode only.

Pin No.	Mnemonic	Description
27	$\overline{CS}$	SPI Chip Select (N).
28	$\overline{RST}$	Reset (Active Low).
29	DCL_BIAS	VCO Core Bias Decouple.
30	VTUNE	V_{TUNE} Input.
31	EXT_LO_IN+	Positive External LO Input.
32	EXT_LO_IN−	Negative External LO Input.
33	VCCVCO_3V3	VCC 3.3 V Supply.
34	VCCDIV_3V3	LO Chain and Divider 3.3 V Supply.
35	VCCFBDIV_3V3	PLL Feedback Divider 3.3 V Supply.
36	VCCLO_MIX_3V3	LO Mixer Output Buffer 3.3 V Supply.
37	VCCLO_AUX_3V3	LO External Output Buffer 3.3 V Supply.
38	LO_OUT+	Positive External LO Output.
39	LO_OUT−	Negative External LO Output.
40	GND	Charge Pump Ground.
41	CPOUT	Charge Pump Output.
42	VCCCP_3V3	Charge Pump 3.3 V Supply.
43	VCCPFD_3V3	PFD 3.3 V Supply.
44	VCCREF_3V3	Reference Input Buffer 3.3 V Supply.
45	REF_IN	Reference Input Buffer.
46	SPILDO_OUT_1V8	SPI 1.8 V LDO External Decouple Output.
47	SDMLDO_OUT_1V8	Sigma-Delta Modulator (SDM) 1.8 V LDO External Decouple Output.
48	VBAT_DIG_3V3	SPI and SDM LDO 3.3 V Input.
49	VCC_IFMIX_Q	Q Channel Mixer VCC Supply.
50	VDCPL_Q	Q Channel Mixer Decoupling.
51	VCC_IFMIX_Q	Q Channel IF Amplifier VCC Supply.
53	IF_QOUT−	Q Channel IF Negative Output.
54	IF_QOUT+	Q Channel IF Positive Output.
56	VCC_3V3_Q	Q Channel 3.3 V Supply.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

All supply pins = 3.3 V, TA = 25°C, high-side LO injection for LO frequencies less than or equal to 1 GHz and equal to 2.8 GHz, low-side LO injection for frequencies between 1 GHz and 2.8 GHz, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, and 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. For linearity measurements, a tone spacing of 75 MHz is used, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

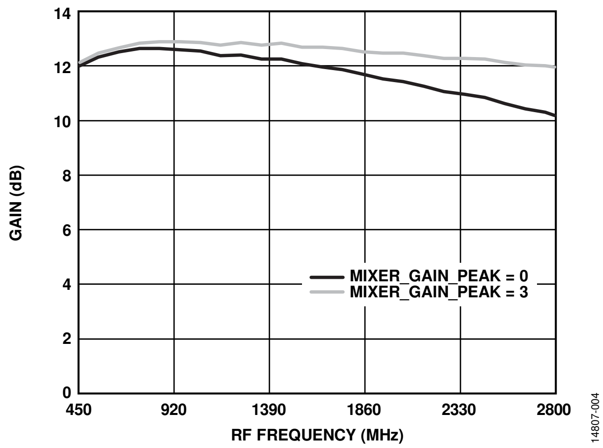


Figure 4. Gain vs. RF Frequency for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

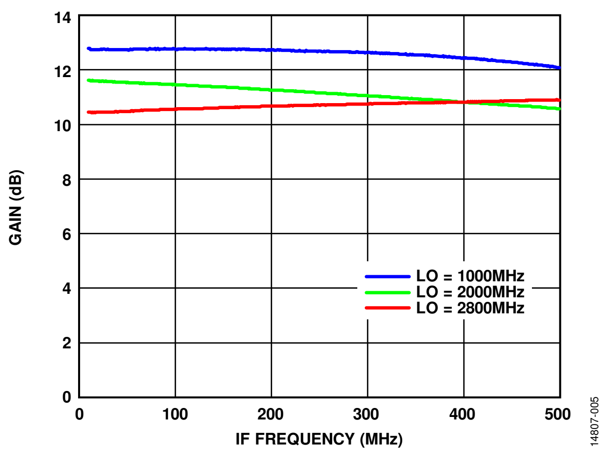


Figure 5. Gain vs. IF Frequency, RF Sweep with Fixed LO, RF to IF Roll-Off

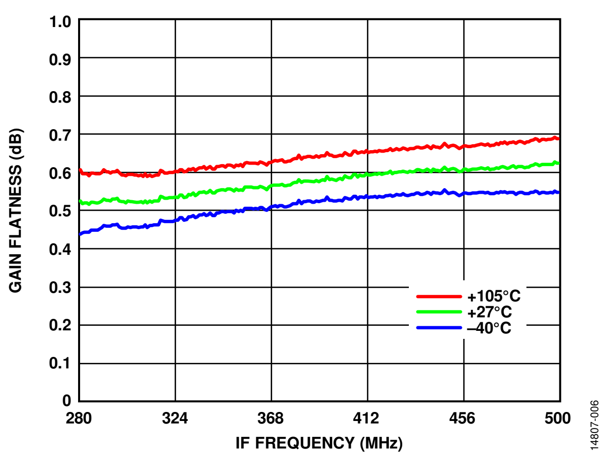


Figure 6. Gain Flatness vs. IF Frequency, Fixed LO Frequency of 2000 MHz, 280 MHz IF Frequency Window

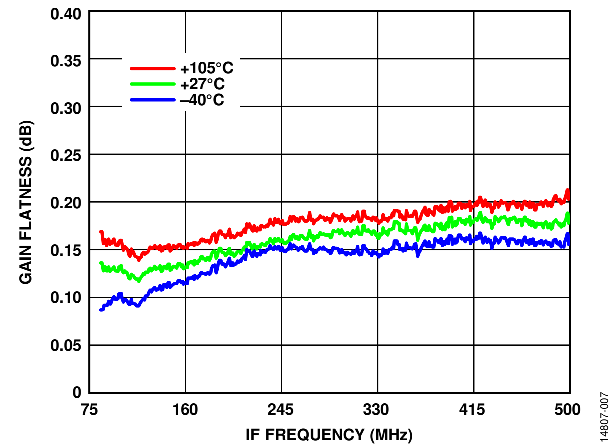


Figure 7. Gain Flatness vs. IF Frequency, Fixed LO Frequency of 2000 MHz, 75 MHz IF Frequency Window

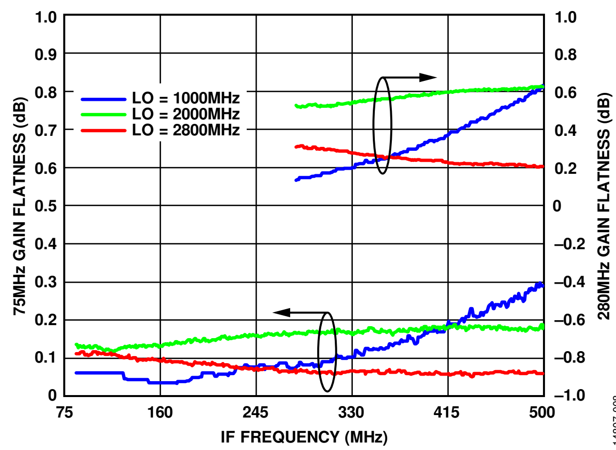


Figure 8. Gain Flatness vs. IF Frequency for Various LOs, 75 MHz (Left Axis) and 280 MHz (Right Axis) IF Frequency Window

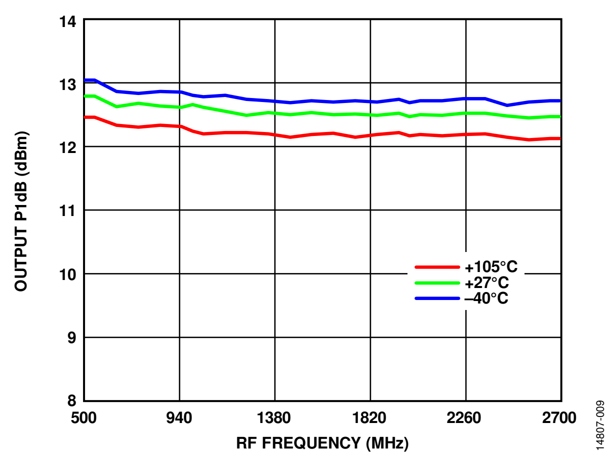


Figure 9. Output P1dB vs. RF Frequency

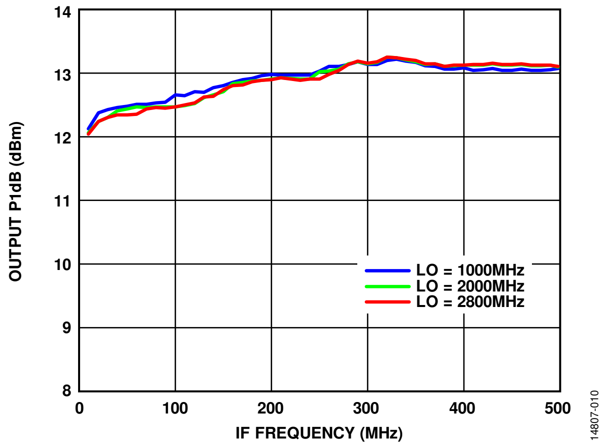


Figure 10. Output P1dB vs. IF Frequency, RF Sweep with Fixed LO, Various LO Frequency

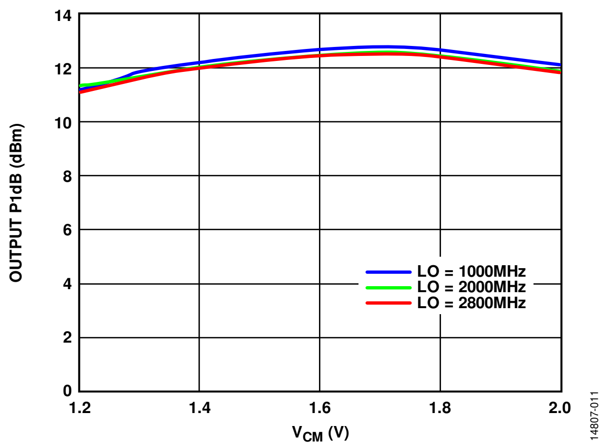


Figure 11. Output P1dB vs. Common-Mode Voltage (V_{CM}), IF = 100 MHz

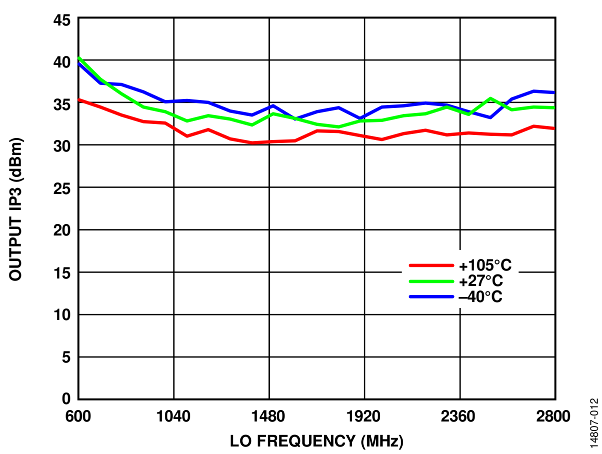


Figure 12. Output IP3 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various Temperature

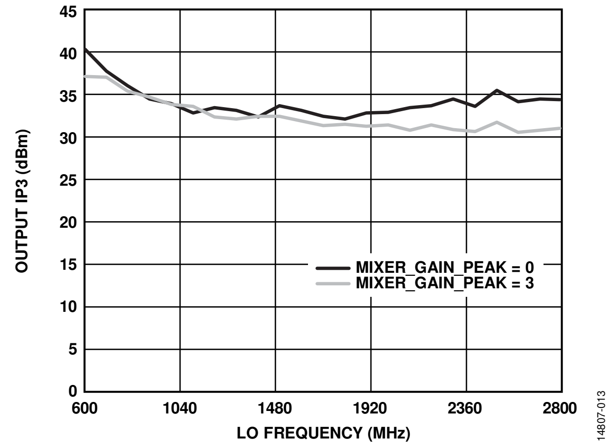


Figure 13. Output IP3 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

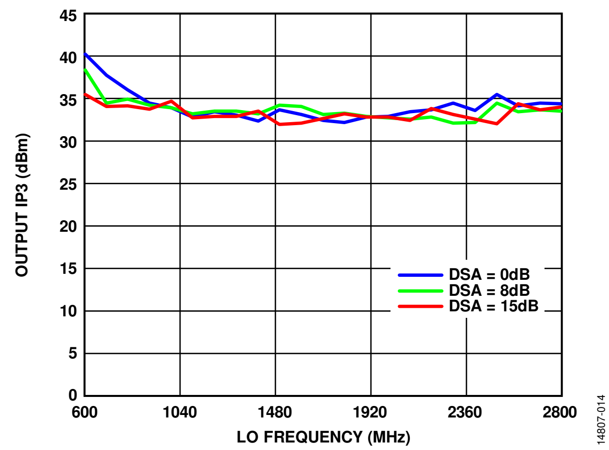


Figure 14. Output IP3 vs. LO Frequency for Various DSA Settings, Measured on −10 dBm for Each Tone at the IF Output

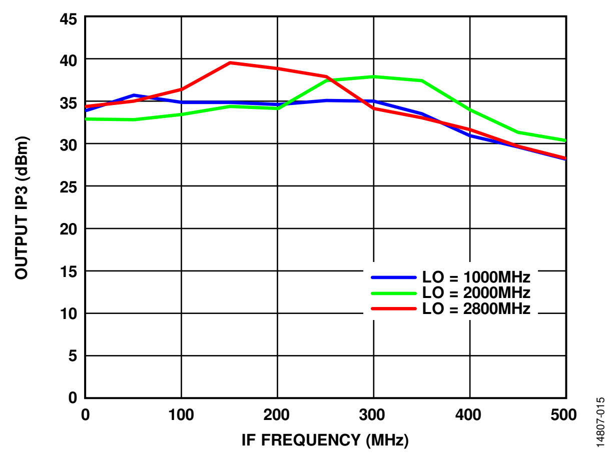


Figure 15. Output IP3 vs. IF Frequency for Various LO Frequencies, Measured on −10 dBm for Each Tone at the IF Output, Low Side LO for 1 GHz

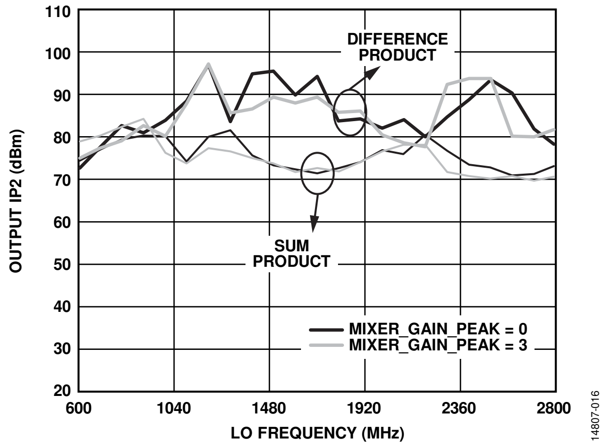


Figure 16. Output IP2 vs. LO Frequency for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

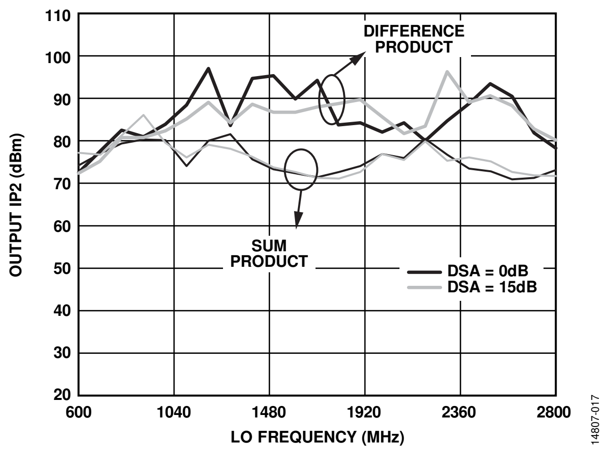


Figure 17. Output IP2 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various DSA Settings

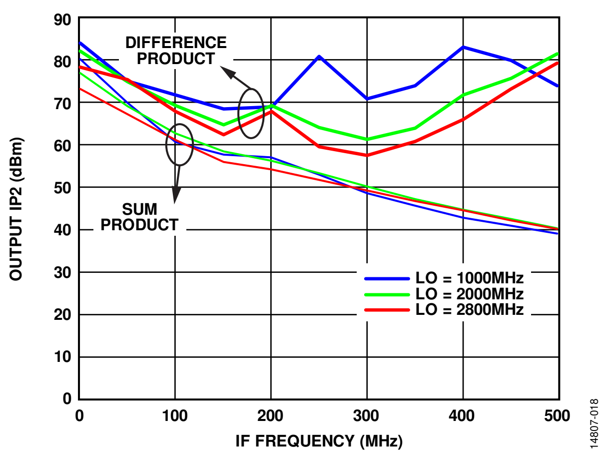


Figure 18. Output IP2 vs. IF Frequency, RF Sweep with Fixed LO, Measured on −10 dBm for Each Tone at the IF Output

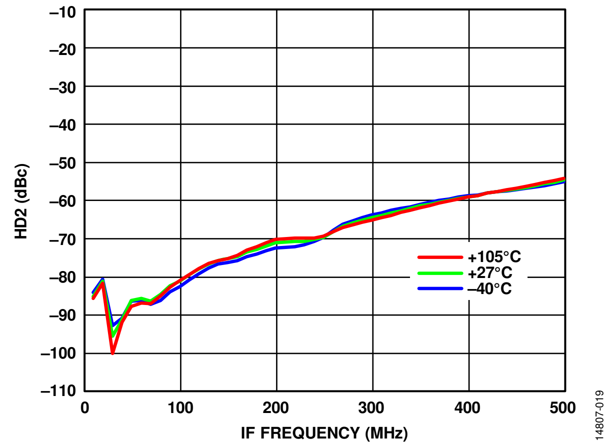


Figure 19. HD2 vs IF Frequency, LO at 2000 MHz and P_{OUT} = −7 dBm

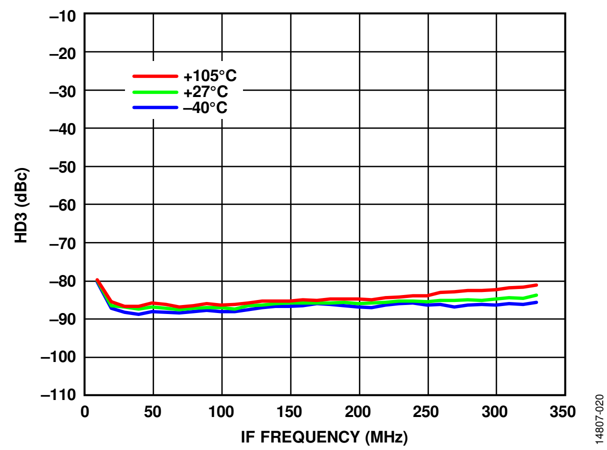


Figure 20. HD3 vs. IF Frequency, LO at 2000 MHz and P_{OUT} = −7 dBm

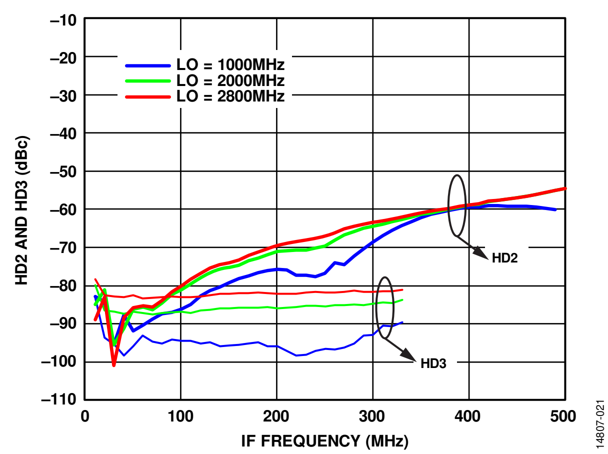


Figure 21. HD2 and HD3 vs. IF Frequency for Various LO Frequencies

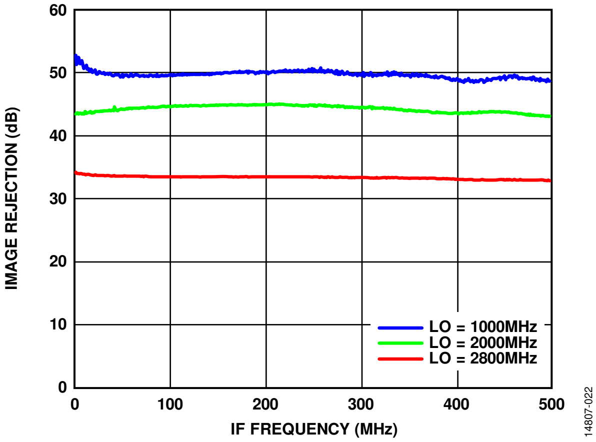


Figure 22. Image Rejection vs. IF Frequency for Various LO Frequencies

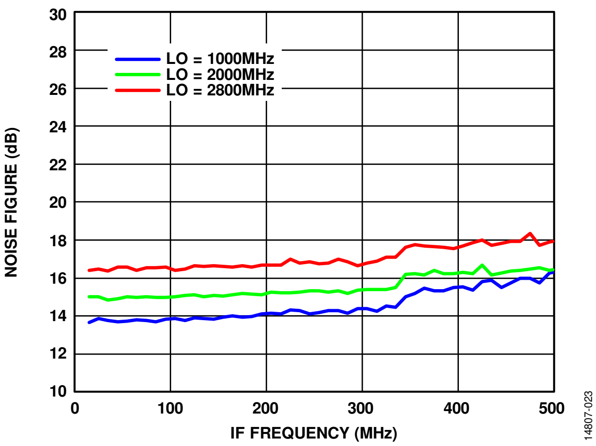


Figure 23. Noise Figure vs. IF Frequency for Various LO Frequencies, Double Side Band

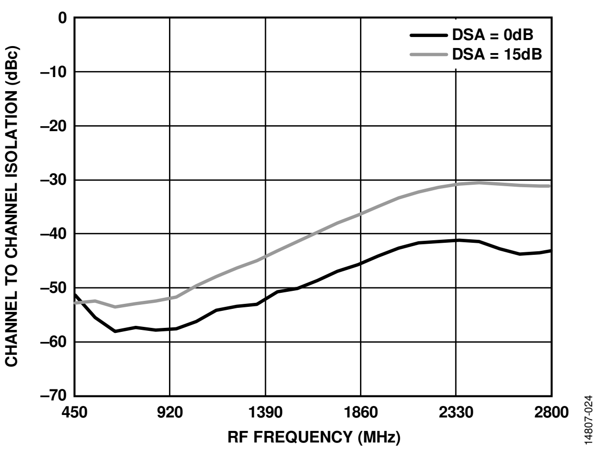


Figure 24. Channel to Channel Isolation vs. RF Frequency

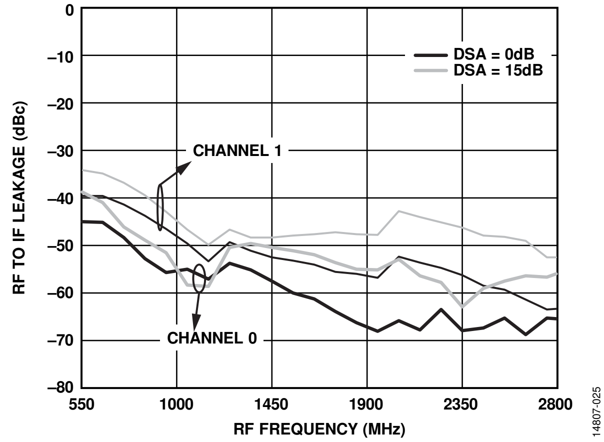


Figure 25. RF to IF Leakage at IF Output

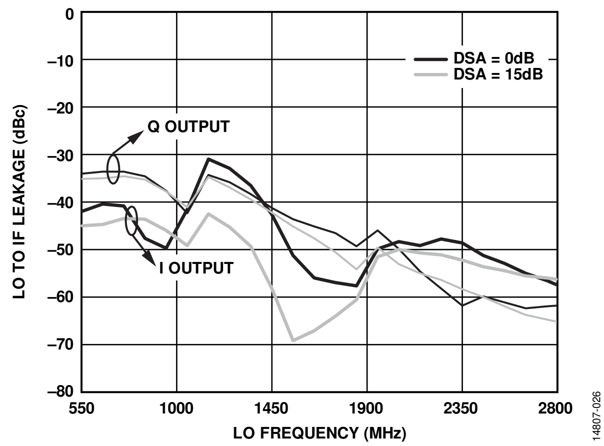


Figure 26. LO to IF Leakage at IF Output

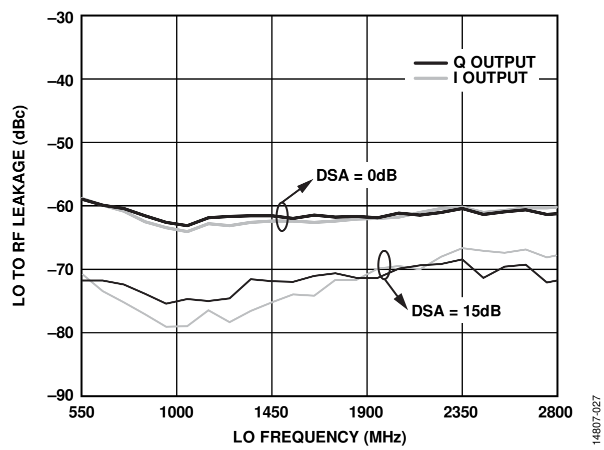


Figure 27. LO to RF Leakage vs. LO Frequency

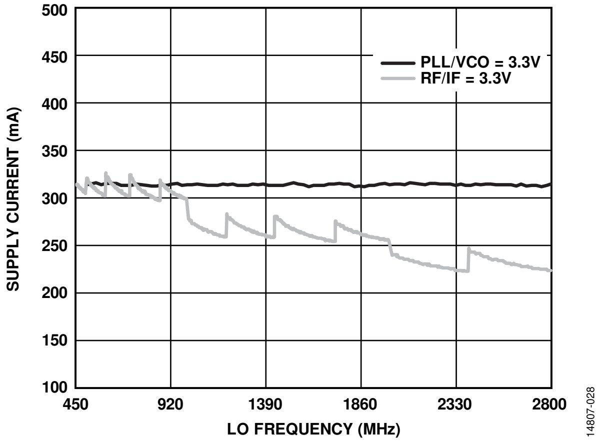


Figure 28. Supply Current vs. LO Frequency

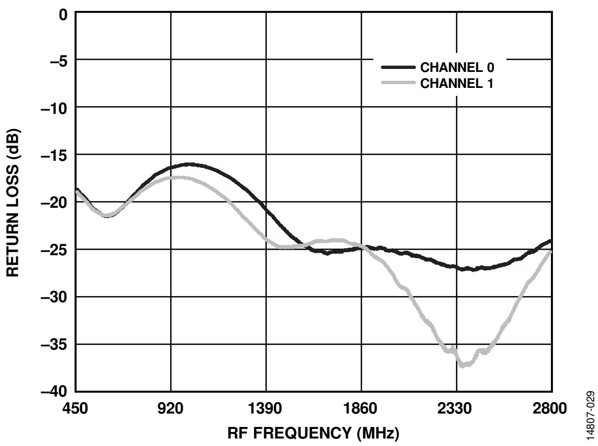


Figure 29. Return Loss vs. RF Frequency for Channel 0 and Channel 1

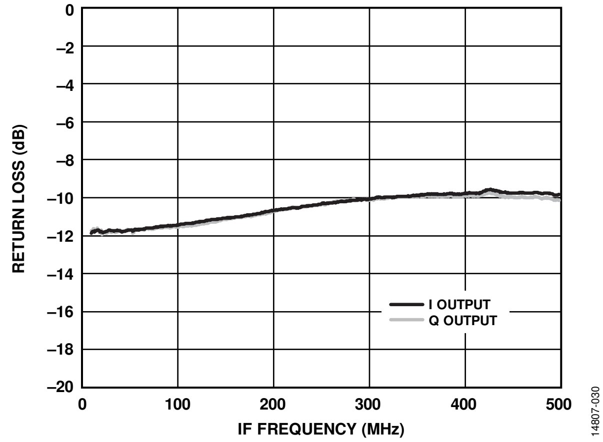


Figure 30. Return Loss vs. IF Frequency, Differential with 25 Ω Series Resistor on Each Leg, Measured with 100 Ω Differential

PHASE-LOCKED LOOP (PLL) PERFORMANCE

All supply pins = 3.3 V, T_A = 25°C, f_{PFD} = 30.72 MHz, f_{REF} = 122.88 MHz, 20 kHz loop filter, measured at LO output, unless otherwise noted.

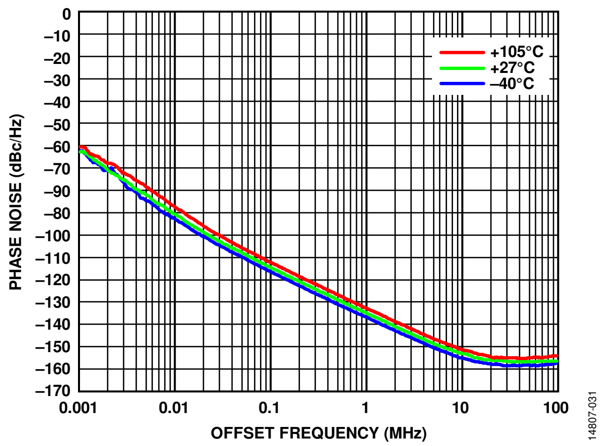


Figure 31. Open-Loop VCO Phase Noise vs. Offset Frequency for Various Temperatures

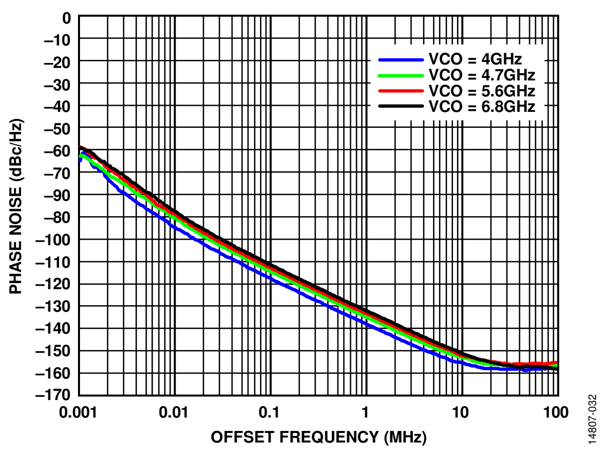


Figure 32. Open-Loop VCO Phase Noise vs. Offset Frequency for Various VCO Frequencies

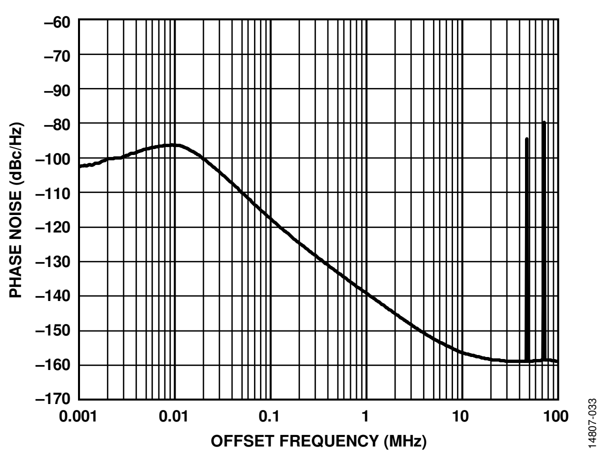


Figure 33. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 1765 MHz

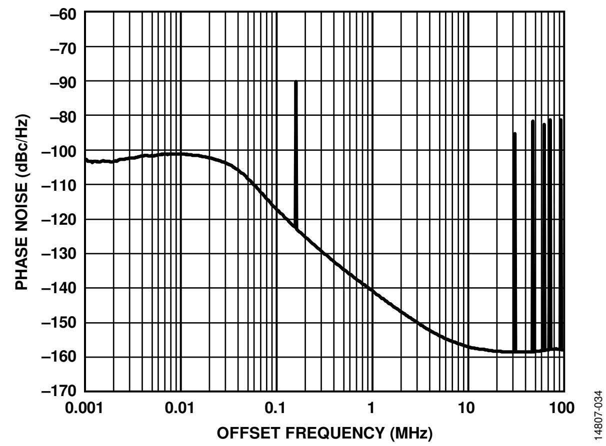


Figure 34. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2350 MHz

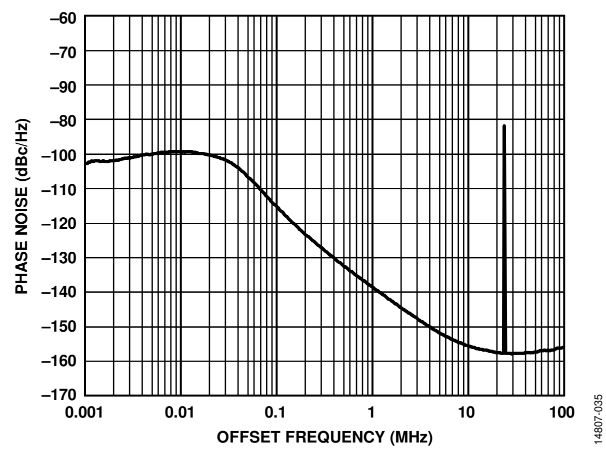


Figure 35. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2720 MHz

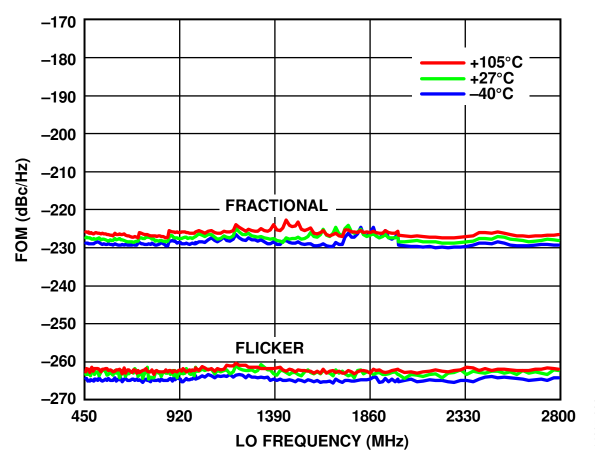


Figure 36. PLL Figure of Merit (FOM) vs. LO Frequency

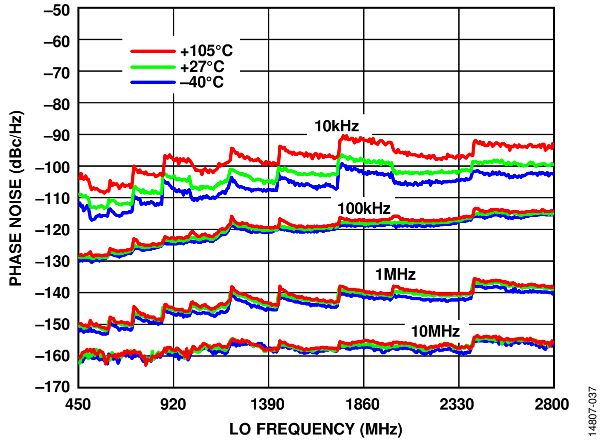


Figure 37. Closed-Loop LO Phase Noise vs. LO Frequency for Various Offset Frequencies and for Various Temperatures

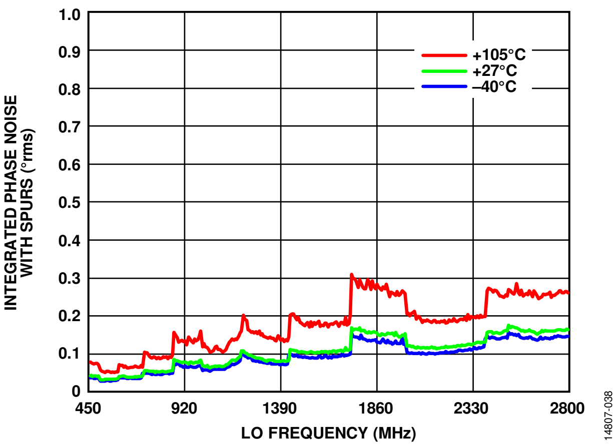


Figure 38. 100 Hz to 10 MHz Integrated Phase Noise with Spurs vs. LO Frequency

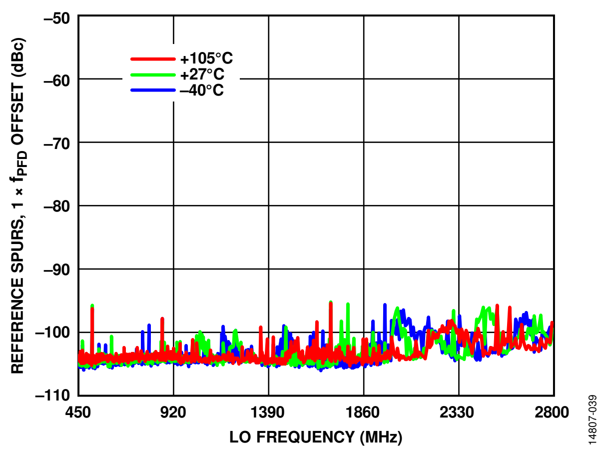


Figure 39. Reference Spurs, 1 × f_{PFD} Offset vs. LO Frequency

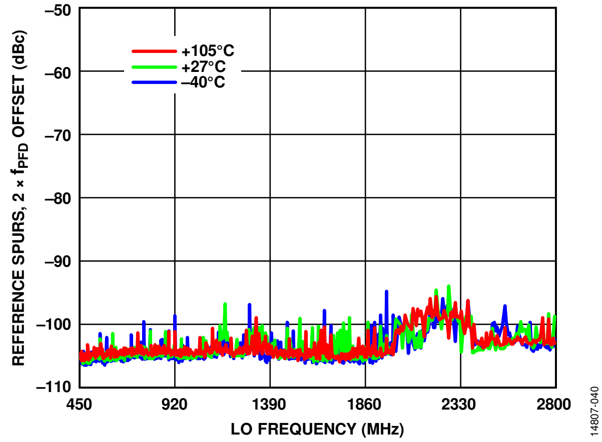


Figure 40. Reference Spurs, 2 × f_{PFD} Offset vs. LO Frequency

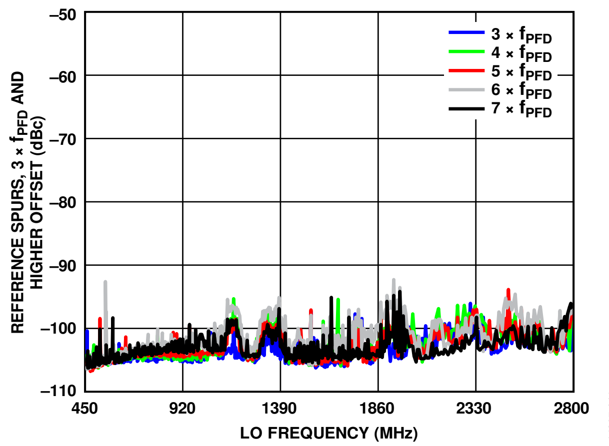


Figure 41. Reference Spurs, 3 × f_{PFD} and Higher Offset vs. LO Frequency

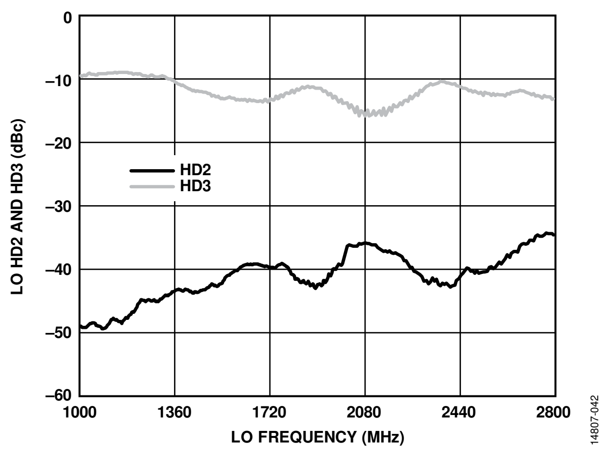


Figure 42. LO HD2 and HD3 vs. LO Frequency

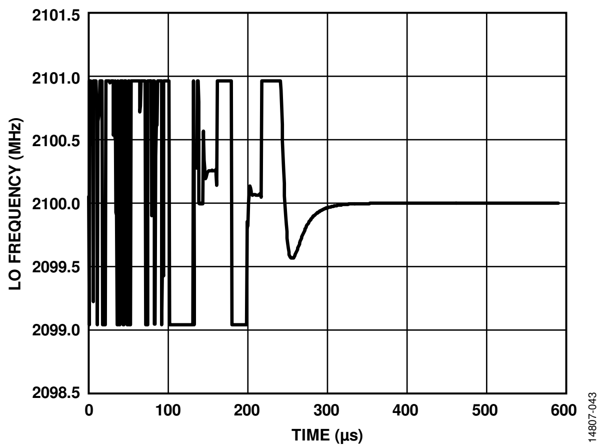


Figure 43. LO Frequency Settling Time, LO = 2.1 GHz

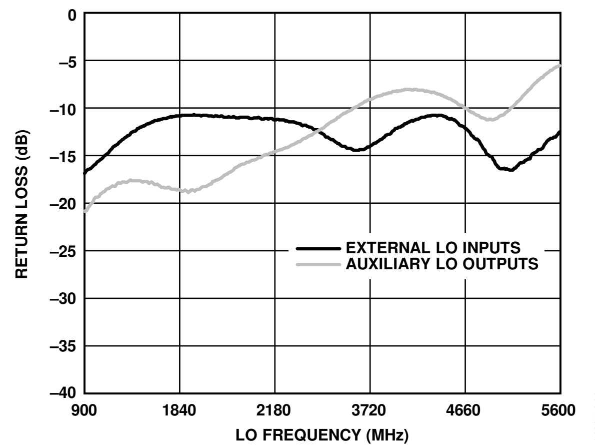


Figure 44. Return Loss vs. LO Frequency for Auxiliary LO Outputs and External LO Inputs

THEORY OF OPERATION

The ADRF6821 integrates many of the essential building blocks for a high bandwidth quadrature demodulator and receiver, especially for the feedback downconverter path for the digital predistortion in cellular base stations. The main features include two single-pole, double-throw (SPDT) RF input switches, a balun, a variable RF attenuator, a pair of active mixers, and two baseband buffers. Additionally, the local oscillator (LO) signals for the mixers are generated by a fractional-N synthesizer and a multicore voltage controlled oscillator (VCO), covering an octave frequency range with low phase noise. A pair of flip-flops then divides the LO frequency by two and generates the in phase and quadrature phase LO signals to drive the mixers. The synthesizer uses a fractional-N phase-locked loop (PLL) with additional frequency dividers to enable continuous LO coverage from 450 MHz to 2800 MHz.

The signal path through the device begins at one of two RF inputs, RFIN_FB0 and RFIN_FB1, selected by the RF switches. The selected single-ended input converts to a differential signal via the integrated balun. The differential RF signal attenuates to an optimal input level via the digital step attenuator with 15 dB of attenuation range in 1 dB steps. The RF signal then mixes with the LO signal in the Gilbert cell mixers down to an intermediate frequency (IF) or baseband. From the mixer, the signal passes through a wideband low-pass filter to remove the higher order mixing terms, followed by a fixed gain linear IF amplifier.

The different sections of the ADRF6821 are controlled through registers programmable via a serial peripheral interface (SPI).

The EN_ANALOG_MASTER bit (Register 0x0020, Bit 1) is the master enable for all enables related to the RF switch, attenuator, mixer, IF amplifiers, divider, and LO drivers. This bit does not control any of the enables related to LO generation blocks.

RF INPUT SWITCH

The ADRF6821 incorporates two SPDT switches, which allow one RF input to be selected while the other RF input can be correctly terminated to 50 Ω. Selection of the desired RF input is achieved externally via two control pins or serially via register writes to the SPI. When compared to the serial write approach, pin control allows faster switching between the RF inputs. Using the RF_SEL0 and RF_SEL1 pins (Pin 9 and Pin 10, respectively), the RF input can be switched from one channel to the other quickly and settle the IF output within 2 µs. When the input is controlled via the SPI serial port, the time for the serial data transfer must also be considered and is dependent on the serial interface clock rate.

The SEL_RFSW_SPI_CONTROL bit (Register 0x0030, Bit 6) selects whether the RF input switch is controlled via the external pins or via the SPI (see Table 10). By default at power-up, the device is configured for pin control. In serial mode control, writing to the RFSW_SEL0 bit (Register 0x0030, Bit 4) allows selection of RF Input 0 and writing to the RFSW_SEL1 bit (Register 0x0030, Bit 5) allows selection of RF Input 1. If only one RFINx port is used, the unused RF input must be properly terminated to improve isolation. It is recommended to use a dc blocking capacitor to GND as termination. Figure 45 shows the recommended configuration when only RFIN_FB0 is employed.

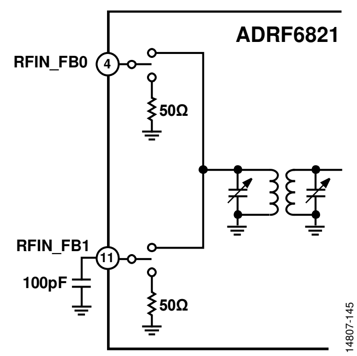


Figure 45. Terminating the Unused Port of the ADRF6821

Table 10. RF Input Selection[1]

SEL_RFSW_SPI_CONTROL Bit, (Register 0x0030, Bit 6)	RFSW_SEL0 Bit, (Register 0x0030, Bit 4)	RFSW_SEL1 Bit, (Register 0x0030, Bit 5)	RF_SEL0 and RF_SEL1 Pins	RF Input Pin
0	X	X	RF_SEL0	RFIN_FB0
0	X	X	RF_SEL1	RFIN_FB1
1	1	0	X	RFIN_FB0
1	0	1	X	RFIN_FB1

[1] X means don't care.

BALUN

The ADRF6821 integrates a balun operating over a 450 MHz to 2800 MHz frequency range. The wideband balun offers the benefit of ease of drivability with single-ended, 50 Ω RF inputs, and the single-ended to differential conversion of the integrated balun provides additional common-mode noise rejection.

RF ATTENUATOR

The RF digital step attenuator follows the balun, and the attenuation range is 0 dB to 15 dB with a step size of 1 dB. The ATTEN_DSA bits (Register 0x0031, Bits[5:2]) in the DSA_CONTROL register determine the setting of the RF digital step attenuator. The EN_DSA (Register 0x0031, Bit [0]) bit enables the RF attenuator.

ACTIVE MIXER

After the RF digital step attenuator, the RF signal is split and provided to a pair of double balanced, Gilbert cell active mixers. The RF signal is then downconverted by the on-chip LO at the mixer, resulting in a baseband output. Enable the mixer and the common-mode controls as listed in Table 11.

Table 11. Demodulator Enable Registers

Register Address	Value	Description
0x0032	0x3E	Demodulator enables
0x0040	0x0F	Common-mode control enables
0x0033	0x2D	Mixer LO common-mode control
0x0034	0x2D	Mixer output stage common-mode control

The ADRF6821 provides a gain peaking circuit to increase the gain for high RF. The amount of gain peaking is controlled by the MIXER_GAIN_PEAK bits (Register 0x003A, Bits[1:0]). Note that increased gain leads to slight degradation of the linearity performance.

The ADRF6821 uses dc compensation digital-to-analog converters (DACs) for both I and Q outputs. DC compensation covers a range of ±40 mV. Control the dc compensation value via the CODE_DC_IDAC_RF0 bits (Register 0x0051) for the I output and the CODE_DC_QDAC_RF0 bits (Register 0x0052) via the Q output for Channel 0. For Channel 1, use the CODE_DC_IDAC_RF1 bits (Register 0x0053) for the I output and the CODE_DC_QDAC_RF1 bits (Register 0x0054) for the Q output. The control words are in signed magnitude format and eight bits wide. The effective least significant bit (LSB) is approximately 0.5 mV.

I AND Q POLARITY

The ADRF6821 offers the flexibility of specifying the polarity of the I and Q outputs, where I can lead Q or vice versa. By addressing SEL_LODRV_PREDRVI_POL (Register 0x0080, Bit 1) or SEL_LODRV_PREDRVQ_POL (Register 0x0080, Bit 2), both the I and Q outputs can be inverted from their default configuration. The flexibility of specifying the polarity becomes important when the I and Q outputs are processed simultaneously in the complex domain, I + jQ.

At power-up, depending on the whether high-side or low-side injection of the LO frequency is applied, the I channel can either lead or lag the Q channel by 90°. When the RF frequency is greater than the LO frequency (low-side LO injection), the Q channel leads the I channel. On the contrary, if the RF frequency is less than the LO frequency (high-side LO injection), the I channel leads the Q channel by 90°.

LOW-PASS FILTERS (LPF) AND IF AMPLIFIERS

From the mixer, the IF or baseband outputs pass through an integrated adjustable LPF to remove the unwanted mixing product. The LPF bandwidth is adjustable over four steps, as listed in Table 12.

Table 12. LPF Bandwidth Selection

EN_LPF_LB_I (Register 0x0060, Bit 0)	EN_LPF_LB_Q (Register 0x0060, Bit 1)	LPF Bandwidth
0	0	1 GHz
0	1	750 MHz
1	0	500 MHz
1	1	250 MHz

From the LPF, the IF or baseband signal passes to a linear output amplifier to drive the baseband output pins (IF_IOUT+, IF_IOUT−, IF_QOUT−, and IF_QOUT+). The IF amplifier provides the overall gain for the ADRF6821 and, with the required 25 Ω series resistors, allows the ADRF6821 to drive a 100 Ω load directly. The ADRF6821 can be interfaced to a variety of analog-to-digital converters (ADCs), and the common-mode output can be adjusted with the external VCM pin. The IF amplifiers are enabled through the EN_IFAMP_I bit (Register 0x0070, Bit 0) and the EN_IFAMP_Q bit (Register 0x0070, Bit 1).

LO GENERATION BLOCK

The ADRF6821 supports the use of both internal and external LO signals for the mixers. The internally generated or externally supplied 2× LO signal is fed to the quadrature divider. The quadrature divider block divides the 2× LO frequency by 2 and then generates two LO signals with a 90° phase difference.

The internal 2× LO is generated by an on-chip VCO, which is tunable over a frequency range of 4000 MHz to 8000 MHz. The output of the VCO is phase locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce 2× LO signals over the 900 MHz to 5600 MHz frequency range to drive the LO divider, steer the VCO outputs through an output divider. Alternatively, an external signal can be used with the dividers to generate the 2× LO signals to the quadrature divider and the demodulators.

Internal LO Mode

For internal LO mode, the ADRF6821 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 46, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and it is divided down by a value calculated with a reference (R) divider together with a doubler bit and a prescaler bit. Then the divided down reference signal passes to the PFD. The PFD compares this signal to the divided down signal from the VCO. The PFD sends an up or down signal to the charge pump if the VCO signal is slow or fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (V_{TUNE}).

The ADRF6821 integrates multiple VCO cores covering an octave range of 4 GHz to 8 GHz. The suitable VCO is selected with the autotune functionality built into the chip. After the user determines the necessary register values, a write to the INT_L register (Address 0x1200) initiates the autotune process.

LO Frequency and Dividers

The signal coming from the VCO or the external LO inputs passes through a series of dividers before it is buffered to drive the demodulator. The programmable, divide by 2 stages divide the frequency of the incoming signal by 1, 2, 4, and 8 before reaching the quadrature divider that further divides the signal frequency by 2 to generate the in phase and quadrature phase LO signals for the mixers. The LO control bits (OUT_DIVRATIO, Register 0x1414, Bits[4:0]) needed to select the different LO frequency ranges are listed in Table 13.

Table 13. Output Divide Ratio for Frequency Ranges

2× LO Frequency (MHz)	OUT_DIVRATIO (Register 0x1414, Bits[4:0])	VCO Frequency
900 to 1000	01000	(2× LO) × 8
1000 to 2000	00100	(2× LO) × 4
2000 to 4000	00010	(2× LO) × 2
4000 to 5600	00001	(2× LO) × 1

PLL Frequency Programming

The INT, FRAC1, FRAC2, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). Calculate the VCO frequency (VCOOUT) by

$$VCOOUT = f_{PFD} \times N \quad (1)$$

where:
VCOOUT is the output frequency of the VCO (without using the output divider).
f_{PFD} is the frequency of the phase frequency detector. Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit (Register 0x120E, Bit 3).
R is the preset divide ratio of the binary 7-bit programmable reference counter, 1 to 255, (Register 0x120C, Bits[6:0]).
T is the REF_{IN} divide by 2 bit, set to 0 or 1, (Register 0x120E, Bit 0).
N is the desired value of the feedback counter. N compromises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD}}{16{,}777{,}216} \quad (3)$$

where:
INT is the 16-bit integer value (23 to 32,767 for the prescaler in 4/5 mode, 75 to 65,535 for the prescaler in 8/9 mode) referenced with Register 0x1201 and Register 0x1200. The recommended setting for the prescaler is 8/9 mode, and it is set by enabling PRE_SEL (Register 0x120B, Bit 1).
FRAC1 is the 24-bit numerator of the primary modulus (0 to 16,777,215) referenced with Register 0x1204, Register 0x1203, and Register 0x1202.
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383) referenced with Register 0x1234, Bits[5:0] and Register 0x1233.
MOD is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383), referenced with Register 0x1209, Bits[5:0] and Register 0x1208.

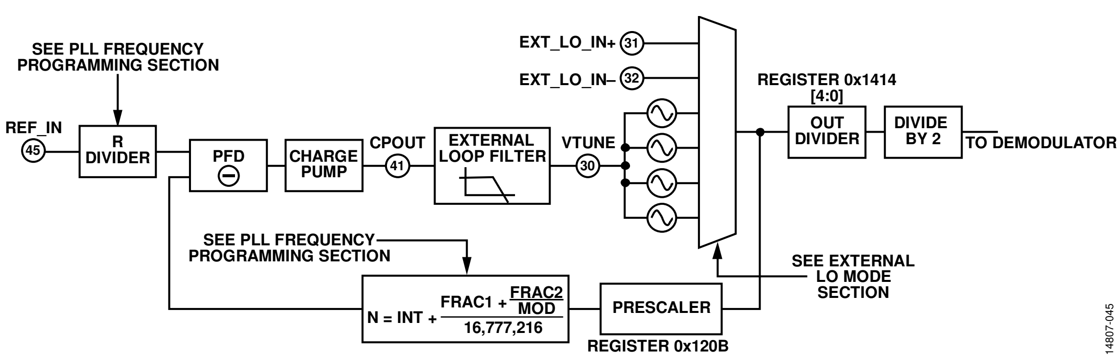


Figure 46. PLL/VCO Block Diagram

Equation 3 results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by VCOOUT/f_{PFD}.
2. The integer value of this number forms INT.
3. Subtract the INT value from the full N value.
4. Multiply the remainder by 2^{24}.
5. The integer value of this number forms FRAC1.
6. Calculate MOD based on the channel spacing (f_{CHSP}) by

   $$MOD = f_{PFD}/GCD(f_{PFD}, f_{CHSP}) \quad (4)$$

   where:
   $GCD(f_{PFD}, f_{CHSP})$ is the greatest common divider of the PFD frequency and the desired channel spacing frequency.

7. Calculate FRAC2 by the following equation:

   $$FRAC2 = ((N − INT) \times 224 − FRAC1)) \times MOD \quad (5)$$

The FRAC2 and MOD fraction result in outputs with zero frequency error for channel spacings when

$$f_{PFD}/GCD(f_{PFD}/f_{CHSP}) < 16,383 \quad (6)$$

where:
f_{PFD} is the frequency of the phase frequency detector.
GCD is a greatest common denominator function.
f_{CHSP} is the desired channel spacing frequency.

After determining the necessary register values for PLL, set the SD_EN_FRAC0 bit (Register 0x122A, Bit 5) to 1. In the integer mode (when FRAC = 0), set the SD_EN_OUT_OFF bit (Register 0x122A, Bit 4) to 1. In the same manner, set the SD_EN_OUT_OFF bit to 0 for fractional mode (that is, when FRAC ≠ 0).

It is recommended to set the charge pump current to be 2.4 mA, by setting the CP_CURRENT bit (Register 0x122E, Bits[3:0]) to 8. With a 20 kHz loop filter, the charge pump current setting results in an optimized performance.

Bleed Setting

The PFD circuitry compares the PFD and divided down VCO signals. The ADRF6821 employs a bleed circuit to put the PFD circuit in the linear operation region. The bleed circuit introduces a delay to the incoming PFD signal, indicated as PFD_OFFSET in Equation 7. Calculate the bleed current, BICP, (Register 0x122F, Bits[7:0]), from the desired PFD_OFFSET, as shown in Equation 7.

$$BICP = Integer(round(float(I_{CP} \times PFD\_OFFSET \times f_{PFD})/960)/255)) \quad (7)$$

where:
I_{CP} is the charge pump current.

The recommended PFD_OFFSET for the 20 kHz loop filter is 2 ns.

PLL Lock Time

The time it takes to lock the PLL after the last register is written into two parts: VCO band calibration and loop settling.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration requires approximately 200 µs. After calibration completes, the feedback action of the PLL causes the VCO to eventually lock to the correct frequency. The speed with which this lock occurs depends on the small signal settling of the loop. Settling time, after calibration, depends on the PLL loop filter bandwidth. With a 20 kHz loop filter bandwidth, settling time is approximately 200 µs.

Lock Detect Control

The ADRF6821 provides two ways of observing lock detection. Lock detection can be monitored from a dedicated register, LOCK_DETECT (Register 0x124D, Bit 0). Lock detection can also be monitored through the dedicated LO_LCKDT pin (Pin 23).

Required PLL/VCO Settings and Register Write Sequence

Configure the PLL registers as described in the PLL Frequency Programming section to achieve the desired frequency, and the last write must be to Register 0x1200 (INT_L). When Register 0x1200 is programmed, an internal VCO calibration initiates, which is the last step to locking the PLL.

External LO Mode

The external LO frequency range is 900 MHz to 5600 MHz and 2× LO signal is used with the internal quadrature divider. To configure for external LO mode, write the following register sequence and apply the differential LO signals to Pin 31 (EXT_LO_IN+) and Pin 32 (EXT_LO_IN−).

Table 14. Register Settings for External LO Mode

Register	Required Value	Description
0x120B	0x00	Disable feedback divider
0x122D	0x00	Disable PFD and charge pump (CP)
0x1240	0x03	Disable VCO adjust
0x1217	0x00	Set VCO select to a low value
0x121F	0x40	Disable calibration
0x1021	0xD8	Disable PLL blocks
0x1414	0xA1	Use external LO

The EXT_LO_IN+ and EXT_LO_IN− input pins must be ac-coupled. When not in use, leave the EXT_LO_IN+ and EXT_LO_IN− pins unconnected.

Quadrature Divider

The quadrature divider block divides the 2× LO frequency generated by either the internal PLL and VCO or the external input by 2. Next, the quadrature divide block generates two LO signals with a 90° phase difference. To enable the divider, disable the bits, EN_IBIASGEN (Register 0x0090, Bit 0), EN_DIVPATH_BUF (Register 0x0090, Bit 1), and EN_DIVPATH_QUADDIV (Register 0x0090, Bit 2). Two separate LO drivers take these LO signals and feed them to the mixers. LO driver paths are enabled via the following registers:

- EN_LODRV_DRVI (Register 0x0090, Bit 3)
- EN_LODRV_DRVQ (Register 0x0090, Bit 4)
- EN_LODRV_PREDRVI (Register 0x0090, Bit 5)
- EN_LODRV_PREDRVQ (Register 0x0090, Bit 6)

REGISTER WRITE SEQUENCE

The proper register write sequence starts with locking the LO frequency or enabling the external LO inputs. After ensuring that the local oscillator is locked in either the internal PLL/VCO or the external LO source, enable the LO_OE bit (Register 0x1414, Bit 6). After enabling the LO_OE bit, the RF and IF blocks can be enabled as defined in the Theory of Operation section.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI of the ADRF6821 allows the user to configure the device for specific functions or operations through a structured register space provided inside the chip. This interface provides users with added flexibility and customization. Addresses are accessed via the SPI and can be written to or read from the SPI.

The serial peripheral interface consists of four control lines: SCLK, SDIO, SDO, and $\overline{CS}$. The serial clock (SCLK) is the serial shift clock, and it synchronizes the serial interface reads and writes. SDIO is the serial data input or the serial data output depending on the instruction sent and the relative position in the timing frame. Chip select bar ($\overline{CS}$) is an active low control that gates the read and write cycles. The falling edge of $\overline{CS}$ in conjunction with the rising edge of SCLK determines the start of the frame. When $\overline{CS}$ is high, all SCLK and SDIO activity is ignored. See Table 6 for the serial timing and its definitions.

The ADRF6821 protocol consists of a read/write followed by 16 register address bits and 8 data bits. Both the address and data fields are organized with the most significant bit (MSB) first and end with the least significant bit (LSB).

The SPI and general-purpose input/output (GPIO) interfaces of the ADRF6821 provides two options for the logic voltage levels, 1.8 V and 3.3 V. The interfaces use 1.8 V logic levels as the default. Enable SPI_18_33_SEL (Register 0x0020, Bit 0) and SPI_1P8_3P3_CTRL (Register 0x1401, Bit 4) for 3.3 V compatible logic levels. See Table 6 for the SPI specifications.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

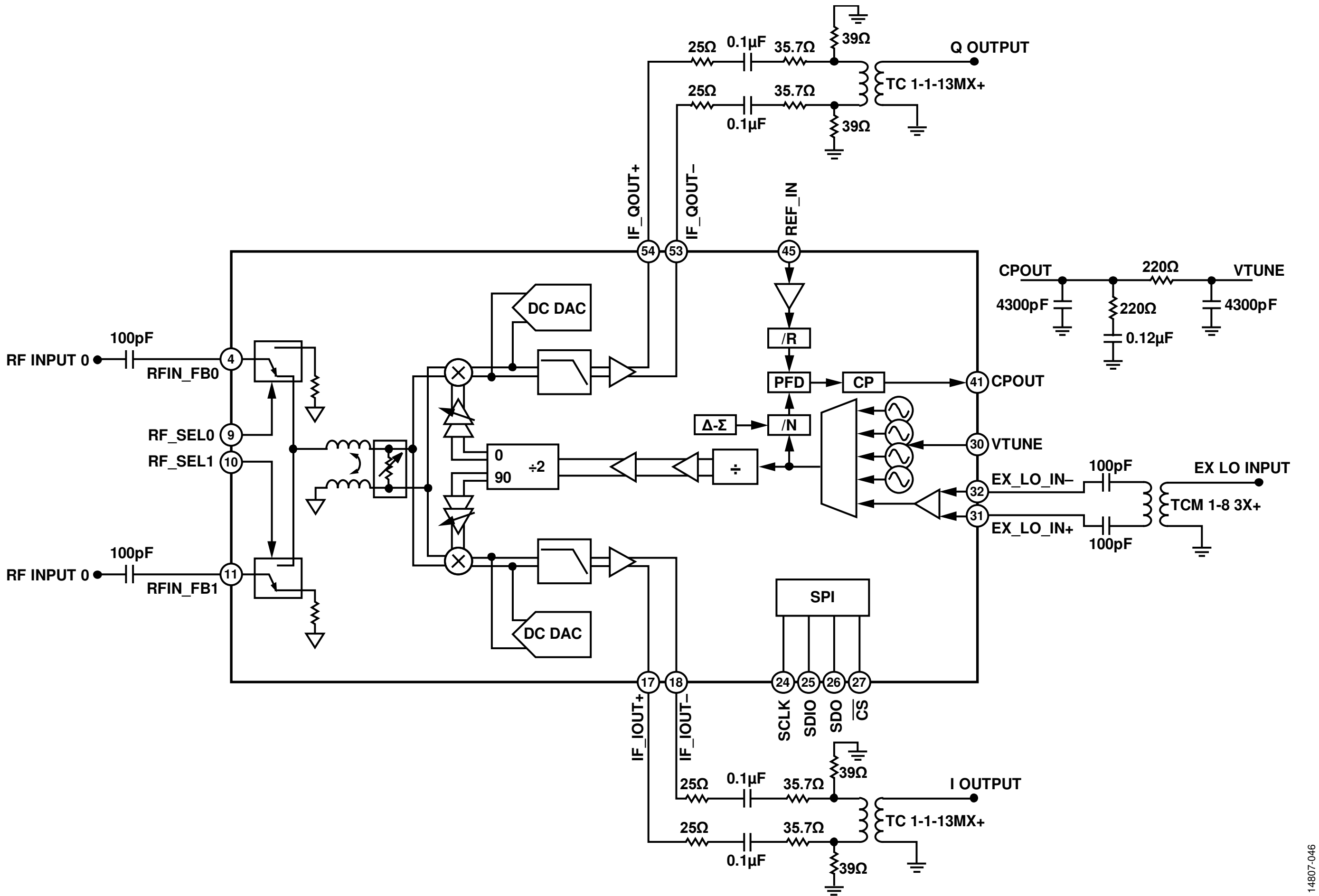


Figure 47. Typical Application Circuit

Table 15. Typical Connections

Pin No.	Mnemonic	Description	Basic Connection
RF Inputs			
4, 11	RFIN_FB0, RFIN_FB1	RF inputs	The single-ended RF inputs have a 50 Ω impedance. These pins must be ac-coupled. Terminate unused RF inputs with a dc blocking capacitor to ground to improve isolation. Refer to the Layout section for the recommended PCB layout.
RF Balun Optimization			
7	RFBT_FB	RF balun tuning inductor	Connect the balun tuning inductor (L_{TUNE}) to ground.
GPIOs			
9, 10	RF_SEL0, RF_SEL1	RF select control pins	Active high. 1.8 V and 3.3 V logic level compatible. See the Theory of Operation section for RF select pin use.
13	SLEEP	Sleep mode enable pin	Active high. 1.8 V and 3.3 V logic level compatible.