Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Integrated Dual RF Receiver

Preliminary Technical Data

ADRV9008-1

FEATURES

Dual receivers
Maximum receiver bandwidth: 200 MHz
Fully integrated, fractional-N, RF synthesizers
Fully integrated clock synthesizer
Multichip phase synchronization for RF LO and baseband clocks
JESD204B datapath interface
Tuneable range: 75 MHz to 6000 MHz

APPLICATIONS

3G/4G/5G FDD, macrocell base stations
Wideband active antenna systems
Massive multiple input, multiple output (MIMO)
Phased array radar
Electronic warfare
Military communications
Portable test equipment

GENERAL DESCRIPTION

The ADRV9008-1 is a highly integrated, dual radio frequency (RF), agile receiver (Rx) offering integrated synthesizers and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption required by 3G/4G/5G macrocell, frequency division duplex (FDD), base station applications.

The receive path consists of two independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, eliminating the need for these functions in the digital baseband. RF front-end control and several auxiliary functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) for the power amplifier (PA) are also integrated.

In addition to automatic gain control (AGC), the ADRV9008-1 also features flexible external gain control modes, allowing significant flexibility in setting system level gain dynamically.

The received signals are digitized with a set of four, high dynamic range, continuous time, sigma-delta (Σ-Δ) ADCs that provide inherent antialiasing. The combination of the direct conversion architecture (which does not suffer from out of band image mixing) and the lack of aliasing relaxes the requirements of the RF filters compared to the requirements of traditional intermediate frequency (IF) receivers.

The fully integrated phase-locked loop (PLL) provides high performance, low power, fractional-N, RF synthesis for the receiver signal paths. An additional synthesizer generates the clocks needed for the converters, digital circuits, and serial interface. A multichip synchronization mechanism synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple ADRV9008-1 chips. The ADRV9008-1 has the isolation that high performance base station applications require. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates, resulting in a single lane per receiver in the widest bandwidth mode. The interface also supports interleaved mode for lower bandwidths, reducing the total number of high speed data interface lanes to one. Both fixed and floating point data formats are supported. The floating point format allows internal AGC to be invisible to the demodulator device.

The core of the ADRV9008-1 can be powered directly from 1.3 V and 1.8 V regulators and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption during normal use. The ADRV9008-1 is packaged in a 12 mm × 12 mm, 196-ball chip scale ball grid array (CSP_BGA).

Rev. PrA **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM

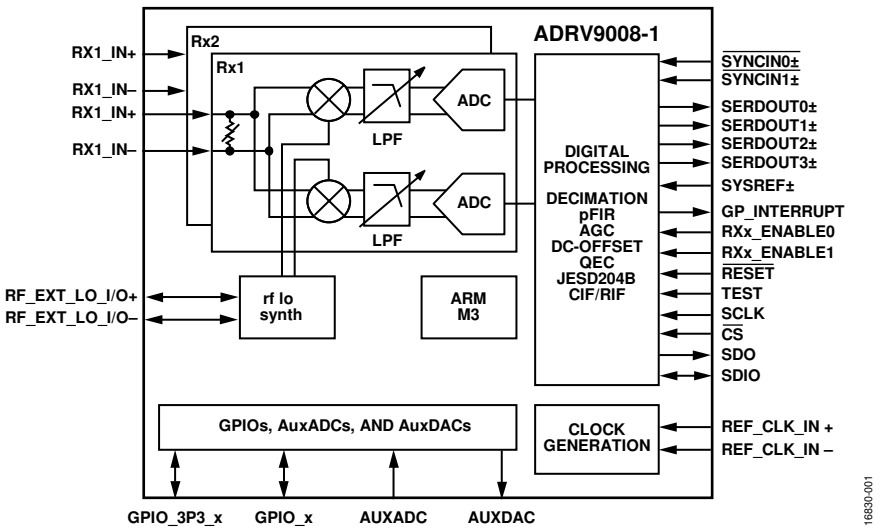

Figure 1.

SPECIFICATIONS

Electrical characteristics at VDDA1P3[1] = 1.3 V, VDDD1P3_DIG = 1.3 V, T_J = full operating temperature range. LO frequency (f_{LO}) = 1800 MHz, unless otherwise noted. The specifications in Table 1 are not deembedded. Refer to the Typical Performance Characteristics section for input/output circuit path loss. The device configuration profile, unless otherwise specified, is as follows: receiver = 200 MHz (IQ rate = 245.76 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVERS						
Center Frequency		75		6000	MHz	
Gain Range			30		dB	
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 30 dB
Bandwidth Ripple			±0.5		dB	200 MHz bandwidth, compensated by programmable FIR filter
			±0.2		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Rx Bandwidth				200	MHz	
Rx Alias Band Rejection		80			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					0 dB attenuation, increases decibel for decibel with attenuation, continuous wave (CW) = 1800 MHz, corresponds to −1 dBFS at ADC
			−11		dBm	75 MHz < f ≤ 3000 MHz
			−10.2		dBm	3000 MHz < f ≤ 4800 MHz
			−9.5		dBm	4800 MHz < f ≤ 6000 MHz
Noise Figure	NF					0 dB attenuation, at Rx port
			12		dB	600 MHz < f ≤ 3000 MHz
			13		dB	3000 MHz < f ≤ 4800 MHz
			15.2		dB	4800 MHz < f ≤ 6000 MHz
Ripple			1.8		dB	At band edge maximum bandwidth mode
Input Third-Order Intercept Point	IIP3					
Difference Product	IIP3,d		12		dBm	Two (P_{HIGH} − 12) dB tones near band edge
Sum Product	IIP3,s		12		dBm	Two (P_{HIGH} − 6) dB tones, at bandwidth/6 offset from the LO
HD3	HD3					(P_{HIGH} − 6) dB CW tone at bandwidth/6 offset from the LO
			−66		dBc	600 MHz < f ≤ 4800 MHz
			−62		dBc	4800 MHz < f ≤ 6000 MHz
Second-Order Input Intermodulation Intercept Point	IIP2		62		dBm	0 dB attenuation, complex
Image Rejection			75		dB	Quadrature error correction (QEC) active, within 200 MHz Rx bandwidth
Input Impedance			100		Ω	Differential (see Figure 168)
Rx to Rx Isolation			65		dB	600 MHz < f ≤ 4800 MHz
			61		dB	4800 MHz < f ≤ 6000 MHz
Rx Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	No more than one spur at this level per 10 MHz of Rx bandwidth
Rx LO Leakage at Rx Input at Maximum Gain						Leakage decreases decibel for decibel with attenuation for first 12 dB
			−70		dBm	600 MHz < f ≤ 3000 MHz
			−65		dBm	3000 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LO SYNTHESIZER						
LO Frequency Step			2.3		Hz	1.5 GHz to 2.8 GHz, 76.8 MHz phase frequency detector (PFD) frequency
LO Spur			−85		dBc	Excludes integer boundary spurs
Integrated Phase Noise						2 kHz to 18 MHz
1900 MHz LO			0.2		°rms	Narrow PLL loop bandwidth (50 kHz)
3800 MHz LO			0.36		°rms	Wide PLL loop bandwidth (300 kHz)
5900 MHz LO			0.54		°rms	Wide PLL loop bandwidth (300 kHz)
Spot Phase Noise						
1900 MHz LO						Narrow PLL loop bandwidth
100 kHz Offset			−100		dBc/Hz	
200 kHz Offset			−115		dBc/Hz	
400 kHz Offset			−120		dBc/Hz	
600 kHz Offset			−129		dBc/Hz	
800 kHz Offset			−132		dBc/Hz	
1.2 MHz Offset			−135		dBc/Hz	
1.8 MHz Offset			−140		dBc/Hz	
6 MHz Offset			−150		dBc/Hz	
10 MHz Offset			−153		dBc/Hz	
3800 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−104		dBc/Hz	
1.2 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	
5900 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−99		dBc/Hz	
1.2 MHz Offset			−119.7		dBc/Hz	
10 MHz Offset			−135.4		dBc/Hz	
LO PHASE SYNCHRONIZATION						Change in LO delay per temperature change
Phase deviation			1.6		ps/°C	
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	150		8000	MHz	Input frequency must be 2× the desired LO frequency
Input Signal Power		0		12	dBm	50 Ω matching at the source
			3		dBm	f_{EXTLO} ≤ 2 GHz, add 0.5 dBm/GHz above 2 GHz
			6		dBm	f_{EXTLO} = 8 GHz
External LO Input Signal Differential						To ensure adequate QEC
Phase Error				3.6	ps	
Amplitude Error				1	dB	
Duty Cycle Error				2	%	
Even-Order Harmonics				−50	dBc	
CLOCK SYNTHESIZER						
Integrated Phase Noise						1 kHz to 100 MHz
1966.08 MHz LO			0.4		°rms	PLL optimized for close in phase noise
Spot Phase Noise						
1966.08 MHz						
100 kHz Offset			−109		dBc/Hz	
1 MHz Offset			−129		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK (REF_CLK_IN)						
Frequency Range		10		1000	MHz	
Signal Level		0.3		2.0	V p-p	AC-coupled, common-mode voltage (V_{CM}) = 618 mV, use <1 V p-p input clock for best spurious performance
AUXILIARY CONVERTERS						
ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA_3P3 – 0.05		V	
DAC						
Resolution			10		Bits	Includes four offset levels
Output Voltage						
Minimum			0.7		V	1 V V_{REF}
Maximum			VDDA_3P3 – 0.3		V	2.5 V V_{REF}
Output Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS): SERIAL PERIPHERAL INTERFACE (SPI), GPIO_x						
Logic Inputs						
Input Voltage						
High Level		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Low Level		0		VDD_INTERFACE × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDD_INTERFACE × 0.8			V	
Low Level				VDD_INTERFACE × 0.2	V	
Drive Capability			3		mA	
DIGITAL SPECIFICATIONS (CMOS): GPIO_3P3_x						
Logic Inputs						
Input Voltage						
High Level		VDDA_3P3 × 0.8		VDDA_3P3	V	
Low Level		0		VDDA_3P3 × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Outputs						
Output Voltage						
High Level		VDDA_3P3 × 0.8			V	
Low Level				VDDA_3P3 × 0.2	V	
Drive Capability			4		mA	
DIGITAL SPECIFICATIONS, LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS)						
Logic Inputs (SYSREF_IN±, SYNCINx±)						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs ($\overline{\text{SYNCOUTx±}}$)						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Output Differential Voltage			225		mV	Programmable in 75 mV steps
Output Offset Voltage			1200		mV	
SPI TIMING						
SCLK Period	t_{CP}	20			ns	
SCLK Pulse Width	t_{MP}	10			ns	
$\overline{\text{CS}}$ Setup to First SCLK Rising Edge	t_{SC}	3			ns	
Last SCLK Falling Edge to $\overline{\text{CS}}$ Hold	t_{HC}	0			ns	
SDIO Data Input Setup to SCLK	t_S	2			ns	
SDIO Data Input Hold to SCLK	t_H	0			ns	
SCLK Rising Edge to Output Data Delay (3-Wire Mode or 4-Wire Mode)	t_{CO}	3		8	ns	
Bus Turnaround Time, Read After Baseband Processor (BBP) Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time, Read After ADRV9008-1 Drives Last Data Bit	t_{HZS}	0		t_{CO}	ns	
JESD204B DATA OUTPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate Per Channel (NRZ)		3125		12288	Mbps	
Rise Time	t_R	24	39.5		ps	20% to 80% in 100 Ω load
Fall Time	t_F	24	39.4		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Differential Output Voltage	V_{DIFF}	360	600	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance		80	94.2	120	Ω	
Total Jitter			15.13		ps	Bit error rate (BER) = 10^{-15}
Uncorrelated Bounded High Probability Jitter	UBHPJ		0.56		ps	
Duty Cycle Distortion	DCD		0.369		ps	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SYSREF_IN± Setup Time to REF_CLK_IN_x		2.5			ns	See Figure 2
SYSREF_IN± Hold Time to REF_CLK_IN_x		−1.5			ns	See Figure 2
Latency	T_{LAT_FRM}					REF_CLK_IN = 245.76 MHz
			89.4		Clock cycles	Rx bandwidth = 200 MHz, IQ rate = 245.76 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			364.18		ns	

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

CURRENT AND POWER CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS					
VDDA1P3[1] Analog Supply	1.267	1.3	1.33	V	
VDDD1P3_DIG Supply	1.267	1.3	1.33	V	
VDDA1P8_AN Supply	1.71	1.8	1.89	V	
VDDA1P8_BB Supply	1.71	1.8	1.89	V	
VDD_INTERFACE Supply	1.71	1.8	2.625	V	CMOS and LVDS supply, 1.8 V to 2.5 V nominal range
VDDA_3P3 Supply	3.135	3.3	3.465	V	
POSITIVE SUPPLY CURRENT					LO at 2600 MHz
200 MHz Rx Bandwidth					Two receivers enabled
VDDA1P3[1] Analog Supply		1645		mA	
VDDD1P3_DIG Supply		984		mA	Rx QEC active
VDDA1P8_AN Supply		0.4		mA	
VDDA1P8_BB Supply		68		mA	
VDD_INTERFACE Supply		8		mA	
VDDA_3P3 Supply		3		mA	No AUXDAC_x or AUXADC_x enabled (if enabled, AUXADC_x adds 2.7 mA, and each AUXDAC_x adds 1.5 mA)
Total Power Dissipation		3.57		W	Typical supply voltages, Rx QEC active

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

TIMING DIAGRAMS

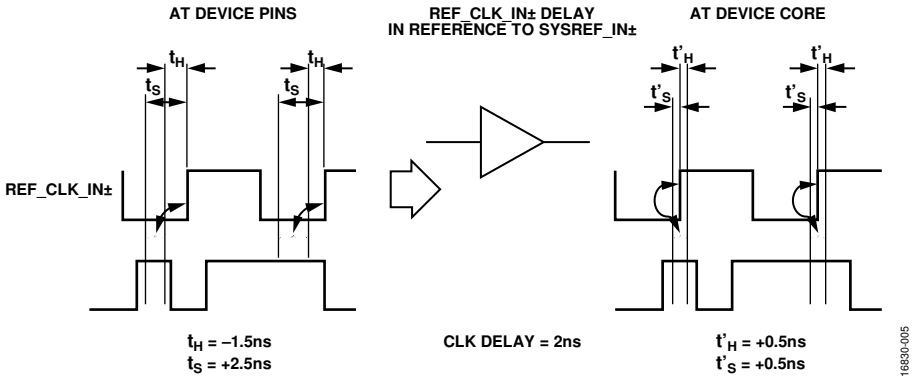

Figure 2. SYSREF_IN± Setup and Hold Timing

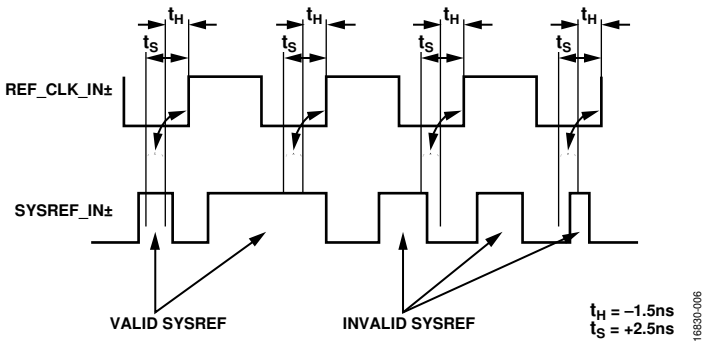

Figure 3. SYSREF_IN± Setup and Hold Timing Examples, Relative to Device Clock

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDA1P3[1] to VSSA	−0.3 V to +1.4 V
VDDD1P3_DIG to VSSD	−0.3 V to +1.4 V
VDD_INTERFACE to VSSA	−0.3 V to +3.0 V
VDDA_3P3 to VSSA	−0.3 V to +3.9 V
VDD_INTERFACE Logic Inputs and Outputs to VSSD	−0.3 V to VDD_INTERFACE + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VDDA1P3_SER
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Port	23 dBm (peak)
Maximum Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_CLOCK_SYNTH, VDDA1P3_RX_LO_BUFFER, and VDDA1P3_CLOCK.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The ADRV9008-1 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL MANAGEMENT

The ADRV9008-1 is a high power device that can dissipate over 3 W depending on the user application and configuration. Because of the power dissipation, the ADRV9008-1 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 4 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum junction temperature shown in Table 3. The device is designed for a lifetime of 10 years when operating at the maximum junction temperature.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance data for the ADRV9008-1 mounted on both a JEDEC 2S2P test board and a 10-layer Analog Devices, Inc., evaluation board are listed in Table 4. Do not exceed the absolute maximum junction temperature rating in Table 3. 10-layer PCB entries refer to the 10-layer Analog Devices evaluation board, which more accurately reflects the PCB used in customer applications.

Table 4. Thermal Resistance[1, 2]

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-196-13	21.1	0.04	4.9	0.3	4.9	°C/W

[1] For the θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 thermal conductivity watts/(meter × Kelvin).
[2] Using enhanced heat removal techniques such as PCB, heat sink, and airflow improves the thermal resistance values.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

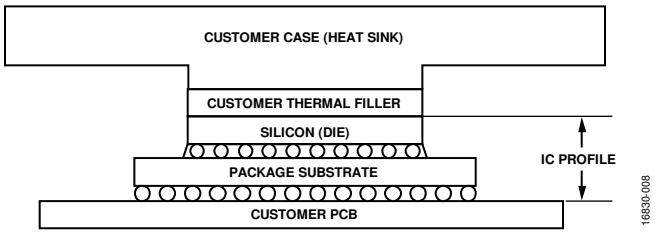

Figure 4. Typical Thermal Management Solution

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	VSSA	VSSA	VSSA	RX2_IN+	RX2_IN–	VSSA	VSSA	RX1_IN+	RX1_IN–	VSSA	VSSA	VSSA	VSSA
B	VDDA1P3_ RX_RF	VSSA	VSSA	VSSA	VSSA	VSSA	RF_EXT_ LO_I/O–	RF_EXT_ LO_I/O+	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
C	GPIO_3p3_0	GPIO_3p3_3	VDDA1P3_RX	VSSA	VDDA1P3_ RF_VCO_LDO	VDDA1P3_RF_ VCO_LDO	VDDA1P1_ RF_VCO	VDDA1P3_ RF_LO	VSSA	VDDA1P3_ AUX_VCO_ LDO	VSSA	VDDA_3P3	GPIO_3p3_9	RBIAS
D	GPIO_3p3_1	GPIO_3p3_4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VDDA1P1_ AUX_VCO	VSSA	VSSA	GPIO_3p3_8	GPIO_3p3_10
E	GPIO_3p3_2	GPIO_3p3_5	GPIO_3p3_6	VDDA1P8_BB	VDDA1P3_BB	VSSA	REF_CLK_IN+	REF_CLK_IN–	VSSA	AUX_SYNTH_ OUT	AUXADC_3	VDDA1P8_AN	GPIO_3p3_7	GPIO_3p3_11
F	VSSA	VSSA	AUXADC_0	AUXADC_1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	AUXADC_2	VSSA	VSSA	VSSA
G	VSSA	VSSA	VSSA	VSSA	VDDA1P3_ CLOCK_ SYNTH	VSSA	VDDA1P3 RF_SYNTH	VDDA1P3 AUX_SYNTH	RF_SYNTH_ VTUNE	VSSA	VSSA	VSSA	VSSA	VSSA
H	DNC	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	GPIO_12	GPIO_11	VSSA	DNC
J	DNC	VSSA	GPIO_18	$\overline{\text{RESET}}$	GP INTERRUPT	TEST	GPIO_2	GPIO_1	SDIO	SDO	GPIO_13	GPIO_10	VSSA	DNC
K	VSSA	VSSA	SYSREF_IN+	SYSREF_IN–	GPIO_5	GPIO_4	GPIO_3	GPIO_0	SCLK	$\overline{\text{CS}}$	GPIO_14	GPIO_9	VSSA	VSSA
L	VSSA	VSSA	$\overline{\text{SYNCIN1–}}$	$\overline{\text{SYNCIN1+}}$	GPIO_6	GPIO_7	VSSD	VDDD1P3_ DIG	VDDD1P3_ DIG	VSSD	GPIO_15	GPIO_8	VDDA1P3_ SER	VDDA1P3_ SER
M	VDDA1P1_ CLOCK_VCO	VSSA	$\overline{\text{SYNCIN0–}}$	$\overline{\text{SYNCIN0+}}$	RX1_ENABLE	VSSD	RX2_ENABLE	VSSD	VSSA	GPIO_17	GPIO_16	VDD_ INTERFACE	VDDA1P3_ SER	VDDA1P3_ SER
N	VDDA1P3_ CLOCK_ VCO_LDO	VSSA	SERDOUT3–	SERDOUT3+	SERDOUT2–	SERDOUT2+	VSSA	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER	VSSA
P	AUX_SYNTH_ VTUNE	VSSA	VSSA	SERDOUT1–	SERDOUT1+	SERDOUT0–	SERDOUT0+	VDDA1P3_ SER	VDDA1P3_ SER	VSSA	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER	VDDA1P3_ SER

ADRV9008-1

16830-900

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1, A2, A3, A4, A7, A8, A11, A12, A13, A14, B2, B3, B4, B5, B6, B9, B10, B11, B12, B13, B14, C4, C9, C11, D3, D4, D5, D6, D7, D8, D9, D11, D12, E6, E9, F1, F2, F5, F6, F7, F8, F9, F10, F12, F13, F14, G1, G2, G3, G4, G6, G10, G11, G12, G13, G14, H2, H3, H4, H5, H6, H7, H8, H9, H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10	Input	VSSA	Analog Supply Voltage (V_{SS}).
A5, A6	Input	RX2_IN+, RX2_IN−	Differential Input for Receiver 1. When unused, connect these pins to ground.
A9, A10	Input	RX1_IN+, RX1_IN−	Differential Input for Receiver 2. When unused, connect these pins to ground.
B1	Input	VDDA1P3_RX_RF	Receiver Mixer Supply.
B7, B8	Input	RF_EXT_LO_I/O−, RF_EXT_LO_I/O+	Differential External LO Input/Output. If these pins are used for external LO, input frequency must be 2× the desired carrier frequency. When unused, do not connect these pins.
C1	Input/ output	GPIO_3p3_0	GPIO Pin Referenced to 3.3 V Supply. The alternate function is AUXDAC_4. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or this pin can be left floating, programmed as outputs, and driven low.
C2	Input/ output	GPIO_3p3_3	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
C13	Input/ output	GPIO_3p3_9	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_9. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D1	Input/ output	GPIO_3p3_1	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_5. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D2	Input/ output	GPIO_3p3_4	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_6. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D13	Input/ output	GPIO_3p3_8	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.

Pin No.	Type	Mnemonic	Description
D14	Input/ output	GPIO_3p3_10	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E1	Input/ output	GPIO_3p3_2	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E2	Input/ output	GPIO_3p3_5	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_7. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E3	Input/ output	GPIO_3p3_6	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_8. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E13	Input/ output	GPIO_3p3_7	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_2. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E14	Input/ output	GPIO_3p3_11	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_3. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
C3	Input	VDDA1P3_RX	1.3 V Supply for Receiver Baseband Circuits, Transimpedance Amplifier (TIA), Baseband Filters, and Auxiliary DACs.
C5, C6	Input	VDDA1P3_RF_VCO_LDO	RF VCO Low Dropout (LDO) Supply Inputs. Connect Pin C5 to Pin C6. Use a separate trace to a common supply point.
C7	Input	VDDA1P1_RF_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
C8	Input	VDDA1P3_RF_LO	1.3 V LO Generator for RF Synthesizer. This pin is sensitive to aggressors.
C10	Input	VDDA1P3_AUX_VCO_LDO	1.3 V Supply.
C12	Input	VDDA_3P3	General-Purpose Output Pull-Up Voltage and Auxiliary DAC Supply Voltage.
C14	Input/ output	RBIAS	Bias Resistor. Tie this pin to ground using a 14.3 kΩ resistor. This pin generates an internal current based on an external 1% resistor.
D10	Input	VDDA1P1_AUX_VCO	1.1 V VCO Supply. Decouple with 1 µF.
E4	Input	VDDA1P8_BB	1.8 V Supply for the ADC and DAC.
E5	Input	VDDA1P3_BB	1.3 V Supply for ADC, DAC, and AUXADC.
E7, E8	Input	REF_CLK_IN+, REF_CLK_IN–	Device Clock Differential Input.
E10	Output	AUX_SYNTH_OUT	Auxiliary PLL Output. When unused, do not connect this pin.
E12	Input	VDDA1P8_AN	1.8 V Bias Supply for Analog Circuitry.
F3, F4, F11, E11	Input	AUXADC_0 to AUXADC_3	Auxiliary ADC Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
G5	Input	VDDA1P3_CLOCK_SYNTH	1.3 V Supply Input for Clock Synthesizer. Use a separate trace on the PCB back to a common supply point.

Pin No.	Type	Mnemonic	Description
G7	Input	VDDA1P3_RF_SYNTH	1.3 V RF Synthesizer Supply Input. This pin is sensitive to aggressors.
G8	Input	VDDA1P3_AUX_SYNTH	1.3 V Auxiliary Synthesizer Supply Input.
G9	Output	RF_SYNTH_VTUNE	RF Synthesizer VTUNE Output.
H1, J1, H14, J14	DNC	DNC	Do Not Connect These Pins.
H11	Input/ output	GPIO_12	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
H12	Input/ output	GPIO_11	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J11	Input/ output	GPIO_13	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J12	Input/ output	GPIO_10	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J3	Input/ output	GPIO_18	Digital GPIO, 1.8 V to 2.5 V. The joint test action group (JTAG) function is TCLK. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J7	Input/ output	GPIO_2	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J8	Input/ output	GPIO_1	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K5	Input/ output	GPIO_5	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDO. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K6	Input/ output	GPIO_4	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is $\overline{\text{TRST}}$. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.

Pin No.	Type	Mnemonic	Description
K7	Input/ output	GPIO_3	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K8	Input/ output	GPIO_0	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K11	Input/ output	GPIO_14	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K12	Input/ output	GPIO_9	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L5	Input/ output	GPIO_6	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDI. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L6	Input/ output	GPIO_7	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TMS. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L11	Input/ output	GPIO_15	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L12	Input/ output	GPIO_8	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
M10	Input/ output	GPIO_17	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
M11	Input/ output	GPIO_16	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J10	Output	SDO	Serial Data Output. In SPI 3-Wire mode, do not connect this pin.
J4	Input	$\overline{\text{RESET}}$	Active Low Chip Reset.
J5	Output	GP_INTERRUPT	General-Purpose Digital Interrupt Output Signal. When unused, do not connect this pin.
J6	Input	TEST	Pin Used for JTAG Boundary Scan. When unused, connect this pin to ground.
J9	Input/ output	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.

Pin No.	Type	Mnemonic	Description
K10	Input	$\overline{CS}$	Serial Data Bus Chip Select, Active Low.
K3, K4	Input	SYSREF_IN+, SYSREF_IN−	LVDS Input.
K9	Input	SCLK	Serial Data Bus Clock.
L13, L14, M13, M14, N8 to N12, N13, P8, P9, P11 to P14	Input	VDDA1P3_SER	1.3 V Supply for JESD204B Serializer.
L3, L4	Input	$\overline{SYNCIN1-}$, $\overline{SYNCIN1+}$	LVDS Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
L7, L10, M6, M8	Input	VSSD	Digital V_{SS}.
L8, L9	Input	VDDD1P3_DIG	1.3 V Digital Core. Connect Pin L8 to Pin L9. Use a separate trace to a common supply point.
M1	Input	VDDA1P1_CLOCK_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
M12	Input	VDD_INTERFACE	Input/Output Interface Supply, 1.8 V to 2.5 V.
M3, M4	Input	$\overline{SYNCIN0-}$, $\overline{SYNCIN0+}$	JESD204B Receiver Channel 1. These pins form the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
M5	Input	RX1_ENABLE	Receiver 1 Enable Pin. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
M7	Input	RX2_ENABLE	Receiver 2 Enable Pin. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
N1	Input	VDDA1P3_CLOCK_VCO_LDO	1.3 V. Use a separate trace to a common supply point.
N3, N4	Output	SERDOUT3−, SERDOUT3+	RF Current Mode Logic (CML) Differential Output 3. When unused, do not connect these pins.
N5, N6	Output	SERDOUT2−, SERDOUT2+	RF CML Differential Output 2. When unused, do not connect these pins.
P1	Output	AUX_SYNTH_VTUNE	Auxiliary Synthesizer VTUNE Output.
P4, P5	Output	SERDOUT1−, SERDOUT1+	RF CML Differential Output 1. When unused, do not connect these pins.
P6, P7	Output	SERDOUT0−, SERDOUT0+	RF CML Differential Output 0. When unused, do not connect these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

The temperature settings refer to the die temperature.

75 MHz TO 525 MHz BAND

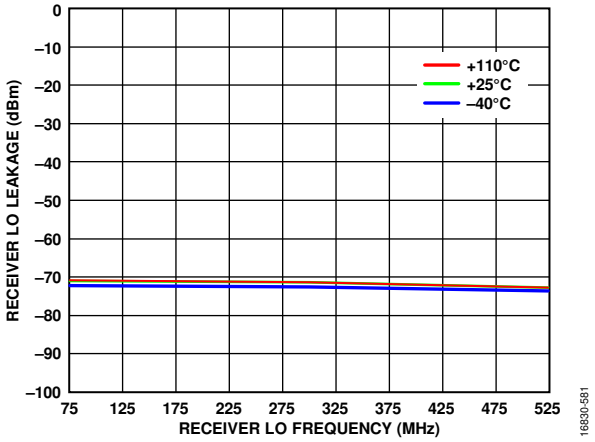

Figure 6. Receiver LO Leakage vs. Receiver LO Frequency, LO = 75 MHz, 300 MHz, and 525 MHz, 0 dB Receiver Attenuation, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate

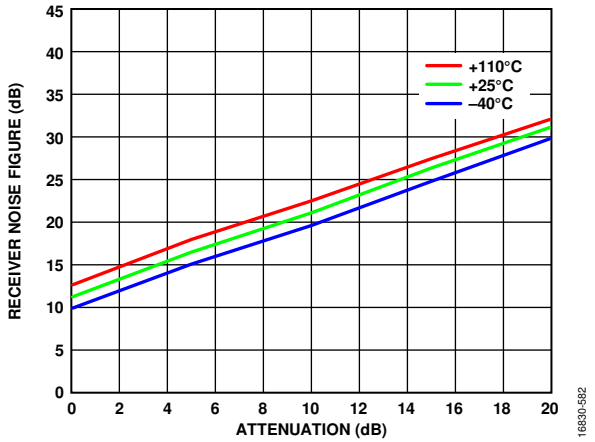

Figure 7. Receiver Noise Figure vs. Attenuation, LO = 75 MHz, 50 MHz Bandwidth, 61.44 MSPS Sample Rate, 1 MHz to 25 MHz Integration Bandwidth

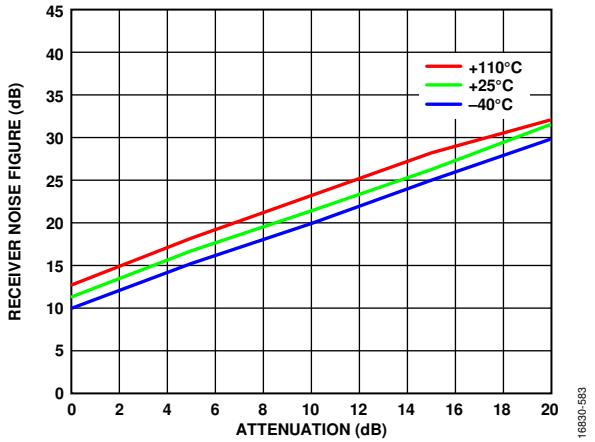

Figure 8. Receiver Noise Figure vs. Attenuation, 300 MHz LO, 50 MHz Bandwidth, 61.44 MSPS Sample Rate, 1 MHz to 25 MHz Integration Bandwidth

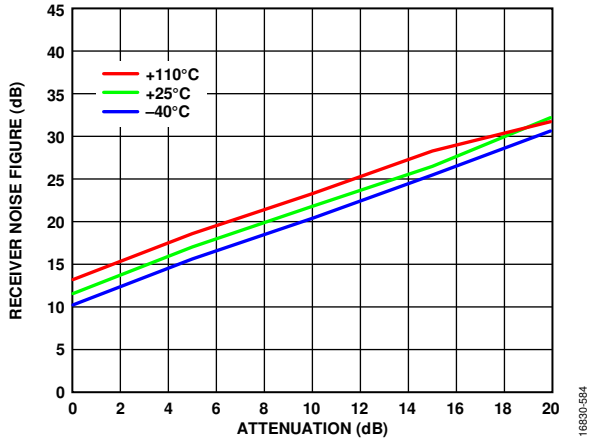

Figure 9. Receiver Noise Figure vs. Attenuation, LO = 525 MHz, 50 MHz Bandwidth, 61.44 MSPS Sample Rate, 1 MHz to 25 MHz Integration Bandwidth

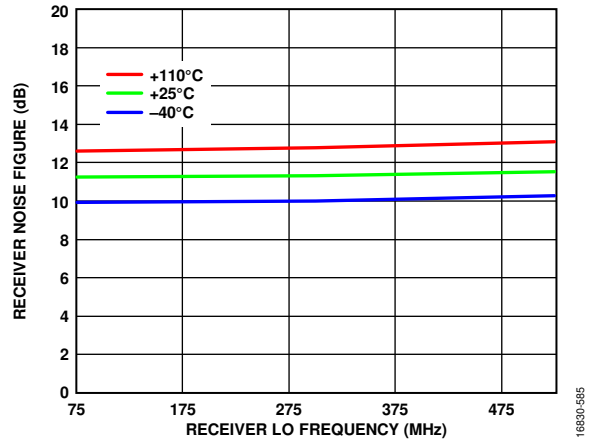

Figure 10. Receiver Noise Figure vs. Receiver LO Frequency, 0 dB Receiver Attenuation, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate, ±25 MHz Integration Bandwidth

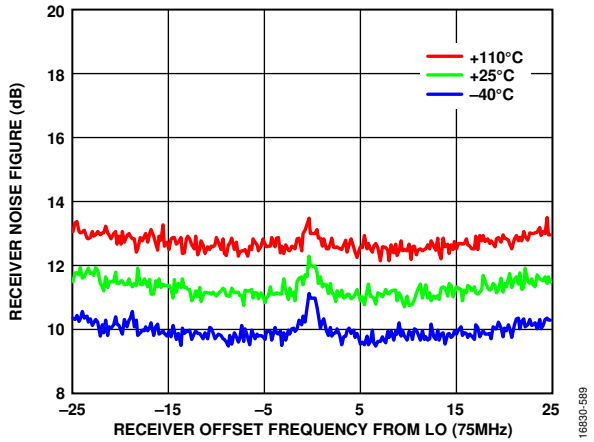

Figure 11. Receiver Noise Figure vs. Receiver Offset Frequency from LO, 200 kHz Integration Bandwidth, LO = 75 MHz

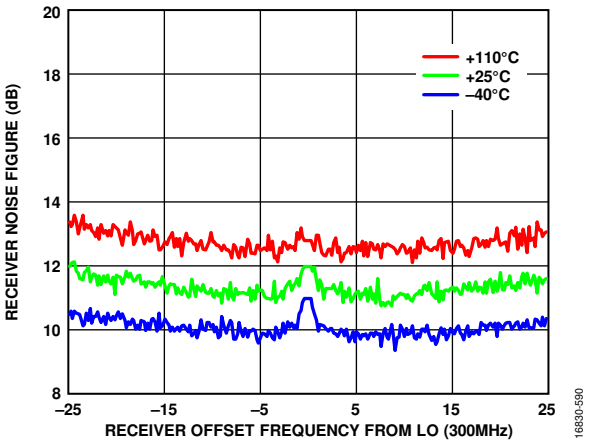

Figure 12. Receiver Noise Figure vs. Receiver Offset Frequency from LO, 200 kHz Integration Bandwidth, LO = 300 MHz

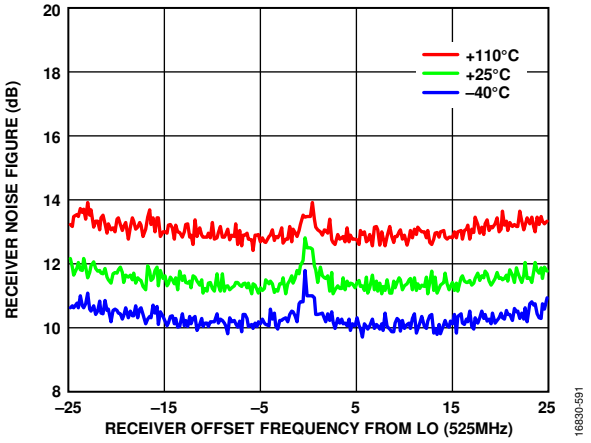

Figure 13. Receiver Noise Figure vs. Receiver Offset Frequency from LO, 200 kHz Integration Bandwidth, LO = 525 MHz

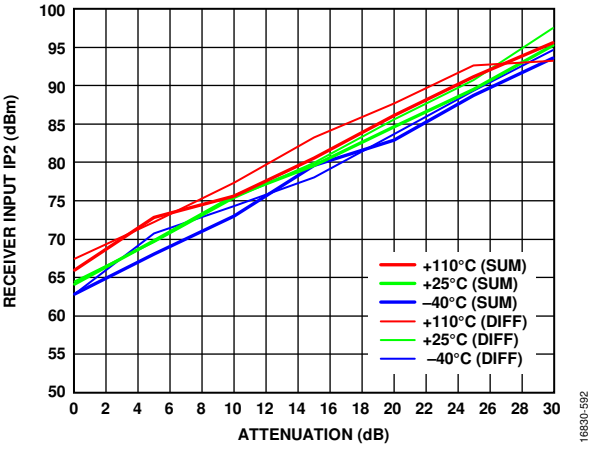

Figure 14. Receiver IIP2 vs. Attenuation, LO = 75 MHz, Tones Placed at 82.5 MHz and 83.5 MHz, –23.5 dBm Plus Attenuation

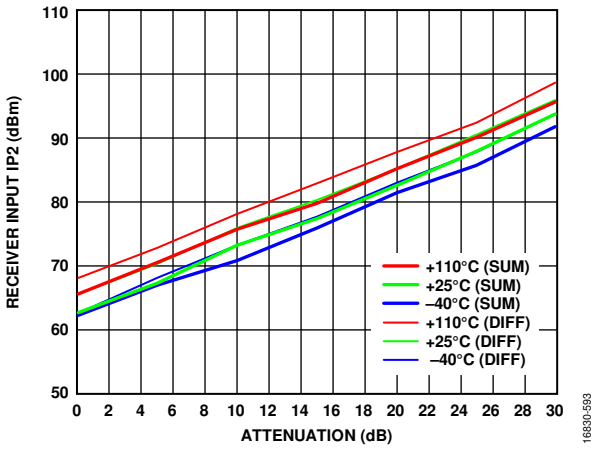

Figure 15. Receiver IIP2 vs. Attenuation, LO = 300 MHz, Tones Placed at 310 MHz and 311 MHz, –23.5 dBm Plus Attenuation

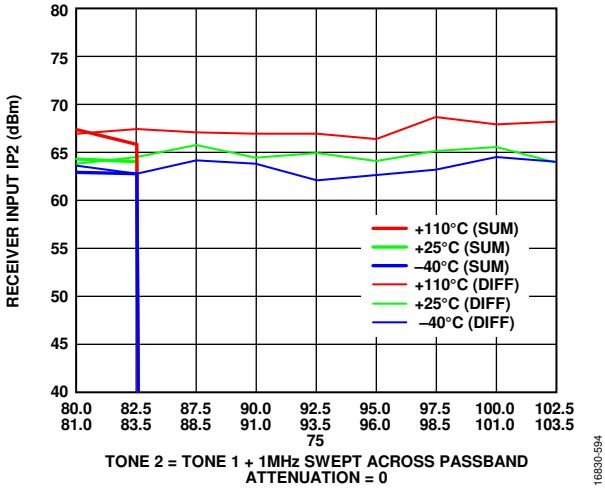

Figure 16. Receiver IIP2 Sum and Difference Across Bandwidth, 0 dB Receiver Attenuation, LO = 75 MHz, 10 Tone pairs, –23.5 dBm Each

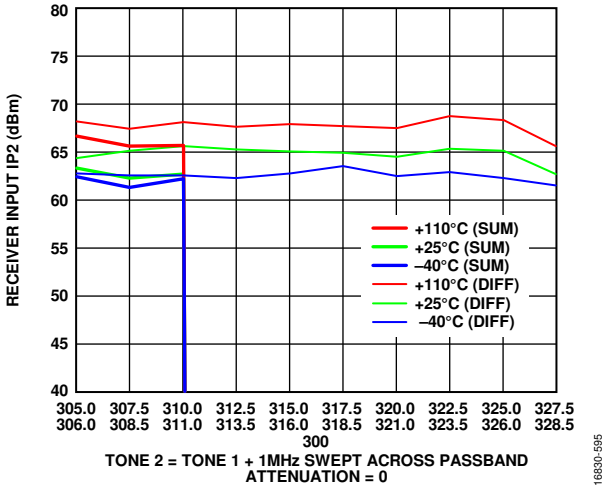

Figure 17. Receiver IIP2 Sum and Difference Across Bandwidth, 0 dB Receiver Attenuation, LO = 300 MHz, 10 Tone pairs, –23.5 dBm Each

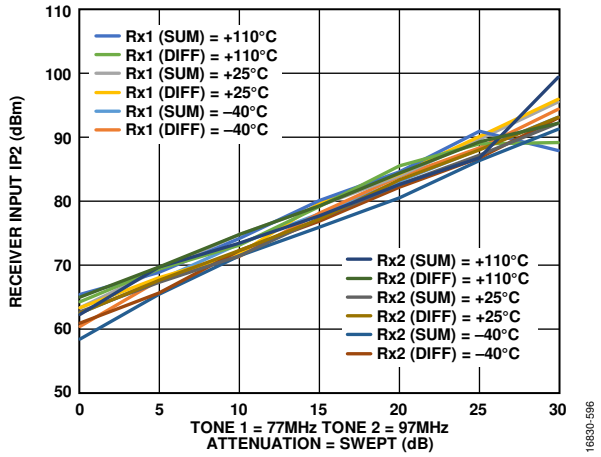

Figure 18. Receiver IIP2 vs. Receiver Attenuation, LO = 75 MHz, Tones Placed at 77 MHz and 97 MHz, –23.5 dBm Plus Attenuation

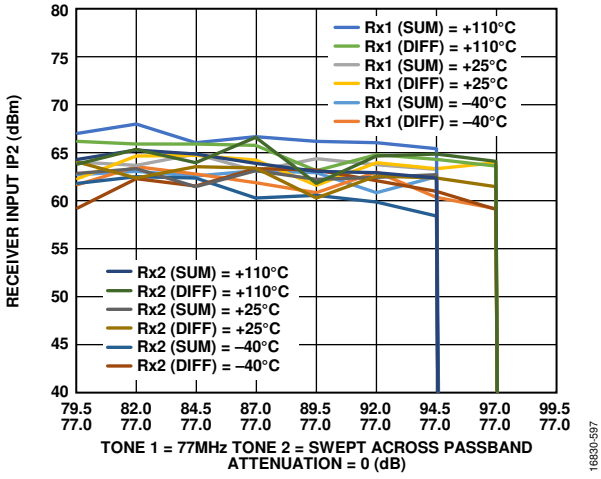

Figure 19. Receiver IIP2 Sum and Difference Across Bandwidth, 0 dB Receiver Attenuation, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 Swept, –23.5 dBm Each

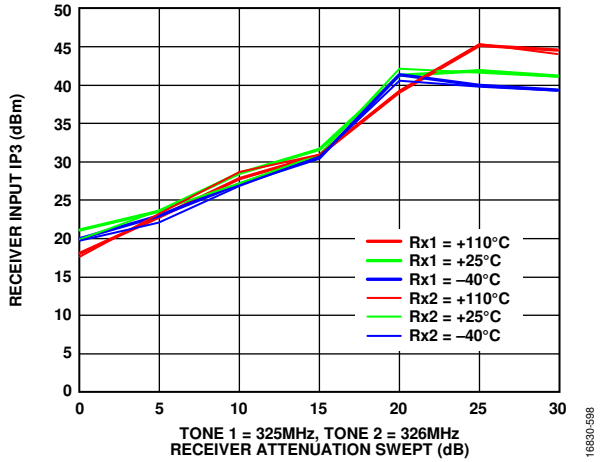

Figure 20. Receiver IIP3 vs. Attenuation, 300 MHz LO, Tone 1 = 325 MHz, Tone 2 = 326 MHz, –21 dBm Plus Attenuation

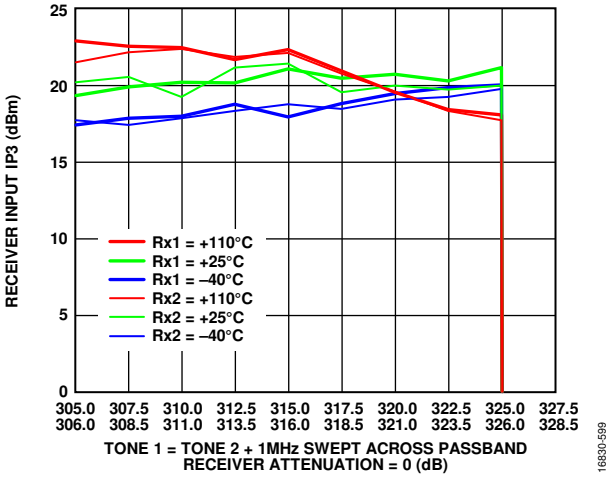

Figure 21. Receiver IIP3 Across Bandwidth, 0 dB Receiver Attenuation, LO = 300 MHz, Tone 1 = Tone 2 + 1 MHz, –21 dBm Each, Swept Across Pass Band

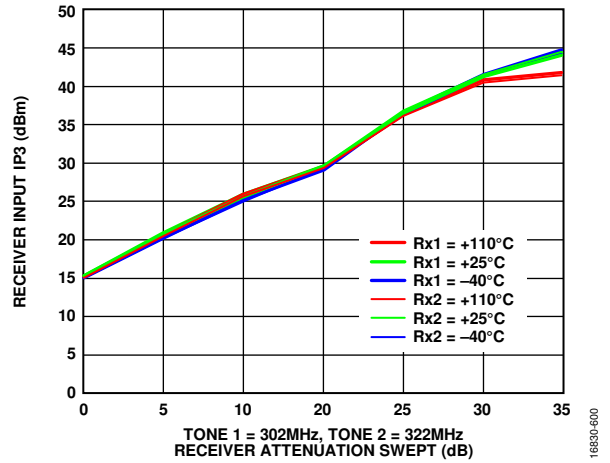

Figure 22. Receiver IIP3 vs. Attenuation, 300 MHz LO, Tone 1 = 302 MHz, Tone 2 = 322 MHz, –19 dBm Plus Attenuation

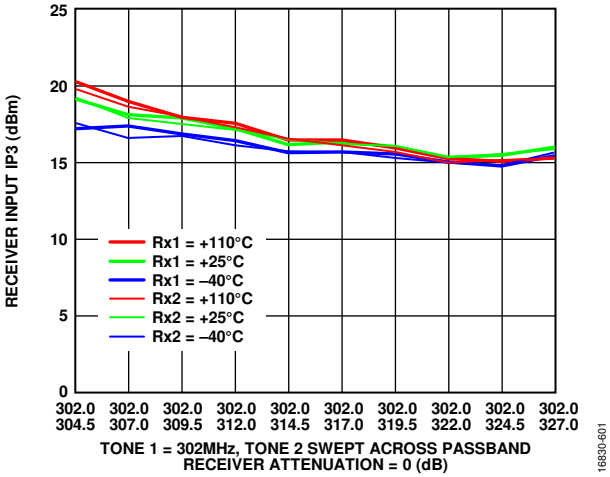

Figure 23. Receiver IIP3 Across Bandwidth, 0 dB Receiver Attenuation, 300 MHz LO, Tone 1 = 302 MHz, Tone 2 Swept Across Pass Band, –19 dBm Each

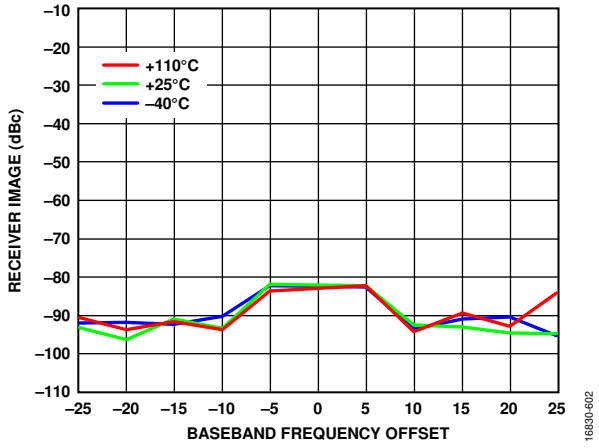

Figure 24. Receiver Image vs. Baseband Frequency Offset, 0 dB Attenuation, 50 MHz RF Bandwidth, Tracking Calibration Active, 61.44 MSPS Sample Rate, LO = 75 MHz

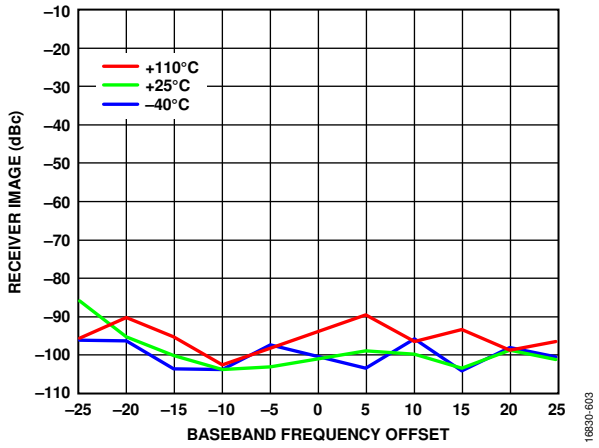

Figure 25. Receiver Image vs. Baseband Frequency Offset, 0 dB Attenuation, 50 MHz RF Bandwidth, Tracking Calibration Active, 61.44 MSPS Sample Rate, LO= 300 MHz

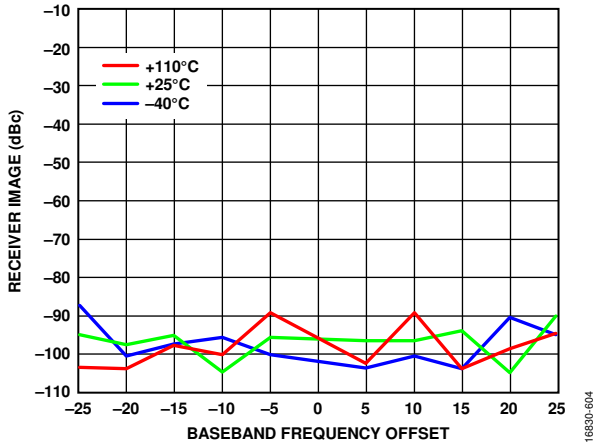

Figure 26. Receiver Image vs. Baseband Frequency Offset, 0 dB Attenuation, 50 MHz RF Bandwidth, Tracking Calibration Active, 61.44 MSPS Sample Rate, LO = 525 MHz

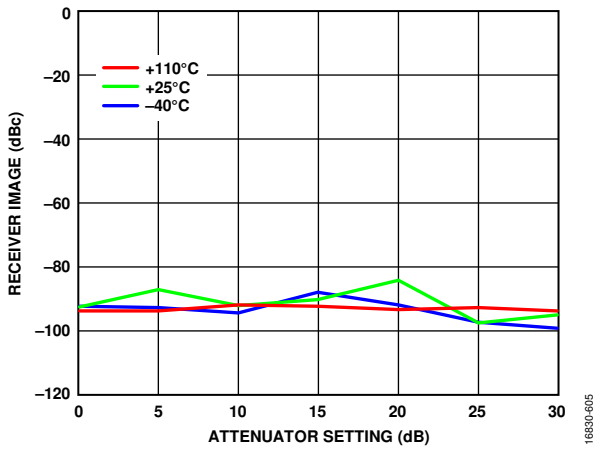

Figure 27. Receiver Image vs. Attenuator Setting, 25 MHz RF Bandwidth, Tracking Calibration Active, 61.44 MSPS Sample Rate, LO = 75 MHz, Baseband Frequency = 25 MHz

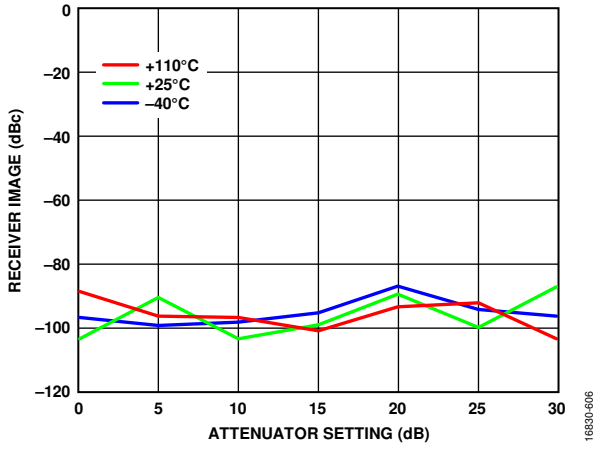

Figure 28. Receiver Image vs. Attenuator Setting, 25 MHz RF Bandwidth, Tracking Calibration Active, 61.44 MSPS Sample Rate, LO = 325 MHz, Baseband Frequency = 25 MHz

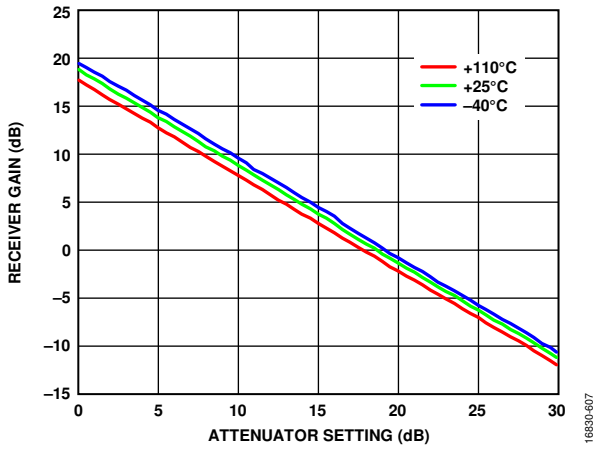

Figure 29. Receiver Gain vs. Attenuator Setting, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate, LO = 75 MHz

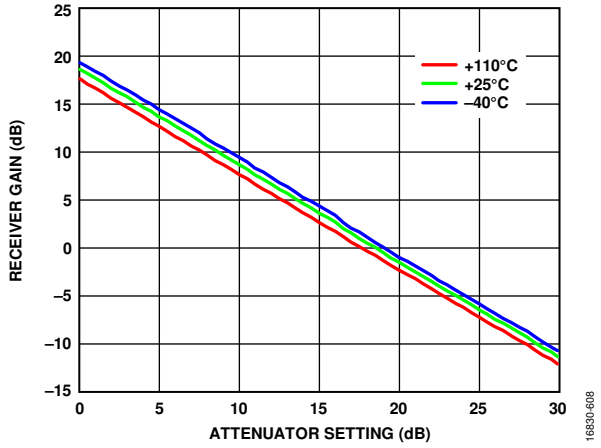

Figure 30. Receiver Gain vs. Attenuator Setting, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate, LO = 325 MHz

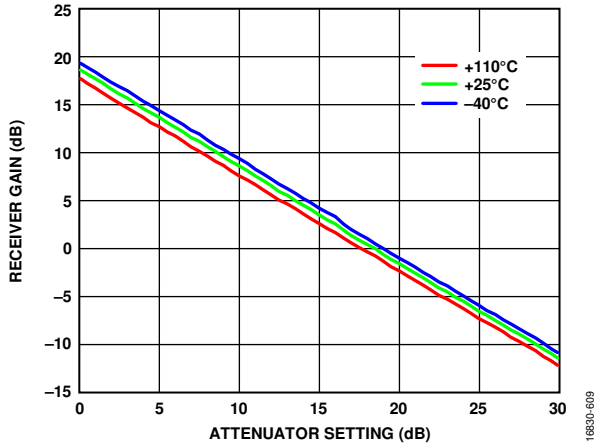

Figure 31. Receiver Gain vs. Attenuator Setting, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate, LO = 525 MHz

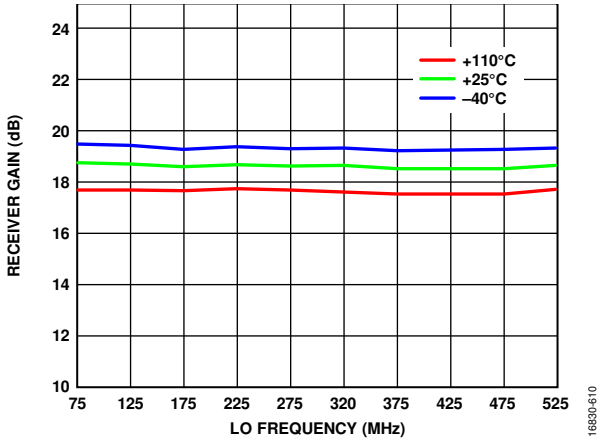

Figure 32. Receiver Gain vs. LO Frequency, 50 MHz RF Bandwidth, 61.44 MSPS Sample Rate

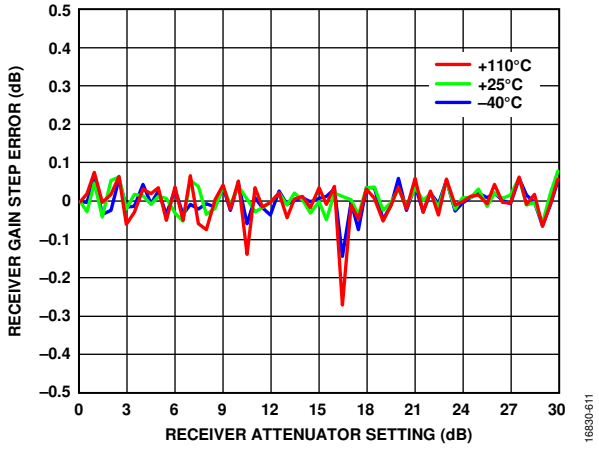

Figure 33. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 75 MHz

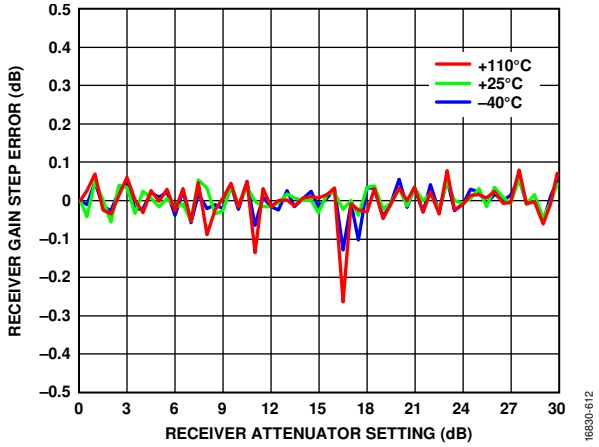

Figure 34. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 325 MHz

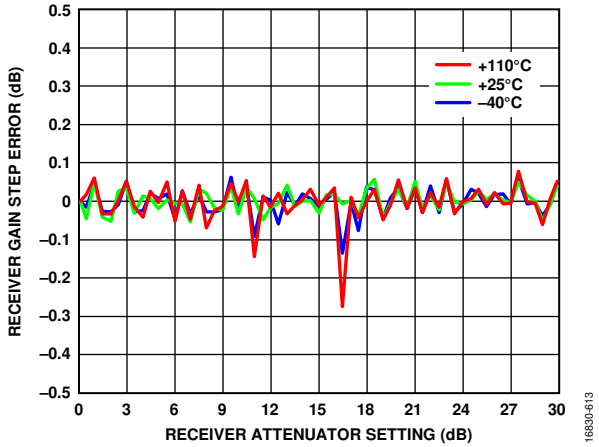

Figure 35. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 525 MHz

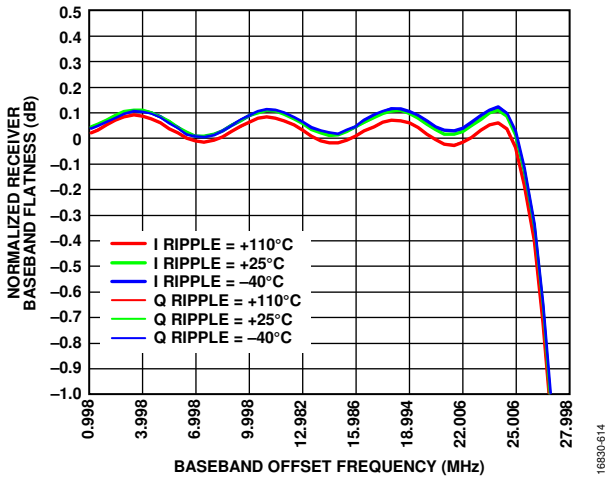

Figure 36. Normalized Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 75 MHz

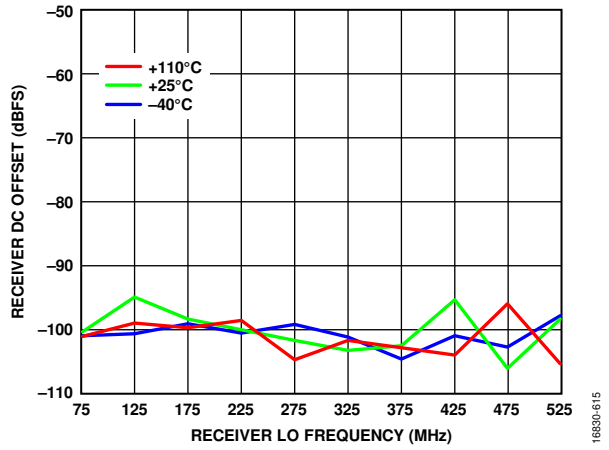

Figure 37. Receiver DC Offset vs. Receiver LO Frequency

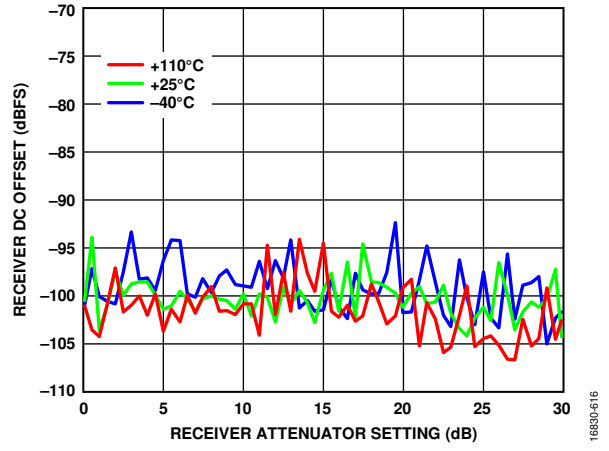

Figure 38. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 75 MHz

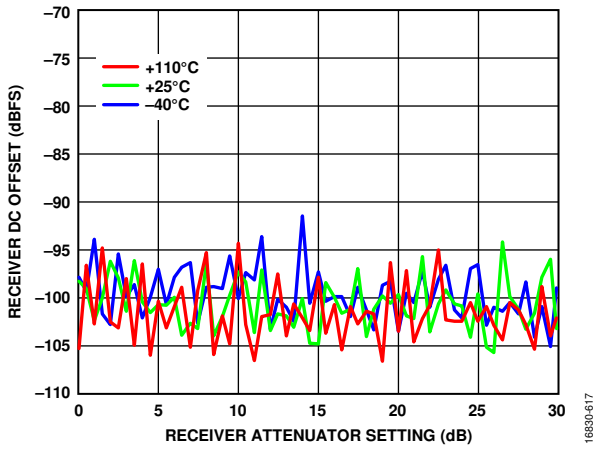

Figure 39. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 525 MHz

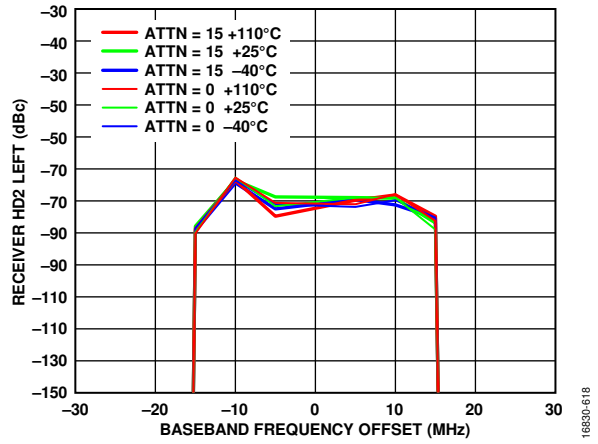

Figure 40. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation. Tone Level –21 dBm at Attenuation = 0. X-Axis is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product is 2× Baseband Frequency). HD2 Canceller Disabled. LO = 75 MHz.

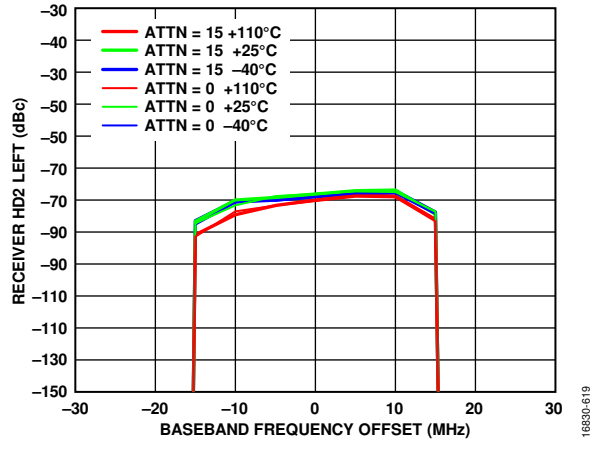

Figure 41. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation. Tone Level –21 dBm at Attenuation = 0. X-Axis is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product is 2× Baseband Frequency). HD2 Canceller Disabled. LO = 300 MHz.

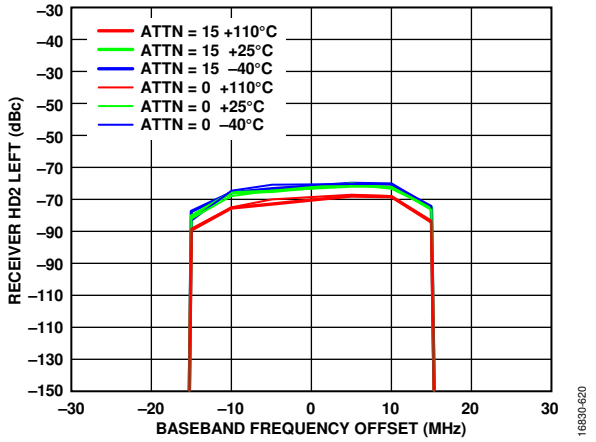

Figure 42. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation. Tone Level –21 dBm at Attenuation = 0. X-Axis = Baseband Frequency Offset of Fundamental Tone and Not Frequency of HD2 Product (HD2 Product = 2× Baseband Frequency). HD2 Canceller Disabled, LO = 525 MHz.

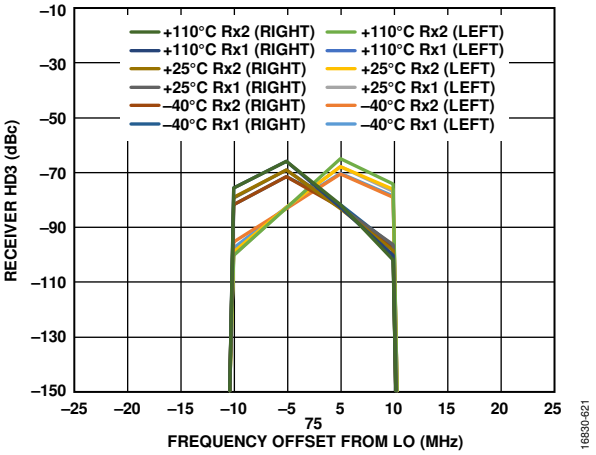

Figure 43. Receiver HD3 Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level –16 dBm at Attenuation = 0, LO = 75 MHz

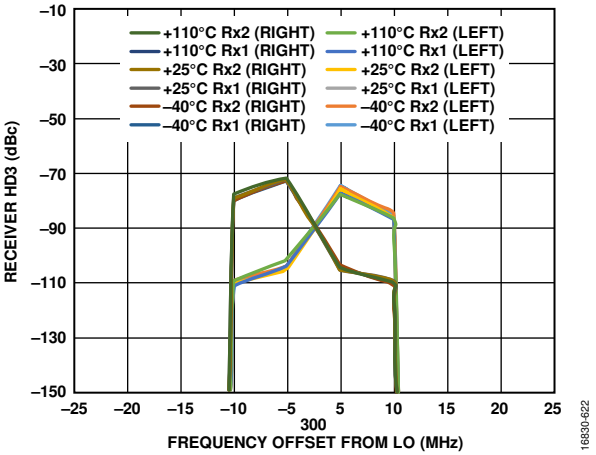

Figure 44. Receiver HD3 Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level –17 dBm at Attenuation = 0, LO = 300 MHz

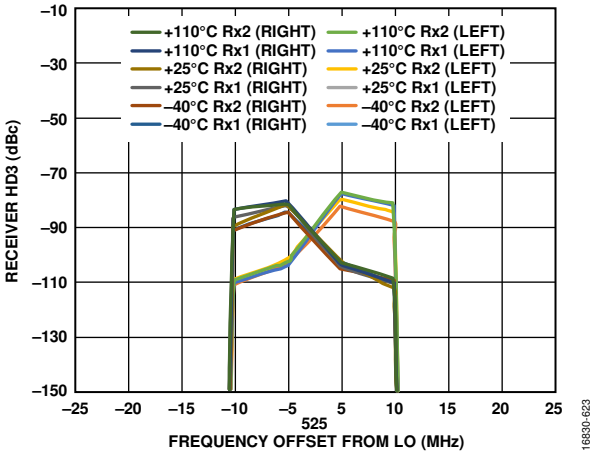

Figure 45. Receiver HD3 Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level –17 dBm at Attenuation = 0, LO = 525 MHz

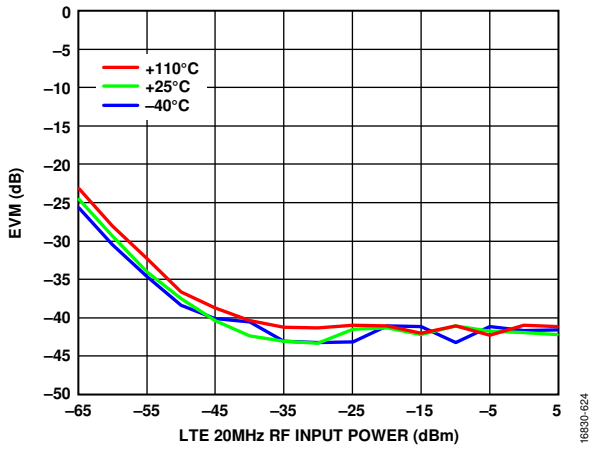

Figure 46. Error Vector Magnitude (EVM) vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 75 MHz, Default AGC Settings

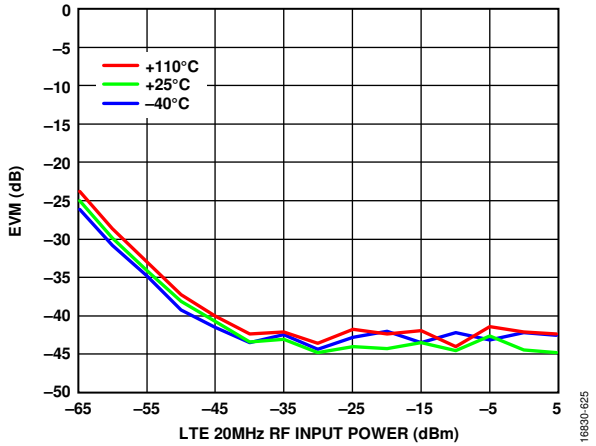

Figure 47. EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 300 MHz, Default AGC Settings

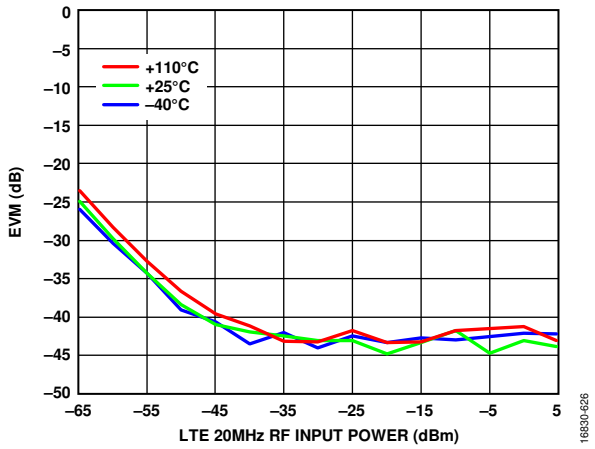

Figure 48. EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 525 MHz, Default AGC Settings

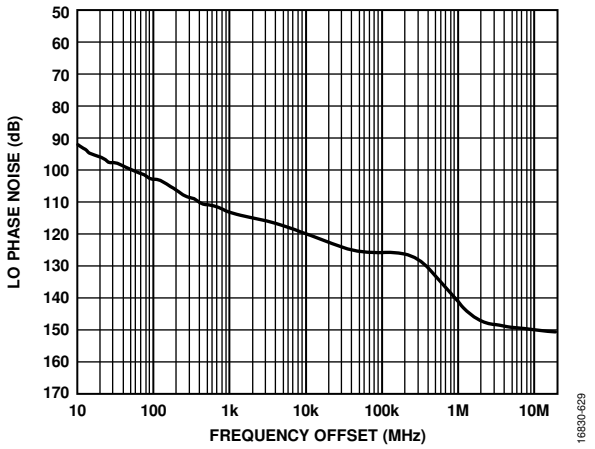

Figure 51. LO Phase Noise vs. Frequency Offset, LO = 300 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

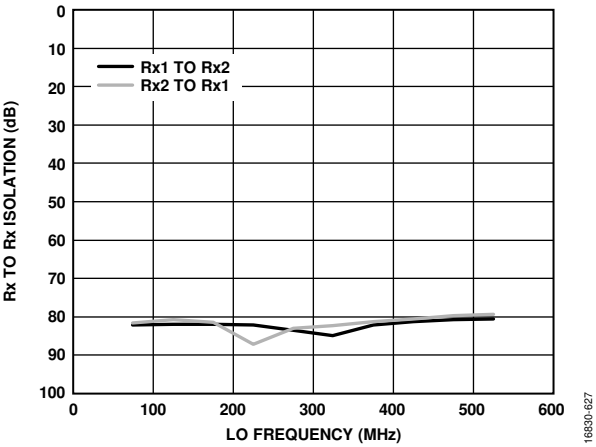

Figure 49. Receiver to Receiver Isolation vs. LO Frequency, 10 MHz Baseband Frequency

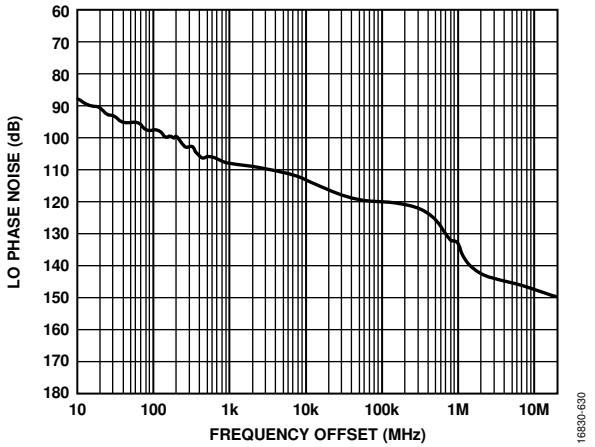

Figure 52. LO Phase Noise vs. Frequency Offset, LO = 525 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

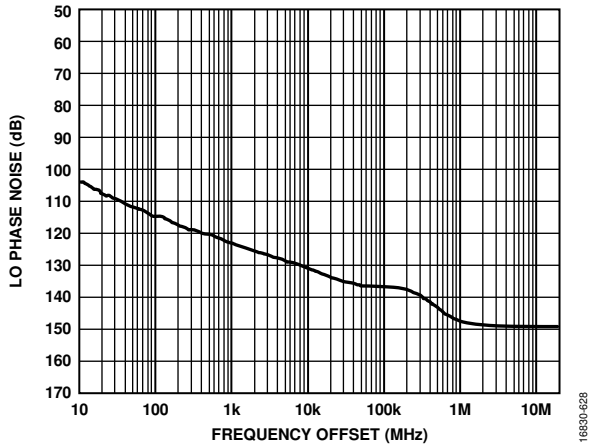

Figure 50. LO Phase Noise vs. Frequency Offset, LO = 75 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz

650 MHz TO 3000 MHz BAND

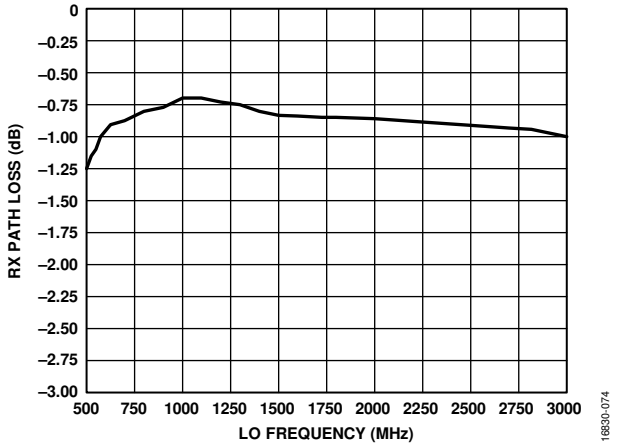

Figure 53. Receiver Matching Circuit Path Loss vs. LO Frequency, Used for Deembedding Performance Data

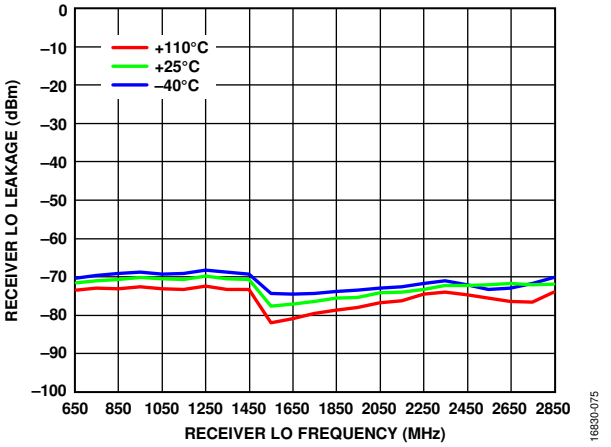

Figure 54. Receiver LO Leakage vs. Receiver LO Frequency, 0 dB Receiver Attenuation, 200 MHz RF Bandwidth, 245.76 MSPS Sample Rate

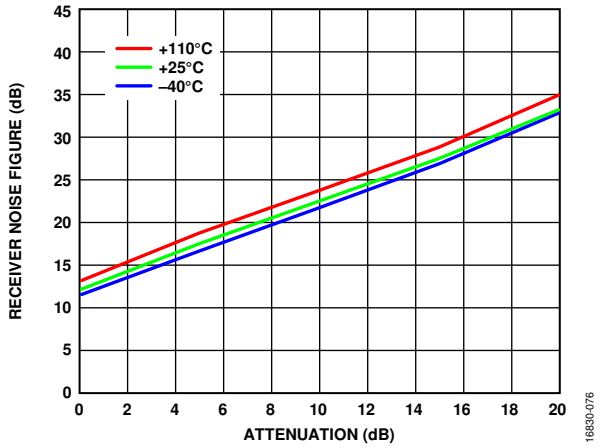

Figure 55. Receiver Noise Figure vs. Attenuation, 650 MHz LO, 200 MHz Bandwidth, 245.76 MSPS Sample Rate, 500 kHz to 100 MHz Integration Bandwidth

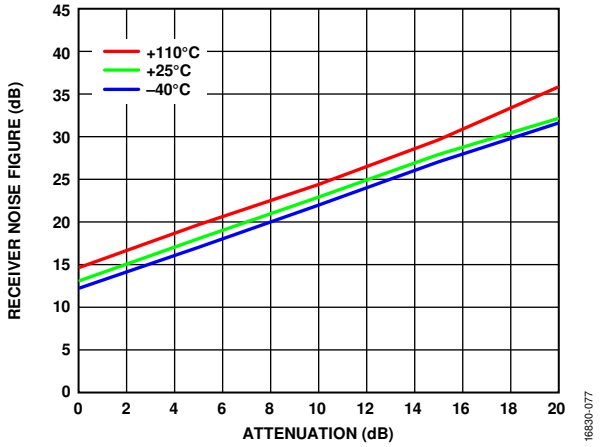

Figure 56. Receiver Noise Figure vs. Attenuation, 1850 MHz LO, 200 MHz Bandwidth, 245.76 MSPS Sample Rate, 500 kHz to 100 MHz Integration Bandwidth

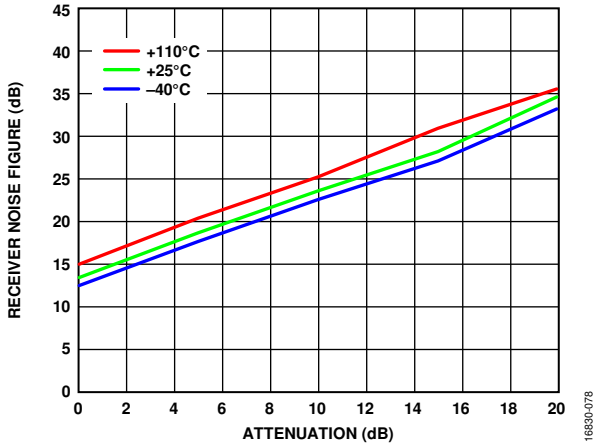

Figure 57. Receiver Noise Figure vs. Attenuation, 2850 MHz LO, 200 MHz Bandwidth, 245.76 MSPS Sample Rate, 500 kHz to 100 MHz Integration Bandwidth

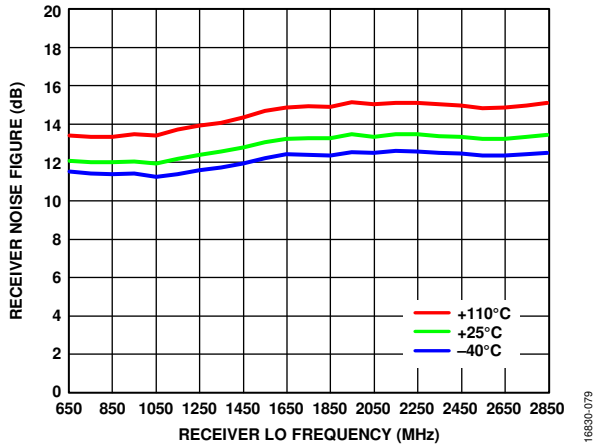

Figure 58. Receiver Noise Figure vs. Receiver LO Frequency, 0 dB Receiver Attenuation, 200 MHz RF Bandwidth, 245.76 MSPS Sample Rate, ±100 MHz Integration Bandwidth