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Integrated Dual RF Transmitter, Receiver, and Observation Receiver

Data Sheet

ADRV9009

FEATURES

Dual transmitters
Dual receivers
Dual input shared observation receiver
Maximum receiver bandwidth: 200 MHz
Maximum tunable transmitter synthesis bandwidth: 450 MHz
Maximum observation receiver bandwidth: 450 MHz
Fully integrated fractional-N RF synthesizers
Fully integrated clock synthesizer
Multichip phase synchronization for RF LO and baseband clocks
JESD204B datapath interface
Tunable range: 75 MHz to 6000 MHz

APPLICATIONS

3G/4G/5G TDD macro cell base stations
TDD active antenna systems
Massive MIMO
Phased array radar
Electronic warfare
Military communications
Portable test equipment

GENERAL DESCRIPTION

The ADRV9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters and receivers, integrated synthesizers, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption demanded by 3G, 4G, and 5G macro cell time division duplex (TDD) base station applications.

The receive path consists of two independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The device also supports a wide bandwidth, time shared observation path receiver (ORx) for use in TDD applications. The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, thus eliminating the need for these functions in the digital baseband. Several auxiliary functions, such as analog to digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) for the power amplifier (PA), and RF front-end control are also integrated.

In addition to automatic gain control (AGC), the ADRV9009 also features flexible external gain control modes, allowing significant flexibility in setting system level gain dynamically.

The received signals are digitized with a set of four high dynamic range, continuous time Σ-Δ ADCs that provide inherent antialiasing. The combination of the direct conversion architecture, which does not suffer from out of band image mixing, and the lack of aliasing, relaxes the requirements of the RF filters when compared to traditional IF receivers.

The transmitters use an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise.

The observation path consists of a wide bandwidth, direct conversion receiver with state-of-the-art dynamic range.

The fully integrated phase-locked loop (PLL) provides high performance, low power, fractional-N RF frequency synthesis for the transmitter (Tx) and receiver (Rx) signal paths. An additional synthesizer generates the clocks needed for the converters, digital circuits, and the serial interface. A multichip synchronization mechanism synchronizes the phase of the RF local oscillator and baseband clocks between multiple ADRV9009 chips. Precautions are taken to provide the isolation demanded in high performance base station applications. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates resulting in two lanes per transmitter, and a single lane per receiver in the widest bandwidth mode. The interface also supports interleaved mode for lower bandwidths, thus reducing the total number of high speed data interface lanes to one. Both fixed and floating point data formats are supported. The floating point format allows internal AGC to be invisible to the demodulator device.

The core of the ADRV9009 can be powered directly from 1.3 V and 1.8 V regulators and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9009 is packaged in a 12 mm × 12 mm, 196-ball chip scale ball grid array (CSP_BGA).

Rev. A Document Feedback

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REVISION HISTORY

6/2018—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

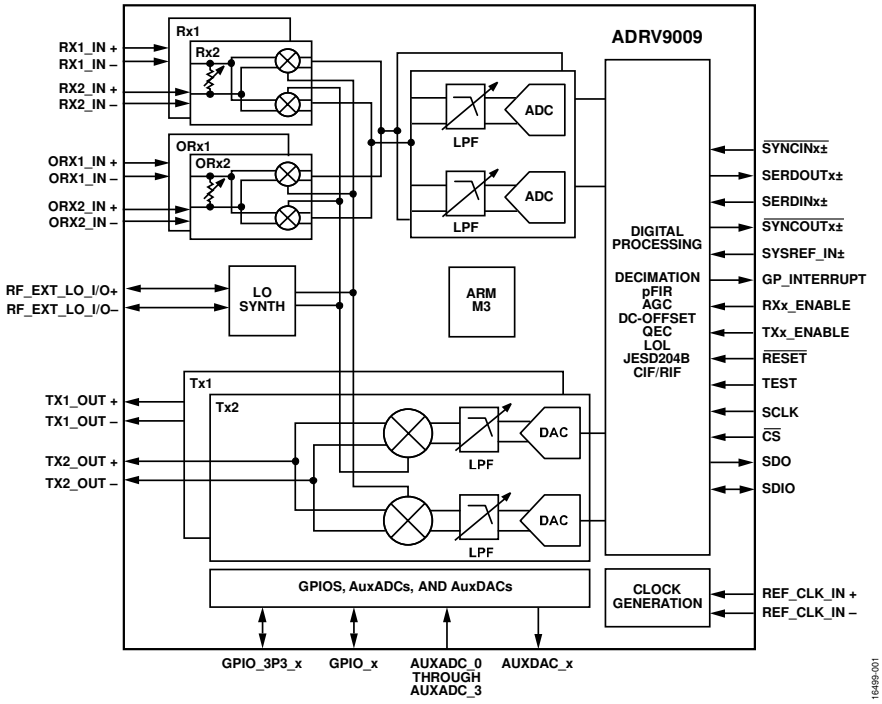

Figure 1.

SPECIFICATIONS

Electrical characteristics at VDDA1P3[1] = 1.3 V, VDDD1P3_DIG = 1.3 V, VDDA1P8_TX = 1.8 V, T_J = full operating temperature range. Local oscillator frequency (f_{LO}) = 1800 MHz, unless otherwise noted. The specifications in Table 1 are not deembedded. Refer to the Typical Performance Characteristics section for input/output circuit path loss. The device configuration profile, unless otherwise specified, is as follows: receiver = 200 MHz (in-phase quadrature (IQ) rate = 245.76 MHz), transmitter = 200 MHz/450 MHz (IQ rate = 491.52 MHz), observation receiver = 450 MHz (IQ rate = 491.52 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS						
Center Frequency		75		6000	MHz	
Transmitter Synthesis Bandwidth				450	MHz	
Transmitter Large Signal Bandwidth				200	MHz	
Peak to Peak Gain Deviation			1.0		dB	450 MHz bandwidth, compensated by programmable finite impulse response (FIR) filter
Gain Slope			±0.1		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz bandwidth
Transmitter Attenuation Power Control Range		0		32	dB	Signal-to-noise ratio (SNR) maintained for attenuation between 0 dB and 20 dB
Transmitter Attenuation Power Control Resolution			0.05		dB	
Transmitter Attenuation Integral Nonlinearity	INL		0.1		dB	For any 4 dB step
Transmitter Attenuation Differential Nonlinearity	DNL		+0.04		dB	Monotonic
Transmitter Attenuation SPI-2 Timing						See Figure 4
Time from $\overline{CS}$ Going High to Change in Transmitter Attenuation	t_{SCH}	19.5		24	ns	
Time Between Consecutive Micro Attenuation Steps	t_{ACH}	6.5		8.1	ns	A large change in attenuation can be broken up into a series of smaller attenuation changes
Time Required to Reach Final Attenuation Value	t_{DCH}			800	ns	Time required to complete the change in attenuation from start attenuation to final attenuation value
Maximum Attenuation Overshoot During Transition		−1.0		+0.5	dB	
Change in Attenuation per Micro Step				0.5	dB	
Maximum Attenuation Change when $\overline{CS}$ Goes High			32		dB	
Adjacent Channel Leakage Ratio (ACLR) Long Term Evolution (LTE)						20 MHz LTE at −12 dBFS
			−67		dB	75 MHz < f ≤ 2800 MHz
			−64		dB	2800 MHz < f ≤ 4800 MHz
			−60		dB	4800 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
In Band Noise Floor						0 dB attenuation; in band noise falls 1 dB for each dB of attenuation for attenuation between 0 dB and 20 dB
			−148		dBm/Hz	600 MHz < f ≤ 3000 MHz
			−149		dBm/Hz	3000 MHz < f ≤ 4800 MHz
			−150.5		dBm/Hz	4800 MHz < f ≤ 6000 MHz
Out of Band Noise Floor						0 dB attenuation; 3 × bandwidth/2 offset
			−153		dBm/Hz	600 MHz < f ≤ 3000 MHz
			−154		dBm/Hz	3000 MHz < f ≤ 4800 MHz
			−155.5		dBm/Hz	4800 MHz < f ≤ 6000 MHz
Interpolation Images			−80		dBc	
Transmitter to Transmitter Isolation			85		dB	75 MHz < f ≤ 600 MHz
			75		dB	600 MHz < f ≤ 2800 MHz
			70		dB	2800 MHz < f ≤ 4800 MHz
			65		dB	4800 MHz < f ≤ 5700 MHz
			56		dB	5700 MHz < f ≤ 6000 MHz
Image Rejection						
Within Large Signal Bandwidth						QEC active
			70		dB	75 MHz < f ≤ 600 MHz
			65		dB	600 MHz < f ≤ 4000 MHz
			62		dB	4000 MHz < f ≤ 4800 MHz
			60		dB	4800 MHz < f ≤ 6000 MHz
Beyond Large Signal Bandwidth			40		dB	Assumes that distortion power density is 25 dB below desired power density
Maximum Output Power						0 dBFS, continuous wave tone into 50 Ω load, 0 dB transmitter attenuation
			9		dBm	75 MHz < f ≤ 600 MHz
			7		dBm	600 MHz < f ≤ 3000 MHz
			6		dBm	3000 MHz < f ≤ 4800 MHz
			4.5		dBm	4800 MHz < f ≤ 6000 MHz
Third Order Output Intermodulation Intercept Point	OIP3					0 dB transmitter attenuation
			29		dBm	75 MHz < f ≤ 600 MHz
			27		dBm	600 MHz < f ≤ 4000 MHz
			23		dBm	4000 MHz < f ≤ 6000 MHz
Carrier Leakage						With LO leakage correction active, 0 dB attenuation; scales decibel for decibel with attenuation; measured in 1 MHz bandwidth, resolution bandwidth and video bandwidth = 100 kHz, rms detector, 100 trace average
Carrier Offset from Local Oscillator (LO)			−84		dBFS	75 MHz < f ≤ 600 MHz
			−82		dBFS	600 MHz < f ≤ 4800 MHz
			−80		dBFS	4800 MHz < f ≤ 6000 MHz
Carrier on LO			−71		dBFS	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Error Vector Magnitude (Third Generation Partnership Project (3GPP) Test Signals)	EVM					
75MHz LO			0.5		%	300 kHz RF PLL loop bandwidth
1900 MHz LO			0.7		%	50 kHz RF PLL loop bandwidth
3800 MHz LO			0.7		%	300 kHz RF PLL loop bandwidth
5900 MHz LO			1.1		%	300 kHz RF PLL loop bandwidth
Output Impedance	Z_{OUT}		50		Ω	Differential (see Figure 428)
OBSERVATION RECEIVER	ORx					
Center Frequency		75		6000	MHz	
Gain Range			30		dB	IIP3 improves decibel for decibel for the first 18 dB of gain attenuation; QEC performance optimized for 0 dB to 6 dB of attenuation only
Analog Gain Step			0.5		dB	For attenuator steps from 0 dB to 6 dB
Peak to Peak Gain Deviation			1		dB	450 MHz bandwidth, compensated by programmable FIR filter
Gain Slope			±0.1		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz RF bandwidth
Receiver Bandwidth				450	MHz	
Receiver Alias Band Rejection		60			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					0 dB attenuation; increases decibel for decibel with attenuation; continuous wave corresponds to −1 dBFS at ADC
			−11		dBm	75 MHz < f ≤ 3000 MHz
			−9.5		dBm	3000 MHz < f ≤ 4800 MHz
			−8		dBm	4800 MHz < f ≤ 6000 MHz
Integrated Noise			−58.5		dBFS	450 MHz integration bandwidth
			−57.5		dBFS	491.52 MHz integration bandwidth
Second-Order Input Intermodulation Intercept Point	IIP2		62		dBm	Maximum observation receiver gain; P_{HIGH} − 14 dB per tone (see the Terminology section) 75 MHz < f ≤ 600 MHz
			62		dBm	Maximum observation receiver gain; P_{HIGH} − 8 dB per tone (see the Terminology section) 600 MHz < f ≤ 3000 MHz
Third-Order Input Intermodulation Intercept Point	IIP3					
Narrow Band			4		dBm	75 MHz < f ≤ 300 MHz; (P_{HIGH} − 14) dB/tone
			11		dBm	300 MHz < f ≤ 600 MHz; (P_{HIGH} − 14) dB/tone
						IM3 product < 130 MHz at baseband; (P_{HIGH} − 8) dB/tone
			12		dBm	600 MHz < f ≤ 3000 MHz
			12		dBm	3000 MHz < f ≤ 4800 MHz
			11		dBm	4800 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Wide Band						
			7		dBm	600 MHz < f ≤ 3000 MHz
			7		dBm	3000 MHz < f ≤ 4800 MHz
			6		dBm	4800 MHz < f ≤ 6000 MHz
Third-Order Intermodulation Product	IM3					IM3 product < 130 MHz at baseband; two tones, each at (P_{HIGH} − 12) dB
			−70		dBc	600 MHz < f ≤ 3000 MHz
			−67		dBc	3000 MHz < f ≤ 4800 MHz
			−62		dBc	4800 MHz < f ≤ 6000 MHz
Fifth-Order Intermodulation Product (1800 MHz)	IM5		−80		dBc	IM5 product < 50 MHz at baseband; two tones, each at (P_{HIGH} − 14) dB
Seventh-Order Intermodulation Product (1800 MHz)	IM7		−80		dBc	IM7 product < 50 MHz at baseband; two tones, each at (P_{HIGH} − 14) dB
Spurious-Free Dynamic Range	SFDR		70		dB	Non IMx related spurs, does not include HDx; (P_{HIGH} − 11) dB input signal
Harmonic Distortion						(P_{HIGH} − 11) dB input signal
Second Order Harmonic Distortion Product	HD2		−80		dBc	In band HD falls within ±25 MHz
			−80		dBc	Out of band HD falls within ±50 MHz
Third-Order Harmonic Distortion Product	HD3		−70		dBc	In band HD falls within ±25 MHz
			−60		dBc	Out of band HD falls within ±50 MHz
Image Rejection						QEC active
Within Large Signal Bandwidth			65		dB	
Outside Large Signal Bandwidth			55		dB	
Input Impedance			100		Ω	Differential (see Figure 429)
Isolation						
			65		dB	600 MHz < f ≤5300 MHz
			55		dB	5300 MHz < f ≤ 6000 MHz
			65		dB	600 MHz < f ≤ 5300 MHz
			55		dB	5300 MHz < f ≤ 6000 MHz
RECEIVERS						
Center Frequency		75		6000	MHz	
Gain Range			30		dB	
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 30 dB
Bandwidth Ripple			±0.5		dB	200 MHz bandwidth, compensated by programmable FIR filter
			±0.2		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Receiver Bandwidth				200	MHz	
Receiver Alias Band Rejection		80			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					0 dB attenuation, increases decibel for decibel with attenuation; continuous wave = 1800 MHz; corresponds to −1 dBFS at ADC
			−11		dBm	75 MHz < f ≤ 3000 MHz
			−10.2		dBm	3000 MHz < f ≤ 4800 MHz
			−9.5		dBm	4800 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Noise Figure	NF					0 dB attenuation, at receiver port
			12		dB	600 MHz < f ≤ 3000 MHz
			13		dB	3000 MHz < f ≤ 4800 MHz
			15.2		dB	4800 MHz < f ≤ 6000 MHz
Ripple			1.8		dB	At band edge maximum bandwidth mode
Input Third-Order Intercept Point	IIP3					
Difference Product	IIP3, d		12		dBm	Two (P_{HIGH} − 12) dB tones near band edge
Sum Product	IIP3, s		12		dBm	Two (P_{HIGH} − 6) dB tones, at bandwidth/6 offset from the LO
HD3	HD3					(P_{HIGH} − 6) dB continuous wave tone at bandwidth/6 offset from the LO
			−66		dBc	600 MHz < f ≤ 4800 MHz
			−62		dBc	4800 MHz < f ≤ 6000 MHz
Second-Order Input Intermodulation Intercept Point	IIP2		62		dBm	0 dB attenuation, complex
Image Rejection			75		dB	Quadrature error correction (QEC) active, within 200 MHz receiver bandwidth
Input Impedance			100		Ω	Differential (see Figure 430)
			65		dB	600 MHz < f ≤ 4800 MHz
			61		dB	4800 MHz < f ≤ 6000 MHz
Receiver Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	No more than one spur at this level per 10 MHz of receiver bandwidth
Receiver LO Leakage at Receiver Input at Maximum Gain						Leakage decreases decibel for decibel with attenuation for first 12 dB
			−70		dBm	600 MHz < f ≤ 3000 MHz
			−65		dBm	3000 MHz < f ≤ 6000 MHz
Isolation						
			65		dB	600 MHz < f ≤ 4800 MHz
			55		dB	4800 MHz < f ≤ 6000 MHz
			65		dB	600 MHz < f ≤ 4800 MHz
			55		dB	4800 MHz < f ≤ 6000 MHz
LO SYNTHESIZER						
LO Frequency Step			2.3		Hz	1.5 GHz to 2.8 GHz, 76.8 MHz phase frequency detector (PFD) frequency
LO Spur			−85		dBc	Excludes integer boundary spurs
Integrated Phase Noise						2 kHz to 18 MHz
1900 MHz LO			0.2		°rms	Narrow PLL loop bandwidth (50 kHz)
3800 MHz LO			0.36		°rms	Wide PLL loop bandwidth (300 kHz)
5900 MHz LO			0.54		°rms	Wide PLL loop bandwidth (300 kHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Spot Phase Noise						
1900 MHz LO						Narrow PLL loop bandwidth
100 kHz Offset			−100		dBc/Hz	
200 kHz Offset			−115		dBc/Hz	
400 kHz Offset			−120		dBc/Hz	
600 kHz Offset			−129		dBc/Hz	
800 kHz Offset			−132		dBc/Hz	
1.2 MHz Offset			−135		dBc/Hz	
1.8 MHz Offset			−140		dBc/Hz	
6 MHz Offset			−150		dBc/Hz	
10 MHz Offset			−153		dBc/Hz	
3800 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−104		dBc/Hz	
1.2 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	
5900 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−99		dBc/Hz	
1.2 MHz Offset			−119.7		dBc/Hz	
10 MHz Offset			−135.4		dBc/Hz	
LO PHASE SYNCHRONIZATION						
Phase Deviation			1.6		ps/°C	Change in LO delay per temperature change
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	150		8000	MHz	Input frequency must be 2× the desired LO frequency
Input Signal Power		0		12	dBm	50 Ω matching at the source
			3		dBm	f_{EXTLO} ≤ 2 GHz; add 0.5 dBm/GHz above 2 GHz
			6		dBm	f_{EXTLO} = 8 GHz
External LO Input Signal Differential						To ensure adequate QEC
Phase Error				3.6	ps	
Amplitude Error				1	dB	
Duty Cycle Error				2	%	
Even-Order Harmonics				−50	dBc	
CLOCK SYNTHESIZER						
Integrated Phase Noise						1 kHz to 100 MHz
1966.08 MHz LO			0.4		°rms	PLL optimized for close in phase noise
Spot Phase Noise						
1966.08 MHz						
100 kHz Offset			−109		dBc/Hz	
1 MHz Offset			−129		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	
REFERENCE CLOCK (REF_CLK_IN)						
Frequency Range		10		1000	MHz	
Signal Level		0.3		2.0	V p-p	AC-coupled, common-mode voltage (V_{CM}) = 618 mV; for best spurious performance, use <1 V p-p input clock

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY CONVERTERS						
ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA_3P3 – 0.05		V	
DAC						
Resolution			10		Bits	Includes four offset levels
Output Voltage						
Minimum			0.7		V	1 V V_{REF}
Maximum			VDDA_3P3 – 0.3		V	2.5 V V_{REF}
Output Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS)—SERIAL PERIPHERAL INTERFACE (SPI), GPIO_x, TXx_ENABLE, ORXx_ENABLE						
Logic Inputs						
Input Voltage						
High Level		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Low Level		0		VDD_INTERFACE × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDD_INTERFACE × 0.8			V	
Low Level				VDD_INTERFACE × 0.2	V	
Drive Capability			3		mA	
DIGITAL SPECFICATIONS (CMOS)—GPIO_3P3_x						
Logic Inputs						
Input Voltage						
High Level		VDDA_3P3 × 0.8		VDDA_3P3	V	
Low Level		0		VDDA_3P3 × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Outputs						
Output Voltage						
High Level		VDDA_ 3P3 × 0.8			V	
Low Level				VDDA_ 3P3 × 0.2	V	
Drive Capability			4		mA	
DIGITAL SPECIFICATIONS (LVDS)						
Logic Inputs (SYSREF_IN±, SYNCINx±)						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs ($\overline{\text{SYNCOUTx±}}$)						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Output Differential Voltage			225		mV	Programmable in 75 mV steps
Output Offset Voltage			1200		mV	
SPI TIMING						
SCLK Period	t_{CP}	20			ns	
SCLK Pulse Width	t_{MP}	10			ns	
$\overline{\text{CS}}$ Setup to First SCLK Rising Edge	t_{SC}	3			ns	
Last SCLK Falling Edge to $\overline{\text{CS}}$ Hold	t_{HC}	0			ns	
SDIO Data Input Setup to SCLK	t_S	2			ns	
SDIO Data Input Hold to SCLK	t_H	0			ns	
SCLK Rising Edge to Output Data Delay (3-Wire or 4-Wire Mode)	t_{CO}	3		8	ns	
Bus Turnaround Time, Read After BBP Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time, Read After ADRV9009 Drives Last Data Bit	t_{HZS}	0		t_{CO}	ns	
JESD204B DATA OUTPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate per Channel, Nonreturn to Zero (NRZ)		3125		12288	Mbps	
Rise Time	t_R	24	39.5		ps	20% to 80% in 100 Ω load
Fall Time	t_F	24	39.4		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Differential Output Voltage	V_{DIFF}	360	600	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance		80	94.2	120	Ω	
Total Jitter			15.13		ps	Bit error rate (BER) = 10^{-15}
Uncorrelated Bounded High Probability Jitter	UBHPJ		0.56		ps	
Duty Cycle Distortion	DCD		0.369		ps	
SYSREF_IN± Setup Time to REF_CLK_IN_x		2.5			ns	See Figure 2
SYSREF_IN± Hold Time to REF_CLK_IN_x		−1.5			ns	See Figure 2
Latency	t_{LAT_FRM}					REF_CLK_IN = 245.76 MHz
			116.5		Clock cycles	Observation receiver bandwidth = 450 MHz, IQ rate = 491.52 MHz; lane rate = 9830.4 MHz, number of converters (M) = 4, number of lanes (L) = 2, converter resolution (N) = 16, number of samples per converter (S) = 1
			237.02		ns	
			89.4		Clock cycles	Receiver bandwidth = 200 MHz, IQ rate = 245.76 MHz; lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			364.18		ns	
JESD204B DATA INPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate per Channel (NRZ)		3125		12288	Mbps	
Differential Voltage	V_{DIFF}	125		750	mV	
VTT Source Impedance	Z_{TT}		8.9	30	Ω	
Differential Impedance	Z_{RDIFF}	80	105.1	120	Ω	
Termination Voltage	V_{TT}					
AC-Coupled		1.267		1.33	V	
Latency	t_{LAT_DEFRM}		74.45		Clock cycles	Device clock = 245.76 MHz, transmitter bandwidth = 200 MHz; IQ rate = 491.52 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			153.5		ns	

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

CURRENT AND POWER CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS					
VDDA1P3[1] Analog Supply	1.267	1.3	1.33	V	
VDDD1P3_DIG Supply	1.267	1.3	1.33	V	
VDDA1P8_TX Supply	1.71	1.8	1.89	V	
VDDA1P8_BB Supply	1.71	1.8	1.89	V	
VDD_INTERFACE Supply	1.71	1.8	2.625	V	CMOS and LVDS supply, 1.8 V to 2.5 V nominal range
VDDA_3P3 Supply	3.135	3.3	3.465	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POSITIVE SUPPLY CURRENT					LO at 2600 MHz
450 MHz Transmitter Bandwidth, Observation Receiver Disabled					Two transmitters enabled
VDDA1P3[1] Analog Supply		1520		mA	
VDDD1P3_DIG Supply		619		mA	Transmitter QEC active
VDDA1P8_TX Supply		455		mA	Transmitter RF attenuation = 0 dB, full-scale continuous wave
		135		mA	Transmitter RF attenuation = 15 dB, full-scale continuous wave
VDDA1P8_BB Supply		30		mA	
VDD_INTERFACE Supply		8		mA	VDD_INTERFACE = 2.5V
VDDA_3P3 Supply		3		mA	No AUXDAC_x or AUXADC_x enabled; if enabled, AUXADC_x adds 2.7 mA and each AUXDAC_x adds 1.5 mA
Total Power Dissipation		3.68		W	Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active
		3.11		W	Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active
450 MHz Transmitter Bandwidth, Observation Receiver Enabled					Two transmitters enabled, one ORX enabled
VDDA1P3[1] Analog Supply		2073		mA	
VDDD1P3_DIG Supply		1541		mA	Transmitter QEC tracking active, observation receiver QEC enabled, transmitter LTE20 centered on LO, observation receiver LTE20 at −16 dBm centered on LO
		2100		mA	Transmitter two tone = −99 MHz and +100 MHz at −7 dBFS each, observation receiver one tone = 100 MHz at −16 dBm.
VDDA1P8_TX Supply		455		mA	Transmitter RF attenuation = 0 dB, full-scale continuous wave
		135		mA	Transmitter RF attenuation = 15 dB, full-scale continuous wave
VDDA1P8_BB Supply		63		mA	
VDD_INTERFACE Supply		8		mA	VDD_INTERFACE = 2.5 V
VDDA_3P3 Power Supply		3		mA	No AUXDAC_x or AUXADC_x enabled; if enabled, AUXADC_x adds 2.7 mA and each AUXDAC_x adds 1.5 mA
Total Power Dissipation		5.66		W	Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active
		5.08		W	Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active
200 MHz Receiver Bandwidth, Observation Receiver Disabled					Two receivers enabled
VDDA1P3[1] Analog Supply		1645		mA	
VDDD1P3_DIG Supply		984		mA	Receiver QEC active
VDDA1P8_TX Supply		0.4		mA	
VDDA1P8_BB Supply		68		mA	
VDD_INTERFACE Supply		8		mA	
VDDA_3P3 Supply		3		mA	No AUXDAC_x or AUXADC_x enabled; if enabled, AUXADC_x adds 2.7 mA and each AUXDAC_x adds 1.5 mA
Total Power Dissipation		3.57		W	Typical supply voltages, Receiver QEC active

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

TIMING DIAGRAMS

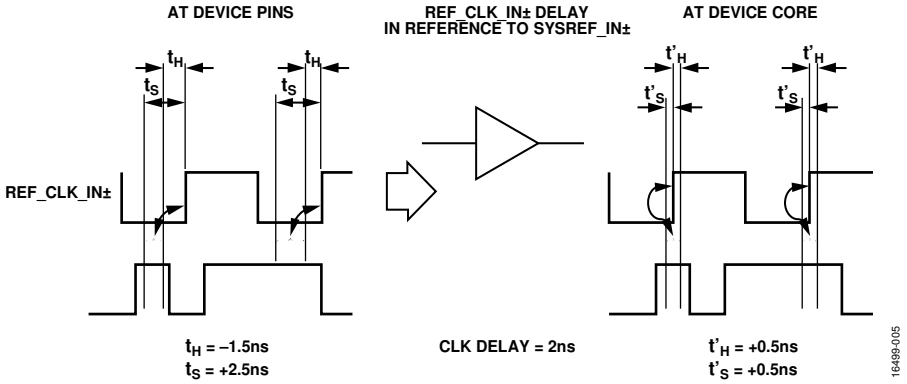

Figure 2. SYSREF_IN± Setup and Hold Timing

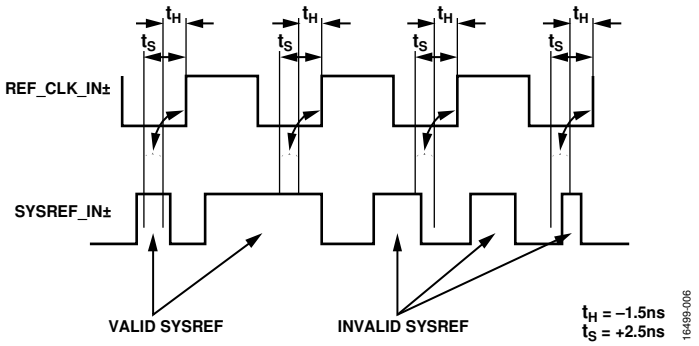

Figure 3. SYSREF_IN± Setup and Hold Timing Examples, Relative to Device Clock

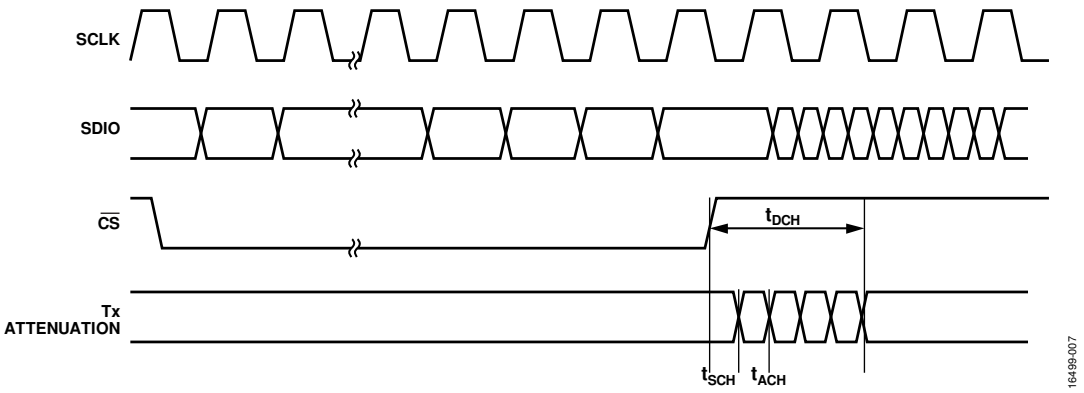

Figure 4. Transmitter Attenuation Update via SPI-2 Port

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDA1P3[1] to VSSA	−0.3 V to +1.4 V
VDDD1P3_DIG to VSSD	−0.3 V to +1.4 V
VDD_INTERFACE to VSSA	−0.3 V to +3.0 V
VDDA_3P3 to VSSA	−0.3 V to +3.9 V
VDDA1P8_TX to VSSA	−0.3 V to +2.0 V
VDD_INTERFACE Logic Inputs and Outputs to VSSD	−0.3 V to VDD_INTERFACE + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VDDA1P3_SER
JESD204B Logic Inputs to VSSA	−0.3 V to VDDA1P3_DES +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Port	23 dBm (peak)
Maximum Transmitter Voltage Standing Wave Ratio (VSWR)	3:1
Maximum Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C

[1] VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_DES, VDDA1P3_CLOCK, VDDA1P3_TX_LO_BUFFER, and VDDA1P3_CLOCK_SYNTH.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The ADRV9009 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL MANAGEMENT

The ADRV9009 is a high power device that can dissipate over 3 W depending on the user application and configuration.

Because of the power dissipation, the ADRV9009 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 5 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum junction temperature shown in Table 3. The device is designed for a lifetime of 10 years when operating at the maximum junction temperature.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance data for the ADRV9009 mounted on both a JEDEC 2S2P test board and a 10-layer Analog Devices, Inc., evaluation board are listed in Table 4. Do not exceed the absolute maximum junction temperature rating in Table 3. 10-layer PCB entries refer to the 10-layer Analog Devices evaluation board, which more accurately reflects the PCB used in customer applications.

Table 4. Thermal Resistance[1, 2]

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-196-13	21.1	0.04	4.9	0.3	4.9	°C/W

[1] For the θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 thermal conductivity watts/(meter × Kelvin).
[2] Using enhanced heat removal techniques such as PCB, heat sink, airflow, and so on, improves the thermal resistance values.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

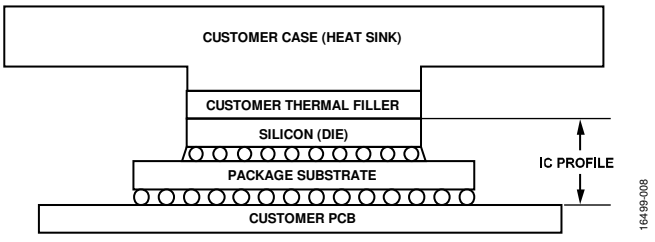

Figure 5. Typical Thermal Management Solution

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 6. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1, A4, A7, A8, A11, A14, B2 to B6, B9 to B14, C4, C9, C11, D3 to D9, D11, D12, E6, E9, F1, F2, F5 to F10, F12 to F14, G1 to G4, G6, G10 to G14, H2 to H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10	Input	VSSA	Analog Supply Voltage (V_{SS}).
A2, A3	Input	ORX2_IN+, ORX2_IN–	Differential Input for Observation Receiver 2. When unused, connect these pins to ground.
A5, A6	Input	RX2_IN+, RX2_IN–	Differential Input for Main Receiver 2. When unused, connect these pins to ground.
A9, A10	Input	RX1_IN+, RX1_IN–	Differential Input for Main Receiver 1. When unused, connect these pins to ground.

Pin No.	Type	Mnemonic	Description
A12, A13	Input	ORX1_IN+, ORX1_IN−	Differential Input for Observation Receiver 1. When unused, connect these pins to ground.
B1	Input	VDDA1P3_RX_RF	Observation Receiver Supply.
B7, B8	Input	RF_EXT_LO_I/O−, RF_EXT_LO_I/O+,	Differential External LO Input/Output. If these pins are used for the external LO, the input frequency must be 2× the desired carrier frequency. When unused, do not connect these pins.
C1	Input/ output	GPIO_3P3_0	GPIO Pin Referenced to 3.3 V Supply. The alternate function is AUXDAC_4. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or this pin can be left floating, programmed as outputs, and driven low.
C2	Input/ output	GPIO_3P3_3	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
C13	Input/ output	GPIO_3P3_9	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_9. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D1	Input/ output	GPIO_3P3_1	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_5. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D2	Input/ output	GPIO_3P3_4	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_6. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D13	Input/ output	GPIO_3P3_8	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
D14	Input/ output	GPIO_3P3_10	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E1	Input/ output	GPIO_3P3_2	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E2	Input/ output	GPIO_3P3_5	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_7. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E3	Input/ output	GPIO_3P3_6	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_8. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
E13	Input/ output	GPIO_3P3_7	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_2. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.

Pin No.	Type	Mnemonic	Description
E14	Input/ output	GPIO_3P3_11	GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_3. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.
C3	Input	VDDA1P3_RX_TX	1.3 V Supply for Transmitter/Receiver Baseband Circuits, Transimpedance Amplifier (TIA), Transmitter Transconductance (GM), Baseband Filters, and Auxiliary DACs.
C5, C6	Input	VDDA1P3_RF_VCO_LDO	RF VCO LDO Supply Inputs. Connect Pin C5 to Pin C6. Use a separate trace on the PCB back to a common supply point.
C7	Input	VDDA1P1_RF_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
C8	Input	VDDA1P3_RF_LO	1.3 V LO Generator for the RF Synthesizer. This pin is sensitive to supply noise.
C10	Input	VDDA1P3_AUX_VCO_LDO	1.3 V Supply.
C12	Input	VDDA_3P3	General-Purpose Output Pull-Up Voltage and Auxiliary DAC Supply Voltage.
C14	Input/ output	RBIAS	Bias Resistor. Tie this pin to ground using a 14.3 kΩ resistor. This pin generates an internal current based on an external 1% resistor.
D10	Input	VDDA1P1_AUX_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
E4	Input	VDDA1P8_BB	1.8 V Supply for the ADC and DAC.
E5	Input	VDDA1P3_BB	1.3 V Supply for the ADC, DAC, and AUXADC.
E7, E8	Input	REF_CLK_IN+, REF_CLK_IN−	Device Clock Differential Input.
E10	Output	AUX_SYNTH_OUT	Auxiliary PLL Output. When unused, do not connect this pin.
E12	Input	VDDA1P8_TX	1.8 V Supply for Transmitter.
F3, F4, F11, E11	Input	AUXADC_0 to AUXADC_3	Auxiliary ADC Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
G5	Input	VDDA1P3_CLOCK_SYNTH	1.3 V Supply Input for Clock Synthesizer. Use a separate trace on the PCB back to a common supply point.
G7	Input	VDDA1P3_RF_SYNTH	1.3 V RF Synthesizer Supply Input. This pin is sensitive to supply noise.
G8	Input	VDDA1P3_AUX_SYNTH	1.3 V Auxiliary Synthesizer Supply Input.
G9	Output	RF_SYNTH_VTUNE	RF Synthesizer VTUNE Output.
H11	Input/ output	GPIO_12	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
H12	Input/ output	GPIO_11	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J11	Input/ output	GPIO_13	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J12	Input/ output	GPIO_10	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J3	Input/ output	GPIO_18	Digital GPIO, 1.8 V to 2.5 V. The joint test action group (JTAG) function is TCLK. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
J7	Input/ output	GPIO_2	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.

Pin No.	Type	Mnemonic	Description
J8	Input/ output	GPIO_1	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K5	Input/ output	GPIO_5	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDO. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K6	Input/ output	GPIO_4	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is $\overline{\text{TRST}}$. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K7	Input/ output	GPIO_3	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K8	Input/ output	GPIO_0	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K11	Input/ output	GPIO_14	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
K12	Input/ output	GPIO_9	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L5	Input/ output	GPIO_6	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDI. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L6	Input/ output	GPIO_7	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TMS. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L11	Input/ output	GPIO_15	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
L12	Input/ output	GPIO_8	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
M10	Input/ output	GPIO_17	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
M11	Input/ output	GPIO_16	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.
H14, J14	Output	TX1_OUT+, TX1_OUT–	Transmitter 1 Output. When unused, do not connect these pins.
H1, J1	Output	TX2_OUT–, TX2_OUT+	Transmitter 2 Output. When unused, do not connect these pins.

Pin No.	Type	Mnemonic	Description
J4	Input	$\overline{\text{RESET}}$	Active Low Chip Reset.
J5	Output	GP_INTERRUPT	General-Purpose Digital Interrupt Output Signal. When unused, do not connect this pin.
J6	Input	TEST	Pin Used for JTAG Boundary Scan. When unused, connect this pin to ground.
J9	Input/ output	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.
J10	Output	SDO	Serial Data Output. In SPI 3-wire mode, do not connect this pin.
K3, K4	Input	SYSREF_IN+, SYSREF_IN–	LVDS Input.
K9	Input	SCLK	Serial Data Bus Clock.
K10	Input	$\overline{\text{CS}}$	Serial Data Bus Chip Select, Active Low.
L3, L4	Input	$\overline{\text{SYNCIN1–}}$, $\overline{\text{SYNCIN1+}}$	LVDS Input. These pins form the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect these pins directly to ground.
L7, L10	Input	VSSD	Digital V_{SS}.
L8, L9	Input	VDDD1P3_DIG	1.3 V Digital Core. Connect Pin L8 and Pin L9 together. Use a wide trace to connect to a separate power supply domain.
L13, L14	Output	$\overline{\text{SYNCOUT1–}}$, $\overline{\text{SYNCOUT1+}}$	LVDS Output. These pins form the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect these pins.
M1	Input	VDDA1P1_CLOCK_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
M3, M4	Input	$\overline{\text{SYNCIN0–}}$, $\overline{\text{SYNCIN0+}}$	LVDS Input. These pins form the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect these pins directly to ground.
M5	Input	RX1_ENABLE	Receiver 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.
M6	Input	TX1_ENABLE	Transmitter 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.
M7	Input	RX2_ENABLE	Receiver 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.
M8	Input	TX2_ENABLE	Transmitter 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.
M12	Input	VDD_INTERFACE	Input/Output Interface Supply, 1.8 V to 2.5 V.
M13, M14	Output	$\overline{\text{SYNCOUT0–}}$, $\overline{\text{SYNCOUT0+}}$	LVDS Output. These pins form the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect these pins.
N1	Input	VDDA1P3_CLOCK_ VCO_LDO	1.3 V Use Separate Trace to Common Supply Point.
N3, N4	Output	SERDOUT3–, SERDOUT3+	RF Current Mode Logic (CML) Differential Output 3. When unused, do not connect these pins.
N5, N6	Output	SERDOUT2–, SERDOUT2+	RF CML Differential Output 2. When unused, do not connect these pins.
N8, P8	Input	VDDA1P3_SER	1.3 V Supply for JESD204B Serializer.
N9, P9	Input	VDDA1P3_DES	1.3 V Supply for JESD204B Deserializer.
N10, N11	Input	SERDIN1–, SERDIN1+	RF CML Differential Input 1. When unused, do not connect these pins.
N13, N12	Input	SERDIN0+, SERDIN0–	RF CML Differential Input 0. When unused, do not connect these pins.
P1	Output	AUX_SYNTH_VTUNE	Auxiliary Synthesizer VTUNE Output.
P4, P5	Output	SERDOUT1–, SERDOUT1+,	RF CML Differential Output 1. When unused, do not connect these pins.
P6, P7	Output	SERDOUT0–, SERDOUT0+,	RF CML Differential Output 0. When unused, do not connect these pins.
P11, P12	Input	SERDIN3–, SERDIN3+	RF CML Differential Input 3. When unused, do not connect these pins.
P13, P14	Input	SERDIN2–, SERDIN2+	RF CML Differential Input 2. When unused, do not connect these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

The temperature settings refer to the die temperature

75 MHz TO 525 MHz BAND

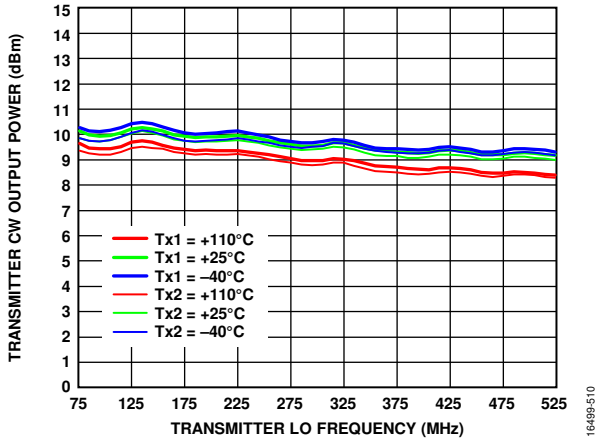

Figure 7. Transmitter Continuous Wave Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter 50 MHz/100 MHz Bandwidth Mode, IQ Rate = 122.88 MHz, Attenuation = 0 dB. Not Deembedded

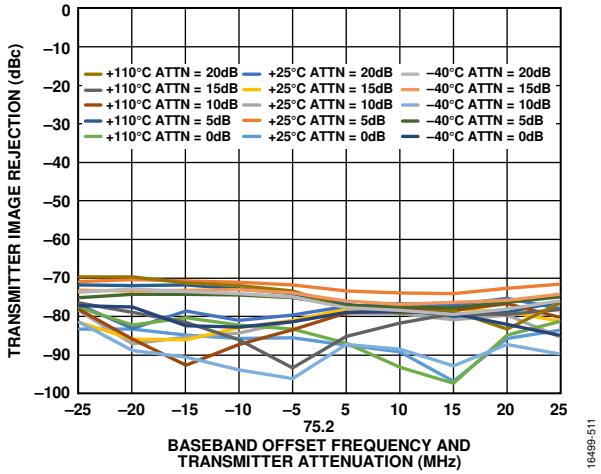

Figure 8. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation QEC Trained with Three Tones Placed At 10 MHz, 48 MHz, and 100 MHz (Tracking On); Total Combined Power = –10 dBFS; Correction Then Frozen (Tracking Turned Off); Continuous Wave Tone Swept Across Large Signal Bandwidth; LO = 75 MHz

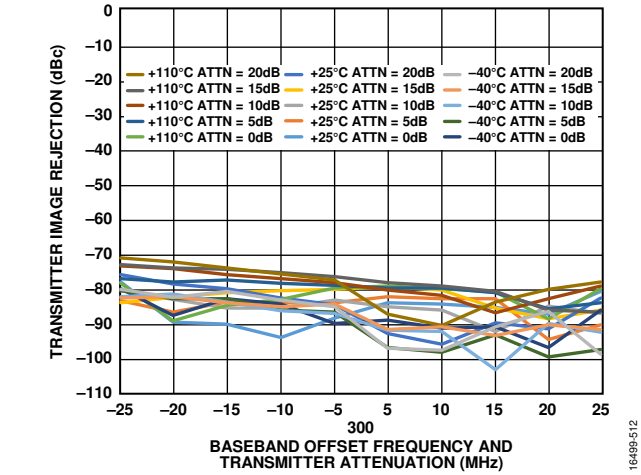

Figure 9. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation; QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = –10 dBFS; Correction Then Frozen (Tracking Turned Off); Continuous Wave Tone Swept Across Large Signal Bandwidth, LO = 300 MHz

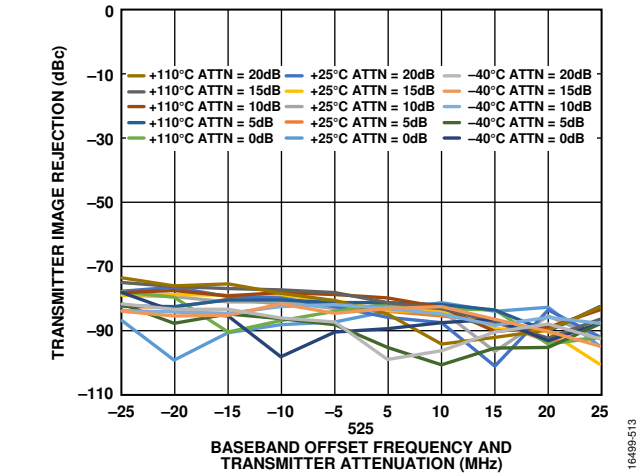

Figure 10. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Transmitter Attenuation; QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On); Total Combined Power = –10 dBFS; Correction Then Frozen (Tracking Turned Off); Continuous Wave Tone Swept Across Large Signal Bandwidth; LO = 525 MHz

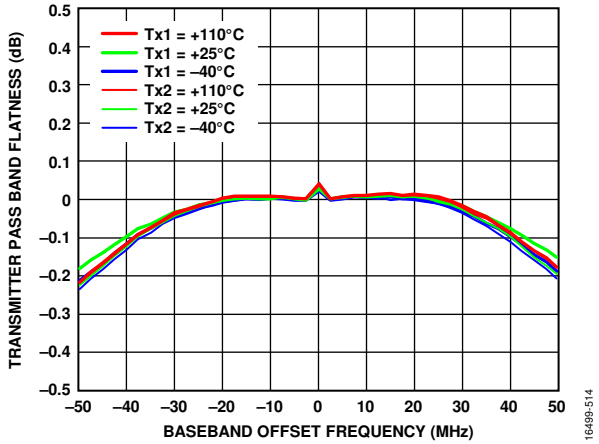

Figure 11. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, Off Chip Match Response Deembedded, LO = 300 MHz, Calibrated at 25°C

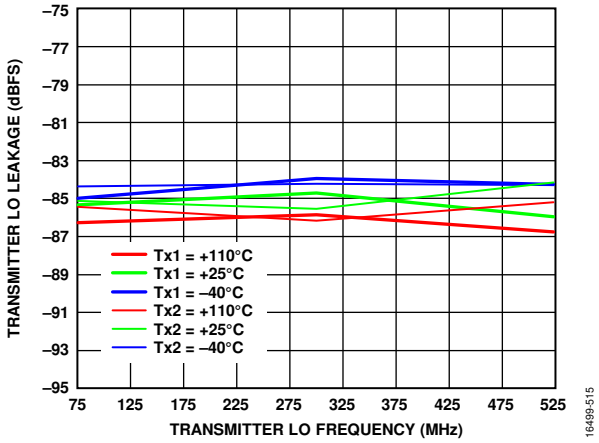

Figure 12. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB, Baseband Tone Frequency = 10 MHz, Tracked

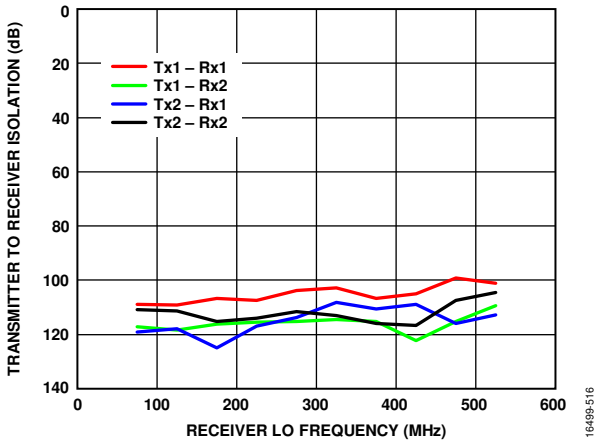

Figure 13. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = 25°C

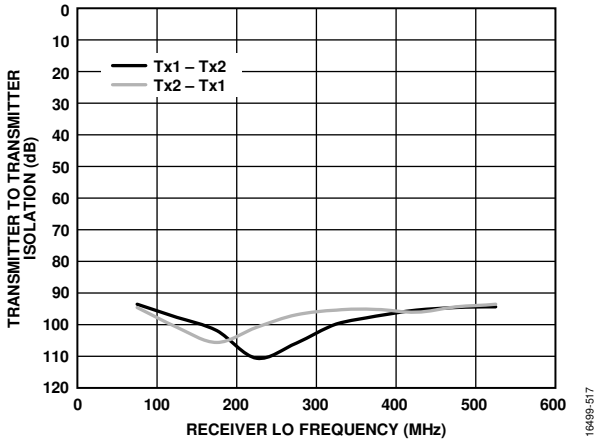

Figure 14. Transmitter to Transmitter Isolation vs. Receiver LO Frequency, Temperature = 25°C

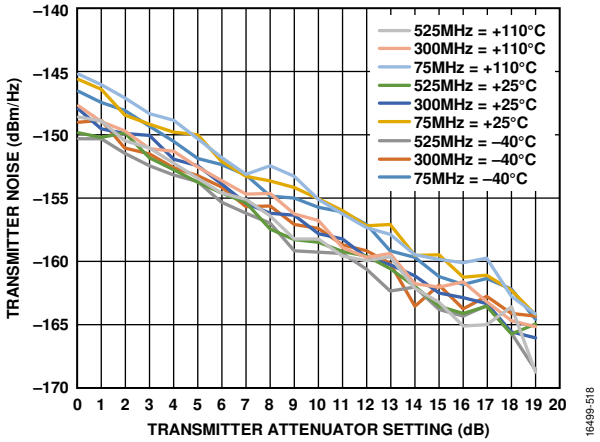

Figure 15. Transmitter Noise vs. Transmitter Attenuation Setting, 50 MHz Offset

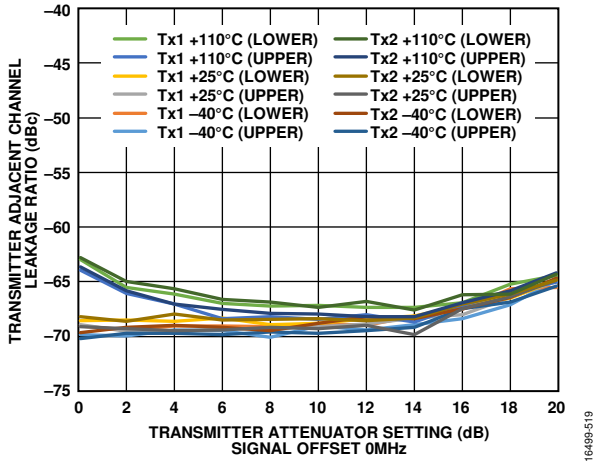

Figure 16. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, Signal Offset = 0 MHz, LO = 75 MHz, LTE20 Peak to Average Ratio (PAR) = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

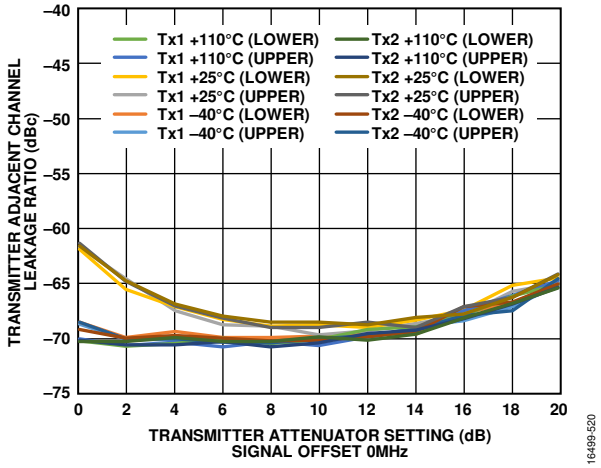

Figure 17. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 300 MHz, LTE20 PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

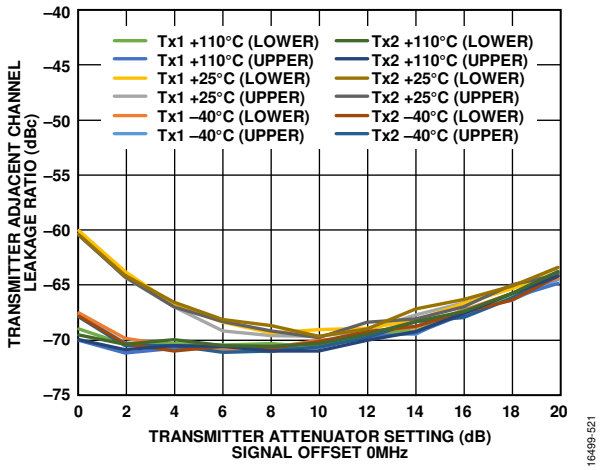

Figure 18. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuation Setting, LO = 525 MHz, LTE20 PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

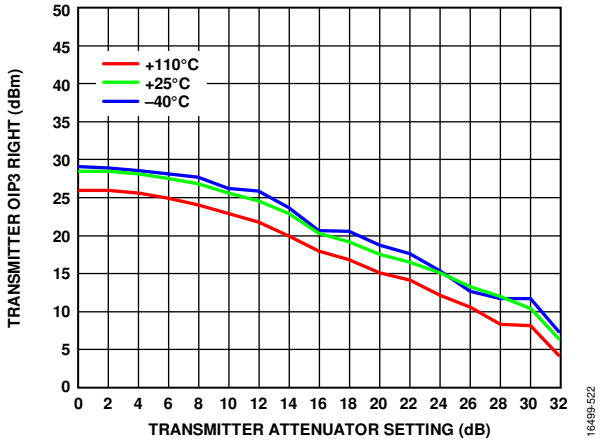

Figure 19. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 75 MHz, Total RMS Power = –12 dBFS, 20 MHz/25 MHz Tones

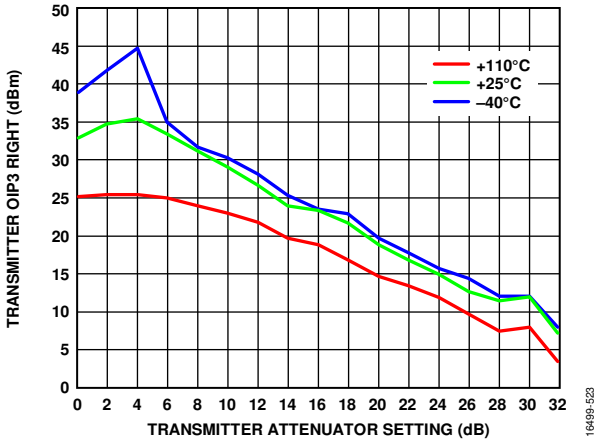

Figure 20. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 300 MHz, Total Root Mean Square (RMS) Power = –12 dBFS, 20 MHz/25 MHz Tones

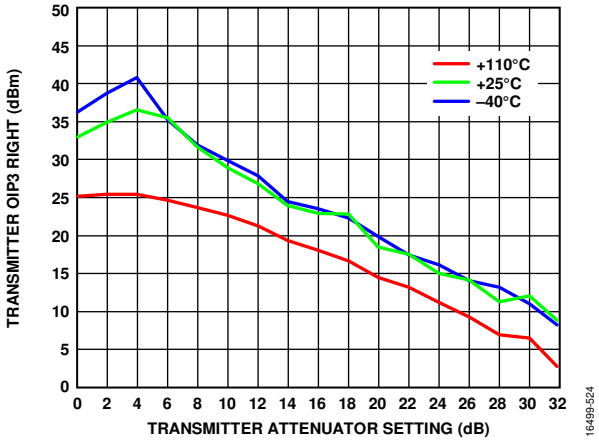

Figure 21. Transmitter OIP3 Right vs. Transmitter Attenuation Setting, LO = 525 MHz, Total RMS Power = –12 dBFS, 20 MHz/25 MHz Tones

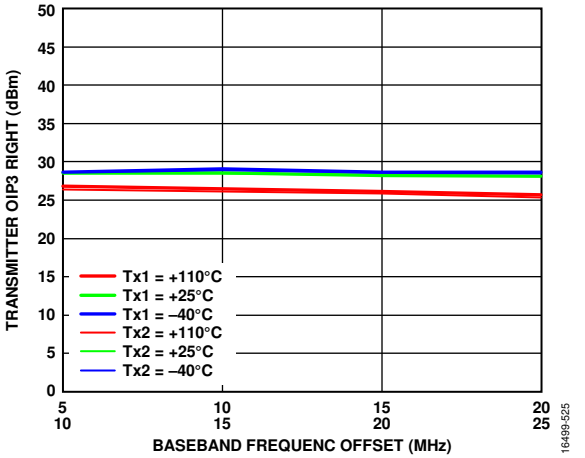

Figure 22. Transmitter OIP3 Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 75 MHz, Total RMS Power = –12 dBFS, 4 dB Transmitter Attenuation

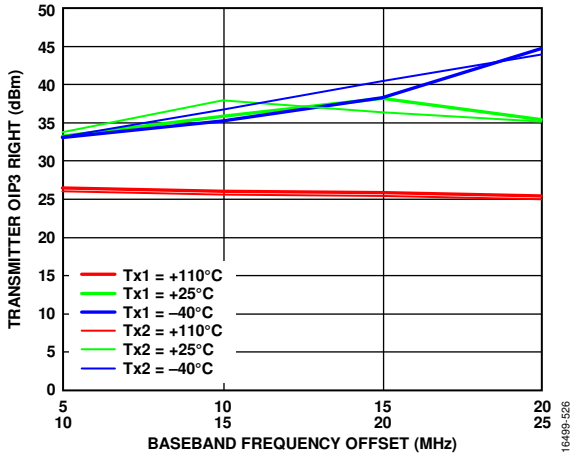

Figure 23. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 300 MHz, Total RMS Power = −12 dBFS, 4 dB Transmitter Attenuation

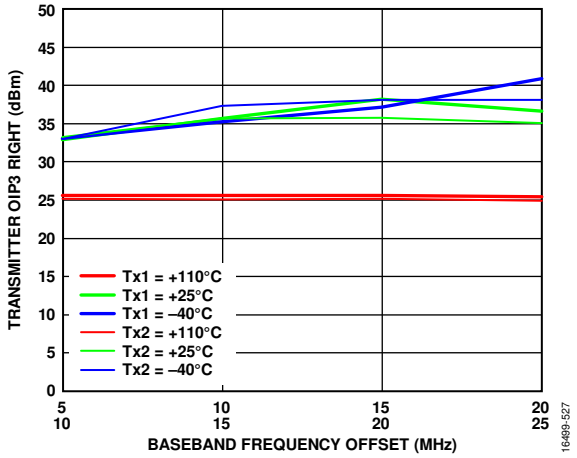

Figure 24. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 525 MHz, Total RMS Power = −12 dBFS, 4 dB Transmitter Attenuation

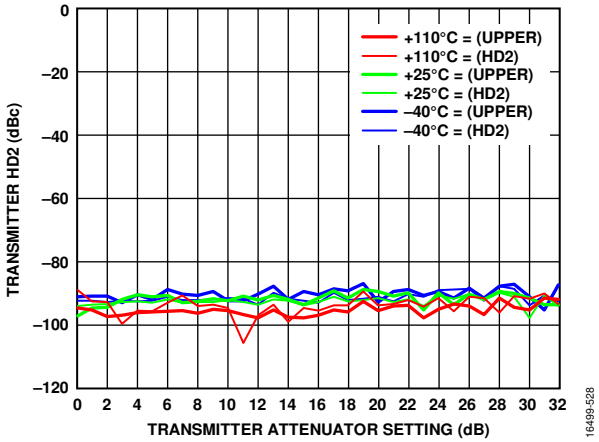

Figure 25. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 75 MHz, Continuous Wave = −15 dBFS

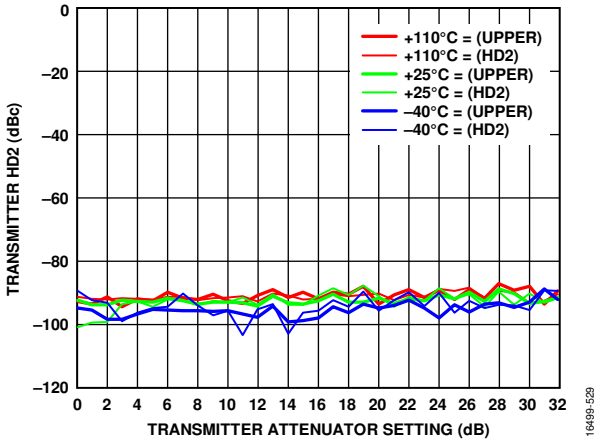

Figure 26. Transmitter HD2 vs. Transmitter Attenuation} Baseband Frequency = 10 MHz, LO = 300 MHz, Continuous Wave = −15 dBFS

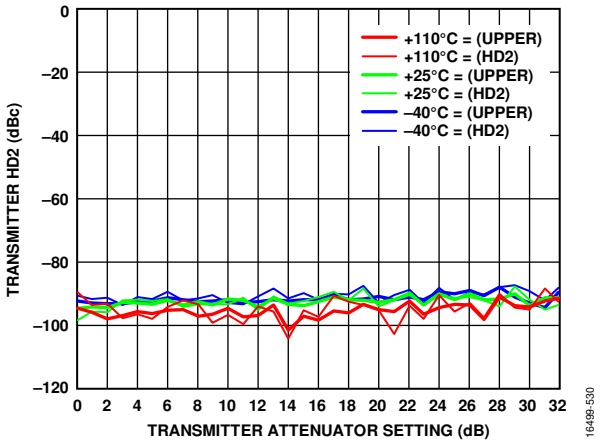

Figure 27. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 525 MHz, Continuous Wave = −15 dBFS

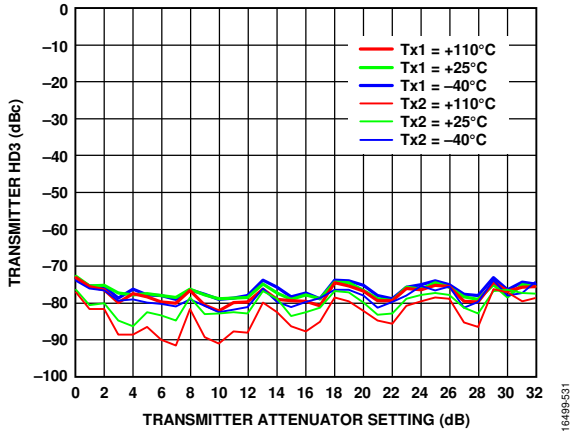

Figure 28. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 75 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

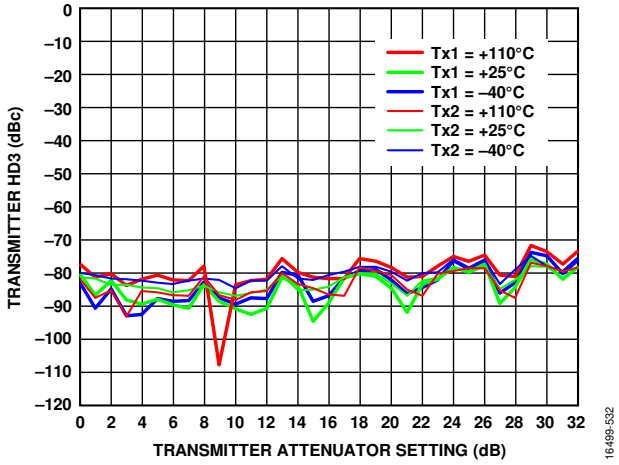

Figure 29. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 300 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

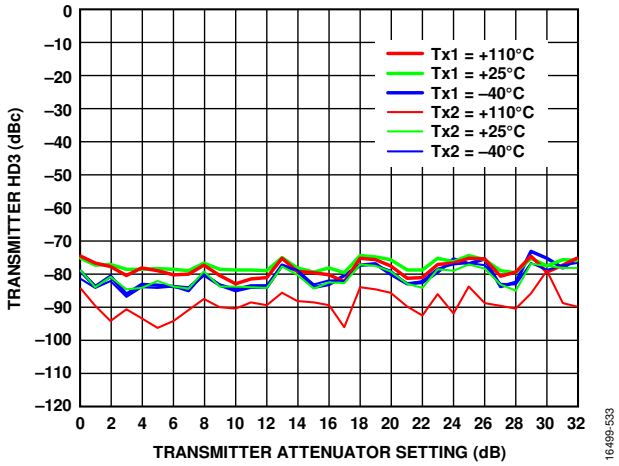

Figure 30. Transmitter HD3 vs. Transmitter Attenuation Setting, LO = 525 MHz, Continuous Wave = −15 dBFS, Baseband Frequency = 10 MHz

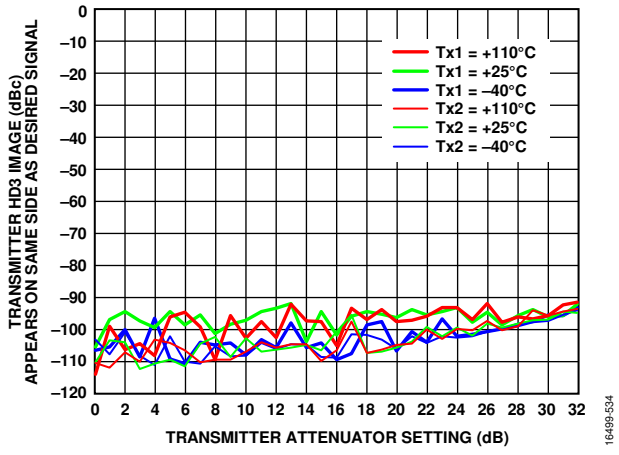

Figure 31. Transmitter HD3 Image on Same Side as Desired Signal vs. Transmitter Attenuation Setting, LO = 75 MHz, Continuous Wave = −15 dBFS

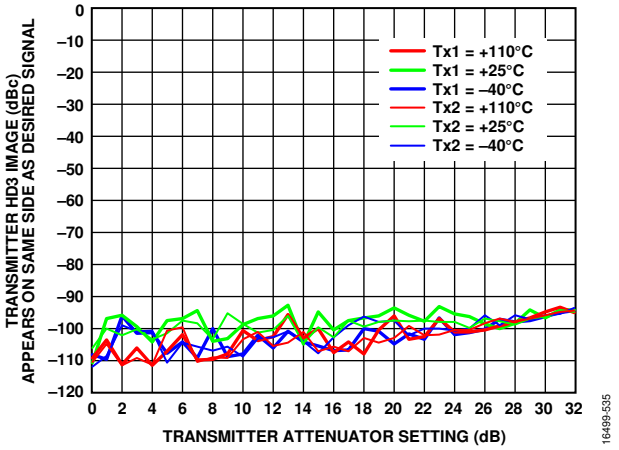

Figure 32. Transmitter HD3 Image, Appears on Same Sideband as Desired Signal vs. Transmitter Attenuation Setting, LO = 300 MHz, Continuous Wave = −15 dBFS

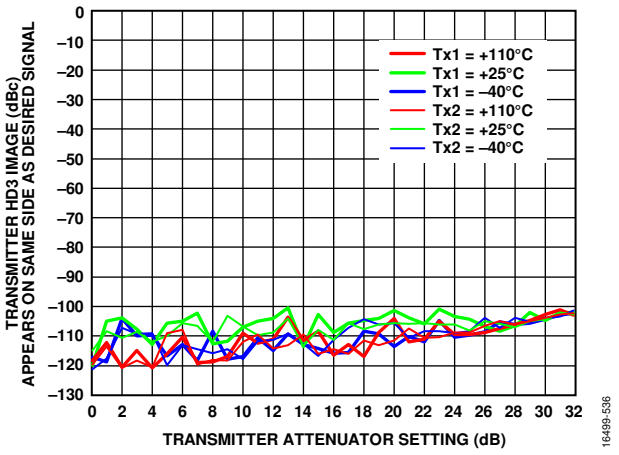

Figure 33. Transmitter HD3 Image on Same Side as Desired Signal vs. Transmitter AttenuationSetting, LO = 525 MHz, Continuous Wave = −15 dBFS

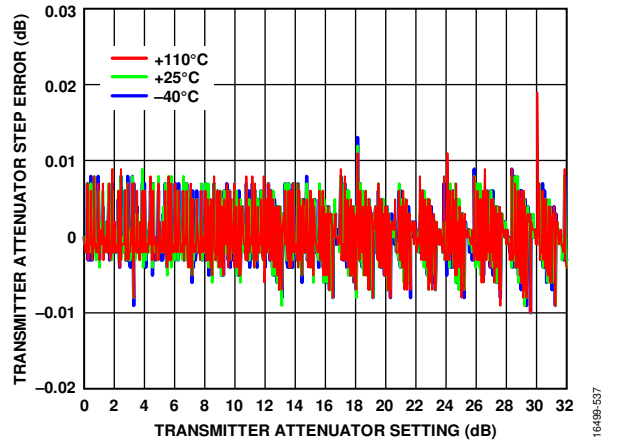

Figure 34. Transmitter Attenuation Step Error vs. Transmitter Attenuation Setting, LO = 75 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS