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Commercial Grade SHARC DSP Microcomputer

ADSP-21061/ADSP-21061L

SUMMARY

High performance signal processor for communications, graphics, and imaging applications

Super Harvard Architecture

- **Four independent buses for dual data fetch, instruction fetch, and nonintrusive I/O**

32-bit IEEE floating-point computation units—multiplier, ALU, and shifter

Dual-ported on-chip SRAM and integrated I/O peripherals—a complete system-on-a-chip

Integrated multiprocessing features

Dual data address generators with modulo and bit-reverse addressing

Efficient program sequencing with zero-overhead looping: single-cycle loop setup

IEEE JTAG Standard 1149.1 test access port and on-chip emulation

32-bit single-precision and 40-bit extended-precision IEEE floating-point data formats or 32-bit fixed-point data format

240-lead MQFP package, thermally enhanced MQFP, 225-ball plastic ball grid array (PBGA)

Lead (Pb) free packages. For more information, see Ordering Guide on Page 52.

KEY FEATURES—PROCESSOR CORE

50 MIPS, 20 ns instruction rate, single-cycle instruction execution

120 MFLOPS peak, 80 MFLOPS sustained performance

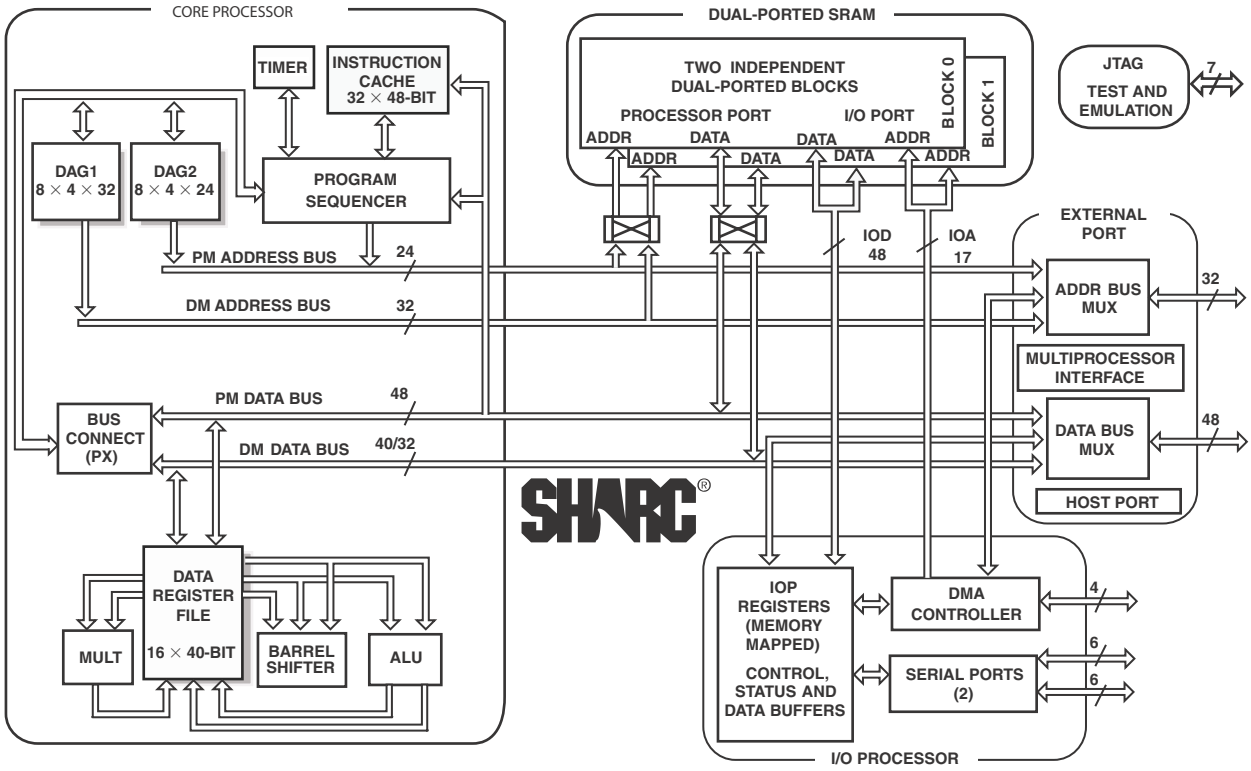

Figure 1. Functional Block Diagram

Rev. D **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

5/13—Rev C to Rev D

Updated Development Tools 7

Added Related Signal Chains 8

Removed the ADSP-21061LAS-176, ADSP-21061LKS-160, and ADSP-21061LKS-176 models from Ordering Guide 52

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21061 (5 V) and ADSP-21061L (3.3 V) processors for 33 MHz, 40 MHz, 44 MHz, and 50 MHz speed grades. The product name“ADSP-21061” is used throughout this data sheet to represent all devices, except where expressly noted.

GENERAL DESCRIPTION

The ADSP-21061 SHARC—Super Harvard Architecture Computer—is a signal processing microcomputer that offers new capabilities and levels of performance. The ADSP-21061 SHARC is a 32-bit processor optimized for high performance DSP applications. The ADSP-21061 builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-21061 has a 20 ns instruction cycle time and operates at 50 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 1 shows performance benchmarks for the ADSP-21061/ADSP-21061L.

The ADSP-21061 SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including 1M bit SRAM memory, a host processor interface, a DMA controller, serial ports, and parallel bus connectivity for glueless DSP multiprocessing.

Table 1. Benchmarks (at 50 MHz)

Benchmark Algorithm	Speed	Cycles
1024 Point Complex FFT (Radix 4, with reversal)	.37 ms	18,221
FIR Filter (per tap)	20 ns	1
IIR Filter (per biquad)	80 ns	4
Divide (y/x)	120 ns	6
Inverse Square Root	180 ns	9
DMA Transfer Rate	300M bps	

The ADSP-21061 continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1, illustrates the following architectural features:

- Computation units (ALU, multiplier, and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Interval timer
- On-chip SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and multiprocessor interface
- DMA controller
- Serial ports
- JTAG test access port

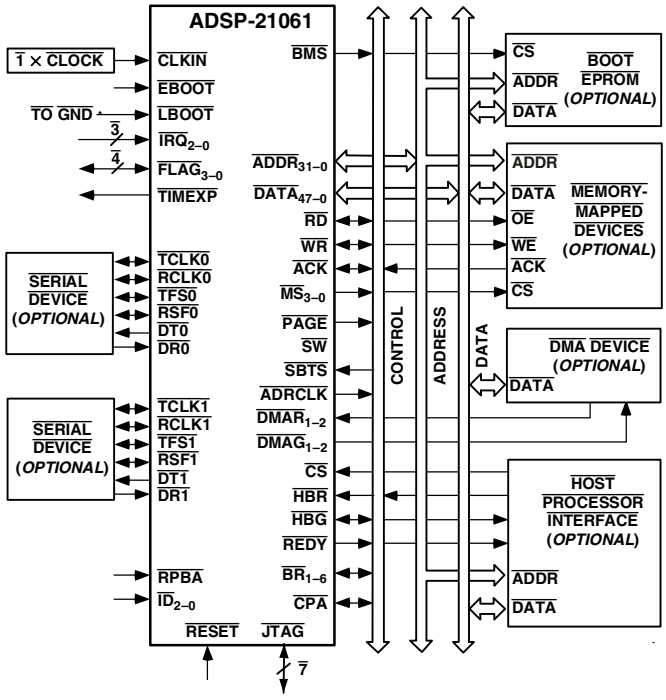

Figure 2. ADSP-21061/ADSP-21061L System Sample Configuration

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21061 includes the following architectural features of the ADSP-21000 family core. The ADSP-21061 processors are code- and function-compatible with the ADSP-21020, ADSP-21060, and ADSP-21062 SHARC processors.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended-precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-21061 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (Figure 1 on Page 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21061 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21061's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21061 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21061 can conditionally execute a multiply, an add, a subtract, and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-21061 processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21061 contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits each. Each bank has eight 16-bit columns with 4k 16-bit words per column. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21061 memory map).

On the ADSP-21061, the memory can be configured as a maximum of 32k words of 32-bit data, 64k words for 16-bit data, 16k words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 1 megabit. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21061's external port.

Off-Chip Memory and Peripherals Interface

The ADSP-21061's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-21061's unified address space. The separate on-chip buses—for program memory, data memory, and I/O—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus. The on-chip Super Harvard Architecture provides three-bus performance, while the off-chip unified address space gives flexibility to the designer.

Addressing of external memory devices is facilitated by on-chip decoding of high order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21061 provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

Host Processor Interface

The ADSP-21061's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-21061's external port and is memory-mapped into the unified address space. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21061's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-21061, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DMA Controller

The ADSP-21061's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

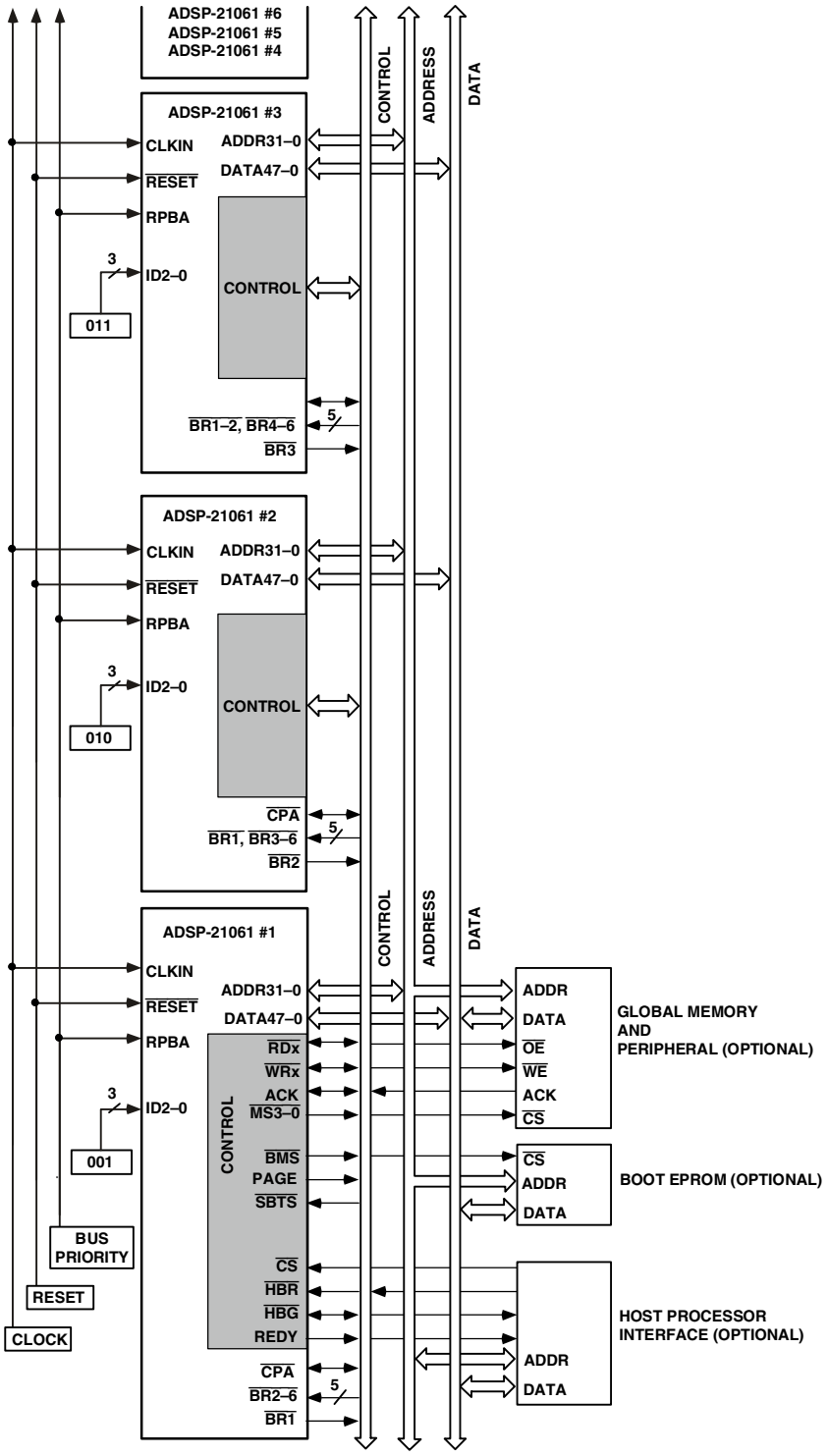

Figure 3. Shared Memory Multiprocessing System

DMA transfers can occur between the ADSP-21061's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21061's internal memory and its serial ports.

DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Six channels of DMA are available on the ADSP-21061—four via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21061s, memory or I/O transfers). Programs can be downloaded to the ADSP-21061 using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports

The ADSP-21061 features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of up to 50 Mbps. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and key mask features to enhance interprocessor communication.

Multiprocessing

The ADSP-21061 offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-21061's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21061s and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 500 Mbps over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21061s and can be used to implement reflective semaphores.

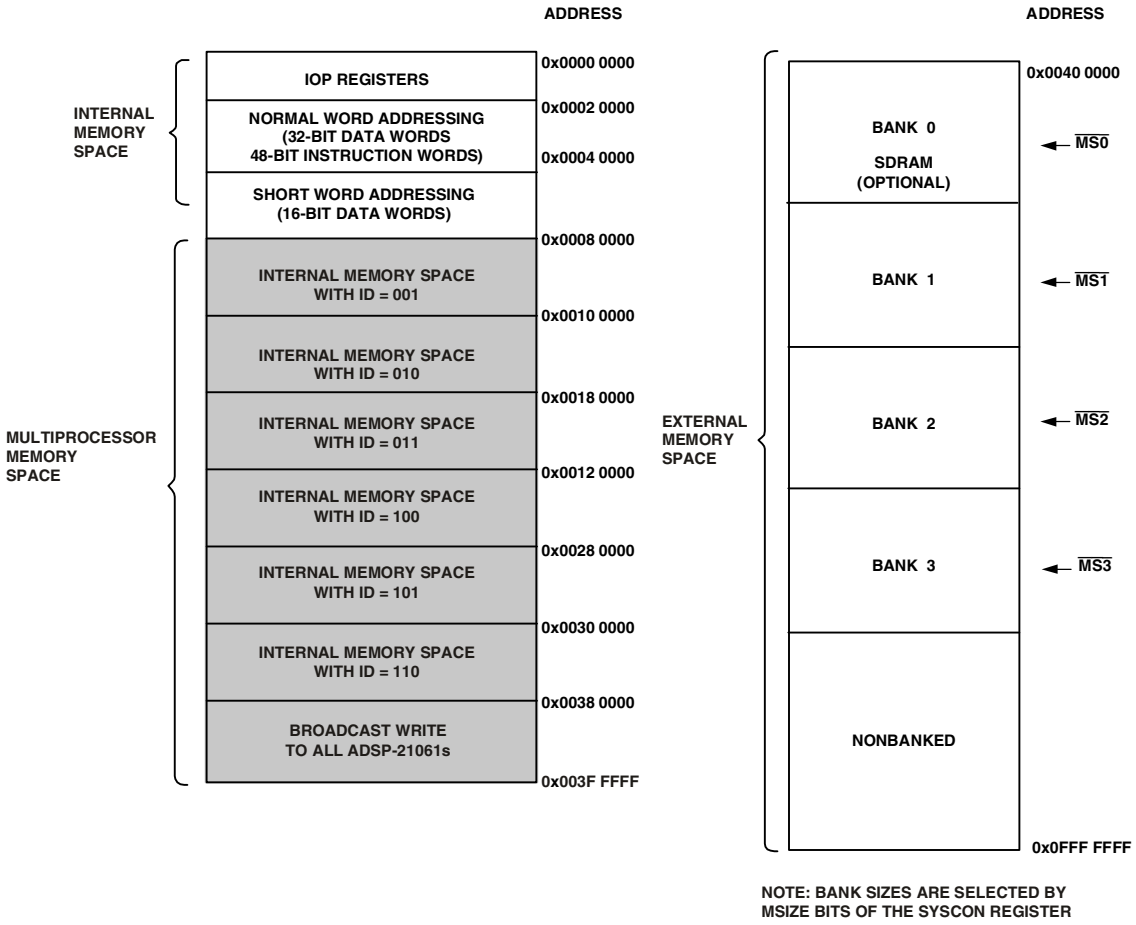

Figure 4. Memory Map

Program Booting

The internal memory of the ADSP-21061 can be booted at system power-up from either an 8-bit EPROM, or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (boot memory select), EBOOT (EPROM boot), and LBOOT (host boot) pins. 32-bit and 16-bit host processors can be used for booting.

PORTING CODE FROM THE ADSP-21060 OR ADSP-21062

The ADSP-21061 is pin compatible with the ADSP-21060/ADSP-21061/ADSP-21062 processors. The ADSP-21061 pins that correspond to the link port pins of the ADSP-21060/ADSP-21062 are no-connects.

The ADSP-21061 is object code compatible with the ADSP-21060/ADSP-21062 processors except for the following functional elements:

- The ADSP-21061 memory is organized into two blocks with eight columns that are 4k deep per block. The ADSP-21060/ADSP-21062 memory has 16 columns per block.
- Link port functions are not available.
- Handshake external port DMA pins DMAR2 and DMAG2 are assigned to external port DMA Channel 6 instead of Channel 8.
- 2-D DMA capability of the SPORT is not available.
- The modify registers in SPORT DMA are not programmable.

On the ADSP-21061, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks that alias into Block 1. This allows any code or data stored in Block 1 on the ADSP-21062 to retain the same addresses on the ADSP- 21061—these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061, use only the first eight columns of each memory bank. Limit your application to 8k of instructions or up to 16k of data in each bank of the ADSP-21062, or any combination of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21061 architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP- 2106x SHARC User's Manual.*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21061 pin definitions are listed below. All pins are identical on the ADSP-21061 and ADSP-21061L. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 2. Pin Descriptions

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address.** The ADSP-21061 outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-21061s. The ADSP-21061 inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data.** The ADSP-21061 inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47 to 16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47 to 8 of the bus. 16-bit short word data is transferred over Bits 31 to 16 of the bus. In PROM boot mode, 8-bit data is transferred over Bits 23 to 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-21061's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-21061 reads from external memory devices or from the internal memory of other ADSP-21061s. External devices (including other ADSP-21061s) must assert $\overline{\text{RD}}$ to read from the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-21061s.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-21061 writes to external memory devices or to the internal memory of other ADSP-21061s. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-21061s.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-21061 asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-21061's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-21061 to synchronous memory devices (including other ADSP-21061s). The ADSP-21061 asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-21061s to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-21061(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21061 deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-21061 deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21061 attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor halts and the memory access is not complete until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21061 deadlock, or used with a DRAM controller.
$\overline{\text{IRQ}}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
FLAG_{3-0}	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** This pin must be asserted by a host processor to request control of the ADSP-21061's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21061 that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21061 places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-21061 bus requests $\overline{\text{BR}}_{6-1}$ in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges a bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21061 until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21061 bus master and is monitored by all others.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21061.
REDY	O (O/D)	**Host Bus Acknowledge.** The ADSP-21061 deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR}}_{2-1}$	I/A	**DMA Request 1** (DMA Channel 7) and **DMA Request 2** (DMA Channel 6).
$\overline{\text{DMAG}}_{2-1}$	O/T	**DMA Grant 1** (DMA Channel 7) and **DMA Grant 2** (DMA Channel 6).
$\overline{\text{BR}}_{6-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21061 processors to arbitrate for bus mastership. An ADSP-21061 only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21061s, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
$\overline{\text{ID2–0}}$	O (O/D)	**Multiprocessing ID.** Determines which multiprocessing bus request ($\overline{\text{BR1}}$– $\overline{\text{BR6}}$) is used by ADSP-21061. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, etc., ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired or changed at reset only.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21061. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21061.
$\overline{\text{CPA}}$	I/O (O/D)	**Core Priority Access.** Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-21061 bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open-drain output that is connected to all ADSP-21061s in the system. The $\overline{\text{CPA}}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTx	O	**Data Transmit (Serial Ports 0, 1).** Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	**Data Receive (Serial Ports 0, 1).** Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50 kΩ internal pull-up resistor.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-21061 is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{BMS}$ inputs determine booting mode. See the table in the $\overline{BMS}$ pin description below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot.** Must be tied to GND.
$\overline{BMS}$	I/O/T*	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{BMS}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-21061 will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{BMS}$ is an output). *EBOOT* / *LBOOT* / *$\overline{BMS}$* / *Booting Mode* 1 / 0 / Output / EPROM (Connect $\overline{BMS}$ to EPROM chip select.) 0 / 0 / 1(Input) / Host Processor. 0 / 0 / 0 (Input) / No Booting. Processor executes from external memory.
CLKIN	I	**Clock In.** External clock input to the ADSP-21061. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{RESET}$	I/A	**Processor Reset.** Resets the ADSP-21061 to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{TRST}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21061. $\overline{TRST}$ has a 20 kΩ internal pull-up resistor.
$\overline{EMU}$	O	**Emulation Status.** Must be connected to the ADSP-21061 EZ-ICE target board connector only. $\overline{EMU}$ has a 50 kΩ internal pull-up resistor.
ICSA	O	**Reserved.** Leave unconnected.
VDD	P	**Power Supply**. (30 pins). See Operating Conditions (5 V) and Operating Conditions (3.3 V).
GND	G	**Power Supply Return.** (30 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{SBTS}$ is asserted, or when the ADSP-21061 is a bus slave)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TDI, TDO, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row, 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the farthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

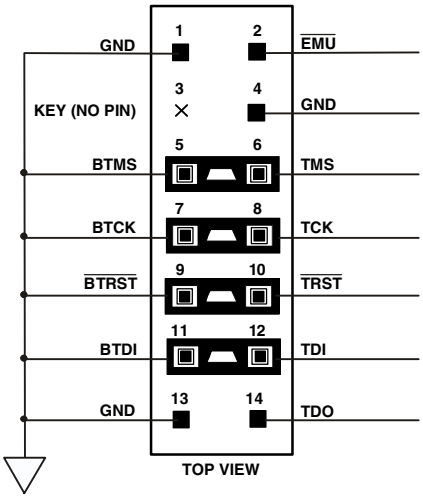

Figure 5. Target Board Connector For ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inches in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 3.

Table 3. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
$\overline{\text{TRST}}$[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
$\overline{\text{EMU}}$	Active Low, 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software startup. After software startup, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21061 processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-21061s (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 below and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x SHARC User's Manual*.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

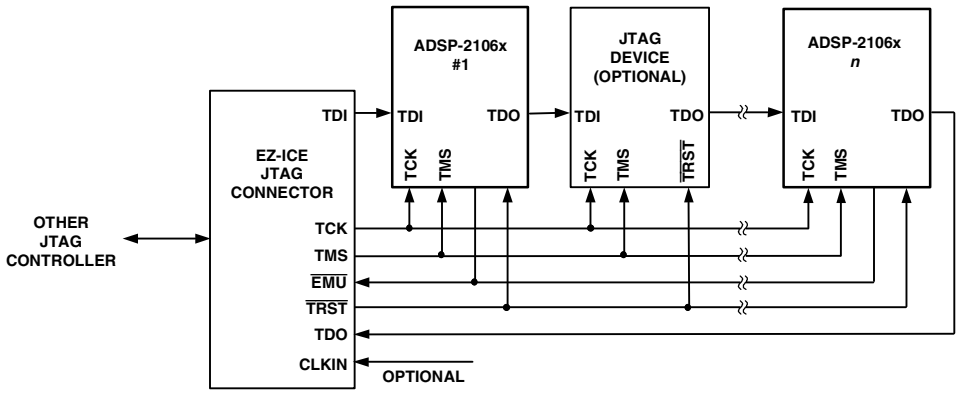

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

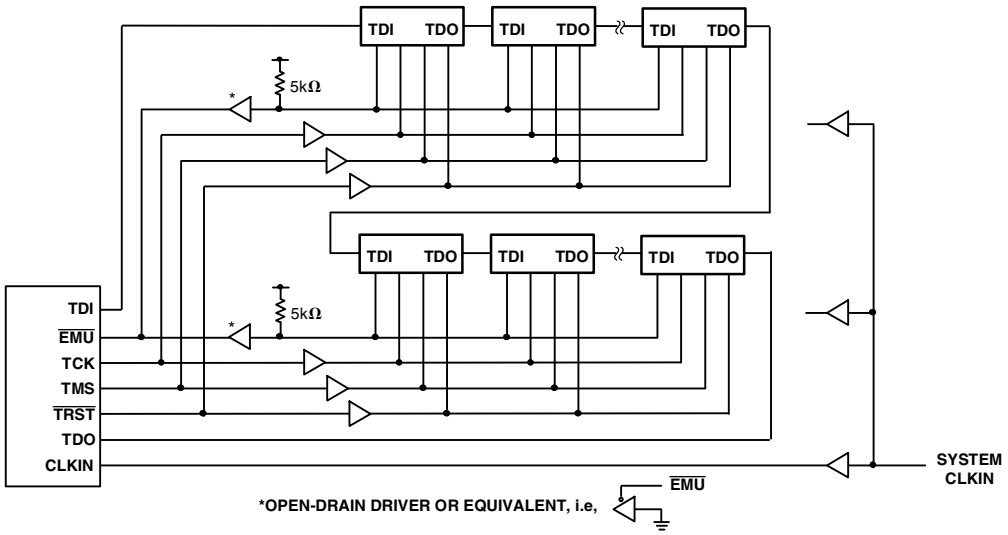

Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

ADSP-21061 SPECIFICATIONS

OPERATING CONDITIONS (5 V)

Parameter	Description	K Grade			Unit
		Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
T_{CASE}	Case Operating Temperature	0		85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 44 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups:DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

%PEAK $I_{DDINPEAK}$ + *%HIGH* $I_{DDINHIGH}$ + *%LOW* $I_{DDINLOW}$ + *%IDLE* I_{DDIDLE} = *power consumption*

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	595	mA
	t_{CK} = 25 ns, V_{DD} = Max	680	mA
	t_{CK} = 20 ns, V_{DD} = Max	850	
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	460	mA
	t_{CK} = 25 ns, V_{DD} = Max	540	mA
	t_{CK} = 20 ns, V_{DD} = Max	670	
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 30 ns, V_{DD} = Max	270	mA
	t_{CK} = 25 ns, V_{DD} = Max	320	mA
	t_{CK} = 20 ns, V_{DD} = Max	390	
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	200	mA
I_{DDIDLE} Supply Current (Idle16)[5]	V_{DD} = Max	55	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.

[5] Idle16 denotes ADSP-2106x state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (5 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 4. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 25 V	= 0.084 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 25 V	= 0.022 W
Data	32	50	× 14.7 pF	× 10 MHz	× 25 V	= 0.059 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 25 V	= 0.002 W

P_{EXT} = 0.167 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ADSP-21061L SPECIFICATIONS

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade			K Grade			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	3.15	3.3	3.45	3.15	3.3	3.45	V
T_{CASE}	Case Operating Temperature	–40		+85	0		+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1,2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 45 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = power\ consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 25 ns, V_{DD} = Max	480	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	535	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 25 ns, V_{DD} = Max	380	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	425	mA
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 25 ns, V_{DD} = Max	220	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	245	mA
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	180	mA
I_{DDIDLE} Supply Current (Idle)[5]	V_{DD} = Max	50	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.

[5] Idle16 denotes ADSP-21061L state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 5. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	5 V	3.3 V
Supply Voltage (V_{DD})	–0.3 V to +7.0 V	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} +0.5 V	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} +0.5 V	–0.5 V to V_{DD} +0.5 V
Load Capacitance	200 pF	200 pF
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C
Lead Temperature (5 seconds)	280°C	280°C
Junction Temperature Under Bias	130°C	130°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

The information presented in Figure 8 provides details about the package branding for the ADSP-21061 processor. For a complete listing of product availability, see Ordering Guide on Page 52.

Figure 8. Typical Package Marking (Actual Marking Format May Vary)

Table 6. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

The timing specifications shown are based on a CLKIN frequency of 50 MHz (t_{CK} = 20 ns). The DT derating enables the calculation of timing specifications within the min to max range of the t_{CK} specification (see Table 7). DT is the difference between the derated CLKIN period (t_{CK}) and a CLKIN period of 25 ns:

$$DT = t_{CK} - 20\ ns$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

For voltage reference levels, see Figure 29 under Test Conditions.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices. (O/D) = Open Drain, (A/D) = Active Drive.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Clock Input

Table 7. Clock Input

Parameter		ADSP-21061 50 MHz, 5 V Min	ADSP-21061 50 MHz, 5 V Max	ADSP-21061L 44 MHz, 3.3 V Min	ADSP-21061L 44 MHz, 3.3 V Max	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Min	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Max	ADSP-21061 33 MHz, 5 V Min	ADSP-21061 33 MHz, 5 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	20	100	22.5	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		7		7		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

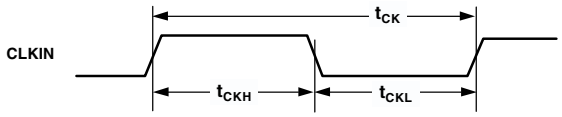

Figure 9. Clock Input

Reset

Table 8. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

[2] Only required if multiple ADSP-21061s must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21061s communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

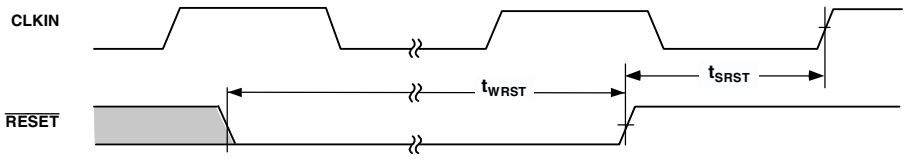

Figure 10. Reset

Interrupts

Table 9. Interrupts

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

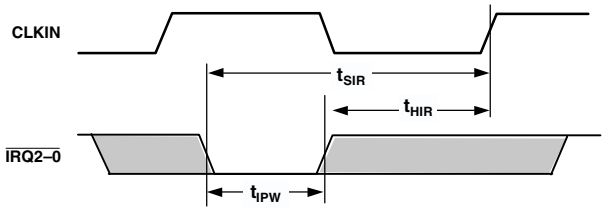

Figure 11. Interrupts

Timer

Table 10. Timer

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

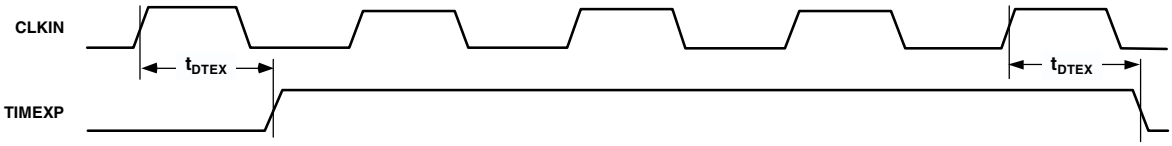

Figure 12. Timer

Flags

Table 11. Flags

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	8 + 5DT/16		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	0 – 5DT/16		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RD}$/$\overline{WR}$ Low[1]		5 + 7DT/16	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		16	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	4		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	3		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable		14	ns

[1] Flag inputs meeting these setup and hold times for Instruction Cycle N will affect conditional instructions in Instruction Cycle N+2.

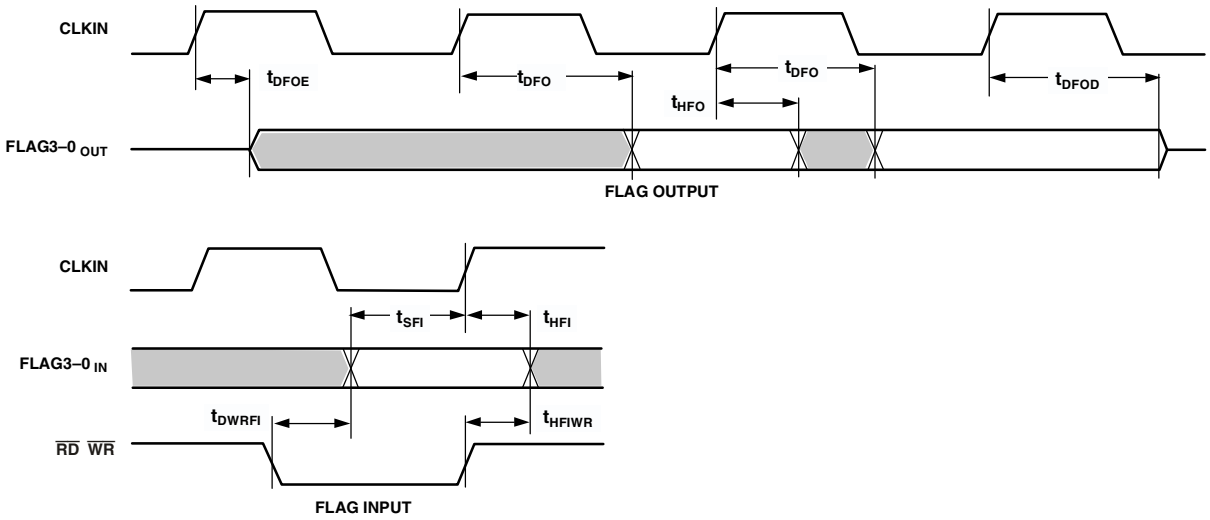

Figure 13. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 12. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 43 for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} (Table 13 on Page 25) for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

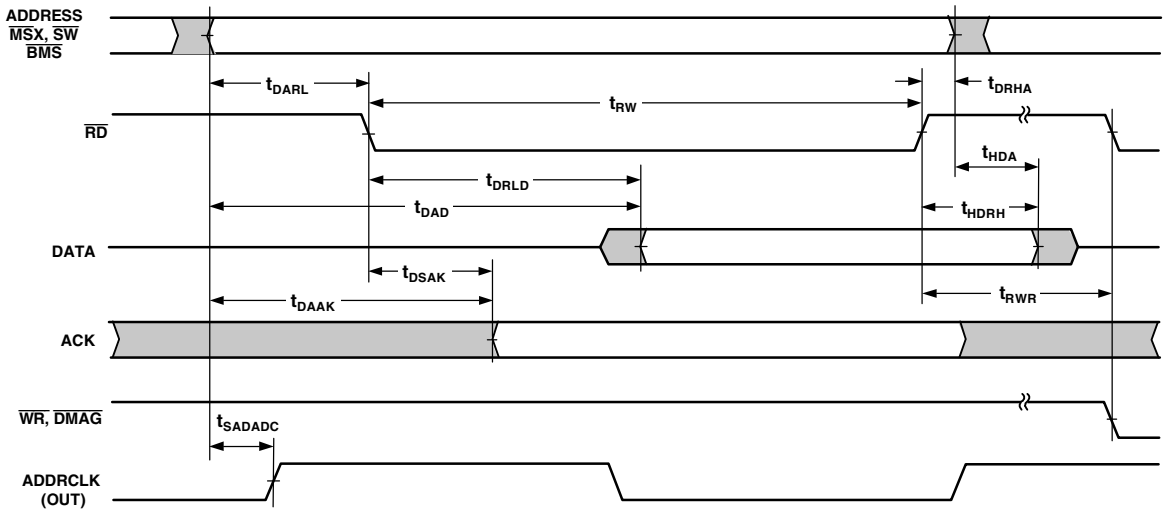

Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 13. Memory Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	13 + 9DT/16 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	7 + DT/2 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	1 + DT/16 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] For more information, see Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

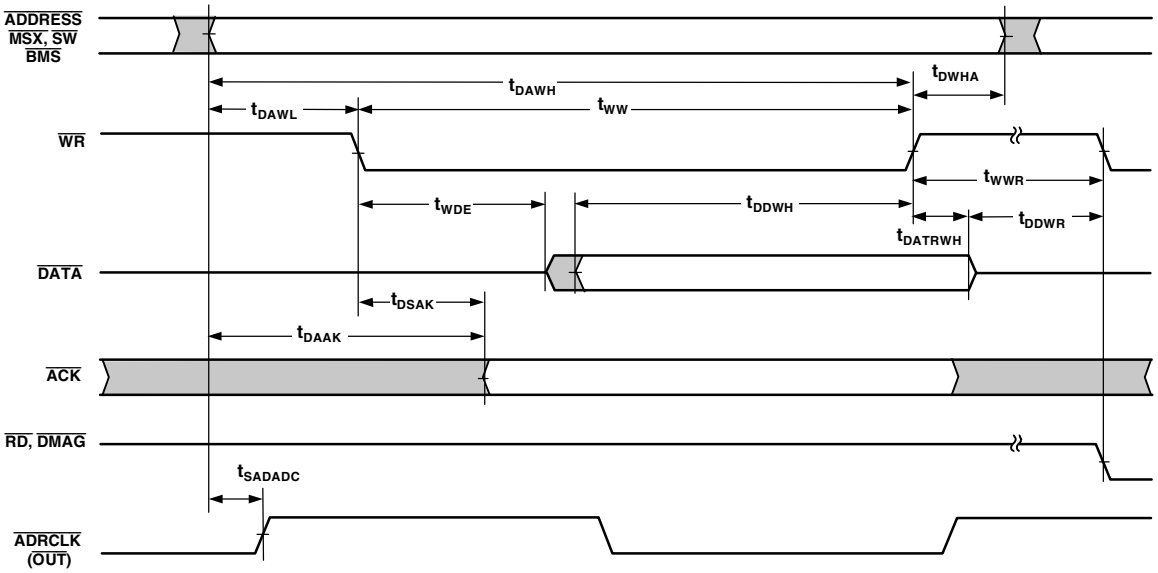

Figure 15. Memory Write—Bus Master