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*dB*COOL™ Remote Thermal Controller and Fan Controller

ADT7460

FEATURES

Controls and monitors up to 4 fan speeds
1 on-chip and 2 remote temperature sensors
Dynamic T_{MIN} control mode optimizes system acoustics intelligently
Automatic fan speed control mode controls system cooling based on measured temperature
Enhanced acoustic mode dramatically reduces user perception of changing fan speeds
Thermal protection feature via $\overline{\text{THERM}}$ output
Monitors performance impact of Intel® Pentium® 4
Processor thermal control circuit via $\overline{\text{THERM}}$ input
2-wire and 3-wire fan speed measurement
Limit comparison of all monitored values
Meets SMBus 2.0 electrical specifications (fully SMBus 1.1-compliant)

APPLICATIONS

Low acoustic noise PCs
Networking and telecommunications equipment

GENERAL DESCRIPTION

The ADT7460[1] *dB*COOL controller is a thermal monitor and multiple PWM fan controller for noise-sensitive applications requiring active system cooling. It can monitor the temperature of up to two remote sensor diodes plus its own internal temperature. It can measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise. The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7460 also provides critical thermal protection to the system by using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

FUNCTIONAL BLOCK DIAGRAM

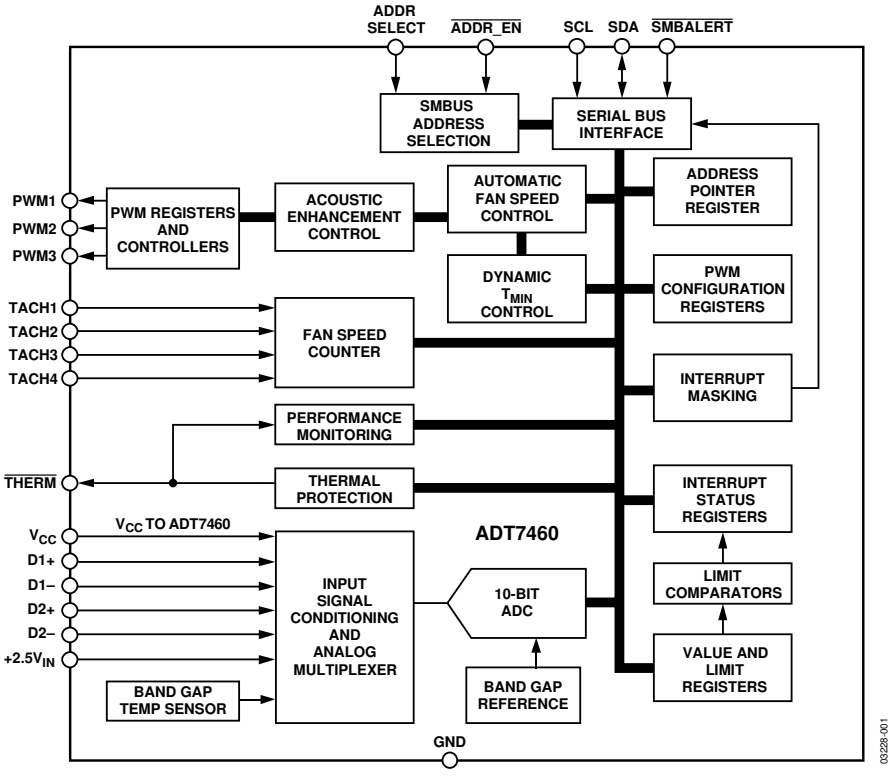

Figure 1.

[1]Protected by U.S. Patent Nos. 6,188,189; 6,169,442; 6,097,239; 5,982,221; and 5,867,012. Other patents pending.

Rev. C

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SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.

Table 1.

Parameter[1, 2, 3]	Min	Typ[4]	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	5.0	5.5	V	
Supply Current, I_{CC}			3	mA	Interface inactive, ADC active
			20	µA	Standby mode
TEMPERATURE-TO-DIGITAL CONVERTER					
Local Sensor Accuracy			±1.5	°C	0°C ≤ T_A ≤ 70°C
			±3	°C	−40°C ≤ T_A ≤ +120°C
Resolution		0.25		°C	
Remote Diode Sensor Accuracy			±1.5	°C	0°C ≤ T_A ≤ 70°C; 0°C ≤ T_D ≤ 120°C
			±2.5	°C	0°C ≤ T_A ≤ 105°C; 0°C ≤ T_D ≤ 120°C
			±3	°C	0°C ≤ T_A ≤ 120°C; 0°C ≤ T_D ≤ 120°C
Resolution		0.25		°C	
Remote Sensor Source Current		180		µA	High level
		11		µA	Low level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE			±1.5	%	
Differential Nonlinearity, DNL			±1	LSB	8 bits
Power Supply Sensitivity		±0.1		%/V	
Conversion Time (Voltage Input)		11.38	13	ms	Averaging enabled
Conversion Time (Local Temperature)		12.09	13.50	ms	Averaging enabled
Conversion Time (Remote Temperature)		25.59	28	ms	Averaging enabled
Total Monitoring Cycle Time		120.17	134.50	ms	Averaging enabled (incl. delay[5])
		13.51	15	ms	Averaging disabled
Input Resistance	80	140	200	kΩ	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±7	%	0°C ≤ T_A ≤ 70°C
			±11	%	0°C ≤ T_A ≤ 105°C
			±13	%	−40°C ≤ T_A ≤ +120°C
Full-Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan count = 0xBFFF
		329		RPM	Fan count = 0x3FFF
		5000		RPM	Fan count = 0x0438
		10000		RPM	Fan count = 0x021C
Internal Clock Frequency	82.8	90.0	97.2	kHz	
OPEN-DRAIN DIGITAL OUTPUTS, PWM1–PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = −8.0 mA, V_{CC} = 3.3 V
High Level Output Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = −4.0 mA, V_{CC} = 3.3 V
High Level Output Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$
SMBUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	

Parameter[1, 2, 3]	Min	Typ[4]	Max	Unit	Test Conditions/Comments
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			5.5	V	Maximum input voltage
Input Low Voltage, V_{IL}			+0.8	V	
	−0.3			V	Minimum input voltage
Hysteresis		0.5		V p-p	
DIGITAL INPUT LOGIC LEVELS ($\overline{THERM}$)					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.8	V	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	−1			µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}			+1	µA	$V_{IN} = 0$
Input Capacitance, C_{IN}		5		pF	
SERIAL BUS TIMING[6]					
Clock Frequency, f_{SCLK}			400	kHz	See Figure 2
Glitch Immunity, t_{SW}			50	ns	
Bus Free Time, t_{BUF}	1.3			µs	See Figure 2
Start Setup Time, $t_{SU;STA}$	0.6			µs	See Figure 2
Start Hold Time, $t_{HD;STA}$	0.6			µs	See Figure 2
SCL Low Time, t_{LOW}	1.3			µs	See Figure 2
SCL High Time, t_{HIGH}	0.6			µs	See Figure 2
SCL, SDA Rise Time, t_R			300	ns	See Figure 2
SCL, SDA Fall Time, t_F			300	µs	See Figure 2
Data Setup Time, $t_{SU;DAT}$	100			ns	See Figure 2
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms	Can be optionally disabled

[1] All voltages are measured with respect to GND, unless otherwise specified.
[2] Logic inputs accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}.
[3] Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and at V_{IH} = 2.0 V for a rising edge.
[4] Typicals are at T_A = 25°C and represent the most likely parametric norm.
[5] The delay is the time between the round robin finishing one set of measurements and starting the next.
[6] Guaranteed by design, not production tested.

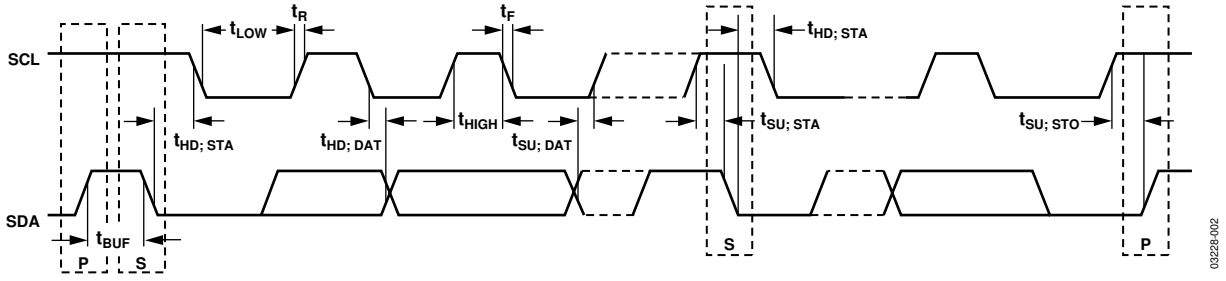

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage (V_{CC})	6.5 V
Voltage on Any Other Input or Output Pin	−0.3 V to +6.5 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
IR Reflow Peak Temperature	220°C
IR Reflow Peak Temperature for Pb Free	260°C
Lead Temperature (Soldering 10 s)	300°C
ESD Rating	1500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

16-Lead QSOP Package:
θ_{JA} = 150°C/W
θ_{JC} = 39°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

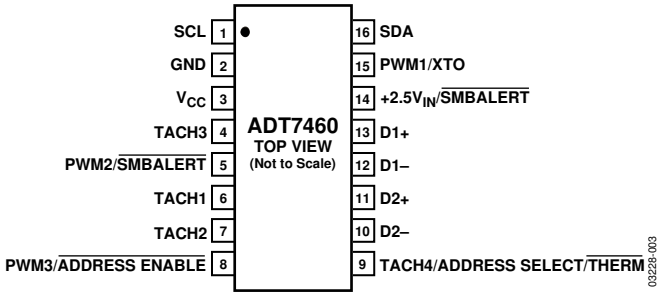

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7460.
3	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7460 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans.
5	PWM2	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse-width modulated output to control Fan 2 speed.
	$\overline{\text{SMBALERT}}$	Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans.
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans.
8	PWM3	Digital I/O (Open Drain). Pulse-width modulated output to control Fan 3/4 speed. Requires 10 kΩ typical pull-up.
	$\overline{\text{ADDRESS}}$ $\overline{\text{ENABLE}}$	If pulled low on power-up, this places the ADT7460 into address select mode, and the state of Pin 9 determines the ADT7460's slave address.
9	TACH4	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans.
	ADDRESS SELECT	If in address select mode, this pin determines the SMBus device address.
	$\overline{\text{THERM}}$	Alternatively, the pin may be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	$+2.5V_{IN}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage.
	$\overline{\text{SMBALERT}}$	Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
15	PWM1/XTO	Digital Output (Open Drain). Pulse-width modulated output to control Fan 1 speed. Requires 10 kΩ typical pull-up.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pull-up.

TYPICAL PERFORMANCE CHARACTERISTICS

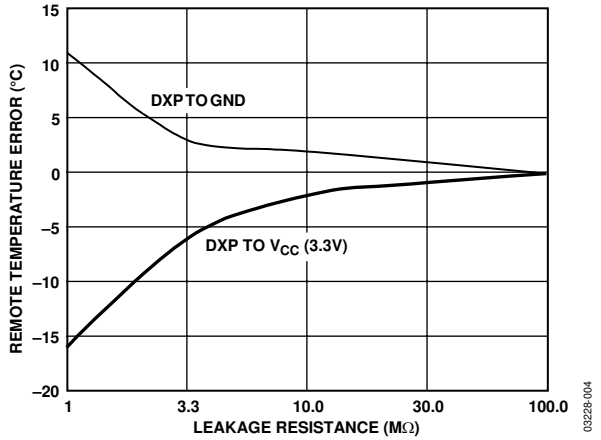

Figure 4. Remote Temperature Error vs. Leakage Resistance

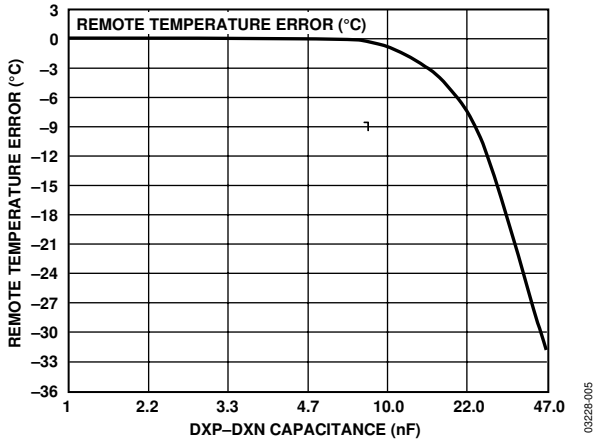

Figure 5. Remote Temperature Error vs. Capacitance between D+ and D–

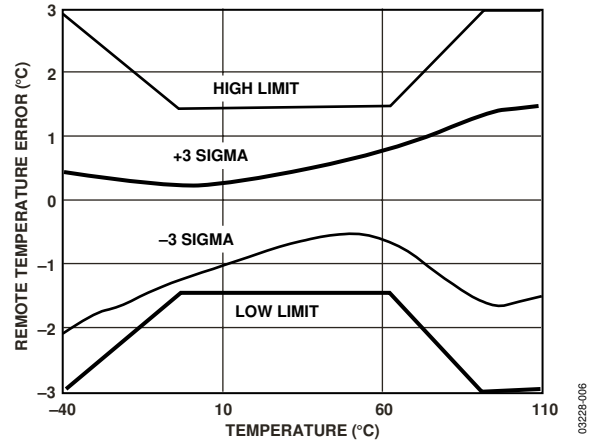

Figure 6. Remote Temperature Error vs. Actual Temperature

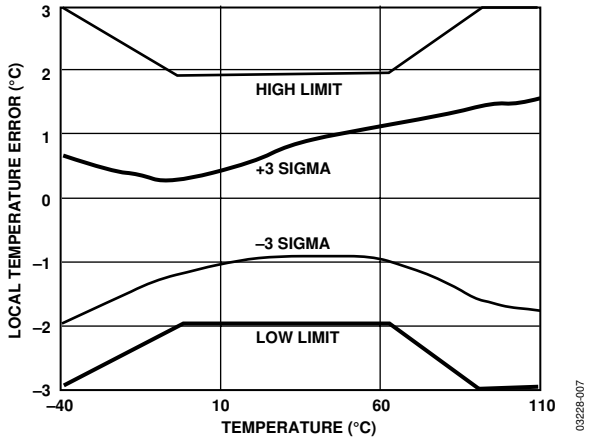

Figure 7. Local Temperature Error vs. Actual Temperature

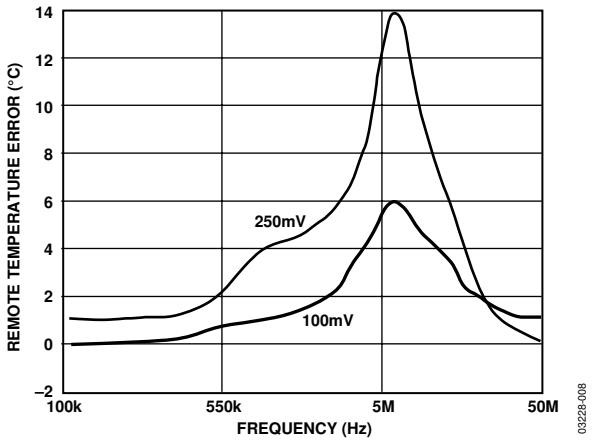

Figure 8. Remote Temperature Error vs. Power Supply Noise Frequency

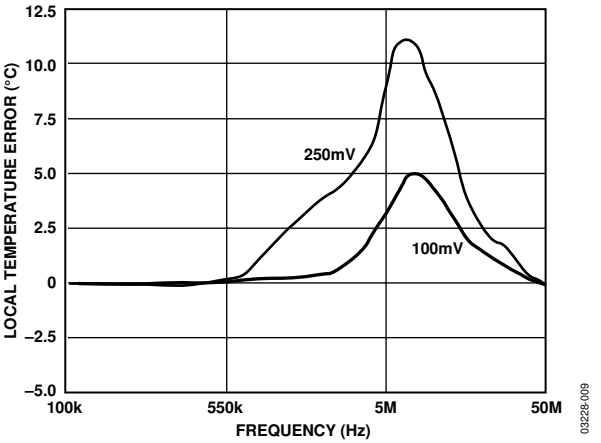

Figure 9. Local Temperature Error vs. Power Supply Noise Frequency

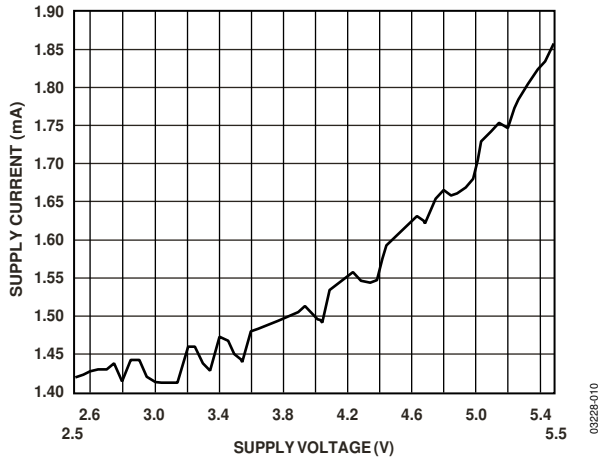

Figure 10. Supply Current vs. Supply Voltage

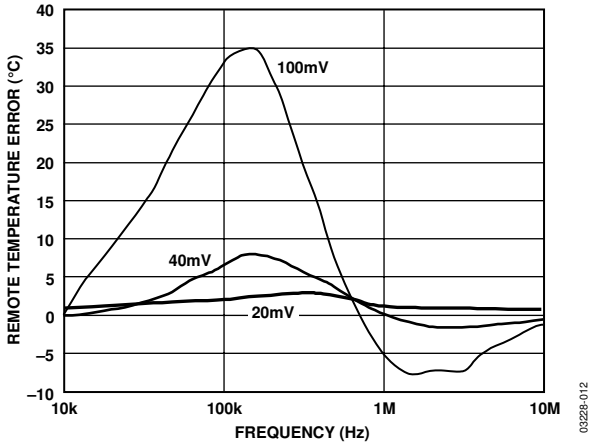

Figure 12. Remote Temperature Error vs. Common-Mode Noise Frequency

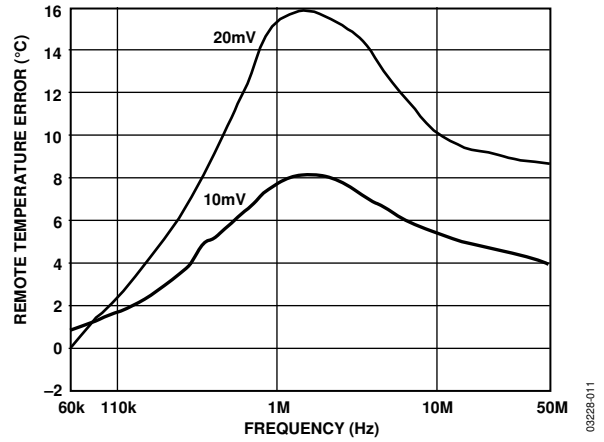

Figure 11. Remote Temperature Error vs. Differential Mode Noise Frequency

PRODUCT DESCRIPTION

The ADT7460 is a thermal monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial System Management Bus (SMBus). The serial bus controller has an optional address line for device selection (Pin 9), a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions of the ADT7460 are performed over the serial bus. In addition, two of the pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to indicate out-of-limit conditions.

MEASUREMENT INPUTS

The device has three measurement inputs, one for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on-chip temperature sensor.

Pin 14 is an analog input with an on-chip attenuator and is configured to monitor 2.5 V.

Power is supplied to the chip via Pin 3, and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5 V supply and monitor it without overranging.

Remote temperature sensing is provided by the D1± and D2± inputs, to which diode-connected, external temperature-sensing transistors, such as a 2N3904 or CPU thermal diode, may be connected.

The ADC also accepts input from an on-chip band gap temperature sensor, which monitors system ambient temperature.

SEQUENTIAL MEASUREMENT

When the ADT7460 monitoring sequence is started, it cycles sequentially through the measurement of 2.5 V input and the temperature sensors. Measured values from these inputs are stored in value registers. These can be read out over the serial bus or can be compared with programmed limits stored in the limit registers. The results of out-of-limit comparisons are stored in the status registers, which can be read over the serial bus to flag out-of-limit conditions.

RECOMMENDED IMPLEMENTATION

Configuring the ADT7460 as in Figure 13 allows the systems designer the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU temperature measured using Remote 1 temperature channel.
- Ambient temperature measured through Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. Allows Intel Pentium 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output.
- $\overline{\text{SMBALERT}}$ system interrupt output.

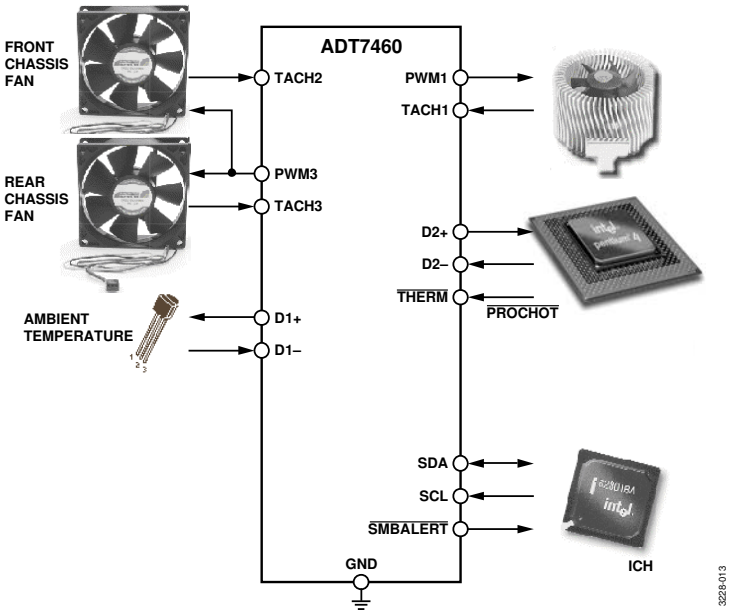

Figure 13. Recommended Implementation

ADT7460 ADDRESS SELECTION

Pin 8 is the dual-function PWM3/$\overline{\text{ADDRESS ENABLE}}$ pin. If Pin 8 is pulled low on power-up, the ADT7460 reads the state of Pin 9 (TACH4/ADDRESS SELECT/$\overline{\text{THERM}}$) to determine the ADT7460's slave address. If Pin 8 is high on power-up, the ADT7460 defaults to SMBus Slave Address 0x2E. This function is described in more detail later.

INTERNAL REGISTERS OF THE ADT7460

Table 4 summarizes the ADT7460's principal internal registers. Table 41 to Table 81 describe the registers in more detail.

Table 4. Summary Internal Registers

Register	Description
Configuration	These registers provide control and configuration of the ADT7460, including alternate pinout functionality.
Address Pointer	This register contains the address that selects one of the other internal registers. When writing to the ADT7460, the first byte of data is always a register address, which is written to the address pointer register.
Status Registers	These registers provide the status of each limit comparison and are used to signal out-of-limit conditions on the temperature, voltage, or fan speed channels. If Pin 14 or Pin 5 is configured as $\overline{\text{SMBALERT}}$, this pin asserts low whenever an unmasked status bit is set.
Interrupt Mask	These registers allow each interrupt status event to be masked when Pin 14 or Pin 5 is configured as an $\overline{\text{SMBALERT}}$ output.
Value and Limit	The results of analog voltage input, temperature, and fan speed measurements are stored in these registers, along with their limit values.
Offset	These registers allow each temperature channel reading to be offset by a twos complement value written to these registers.
T_{MIN}	These registers program the starting temperature for each fan under automatic fan speed control.
T_{RANGE}	These registers program the temperature-to-fan speed control slope in automatic fan speed control mode for each PWM output.
Operating Point	These registers define the target operating temperatures for each thermal zone when running under dynamic T_{MIN} control. This function allows the cooling solution to adjust dynamically in response to measured temperature and system performance.
Enhance Acoustics	These registers allow each PWM output controlling fan to be tweaked to enhance the system's acoustics.

THEORY OF OPERATION

SERIAL BUS INTERFACE

Control of the ADT7460 is carried out using the serial System Management Bus (SMBus). The ADT7460 is connected to this bus as a slave device, under the control of a master controller.

The ADT7460 has a 7-bit serial bus address. When the device is powered up with Pin 8 (PWM3/$\overline{\text{ADDRESS ENABLE}}$) high, the ADT7460 has a default SMBus address of 0101110 or 0x2E. If more than one ADT7460 is to be used in a system, each ADT7460 should be placed in address select mode by strapping Pin 8 low on power-up. The logic state of Pin 9 then determines the device's SMBus address. The logic state of these pins is sampled on power-up.

The device address is sampled and latched on the first valid SMBus transaction, more precisely, on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDRESS ENABLE}}$ /ADDRESS SELECT pins. Any attempted changes in the address has no effect after this.

Table 5. Address Select Mode

Pin 8 State	Pin 9 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ pull-up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (default)

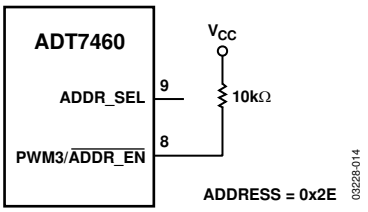

Figure 14. Default SMBus Address 0x2E

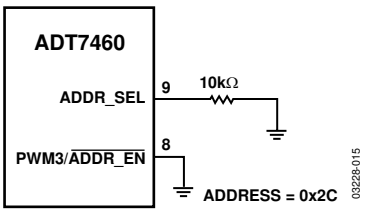

Figure 15. SMBus Address 0x2C (Pin 9 = 0)

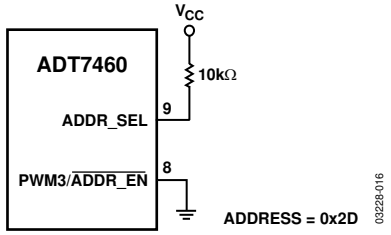

Figure 16. SMBus Address 0x2D (Pin 9 = 1)

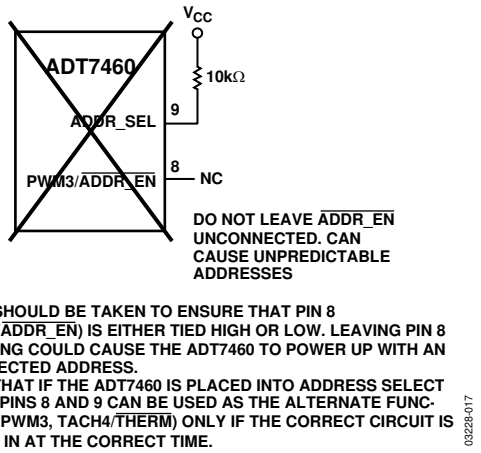

Figure 17. Unpredictable SMBus Address if Pin 8 is Unconnected

The facility to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7460 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the star condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{\text{W}}$ bit, which determine the direction of the data transfer, that is, whether data is written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master writes to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADT7460, write operations contain either one or two bytes, and read operations contain one byte.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written in that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 18. The device address is sent over the bus followed by R/$\overline{W}$ being set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

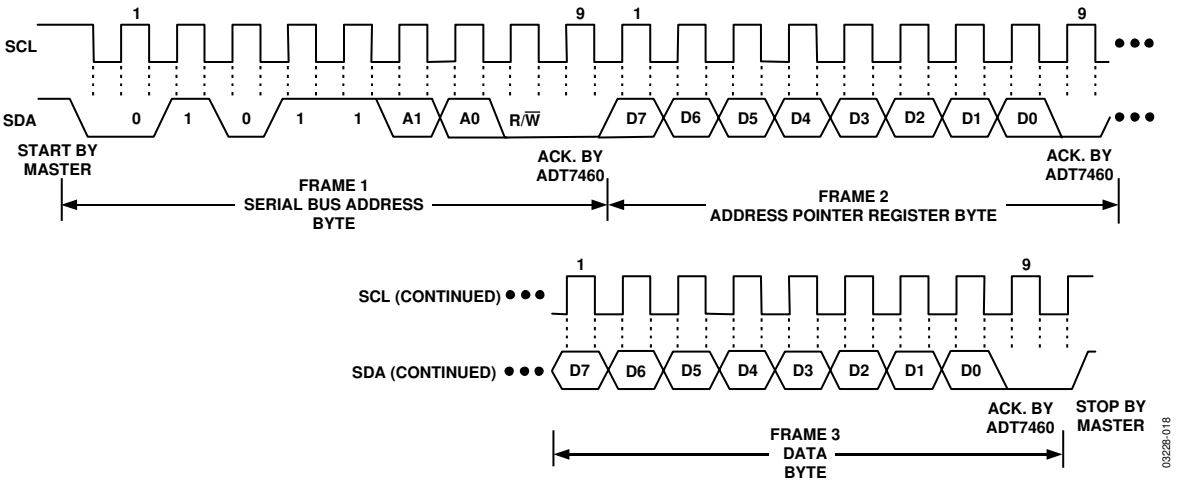

Figure 18. Writing a Register Address to the Address Pointer Register, Then Writing Data to the Selected Register

When reading data from a register, there are two possibilities:

- If the ADT7460's address pointer register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7460 as before, but only the data byte containing the register address is sent because data is not to be written to the register. This is shown in Figure 19.

  A read operation is then performed, consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 20.

- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, so Figure 19 can be omitted.

It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In Figure 18 to Figure 20, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.

In addition to supporting the Send Byte and Receive Byte protocols, the ADT7460 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information).

If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7460 are discussed below. The following abbreviations are used in the diagrams:

S—start
P—stop
R—read
W—write
A—acknowledge
$\overline{A}$—no acknowledge

The ADT7460 uses the following SMBus write protocols:

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

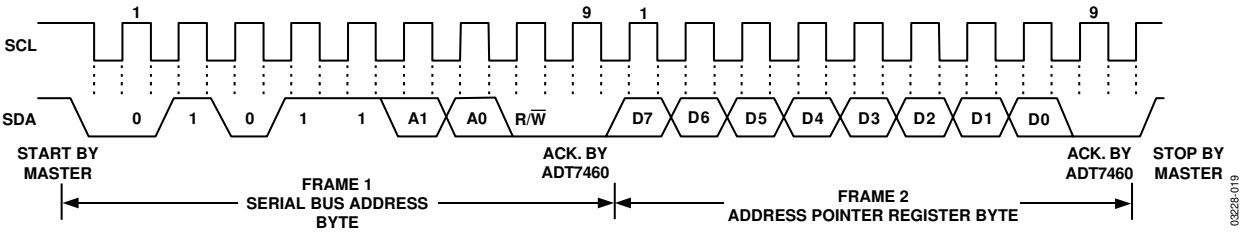

Figure 19. Writing to the Address Pointer Register Only

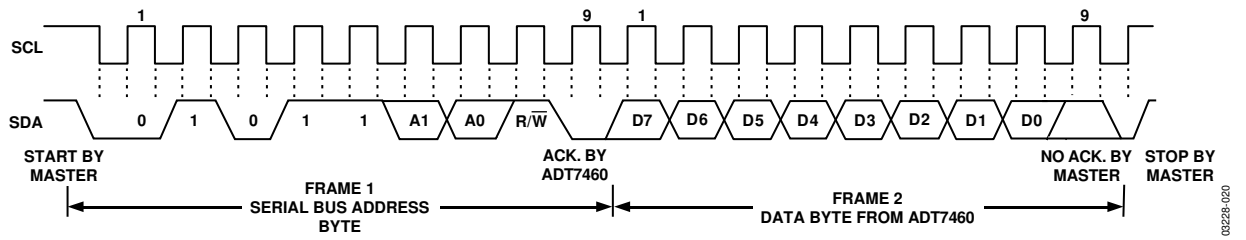

Figure 20. Reading Data from a Previously Selected Register

For the ADT7460, the send byte protocol is used to write to the address pointer register for a subsequent single-byte read from the same address. This is illustrated in Figure 21.

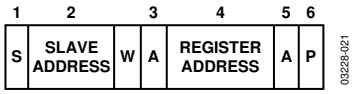

Figure 21. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single-byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

This is illustrated in Figure 22.

Figure 22. Single-Byte Write to a Register

Read Operations

The ADT7460 uses the following SMBus read protocols.

Receive Byte

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

In the ADT7460, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or by write byte operation.

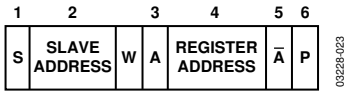

Figure 23. Single-Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as an interrupt output or can be used as an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address, which must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known, and it can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7460 has responded to the alert response address, the master must read the status registers and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7460 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the ADT7460 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 6. Configuration Register 1 (Reg. 0x40)

Bit	Description
<6> TODIS	0: SMBus timeout enabled (default)
<6> TODIS	1: SMBus timeout disabled

VOLTAGE MEASUREMENT INPUT

The ADT7460 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}.

Pin 14 may be configured to measure a 2.5 V supply. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). Setting Bit 7 of Configuration Register 1 (Reg. 0x40) allows a 5 V supply to power the ADT7460 and be measured without overranging the V_{CC} measurement channel. The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of 2.5 V without any external components. To allow the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (768d or 0x300) for the nominal input voltage and so has adequate headroom to deal with overvoltages.

Input Circuitry

The internal structure for the 2.5 V analog input is shown in Figure 24. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives the input immunity to high frequency noise.

Table 7. Voltage Measurement Registers

Register	Description	Default
0x20	2.5 V reading	0x00
0x22	V_{CC} reading	0x00

Associated with the voltage measurement channels are a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 8. 2.5 V Limit Registers

Register	Description	Default
0x44	2.5 V low limit	0x00
0x45	2.5 V high limit	0xFF
0x48	V_{CC} low limit	0x00
0x49	V_{CC} high limit	0xFF

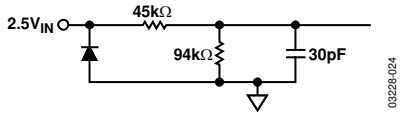

Figure 24. Structure of Analog Inputs

Table 9 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 711 µs and averages 16 conversions to reduce noise; a measurement takes nominally 11.38 ms.

Table 9. 10-Bit A/D Output Code vs. V_{IN}

Input Voltage			A/D Output	
5 V_{IN}	**V_{CC} (3.3 V_{IN})[1]**	**2.5 V_{IN}**	**Decimal**	**Binary (10 Bits)**
<0.0065	<0.0042	<0.0032	0	00000000 00
0.0065–0.0130	0.0042–0.0085	0.0032–0.0065	1	00000000 01
0.0130–0.0195	0.0085–0.0128	0.0065–0.0097	2	00000000 10
0.0195–0.0260	0.0128–0.0171	0.0097–0.0130	3	00000000 11
0.0260–0.0325	0.0171–0.0214	0.0130–0.0162	4	00000001 00
0.0325–0.0390	0.0214–0.0257	0.0162–0.0195	5	00000001 01
0.0390–0.0455	0.0257–0.0300	0.0195–0.0227	6	00000001 10
0.0455–0.0521	0.0300–0.0343	0.0227–0.0260	7	00000001 11
0.0521–0.0586	0.0343–0.0386	0.0260–0.0292	8	00000010 00
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1.6675–1.6740	1.1000–1.1042	0.8325–0.8357	256 (1/4 scale)	01000000 00
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3.3300–3.3415	2.2000–2.2042	1.6650–1.6682	512 (1/2 scale)	10000000 00
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
5.0025–5.0090	3.3000–3.3042	2.4975–2.5007	768 (3/4 scale)	11000000 00
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
6.5983–6.6048	4.3527–4.3570	3.2942–3.2974	1013	11111101 01
6.6048–6.6113	4.3570–4.3613	3.2974–3.3007	1014	11111101 10
6.6113–6.6178	4.3613–4.3656	3.3007–3.3039	1015	11111101 11
6.6178–6.6244	4.3656–4.3699	3.3039–3.3072	1016	11111110 00
6.6244–6.6309	4.3699–4.3742	3.3072–3.3104	1017	11111110 01
6.6309–6.6374	4.3742–4.3785	3.3104–3.3137	1018	11111110 10
6.6374–6.4390	4.3785–4.3828	3.3137–3.3169	1019	11111110 11
6.6439–6.6504	4.3828–4.3871	3.3169v3.3202	1020	11111111 00
6.6504–6.6569	4.3871–4.3914	3.3202–3.3234	1021	11111111 01
6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	1022	11111111 10
>6.6634	>4.3957	>3.3267	1023	11111111 11

[1] The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), the V_{CC} output codes are the same as for the 5 V_{IN} column.

ADDITIONAL ADC FUNCTIONS FOR VOLTAGE MEASUREMENTS

A number of other functions are available on the ADT7460 to offer the systems designer increased flexibility.

Turn-Off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. If the user wants to speed up conversion, setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16 times faster (711 µs), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (Reg. 0x73) removes the attenuation circuitry from the 2.5 V input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7460 into single-channel ADC conversion mode. In this mode, the ADT7460 can be made to read a single voltage channel only. If the internal ADT7460 clock is used, the selected input is read every 711 µs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 Minimum High Byte register (Reg. 0x55).

Table 10. Configuration Register 2 (Reg. 0x73)

Bit	Description
<4>	1: averaging off
<5>	1: bypass input attenuators
<6>	1: single-channel convert mode

Table 11. TACH1 Minimum High Byte (Reg. 0x55)

Bit	Description	
<7:5>	Selects ADC channel for single-channel convert mode	
	Value	Channel Selected
	000	2.5 V
	010	V_{CC}

TEMPERATURE MEASUREMENT SYSTEM

Local Temperature Measurement

The ADT7460 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 0x26). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 12. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside this range are not possible.

Remote Temperature Measurement

The ADT7460 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pins 12 and 13, or Pins 10 and 11.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7460 is to measure the change in V_{BE} when the device is operated at two different currents. This is given by

$$\Delta V_{BE} = KT/q \times In(N)$$

where:

K is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvins.
N is the ratio of the two currents.

Figure 25 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors. It could equally well be a discrete transistor, such as a 2N3904.

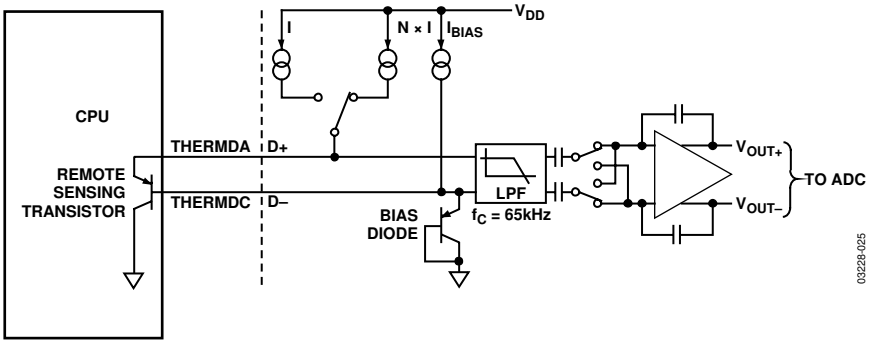

Figure 25. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded, and it should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input, and the base to the D+ input. Figure 26 and Figure 27 show how to connect the ADT7460 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise and to a chopper stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 25.5 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 12. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

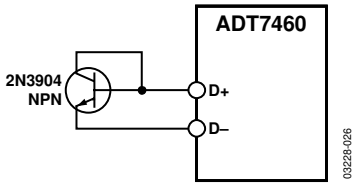

Figure 26. Measuring Temperature by Using an NPN Transistor

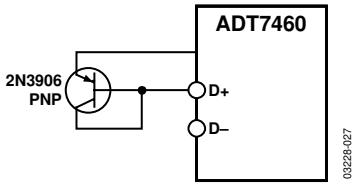

Figure 27. Measuring Temperature by Using a PNP Transistor

Table 12. Temperature Data Format

Temperature	Digital Output (10-Bit)[1]
−128°C	1000 0000 **00**
−125°C	1000 0011 **00**
−100°C	1001 1100 **00**
−75°C	1011 0101 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

[1] Bold denotes 2 LSBs of measurement in the Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

Table 13. Temperature Measurement Registers

Register	Description	Default
0x25	Remote 1 temperature	0x80
0x26	Local temperature	0x80
0x27	Remote 2 temperature	0x80
0x77	Extended Resolution 2	0x00

Table 14. Extended Resolution Temperature Measurement Register Bits (Addr = 0x77)

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 temperature LSBs
<5:4>	LTMP	Local temperature LSBs
<3:2>	TDM1	Remote 1 temperature LSBs

Reading Temperature from the ADT7460

It is important to note that temperature can be read from the ADT7460 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25 C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read, and vice versa.

Nulling Out Temperature Errors

As CPUs run faster, it becomes more difficult to avoid high frequency clocks when routing the D+, D– traces around a system board. Even when recommended layout guidelines are followed, there may still be temperature errors attributed to noise being coupled onto the D+/D– lines. High frequency noise generally has the effect of giving temperature measurements that are too high by a constant amount. The ADT7460 has temperature offset registers at Addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, one can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement. The LSB adds 0.25°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±32°C with a resolution of 0.25°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Table 15. Temperature Offset Registers

Register	Description	Default
0x70	Remote 1 temperature offset	0x00 (0°C)
0x71	Local temperature offset	0x00 (0°C)
0x72	Remote 2 temperature offset	0x00 (0°C)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 16. Temperature Measurement Limit Registers

Register	Description	Default
0x4E	Remote 1 temperature low limit	0x81
0x4F	Remote 1 temperature high limit	0x7F
0x50	Local temperature low limit	0x81
0x51	Local temperature high limit	0x7F
0x52	Remote 2 temperature low limit	0x81
0x53	Remote 2 temperature high limit	0x7F

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Registers 0x6A to 0x6C are the $\overline{\text{THERM}}$ limits. When a temperature exceeds its $\overline{\text{THERM}}$ limit, all fans run at 100% duty cycle. The fans continue running at 100% until the temperature drops below $\overline{\text{THERM}}$ – Hysteresis. (This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2, Register 0x78). The hysteresis value for that $\overline{\text{THERM}}$ limit is the value programmed into Registers 0x6D and 0x6E (hysteresis registers). The default hysteresis value is 4°C.

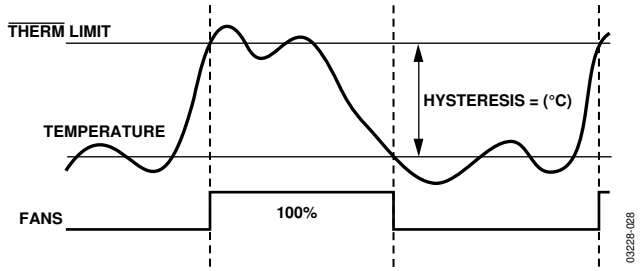

Figure 28. $\overline{\text{THERM}}$ Limit Operation

ADDITIONAL ADC FUNCTIONS FOR TEMPERATURE MEASUREMENT

A number of other functions are available on the ADT7460 to offer the systems designer increased flexibility:

Turn-Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it may be necessary to take a very fast measurement, for example, of CPU temperature. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This takes a reading every 15.5 ms. Each remote temperature measurement takes 4 ms and the local temperature measurement takes 1.4 ms.

Single-Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7460 into single-channel ADC conversion mode. In this mode, the ADT7460 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (Reg. 0x55).

Table 17. Configuration Register 2 (Reg. 0x73)

Bit	Description
<4>	1: Averaging off
<6>	1: single-channel convert mode

Table 18. TACH1 Minimum High Byte (Reg. 0x55)

Bit	Description	
<7:5>	Selects ADC channel for single-channel convert mode	
	Value	Channel Selected
	101	Remote 1 temp
	110	Local temp
	111	Remote 2 temp

LIMITS, STATUS REGISTERS, AND INTERRUPTS

Limit Values

Associated with each measurement channel on the ADT7460 are high and low limits. These can form the basis of system status monitoring: a status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-Bit Limits

The following is a list of 8-bit limits on the ADT7460.

Table 19. Voltage Limit Registers

Register	Description	Default
0x44	2.5 V low limit	0x00
0x45	2.5 V high limit	0xFF
0x48	V_{CC} low limit	0x00
0x49	V_{CC} high limit	0xFF

Table 20. Temperature Limit Registers

Register	Description	Default
0x4E	Remote 1 temperature low limit	0x81
0x4F	Remote 1 temperature high limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ limit	0x64
0x50	Local temperature low limit	0x81
0x51	Local temperature high limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ limit	0x64
0x52	Remote 2 temperature low limit	0x81
0x53	Remote 2 temperature high limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ limit	0x64

Table 21. $\overline{\text{THERM}}$ Timer Limit Register

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ timer limit	0x00

16-Bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Since fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Since fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 22. Fan Limit Registers

Register	Description	Default
0x54	TACH1 minimum low byte	0xFF
0x55	TACH1 minimum high byte	0xFF
0x56	TACH2 minimum low byte	0xFF
0x57	TACH2 minimum high byte	0xFF
0x58	TACH3 minimum low byte	0xFF
0x59	TACH3 minimum high byte	0xFF
0x5A	TACH4 minimum low byte	0xFF
0x5B	TACH4 minimum high byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7460 can be enabled for monitoring. The ADT7460 measures all parameters in round-robin format and sets the appropriate status bit for out-of-limit conditions. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

- High limit: > comparison performed
- Low limit: < or = comparison performed

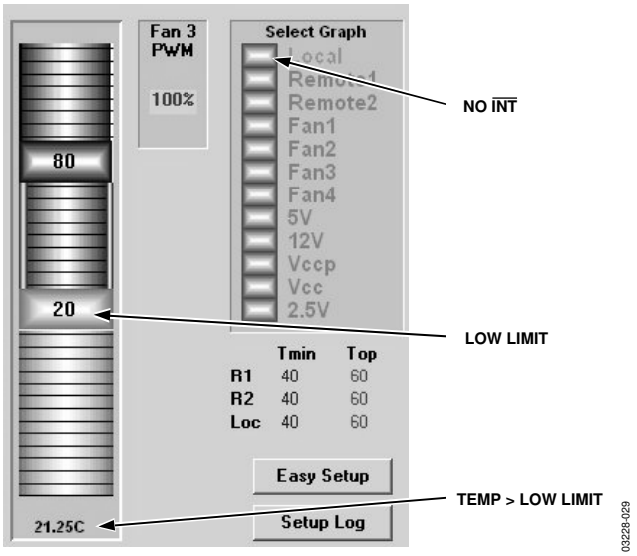

Figure 29. Temperature > Low Limit: No $\overline{\text{INT}}$

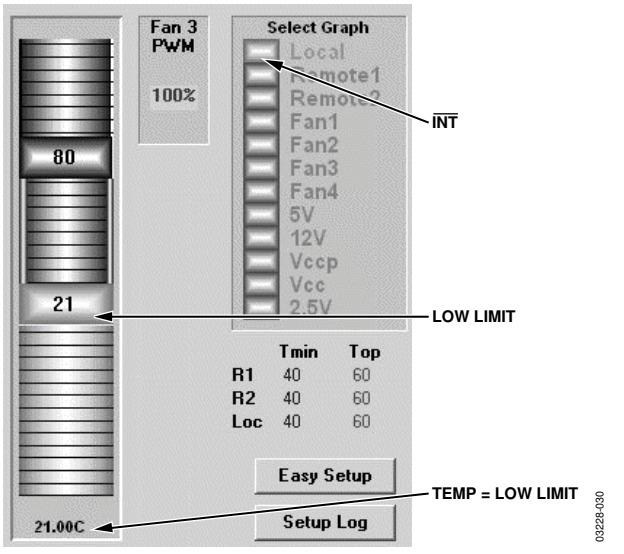

Figure 30. Temperature = Low Limit: $\overline{\text{INT}}$ Occurs

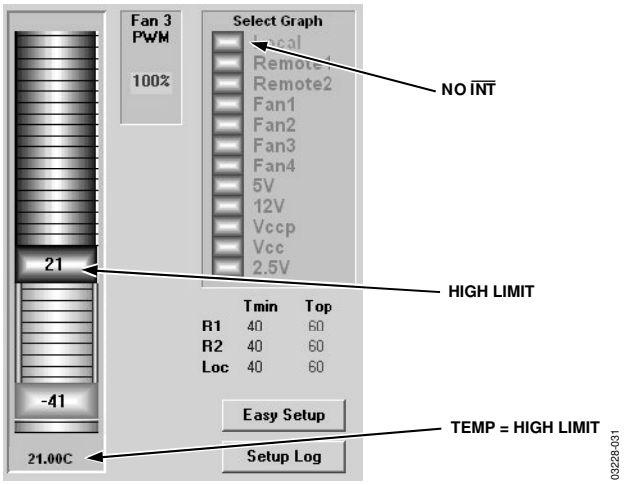

Figure 31. Temperature = High Limit: No $\overline{INT}$

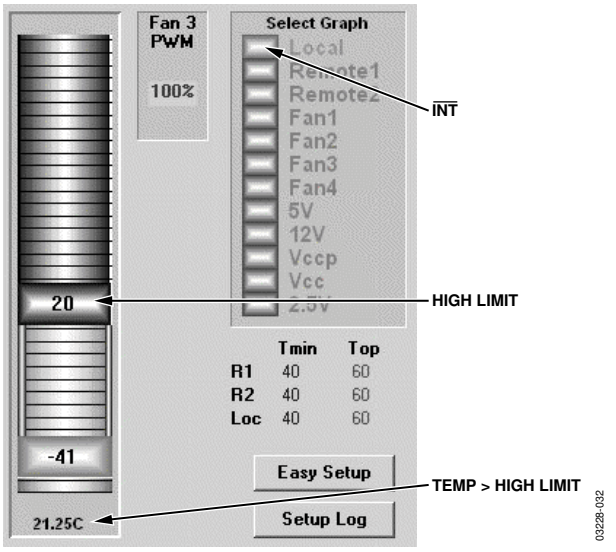

Figure 32. Temperature > High Limit: $\overline{INT}$ Occurs

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally allowed to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, since the most recently measured value of any input can be read out at any time. For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is

- Two supply voltage inputs (2.5 V and V_{CC})
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round-robin conversions and takes 11.38 ms for each voltage measurement, 12 ms for a local temperature reading, and 25.5 ms for each remote temperature reading.

The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally

$$(2 \times 11.38) + 12\ (2 \times 25.5) = 85.76\ \text{ms}$$

The round robin starts again 35 ms later. Therefore, all channels are measured approximately every 120 ms.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

STATUS REGISTERS

The results of limit comparisons are stored in Status Registers 1 and 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out-of-limits, the corresponding status register bit is set to 1.

The state of the various measurement channels may be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Status Register 1 (Reg. 0x41), 1 means that an out-of-limit event has been flagged in Status Register 2. This means that you need only read Status Register 2 when this bit is set. Alternatively, Pin 5 or Pin 14 can be configured as an $\overline{SMBALERT}$ output. This automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are "sticky." Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{SMBALERT}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the interrupt status registers.

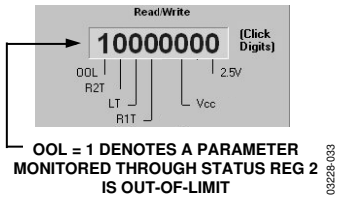

Figure 33. Status Register 1

Table 23. Status Register 1 (Reg. 0x41)

Bit	Mnemonic	Description
7	OOL	1 denotes a bit in Status Register 2 is set and Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 temperature high or low limit has been exceeded.
5	LT	1 indicates that the Local temperature high or low limit has been exceeded.
4	R1T	1 indicates that the Remote 1 temperature high or low limit has been exceeded.
3	-	Unused
2	VCC	1 indicates that the VCC high or low limit has been exceeded.
1	-	Unused
0	2.5 V	1 indicates that the 2.5 V high or low limit has been exceeded.

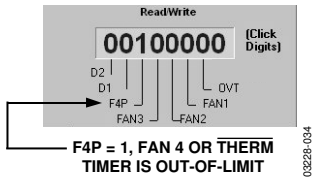

Figure 34. Status Register 2

Table 24. Status Register 2 (Reg. 0x42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2– inputs.
6	D1	1 indicates an open or short on D2+/D2– inputs.
5	F4P	1 indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ timer limit has been exceeded if the $\overline{\text{THERM}}$ timer function is used.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.
0	-	Unused

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7460 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

Figure 35 shows how the $\overline{\text{SMBALERT}}$ output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky since they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.

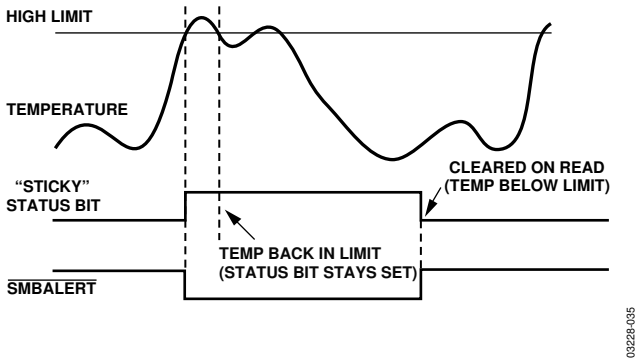

Figure 35. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

HANDLING $\overline{\text{SMBALERT}}$ INTERRUPTS

To prevent the system from being tied up servicing interrupts, it is recommend to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 36.

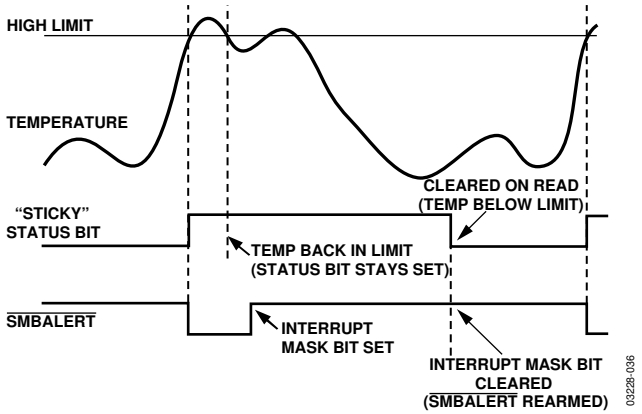

Figure 36. How Masking the Interrupt Source Affects SMBALERT Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent SMBALERT interrupts. Note that masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set as normal.

Table 25. Interrupt Mask Register 1 (Reg. 0x74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature.
5	LT	1 masks SMBALERT for local temperature.
4	R1T	1 masks SMBALERT for Remote 1 temperature.
3	-	Unused
2	VCC	1 masks SMBALERT for the VCC channel.
1	-	Unused
0	2.5 V	1 masks SMBALERT for the 2.5 V channel.

Table 26. Interrupt Mask Register 2 (Reg. 0x75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).
0	-	Unused

Enabling the SMBALERT Interrupt Output

The SMBALERT interrupt function is disabled by default. Pin 5 or Pin 14 can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Table 27. Config Register 4 (Reg. 0x7D)

Pin No.	Bit Setting
14	<0> AL2.5V = 1

Table 28. Config Register 3 (Reg. 0x78)

Pin No.	Bit Setting
5	<0> ALERT = 1

To Assign THERM Functionality to Pin 9

Pin 9 can be configured as the THERM pin on the ADT7460. To configure Pin 9 as the THERM pin, set the THERM ENABLE Bit (Bit 1) in Configuration Register 3 (Address 0x78) = 1.

THERM as an Input

When configured as an input, the THERM pin allows the user to time assertions on the pin. This can be useful for connecting to the PROCHOT output of a CPU to gauge system performance. For more information on timing THERM assertions and generating SMBALERTs based on THERM, see the Generating Interrupts from Events section.

The user can also set up the ADT7460 so when the THERM pin is driven low externally, the fans run at 100%. The fans run at 100% while the THERM pin is pulled low.

This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00 or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling THERM low externally has no effect. See Figure 37 for more information.

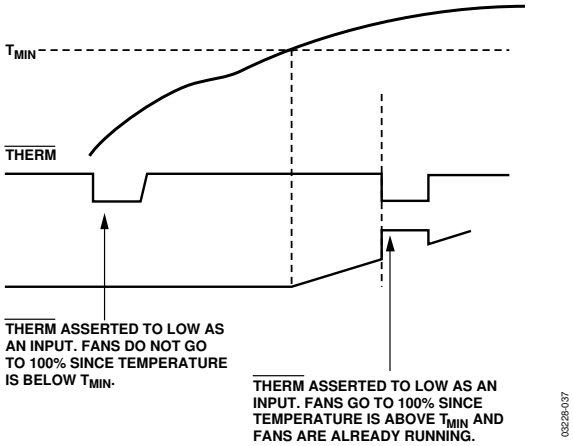

Figure 37. Asserting THERM Low as an Input in Automatic Fan Speed Control Mode

THERM TIMER

The ADT7460 has an internal timer to measure THERM assertion time. For example, the THERM input may be connected to the PROCHOT output of a Pentium 4 CPU and measure system performance. The THERM input may also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7460's THERM input and stopped on the negation of the pin. The timer counts THERM times cumulatively, therefore, the timer resumes counting on the next THERM assertion. The THERM timer continues to accumulate THERM assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit THERM timer register (Reg. 0x79) is designed such that Bit 0 is set to 1 on the first THERM assertion. Once the cumulative THERM assertion time exceeds 45.52 ms, Bit 1 of the THERM timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms.

Figure 38 illustrates how the THERM timer behaves as the THERM input is asserted and negated. Bit 0 is set on the first THERM assertion detected. This bit remains set until the cumulative THERM assertions exceed 45.52 ms. At this time, Bit 1 of the THERM timer is set, and Bit 0 is cleared. Bit 0 now reflects timer readings with a resolution of 22.76 ms.

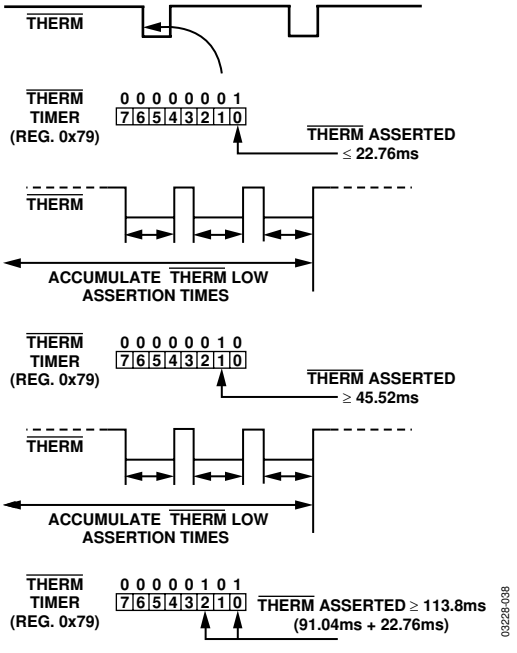

Figure 38. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

After a THERM timer read (Reg. 0x79)

- The contents of the timer is cleared on read.
- The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming the THERM limit has been exceeded).

If the THERM timer is read during a THERM assertion

- The contents of the timer are cleared.
- Bit 0 of the THERM timer is set to 1 (since a THERM assertion is occurring).
- The THERM timer increments from 0.
- If the THERM limit (Reg. 0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM Events

The ADT7460 can generate SMBALERTs when a programmable THERM limit has been exceeded. This allows the systems designer to ignore brief, infrequent THERM assertions while capturing longer THERM events. Register 0x7A is the THERM limit register. This 8-bit register allows a limit from 0 seconds (first THERM assertion) to 5.825 seconds to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM limit register. If the THERM timer value exceeds the THERM limit value, the F4P bit (Bit 5) of Status Register 2 is set and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 is still set if the THERM limit is exceeded.

Figure 39 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing 0x00 to the THERM limit register (Reg. 0x7A) causes SMBALERT to be generated on the first THERM assertion. A THERM limit of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.

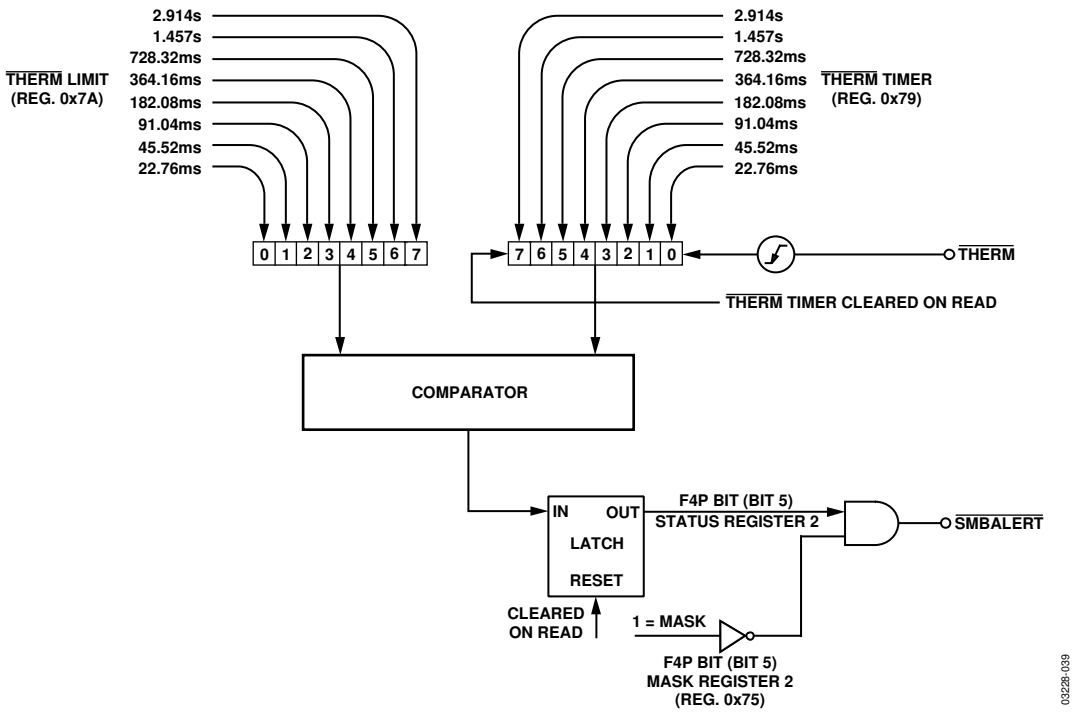

Figure 39. Functional Diagram of ADT7460's $\overline{THERM}$ Monitoring Circuitry