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ADT7462

Flexible Temperature, Voltage Monitor, and System Fan Controller

The ADT7462 is a flexible systems monitor IC, suitable for use in a wide variety of applications. It can monitor temperature in up to three remote locations, as well as its ambient temperature.

There are up to four PWM outputs. These can be used to control the speed of a cooling fan by varying the % duty cycle of the PWM drive signal applied to the fan. The ADT7462 supports high frequency PWM for 4-wire fans and low frequency PWM for 2-wire and 3-wire fans. Up to eight TACH inputs can be used to measure the speed of 3-wire and 4-wire fans. There are up to 13 voltage monitoring inputs, ranging from 12 V to 0.9 V.

The ADT7462 is fully compatible with SMBus 1.1 and SMBus 1.0. The ADT7462 also includes a $\overline{\text{THERM}}$ I/O and a $\overline{\text{RESET}}$ I/O.

The ADT7462 is available in a 32-lead LFCSP_VQ. Many of the pins are multi-functional. Five easy configuration options can be set up using the easy configuration register. Users choose the configuration closest to their requirements; individual pins can be reconfigured after the easy configuration option has been chosen.

Features

- One Local and Up to Three Remote Temperature Channels Series Resistance Cancellation On Remote Channels
- Thermal Protection Using $\overline{\text{THERM}}$ Pins
- Up to Four PWM Fan Drive Outputs Supports Both High and Low Frequency PWM Drives
- Up to Eight TACH Inputs Measures the Speed of 3-wire and 4-wire Fans
- Automatic Fan Speed Control Loop Includes Dynamic T_{MIN} Control
- Monitors Up to 13 V Inputs
- Monitors Up to 7 VID Inputs; Includes On-The-Fly (OTF) VID Support
- Bidirectional Reset
- Chassis Intrusion Detect
- SMBus 1.1 and SMBus 1.0 Compatible
- 3.3 V and 5.0 V Operation
- Extended Operating Range from −40°C to +125°C
- Space-saving 32-lead Chip Scale Package
- This is a Pb-Free Device*

Applications

- Servers and Personal Computers
- Telecommunications Equipment
- Test Equipment and Measurement Instruments

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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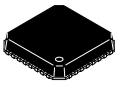
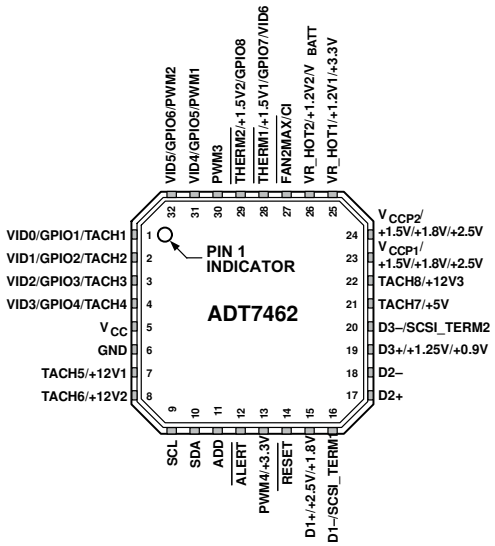


LFCSP−32
CASE 932

PIN ASSIGNMENT



MARKING DIAGRAM

ADT7462ACPZ	= Specific Device Code
#	= Pb-Free Package
YYWW	= Date Code
AL	= Assembly Lot
CC	= Country Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 81 of this data sheet.

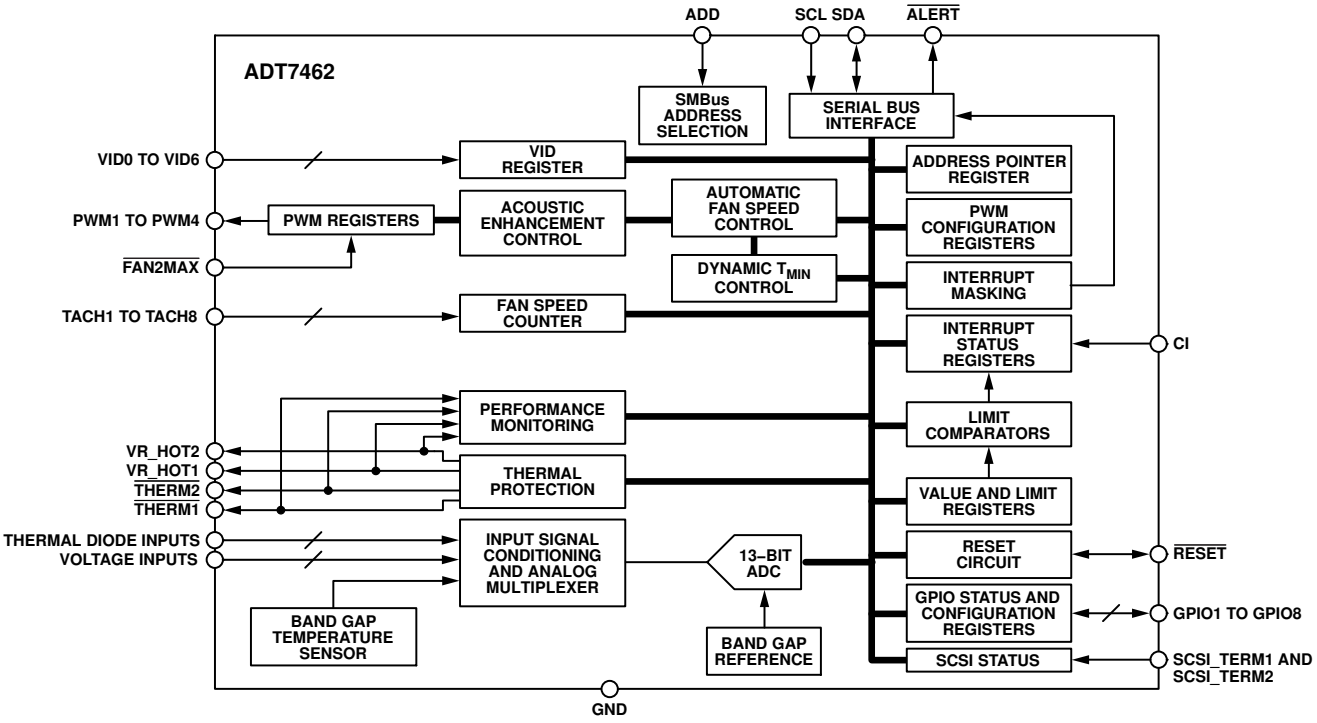


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Supply Voltage	6.5	V
Voltage on +12V Pin	20	V
Voltage on V_{BATT} Pin	4.0	V
Voltage on Any Other Input or Output Pin	–0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Operating Temperature Range	–40 to +125	°C
Storage Temperature Range	–65 to +150	°C
Lead Temperature, Soldering Lead Temperature (Soldering, 10 sec) IR Reflow Peak Temperature	 300 260	°C
ESD Rating	1500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
32-lead LFCSP_VQ	32.5	32.71	°C/W

1. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description	POR Default
1	VID0/GPIO1/TACH1	VID0: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO1: Open-Drain I/O. General-purpose input/output. TACH1: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.	TACH1
2	VID1/GPIO2/TACH2	VID1: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO2: Open-Drain I/O. General-purpose input/output. TACH2: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.	TACH2
3	VID2/GPIO3/TACH3	VID2: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO3: Open-Drain I/O. General-purpose input/output. TACH3: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.	TACH3
4	VID3/GPIO4/TACH4	VID3: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO4: Open-Drain I/O. General-purpose input/output. TACH4: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4.	TACH4
5	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. The ADT7462 can also be powered from a 5.0 V supply.	V_{CC}
6	GND	Ground Pin.	GND
7	TACH5/+12V1	TACH5: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 5. +12V1: Analog Input. Monitors 12 V Power Supply 1. Attenuators switched on by default.	TACH5
8	TACH6/+12V2	TACH6: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 6. +12V2: Analog Input. Monitors 12 V Power Supply 2. Attenuators switched on by default.	TACH6
9	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.	SCL
10	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pullup.	SDA
11	ADD	The state of this pin on powerup determines the SMBus device address.	ADD
12	$\overline{\text{ALERT}}$	Active Low Open-Drain Digital Output. Requires 10 kΩ typical pullup. The $\overline{\text{ALERT}}$ pin is used to signal out-of-limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus $\overline{\text{ALERT}}$.	$\overline{\text{ALERT}}$
13	PWM4/+3.3V	PWM4: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 4. +3.3V: Analog Input. Monitors 3.3 V power supply.	PWM4
14	$\overline{\text{RESET}}$	Active Low Open-Drain Digital I/O. Power-on reset, 5 mA driver (weak 100 kΩ pullup), active low output (100 kΩ pullup) with a 180 ms typical pulse width. $\overline{\text{RESET}}$ is asserted whenever V_{CC} is below the reset threshold. It remains asserted for approximately 180 ms after V_{CC} rises above the reset threshold. Pin 14 also functions as an active low $\overline{\text{RESET}}$ input and resets all unlocked registers to their default values.	$\overline{\text{RESET}}$
15	D1+/+2.5V/+1.8V	D1+: Anode Connection to Thermal Diode 1. +2.5V: Monitors 2.5 V analog input. +1.8V: Monitors 1.8 V analog input.	D1+
16	D1−/SCSI_TERM1	D1−: Cathode Connection to Thermal Diode 1. SCSI_TERM1: Digital Input, SCSI Termination 1.	D1−
17	D2+	Anode Connection to Thermal Diode 2.	D2+
18	D2−	Cathode Connection to Thermal Diode 2.	D2−
19	D3+/+1.25V/+0.9V	D3+: Anode Connection to Thermal Diode 3. +1.25V: Monitors 1.25 V analog input. +0.9V: Monitors 0.9 V analog input.	D3+
20	D3−/SCSI_TERM2	D3−: Cathode connection to Thermal Diode 3. SCSI_TERM2: Digital Input, SCSI Termination 2.	D3−
21	TACH7/+5V	TACH7: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 7. +5V: Analog Input. Monitors 5.0 V power supply.	TACH7

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description	POR Default
22	TACH8/+12V3	TACH8: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 8. +12V3: Analog Input. Monitors 12 V Power Supply 3.	TACH8
23	V_{CCP1}/+1.5V/+1.8V/+2.5V	V_{CCP1}: Monitors 1.2 V analog input. +1.5V: Monitors 1.5 V analog input. +1.8V: Monitors 1.8 V analog input. +2.5V: Monitors 2.5 V analog input.	+1.8V
24	V_{CCP2}/+1.5V/+1.8V/+2.5V	V_{CCP2}: Monitors 1.2 V analog input. +1.5V: Monitors 1.5 V analog input. +1.8V: Monitors 1.8 V analog input. +2.5V: Monitors 2.5 V analog input.	+2.5V
25	VR_HOT1/+1.2V1/+3.3V	VR_HOT1: Digital Input Indicating Overtemperature Event on Voltage Regulator. +1.2V1: 0 V to 1.2 V Analog Input. For example, can be used to monitor G_{BIT}. +3.3V: Analog Input. Monitors 3.3 V power supply.	+3.3V
26	VR_HOT2/+1.2V2/V_{BATT}	VR_HOT2: Digital Input Indicating Overtemperature Event on Voltage Regulator. +1.2V2: 0 V to 1.2 V Analog Input. For example, can be used to monitor FSB_V_{TT}. V_{BATT}: Analog Input. Monitors battery voltage, nominally 3.0 V.	V_{BATT}
27	$\overline{\text{FAN2MAX}}$/CI	$\overline{\text{FAN2MAX}}$: Sets fan to maximum speed when a fan fault condition occurs. Bidirectional open drain, active low I/O. CI: An active high input that captures a chassis intrusion event in Bit 7 of the digital status register. This bit remains set until cleared, as long as battery voltage is applied to the V_{BATT} input, even when the ADT7462 is powered off.	CI
28	$\overline{\text{THERM1}}$/+1.5V1/GPIO7/VID6	$\overline{\text{THERM1}}$: Can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the Intel® Pentium® 4 processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. +1.5V1: 0 V to 1.5 V Analog Input. Can be used to monitor ICH. GPIO7: Open-Drain I/O. General-purpose input/output. VID6: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97).	$\overline{\text{THERM1}}$
29	$\overline{\text{THERM2}}$/+1.5V2/GPIO8	$\overline{\text{THERM2}}$: Can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the Intel® Pentium® 4 processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. +1.5V2: 0 V to 1.5 V Analog Input. Can be used to monitor 3GIO. GPIO8: Open-Drain I/O. General-purpose input/output.	$\overline{\text{THERM2}}$
30	PWM3	Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 3.	PWM3
31	VID4/GPIO5/PWM1	VID4: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO5: Open-Drain I/O. General-purpose input/output. PWM1: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 1.	PWM1
32	VID5/GPIO6/PWM2	VID5: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO6: Open-Drain I/O. General-purpose input/output. PWM2: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 2.	PWM2

Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments		Min	Typ	Max	Unit
Power Supply						
Supply Voltage			3.0	3.3	5.5	V
Supply Current, I_{CC}	ADC Active, Interface Inactive (Note 2)		–	1.5	4.0	mA
Temperature-to-Digital Converter	**T_A Conditions**	**V_{CC} Conditions**				
Internal Sensor, T_A, Accuracy	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +100°C	3 V ≤ V_{CC} ≤ 3.6 V 3 V ≤ V_{CC} ≤ 3.6 V 4.5 V ≤ V_{CC} ≤ 5.5 V 4.5 V ≤ V_{CC} ≤ 5.5 V	– – – –	±0.5 – – –	±2.25 ±3.25 ±3.0 ±4.0	°C
Resolution			–	–	0.25	°C
Remote Sensor, T_D, Accuracy (–40°C ≤ T_D ≤ +125°C)	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +100°C	3 V ≤ V_{CC} ≤ 3.6 V 3 V ≤ V_{CC} ≤ 3.6 V 4.5 V ≤ V_{CC} ≤ 5.5 V 4.5 V ≤ V_{CC} ≤ 5.5 V	– – – –	±0.5 – – –	±2.25 ±3.25 ±2.75 ±3.5	°C
Resolution			–	–	0.25	°C
Remote Sensor Source Current (Note 3)	High Level Mid Level Low Level		– – –	85 34 5.0	– – –	μA
Series Resistance Cancellation (Note 3)	The ADT7462 Cancels 2 kΩ in Series with the Remote Thermal Diode		–	2.0	–	kΩ
ANALOG−TO−DIGITAL CONVERTER						
Total Unadjusted Error, TUE (Note 4 and 5)			–	–	±3.5	%
Differential Non-linearity, DNL	8 Bits		–	–	±1.0	LSB
Conversion Time (Voltage Input) (Note 3)			–	8.53	9.86	ms
Conversion Time (Local Temperature) (Note 3)			–	9.01	10.38	ms
Conversion Time (Remote Temperature) (Note 3)			–	38.36	42.09	ms
INPUT RESISTANCE						
Pin 7, Pin 8, Pin 13, Pin 21, Pin 22, Pin 25, Pin 28, Pin 29	Attenuators Enabled		–	140	–	kΩ
Pin 15, Pin 19	Attenuators Enabled		–	225	–	kΩ
Pin 23, Pin 24	Attenuators Enabled		–	66	–	kΩ
Pin 26, V_{BATT} and +1.2V2 (When Measured)	Attenuators Cannot Be Disabled		100	120	140	kΩ
V_{BATT} Current Drain (When Measured)	CR2032 Battery Life > 10 Years		–	80	100	nA
V_{BATT} Current Drain (When Not Measured)	CR2032 Battery Life > 10 Years		–	16	–	nA
FAN RPM TO DIGITAL CONVERTER						
Accuracy			–	–	±8.0	%
Internal Clock Frequency			82.8	90	97.2	kHz
OPEN-DRAIN OUTPUTS (PWM, GPIO)						
High Level Output Leakage Current, I_{OH}	V_{OUT} = V_{CC}		–	0.1	±1.0	μA
Output Low Voltage, V_{OL}	I_{OUT} = –3 mA, V_{CC} = +3.3 V		–	–	0.4	V
DIGITAL OUTPUT ($\overline{\text{RESET}}$,$\overline{\text{ALERT}}$, $\overline{\text{THERM}}$)						
Output Low Voltage, V_{OL}	I_{OUT} = –3 mA, V_{CC} = +3.3 V		–	–	0.4	V
$\overline{\text{RESET}}$ Pulse Width (Note 3)			140	180	–	ms
$\overline{\text{RESET}}$ Threshold	Falling Voltage		3.0	3.05	3.1	V
$\overline{\text{RESET}}$ Hysteresis (Note 3)			–	70	–	mV

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPEN-DRAIN SERIAL BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = –3 mA, V_{CC} = +3.3 V	–	–	0.4	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	±1.0	μA
SERIAL BUS DIGITAL INPUTS (SDA AND SCL)					
Input High Voltage, V_{IH}		2.1	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
DIGITAL INPUT LOGIC LEVELS (VID0 to VID6) AND $\overline{\text{THERM}}$, TACH, GPIO, VR_HOT, SCSI_TERM)					
Input High Voltage, V_{IH}	Bit 3 and Bit 4 of Configuration Register 3 = 0	1.7	–	–	V
Input Low Voltage, V_{IL}	Bit 3 and Bit 4 of Configuration Register 3 = 0	–	–	0.8	V
Input High Voltage, V_{IH} (VID0 to VID6)	Bit 3 of Configuration Register 3 = 1	0.65	–	–	V
Input High Voltage, V_{IH} ($\overline{\text{THERM}}$)	Bit 4 of Configuration Register 3 = 1	2/3 V_{CCP1}	–	–	V
Input Low Voltage, V_{IL}	Bit 3 and Bit 4 of Configuration Register 3 = 1	–	–	0.4	V
Hysteresis		–	500	–	mV
DIGITAL INPUT CURRENTS					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	–1.0	–	–	μA
Input Low Current, I_{IL}	V_{IN} = 0	–	–	+1.0	μA
Input Capacitance (Note 3)		–	5.0	–	pF
SERIAL BUS TIMING (Note 3)					
Clock Frequency	See Figure 2	–	–	400	kHz
Glitch Immunity, t_{SW}	See Figure 2	–	50	–	ns
Bus Free Time	See Figure 2	1.3	–	–	μs
Start Setup Time, $t_{SU;STA}$	See Figure 2	0.6	–	–	μs
Start Hold Time, $t_{HD;STA}$	See Figure 2	0.6	–	–	μs
SCL Low Time, t_{LOW}	See Figure 2	1.3	–	–	μs
SCL High Time, t_{HIGH}	See Figure 2	0.6	–	–	μs
SCL, SDA Rise Time, t_R	See Figure 2	–	–	1000	ns
SCL, SDA Fall Time, t_F	See Figure 2	–	–	300	ns
Data Setup Time, $t_{SU;DAT}$	See Figure 2	100	–	–	ns
Detect Clock Low Timeout	Can Be Optionally Enabled	–	25	–	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typical values are at T_A = 25°C and represent the most likely parametric norm. Logic inputs accept input high voltages up to 5.0 V, even when the device is operating at supply voltages below 5.0 V. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.0 V for a rising edge.
2. Unused digital inputs connected to GND.
3. Guaranteed by design, not production tested.
4. Note that this specification does not apply if Pin 26 (V_{BATT}, +1.2V) is being measured in single-channel mode. See Figure 16 in the Typical Performance Characteristics section for V_{BATT} accuracy.
5. For Pin 23 and Pin 24 configured as +1.8V or +2.5V only, restricted conditions of $V_{CC} \geq 3.3$ V and +25°C ≤ T_A ≤ +125°C apply.

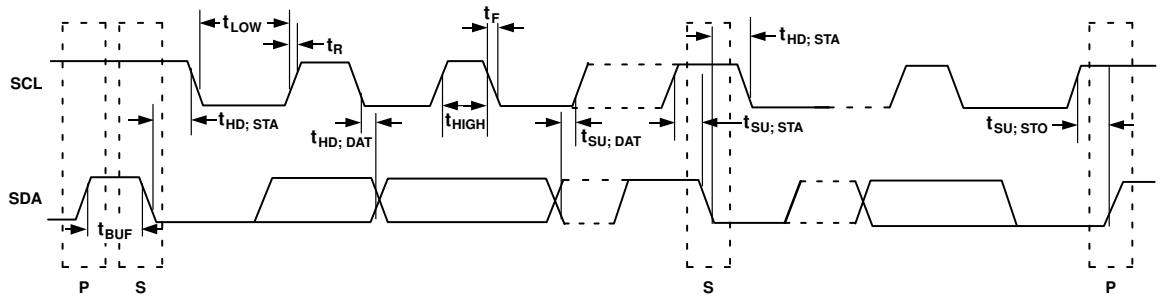


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

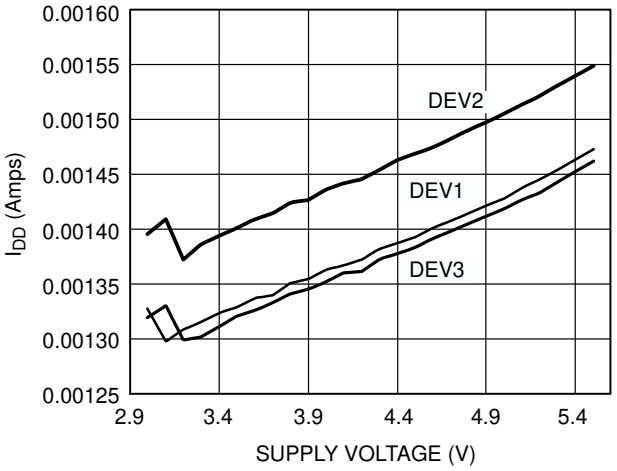


Figure 3. Supply Current vs. Supply Voltage

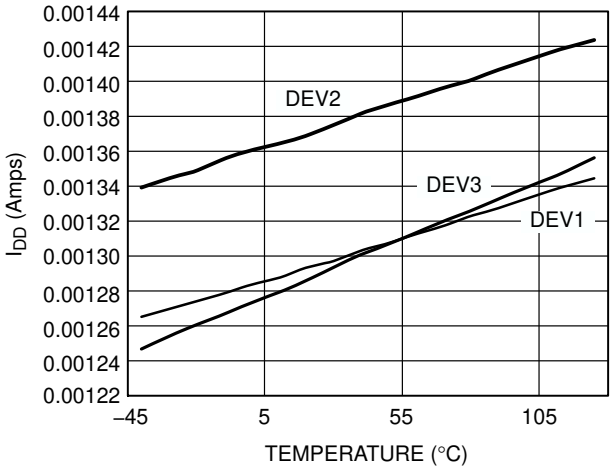


Figure 4. Supply Current vs. Temperature

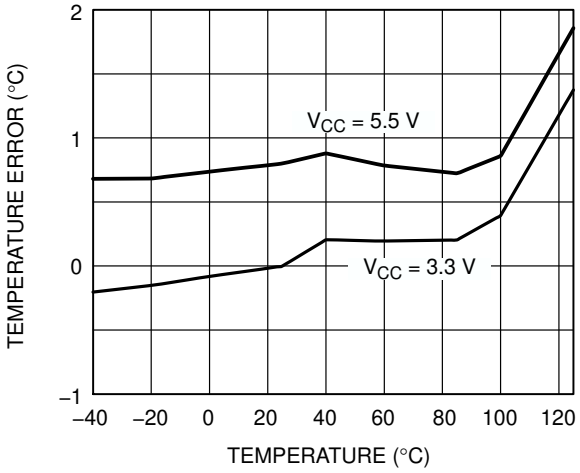


Figure 5. Local Sensor Temperature Error

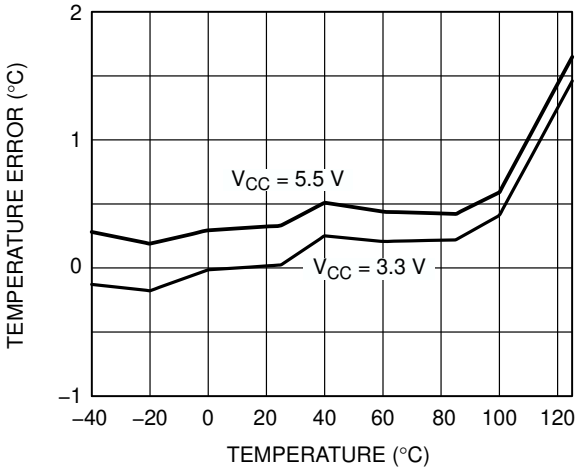


Figure 6. Remote Sensor Temperature Error

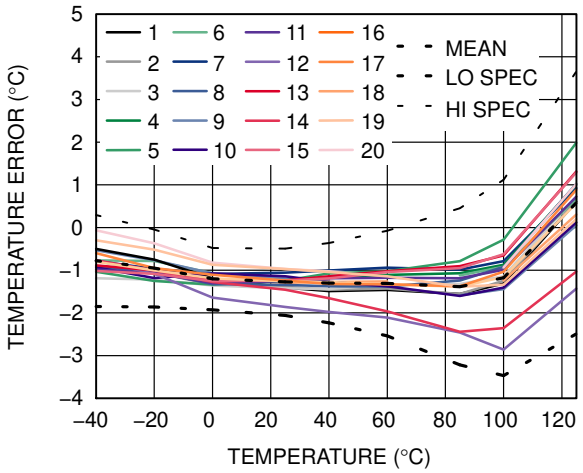


Figure 7. Temperature Error Measuring Intel Pentium® 4 Processor

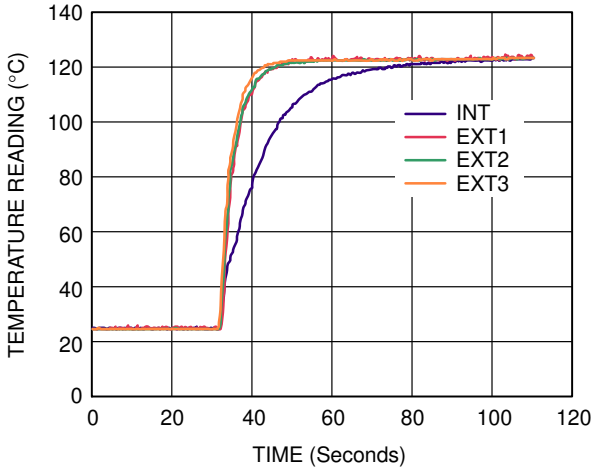


Figure 8. ADT7462 Response to Thermal Shock

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

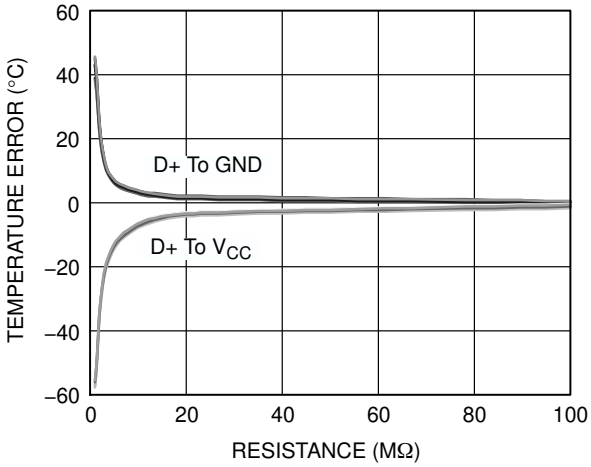


Figure 9. Remote Temperature Error vs. Resistance (SRC)

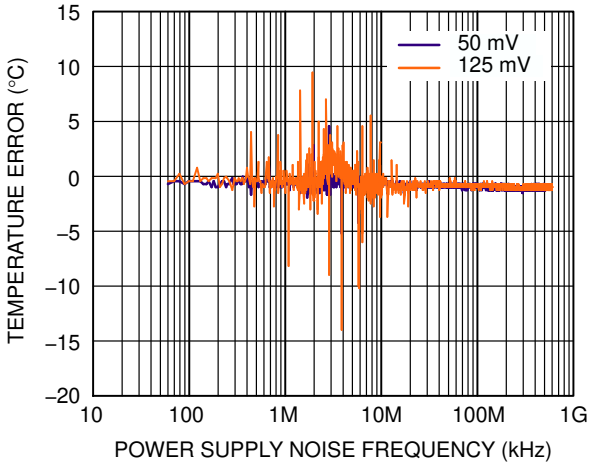


Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

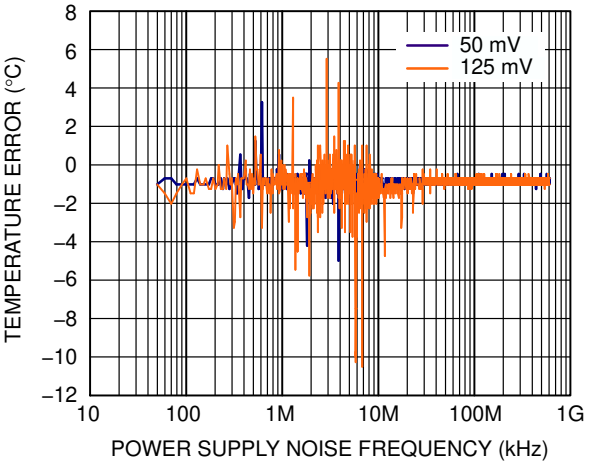


Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

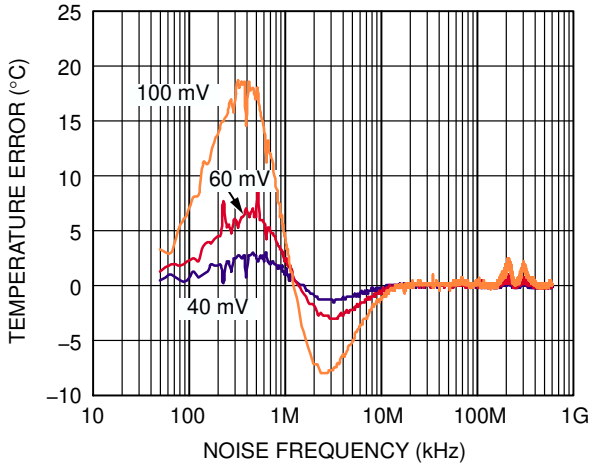


Figure 12. Remote Temperature Error vs. Common-Mode Noise Frequency

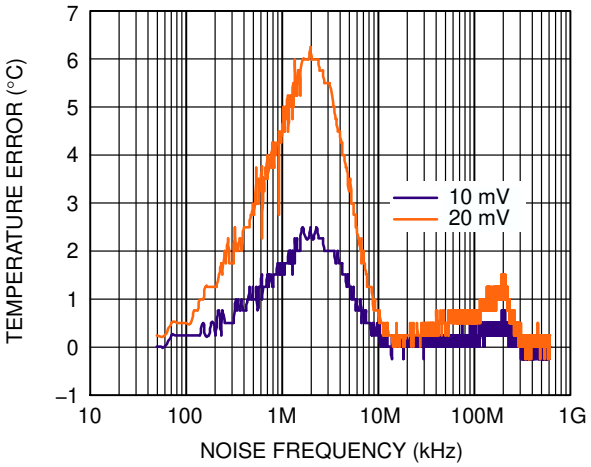


Figure 13. Remote Temperature Error vs. Differential-Mode Noise Frequency

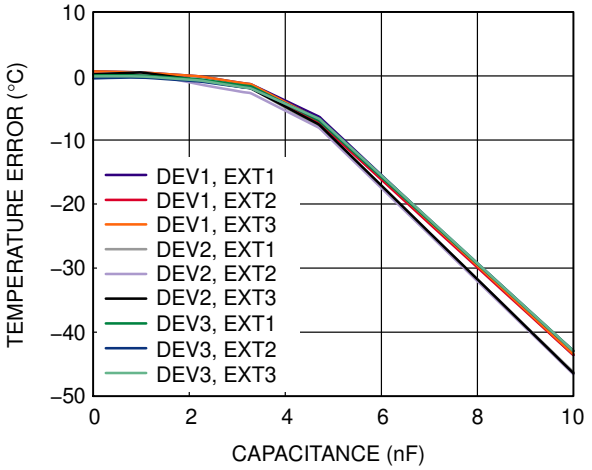


Figure 14. Remote Temperature Error vs. Capacitance Between D+ and D–

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

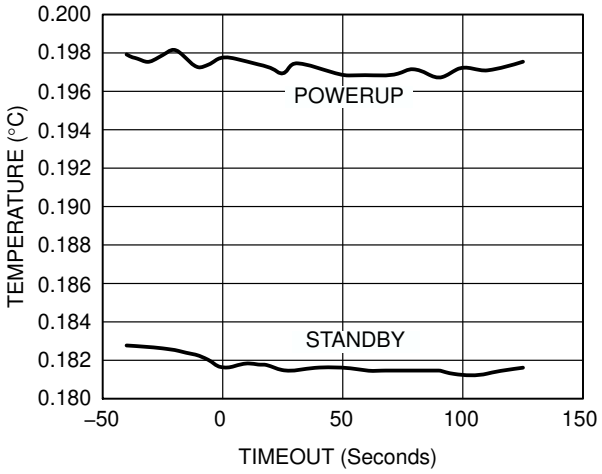


Figure 15. Local Temperature vs. Power-On Reset Timeout

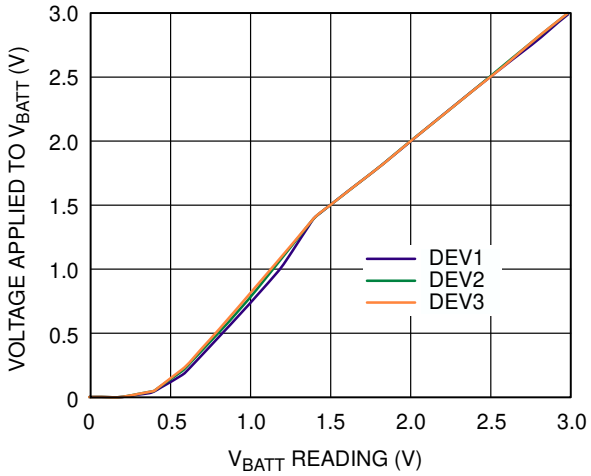


Figure 16. Applied Voltage vs. V_{BATT} Reading

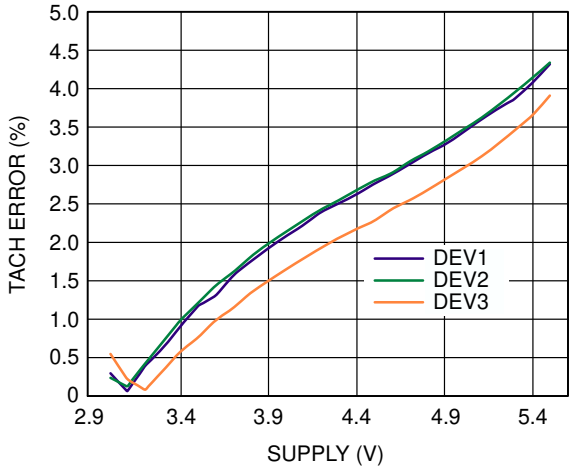


Figure 17. TACH Accuracy vs. Supply Voltage

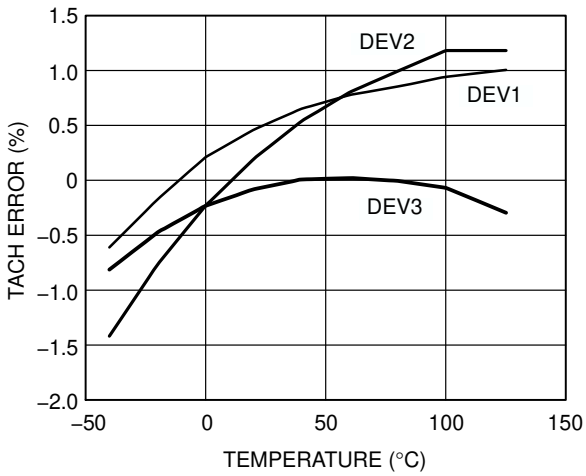


Figure 18. TACH Accuracy vs. Temperature

Function Description: Easy Configuration Options

There are a number of multifunctional pins on the ADT7462 that need to be configured on powerup to suit the desired application. Note that due to the large number of pins that need to be configured, it could take several SMBus transactions to achieve the required configuration. For this reason, the ADT7462 has five easy configuration options. The user sets a bit in the easy configuration option register (0x14) to set up the required configuration (see Table 5).

Table 5. EASY CONFIGURATION REGISTER SETTINGS

Easy Configuration Option	Register 0x14 Setting
Option 1	Bit 0 = 1
Option 2	Bit 1 = 1
Option 3	Bit 2 = 1
Option 4	Bit 3 = 1
Option 5	Bit 4 = 1

Once the most convenient easy configuration option has been set, the user can configure any of the pins individually. The setup complete bit (Bit 5 of Register 0x01) must then be set to 1 to indicate that the ADT7462 is configured correctly, and then monitoring of the selected channels begins.

The following is a detailed description of the five easy configuration options that are available.

Configuration Option 1

Configuration Option 1 is the default configuration. It is also the most suitable for thermal monitoring, voltage monitoring, and fan control for single and dual processor systems. Features of Configuration Option 1 include the following:

- One Local and Three Remote Temperature Channels
- Four PWM Drives and Eight TACH Inputs
- Two $\overline{\text{THERM}}$ I/Os
- Voltage Monitoring
- +3.3V
- +2.5V
- +1.8V
- V_{BATT}
- $\overline{\text{RESET}}$ I/O
- CI (Chassis Intrusion) or $\overline{\text{FAN2MAX}}$

Figure 19 shows the pin configuration when Configuration Option 1 is chosen.

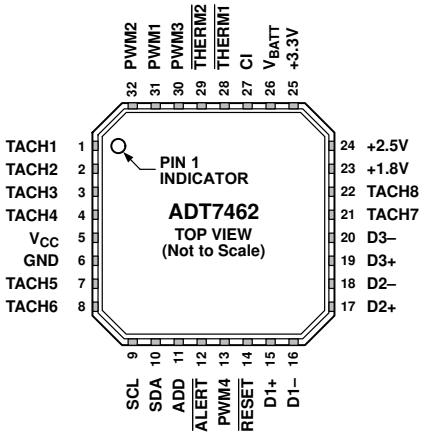


Figure 19. Configuration Option 1

Table 6. CONFIGURATION OPTION 1

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1–	Pin Configuration Reg 1	Bit 6 = 1
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3–	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	+1.8V	Pin Configuration Reg 2	Bits [1:0] = 10
24	+2.5V	Pin Configuration Reg 3	Bits [7:6] = 01
25	+3.3V	Pin Configuration Reg 3	Bits [5:4] = 00
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	CI	Pin Configuration Reg 3	Bit 1 = 1
28†	$\overline{\text{THERM1}}$	Pin Configuration Reg 4	Bits [7:6] = 1×
29	$\overline{\text{THERM2}}$	Pin Configuration Reg 4	Bits [5:4] = 1×
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 2

Configuration Option 2 is used for thermal monitoring and fan control for Processor 1 and Processor 2 in a dual processor system. It can also monitor one set of VIDs, if required. Features of Configuration Option 2 include the following:

- One Local and Three Remote Thermal Channels
- Up to Four PWM Drives and Up to Eight TACH Inputs (VID Pins and TACHs/PWMs are Muxed Together)
- Two $\overline{\text{THERM}}$ I/Os
- Two VRD Inputs
- $\overline{\text{RESET}}$ I/O
- Two V_{CCP} Voltage Monitoring Channels

Figure 20 shows the pin configuration when Configuration Option 2 is chosen.

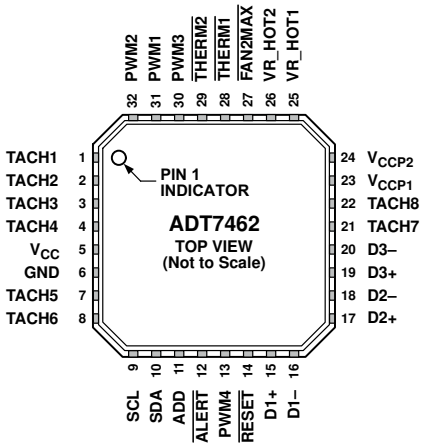


Figure 20. Configuration Option 2

Table 7. CONFIGURATION OPTION 2

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1–	Pin Configuration Reg 1	Bit 6 = 1
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3–	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	VR_HOT1	Pin Configuration Reg 3	Bits [5:4] = 1×
26	VR_HOT2	Pin Configuration Reg 3	Bits [3:2] = 1×
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28†	$\overline{\text{THERM1}}$	Pin Configuration Reg 4	Bits [7:6] = 1×
29	$\overline{\text{THERM2}}$	Pin Configuration Reg 4	Bits [5:4] = 1×
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 3

Configuration Option 3 is used to monitor all the voltages in the system for Processor 1 and Processor 2. Additional pins can be configured for fan control, VIDs, or GPIOs, as required. Features of Configuration Option 3 include the following:

- Up to 13 Different Voltages Monitored
- Three +12V
- +5V
- +3.3V
- +2.5V
- +1.8V
- Two +1.5V
- Two +1.2V (V_{CCP1}, V_{CCP2})
- 0.9V
- V_{BATT}
- One Local and One Remote Temperature Channels
- Up to Three PWM Drives and Up to Four TACH Inputs
- $\overline{\text{RESET}}$ I/O

Figure 21 shows the pin configuration when Configuration Option 3 is chosen.

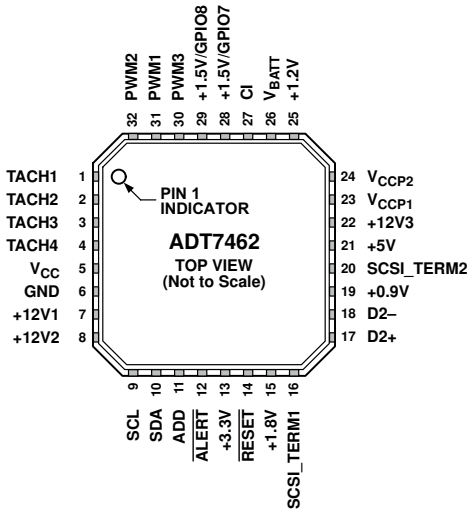


Figure 21. Configuration Option 3

Table 8. CONFIGURATION OPTION 3

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	+12V1	Pin Configuration Reg 1	Bit 0 = 0
8	+12V2	Pin Configuration Reg 2	Bit 7 = 0
13	+3.3V	Pin Configuration Reg 2	Bit 6 = 0
15	+1.8V	Pin Configuration Reg 1	Bit 6 = 0
16	SCSI_ TERM1	Pin Configuration Reg 1	Bit 6 = 0
19	+0.9V	Pin Configuration Reg 1	Bit 5 = 0
20	SCSI_ TERM2	Pin Configuration Reg 1	Bit 5 = 0
21	+5V	Pin Configuration Reg 2	Bit 3 = 0
22	+12V3	Pin Configuration Reg 2	Bit 2 = 0
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	+1.2V	Pin Configuration Reg 3	Bits [5:4] = 01
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	CI	Pin Configuration Reg 3	Bit 1 = 1
28†	+1.5V/ GPIO7	Pin Configuration Reg 4	Bits [7:6] = 01
29	+1.5V/ GPIO8	Pin Configuration Reg 4	Bits [5:4] = 01
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 4

Configuration Option 4 is used to monitor temperature, voltages, and fans for Processor 1 in a dual processor system. Features of Configuration Option 4 include the following:

- One Local and Two Remote Temperature Channels
- Up to Four PWM Drives and Six TACH Inputs
- Up to Eight Voltages Monitored
- +12V
- +5V
- +3.3V
- Two +1.5V
- +1.2V (V_{CCP1})
- +0.984V (Mem_V_{TT})
- V_{BATT}
- $\overline{\text{THERM}}$ I/O
- VRD Input
- $\overline{\text{RESET}}$ I/O

Figure 22 shows the pin configuration when Configuration Option 4 is chosen.

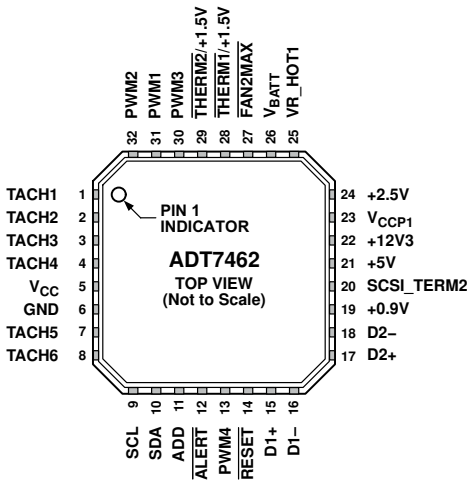


Figure 22. Configuration Option 4

Table 9. CONFIGURATION OPTION 4

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1–	Pin Configuration Reg 1	Bit 6 = 1
19	+0.9V	Pin Configuration Reg 1	Bit 5 = 0
20	SCSI_ TERM2	Pin Configuration Reg 1	Bit 5 = 0
21	+5V	Pin Configuration Reg 2	Bit 3 = 0
22	+12V3	Pin Configuration Reg 2	Bit 2 = 0
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	+2.5V	Pin Configuration Reg 3	Bits [7:6] = 01
25	VR_HOT1	Pin Configuration Reg 3	Bits [5:4] = 1×
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28 †*	$\overline{\text{THERM1}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
29*	$\overline{\text{THERM2}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

*It is not possible to configure +1.5V monitoring on Pin 29 and $\overline{\text{THERM1}}$ on Pin 28. Pin 28 must both be configured as either +1.5V monitoring or as $\overline{\text{THERM}}$ I/O (see Table 51).

Configuration Option 5

Configuration Option 5 is used to monitor temperature, voltages, and fans for Processor 2 in a dual processor system. Features of Configuration Option 5 include the following:

- One Local and Two Remote Temperature Channels
- Up to Three PWM Drives and Up to Six TACH Inputs
- Voltage Monitoring
- Two +12V
- +3.3V
- Mem_Core (+1.969V)
- +1.8 V
- Two +1.5V
- +1.2V (V_{CCP2})
- $\overline{\text{RESET}}$ I/O

Figure 23 shows the pin configuration when Configuration Option 5 is chosen.

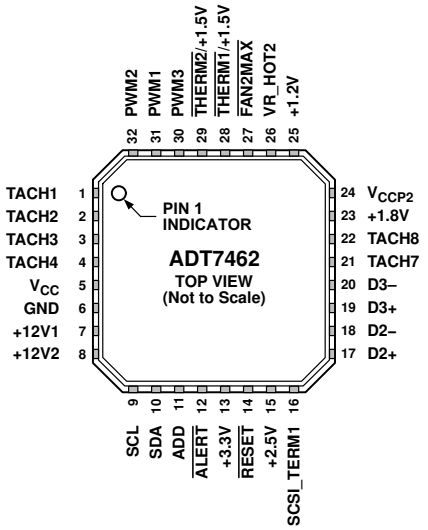


Figure 23. Configuration Option 5

Table 10. CONFIGURATION OPTION 5

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	+12V1	Pin Configuration Reg 1	Bit 0 = 0
8	+12V2	Pin Configuration Reg 2	Bit 7 = 0
13	+3.3V	Pin Configuration Reg 2	Bit 6 = 0
15	+2.5V	Pin Configuration Reg 1	Bit 6 = 0
16	SCSI_ TERM1	Pin Configuration Reg 1	Bit 6 = 0
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3–	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	+1.8V	Pin Configuration Reg 2	Bits [1:0] = 10
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	+1.2V	Pin Configuration Reg 3	Bits [5:4] = 01
26	VR_HOT2	Pin Configuration Reg 3	Bits [3:2] = 1×
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28 †*	$\overline{\text{THERM1}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
29*	$\overline{\text{THERM2}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

*It is not possible to configure +1.5V monitoring on Pin 29 and $\overline{\text{THERM1}}$ on Pin 28. Pin 28 must both be configured as either +1.5V monitoring or as $\overline{\text{THERM}}$ I/O (see Table 51).

Serial Bus Interface

The ADT7462 is controlled through use of the serial system management bus (SMBus). The ADT7462 is connected to this bus as a slave device, under the control of a master controller. The SMBus interface in the ADT7462 is fully SMBus 1.1 and SMBus 1.0 compliant. The SMBus address is determined by the state of the ADD input on powerup.

ADD Input

The ADD pin is a three-state input to the ADT7462. It is used to determine the SMBus address used. This pin is sampled on powerup only. Any changes subsequent to powerup are not reflected until the ADT7462 is powered down and back up again. The corresponding 7-bit SMBus address for the state of the ADD pin is shown in Table 11.

Table 11. CORRESPONDING SMBUS ADDRESSES FOR ADD INPUT

ADD Pin	SMBus Version	SMBus Address
High	N/A	N/A
Float	SMBus 1.1	0x5C
Low	SMBus 1.1	0x58

SMBus Fixed Address

The ADT7462 supports SMBus fixed address mode and is fully backward compatible with SMBus 1.1 and SMBus 1.0. The ADT7462 powers up with a fixed SMBus address that cannot be changed by the assign address call. The fixed address is set by the state of the ADD input pin on powerup. The ADT7462 also responds to the SMBus device default address of 0x61.

SMBus Operation

The SMBus specification defines specific conditions for different types of read and write operations. The general SMBus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device.
2. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the 9th clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from it or written to it. If the R/$\overline{W}$ bit = 0, the master writes to the slave device. If the R/$\overline{W}$ bit = 1, the master reads from the slave device.
3. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
4. When all data bytes have been read or written, stop conditions are established. In write mode, the master releases the data line during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the 9th clock pulse. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse and then takes it high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

For the ADT7462, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or to read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 24. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities.

- If the ADT7462 address pointer register value is unknown or not the desired value, it must be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7462 as before, but only the data byte containing the register address is sent because no data is written to the register (see Figure 25).
  A read operation is then performed, consisting of the serial bus address and the R/$\overline{W}$ bit set to 1, followed by

the data byte read from the data register (see Figure 26).

- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 26).

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value.

However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7462 also supports the read byte protocol (see System Management Bus Specifications Rev. 2.0 for more information).

If several read or write operations must be performed in succession, then the master can send a repeat start condition, instead of a stop condition, to begin a new operation.

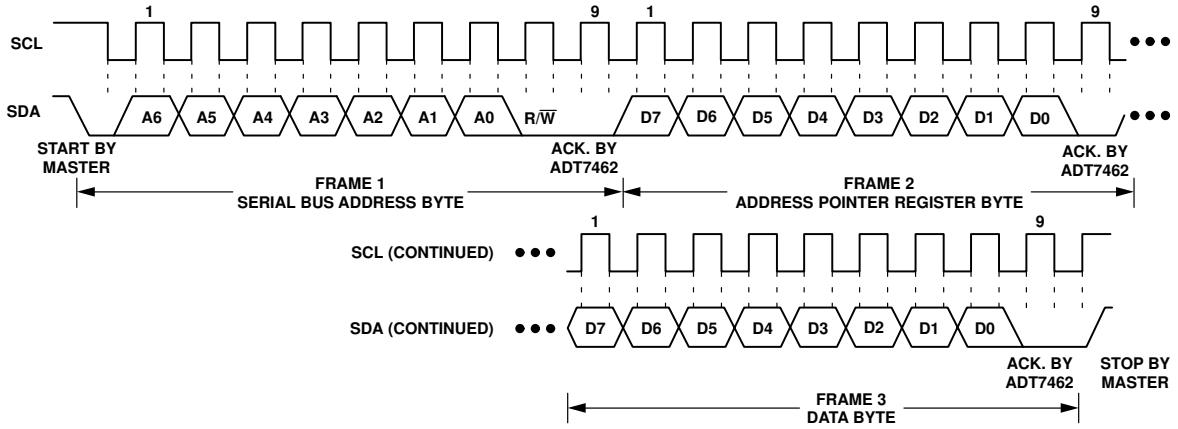


Figure 24. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

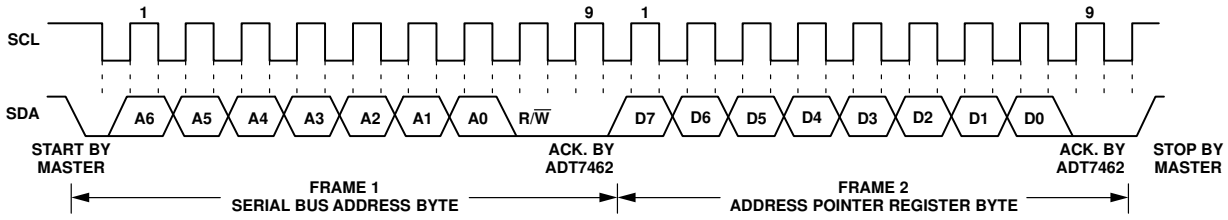


Figure 25. Writing to the Address Pointer Register Only

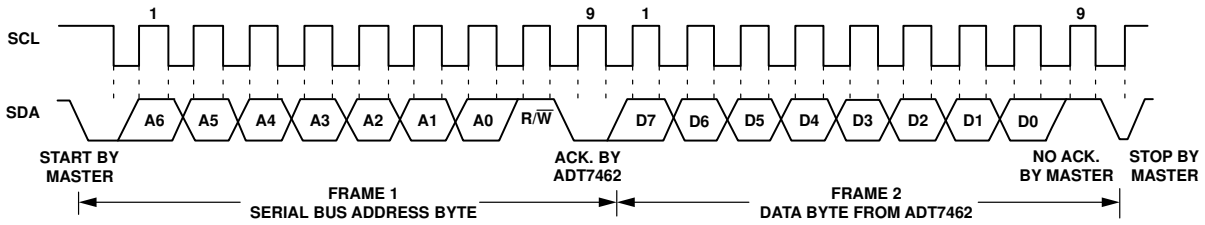


Figure 26. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7462 are discussed below. The following abbreviations are used in the diagrams:

- S – Start
- P – Stop
- R – Read
- W – Write
- A – Acknowledge
- $\overline{A}$ – No Acknowledge

The ADT7462 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code.
5. The slave asserts an ACK on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

For the ADT7462, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is shown in Figure 27.

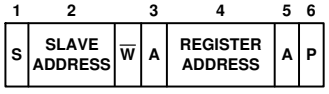


Figure 27. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code.
5. The slave asserts an ACK on SDA.
6. The master sends a data byte.
7. The slave asserts an ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

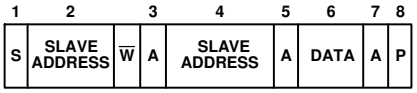


Figure 28. Single-byte Write to a Register

Block Write

In this operation, the master device writes a block of data to a slave device. The start address for a block write must be set previously. In the case of the ADT7462, this is done by a send byte operation to set a RAM address. The user writes the number of registers to be written to in the block read command to the #Bytes bits of the Configuration 0 register.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block write. The ADT7462 command code for a block write is 0xA0 (1010 0000).
5. The slave asserts an ACK on SDA.
6. The master sends the data bytes (the number of data bytes sent is written to the #Bytes bits of the Configuration 0 register).
7. The slave asserts an ACK on SDA after each data byte.
8. The master sends a packet error checking (PEC) byte.
9. The ADT7462 checks the PEC byte and issues an ACK, if correct. If incorrect (NO ACK), the master resends the data bytes.
10. The master asserts a stop condition on SDA to end the transaction.

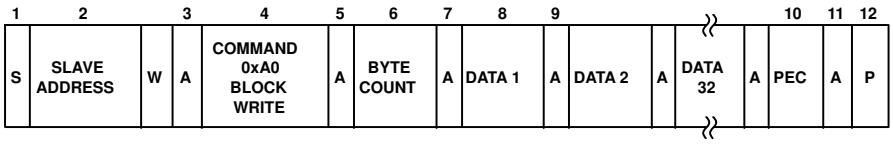


Figure 29. Block Write to ADT7462

Read Operations

The ADT7462 uses the following SMBus read protocols.

Receive Byte

The receive byte is useful when repeatedly reading a single register. The register address must be set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an ACK on SDA.
4. The master receives a data byte.
5. The master asserts a NO ACK on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

For the ADT7462, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write a byte operation.

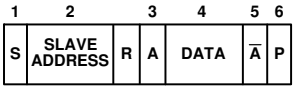


Figure 30. Single-byte Read from a Register

Block Read

In this operation, the master device reads a block of data from a slave device. The start address for a block read must be set previously, as well as the number of bytes to be read (maximum = 32). In the case of the ADT7462, the start address is activated by a send byte operation to set a RAM address. The number of bytes to be read should be written to the #Bytes bits in the Configuration 0 register. The block read operation consists of a send byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADT7462 command code for a block read is 0xA1 (1010 0001).
5. The slave asserts an ACK on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts an ACK on SDA.
9. The ADT7462 sends a byte count telling the master how many data bytes to expect. The maximum number of bytes is 32.
10. The master asserts an ACK on SDA.
11. The master receives the expected number of data bytes.
12. The master asserts an ACK on SDA after each data byte.
13. The ADT7462 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.
14. A NO ACK is generated after the PEC byte to signal the end of the read.
15. The master asserts a stop condition on SDA to end the transaction.

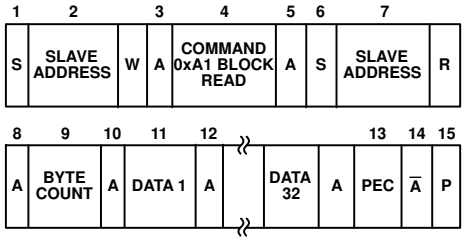


Figure 31. Block Read from RAM

Note that although the ADT7462 supports packet error checking (PEC), its use is optional. The PEC byte is calculated using CRC−8. The frame check sequence (FCS) conforms to CRC−8 by the polynomial.

$$C(x) = x^8 + x^2 + x + 1$$

Consult the SMBus 1.1 specifications for more information.

Alert Response Address

Alert Response Address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the ARA, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7462 has responded to the ARA, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7462 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the ADT7462 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus while the device is expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 3 (0x03)

Bit 1 SCL_Timeout = 1; SCL Timeout Enabled

Bit 1 SCL_Timeout = 0; SCL Timeout Disabled (Default)

Bit 2 SDA_Timeout = 1; SDA Timeout Enabled

Bit 2 SDA_Timeout = 0; SDA Timeout Disabled (Default)

Temperature and Voltage Measurement

Temperature Measurement

The ADT7462 can measure its own ambient temperature and the temperature of up to three remote thermal diodes. These diodes can be discrete diode-connected 2N3904/2N3906s or they can be located on a processor die. Figure 32 shows how to connect a remote NPN or PNP transistor.

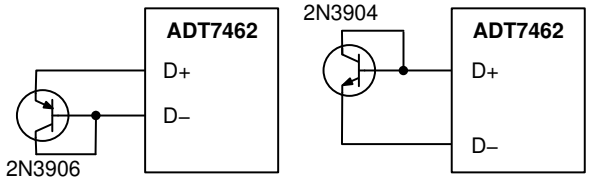


Figure 32. How to Measure Temperature Using Discrete Transistors

Remote Thermal Diode 1 connects to Pin 15 and Pin 16.

Remote Thermal Diode 2 connects to Pin 17 and Pin 18.

Remote Thermal Diode 3 connects to Pin 19 and Pin 20.

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor, operated at constant current. Unfortunately, this technique requires calibration to cancel the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADT7462 is to measure the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents; use of a third current allows automatic cancellation of any resistances in series with the external temperature sensor.

Figure 33 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (recommended maximum value 1000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. As shown in Figure 33, N1 × I and N2 × I are different multiples of the Current I. The currents through the temperature diode are switched between I and N1 × I, giving ΔV_{BE1}, and then between I and N2 × I, giving ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also be shown to cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles for low conversion rates.

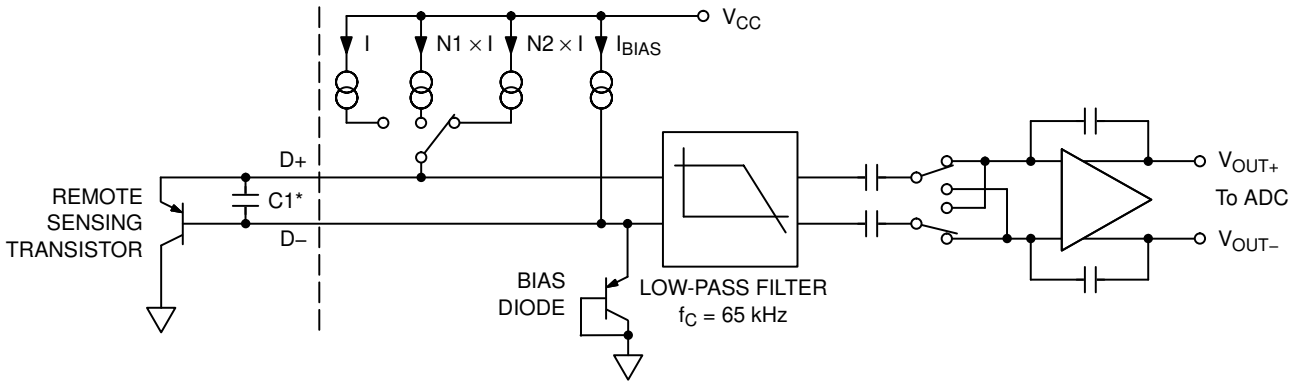
Signal conditioning and measurement of the internal temperature sensor are performed in the same manner (see Figure 33).

Temperature Measurement Results

The results of the local and remote temperature measurements are stored in the local and remote temperature value registers and are compared with limits programmed into the local and remote high and low limit registers.

Table 12. TEMPERATURE MEASUREMENT REGISTERS

Temperature Value	Register Address
Local Temperature, LSB	Register 0x88, Bits [7:6]
Local Temperature, MSB	Register 0x89
Remote 1 Temperature, LSB	Register 0x8A, Bits [7:6]
Remote 1 Temperature, MSB	Register 0x8B
Remote 2 Temperature, LSB	Register 0x8C, Bits [7:6]
Remote 2 Temperature, MSB	Register 0x8D
Remote 3 Temperature, LSB	Register 0x8E, Bits [7:6]
Remote 3 Temperature, MSB	Register 0x8F



*CAPACITOR C1 IS OPTIONAL. IT SHOULD ONLY BE USED IN NOISY ENVIRONMENTS.

Figure 33. Input Signal Conditioning

The temperature value is stored in two registers. The MSB has a resolution of 1°C. Only two bits in the temperature LSB register are used, Bit 7 and Bit 6, giving a temperature measurement resolution of 0.25°C. The temperature measurement range for both local and remote measurements is from −64°C to +191°C. However, the ADT7462 itself should never be operated outside its operating temperature range, which is from −40°C to +125°C. For the remote diode, the user should refer to the data sheet of the diode.

Table 13. TEMPERATURE DATA FORMAT

Temperature Value	MSB	LSB
−64°C	0000 0000	0000 0000
−50.25°C	0000 1110	0100 0000
−25°C	0010 0111	0000 0000
0°C	0100 0000	0000 0000
+25°C	0101 1001	0000 0000
+50.25°C	0111 0010	0100 0000
+100°C	1010 0100	0000 0000

When reading the full temperature value, the LSB should be read first and then the MSB. Reading the LSBs causes the current MSBs to be frozen until they are read. Reading the MSBs only does not cause any register to be locked. This is useful when a temperature reading with 1°C resolution is required.

Series Resistance Cancellation

Parasitic resistance in series with the remote diode D+ and D− inputs can be caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.8°C offset per ohm of parasitic resistance in series with the remote diode.

The ADT7462 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The ADT7462 is designed to automatically cancel typically up to 2 kΩ of resistance. By using an advanced temperature measurement method, the process is transparent to the user. This feature also allows an RCR filter to be added to the sensor path, allowing the part to be used accurately in noisy environments.

Temperature Limits

Each temperature measurement channel has a high and low temperature limit associated with it. The temperature measurements are compared with these limits, and the results of these comparisons are stored in status registers. A Logic 0 indicates an in-limit comparison, and a Logic 1 indicates an out-of-limit comparison. The ADT7462 can generate an $\overline{\text{ALERT}}$, if configured to do so, after a status bit is set. For more information on the status registers and $\overline{\text{ALERT}}$, see the Status and Mask Registers $\overline{\text{ALERT}}$ section.

Each temperature channel also has a $\overline{\text{THERM1}}$ and a $\overline{\text{THERM2}}$ temperature limit associated with it. When these temperature limits are exceeded, the corresponding $\overline{\text{THERM}}$ pin is asserted low (if $\overline{\text{THERM}}$ is configured as an output), and the fans are boosted to full speed (if the boost bit is set). Table 14 shows a complete list of all the temperature limits and their default values.

Table 14. TEMPERATURE LIMIT REGISTERS

Temperature Value	Register Address	Default
Local Low Temperature Limit	0x44	0x40
Remote 1 Low Temperature Limit	0x45	0x40
Remote 2 Low Temperature Limit	0x46	0x40
Remote 3 Low Temperature Limit	0x47	0x40
Local High Temperature Limit	0x48	0x95
Remote 1 High Temperature Limit	0x49	0x95
Remote 2 High Temperature Limit	0x4A	0x95
Remote 3 High Temperature Limit	0x4B	0x95
Local $\overline{\text{THERM1}}$ Temperature Limit	0x4C	0xA4
Remote 1 $\overline{\text{THERM1}}$ Temperature Limit	0x4D	0xA4
Remote 2 $\overline{\text{THERM1}}$ Temperature Limit	0x4E	0xA4
Remote 3 $\overline{\text{THERM1}}$ Temperature Limit	0x4F	0xA4
Local $\overline{\text{THERM2}}$ Temperature Limit	0x50	0xA4
Remote 1 $\overline{\text{THERM2}}$ Temperature Limit	0x51	0xA4
Remote 2 $\overline{\text{THERM2}}$ Temperature Limit	0x52	0xA4
Remote 3 $\overline{\text{THERM2}}$ Temperature Limit	0x53	0xA4

Offset Registers

The ADT7462 has temperature offset registers at Register 0x56 to Register 0x59 for the local, Remote 1, Remote 2, and Remote 3 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise and cancel it using the offset registers. The offset registers automatically add a twos complement, 8-bit reading to every temperature measurement. The LSBs add 0.5°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of 0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Temperature Offset Registers

Register 0x56 Local Temperature Offset = 0x00 (0°C Default)

Register 0x57 Remote 1 Temperature Offset = 0x00 (0°C Default)

Register 0x58 Remote 2 Temperature Offset = 0x00 (0°C Default)

Register 0x59 Remote 3 Temperature Offset = 0x00 (0°C Default)

Layout Considerations

Digital boards can be electrically noisy environments. The ADT7462 measures very small voltages from the remote sensor, so care must be taken to minimize noise induced at the sensor inputs. The following precautions should be taken:

- Place the ADT7462 as close as possible to the remote sensing diode. Provided that the worst noise sources, such as clock generators, data/address buses, and CRTs, are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. To minimize inductance and reduce noise pickup, a 5 mil track width and spacing is recommended. If possible, provide a ground plane under the tracks.

Figure 34. Typical Arrangement of Signal Tracks

- Minimize the number of copper/solder joints that can cause thermo-couple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and at the same temperature.
- Thermocouple effects should not be a major problem because 1°C corresponds to about 200 mV, and thermocouple voltages are about 3 mV/°C of temperature difference. Unless there are two thermocouples with a large temperature differential between them, thermocouple voltages should be much less than 200 mV.
- Place a 0.1 μF bypass capacitor close to the V_{CC} pin. In extremely noisy environments, an input filter capacitor can be placed across D+ and D− close to the ADT7462. This capacitance can affect the temperature measurement, so care must be taken to ensure that any capacitance seen at D+ and D− is a maximum of 1000 pF. This maximum value includes the filter capacitance, plus any cable or stray capacitance between the pins and the sensor diode.
- If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This works from about 6 feet up to 12 feet.
- For really long distances (up to 100 feet), use shielded twisted pair, such as Belden No. 8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND close to the ADT7462. Leave the remote end of the shield unconnected to avoid ground loops.
- Because the measurement technique uses switched current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, the filter capacitance can be reduced or removed.

Noise Filtering

For temperature sensors operating in noisy environments, the industry-standard practice is to place a capacitor across the D+ and D− pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. While this capacitor does reduce noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The ADT7462 has a major advantage over other devices in eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the device. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7462 and the remote temperature sensor to operate in noisy environments. Figure 35 shows a low-pass RCR filter, with the following values:

R = 100 Ω

C = 1 nF

This filtering reduces both common-mode noise and differential noise.

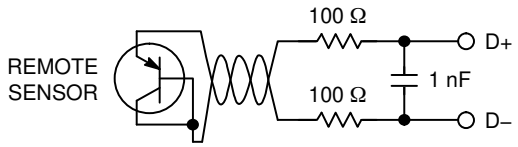


Figure 35. Filter Between Remote Sensor and ADT7462

Voltage Measurement

The ADT7462 is capable of measuring up to 13 different voltage inputs at one time. Table 15 is a list of the voltage measurement inputs and the corresponding input pins. Each pin can be configured to measure the desired voltage option using the Pin Configuration 1 (0x10) to Pin Configuration 4 (0x13) registers or the easy configuration options.

Input Circuit

The internal structure for the voltage inputs is shown in Figure 36. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order, low-pass filter that gives the input immunity to high frequency noise.

Voltages with full-scale values greater than the reference are divided so that the full-scale value equals the reference (2.25 V). All analog inputs are multiplexed into the on-chip, successive approximation ADC. This ADC has a resolution of ten bits. The basic input range is from 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of larger and smaller voltages. To allow a tolerance for these voltages, the ADC produces an output of 3/4 full scale (decimal 768 or 0x300) for the nominal input voltage and so has enough headroom to cope with overvoltages.

A list of corresponding LSB and full-scale values for each input voltage is shown in Table 16.

Table 15. VOLTAGE INPUTS

Pin	Voltage Measured
7	+12V1
8	+12V2
13	+3.3V
15	+2.5V / +1.8V
19	+1.25V / +0.9V
21	+5V
22	+12V3
23	V_{CCP1} / +1.5V / +1.8V / +2.5V
24	V_{CCP2} / +1.5V / +1.8V / +2.5V
25	+1.2V1 (G_{BIT}) / +3.3V
26	+1.2V2 (FSB_V_{TT}) / V_{BATT}
28	+1.5V1 (ICH)
29	+1.5V2 (3GIO)

Table 16. INPUT RANGE CODE CONVERSION

Nominal Input Voltage (3/4 Scale)	Pin No.	1 LSB Value	Full Scale
+12V	7, 8, 22	0.0625	16 V
+5V	21	0.026	6.67 V
V_{CCP1}, V_{CCP2}	23, 24	0.00625	1.6 V
V_{CCP1}, when VIDs are Enabled	23	0.0125	3.2 V
+3.3V	13, 25	0.0172	4.4 V
V_{BATT}	26	0.0156	4.0 V
+2.5V	15, 23, 24	0.013	3.33 V
+1.8V	15, 23, 24	0.0094	2.4 V
+1.5V	23, 24, 28, 29	0.0078	2.0 V
+1.25V	19	0.0065	1.667 V
+1.2V	25, 26	0.00625	1.6 V
+0.9V	19	0.00469	1.2 V

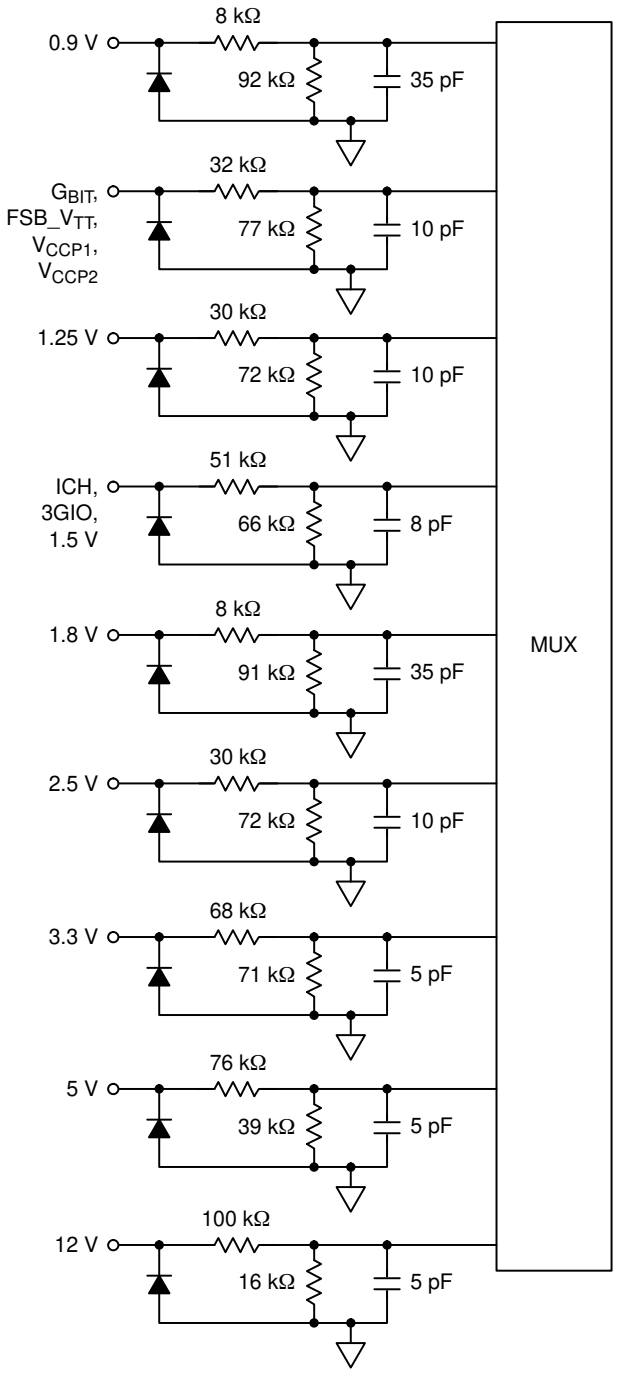


Figure 36. Voltage Input Structures

Example Calculations

Given the LSB value for each channel, the corresponding code for each voltage (or vice versa) can be calculated.

$$\text{Code} = \frac{\text{Voltage}}{1\ \text{LSB}}$$

Example:

The code for 1.8 V in a 1.8 V channel is:

$$\text{Code} = \frac{1.8}{0.0094} = 192\ (\text{that is, } 3/4\ \text{scale})$$

Similarly, the voltage, given the code in a particular channel, is calculated as follows:

$$\text{Voltage} = \text{Code} \times 1\ \text{LSB}$$

where:

10 V is connected to the 12 V channel.

1 LSB = 0.0625.

Code = 160 decimal.

Voltage Measurement and Limit Registers

The corresponding register locations for voltage measurements are listed in Table 17. Each voltage measurement channel has a high and low voltage limit associated with it. The voltage measurements are compared with these limits. The results of these comparisons are stored in status registers. A Logic 0 indicates an in-limit condition, and a Logic 1 indicates an out-of-limit condition. The ADT7462 can generate an $\overline{\text{ALERT}}$, if configured to do so, when a status bit is set. For more information on the status registers and $\overline{\text{ALERT}}$, see the Status and Mask Registers $\overline{\text{ALERT}}$ section. A complete list of all the high and low voltage limits in the ADT7462 and their default values is contained in Table 17.

Table 17. VOLTAGE VALUE AND LIMIT REGISTERS

Voltage Value	Pin No.	Value Register Address	Low Limit		High Limit	
			Register	Default	Register	Default
+12V1	7	0xA3	0x6D	0x00	0x7C	0xFF
+12V2	8	0xA5	0x6E	0x00	0x7D	0xFF
+3.3V	13	0x96	0x70	0x00	0x68	0xFF
+1.8V or +2.5V	15	0x8B	0x45	0x40	0x49	0x95
+1.25V or +0.9V	19	0x8F	0x47	0x40	0x4B	0x95
+5V	21	0xA7	0x71	0x00	0x7E	0xFF
+12V3	22	0xA9	0x6F	0x00	0x7F	0xFF
V_{CCP1}, +1.5V, +1.8V, +2.5V	23	0x90	0x72	0x20	0x69	0xFF
V_{CCP2}, +1.5V, +1.8V, +2.5V	24	0x91	0x73	0x00	0x6A	0xFF
+1.2V1 (G_{BIT}) or +3.3V	25	0x92	0x74	0x00	0x6B	0xFF
+1.2V2 (FSB_V_{TT}) or V_{BATT}	26	0x93	0x75	0x80	0x6C	0xFF
+1.5V1 (ICH)	28	0x94	0x77	0x00	0x50	0xA4
+1.5V2 (3GIO)	29	0x95	0x76	0x00	0x4C	0xA4

Battery Measurement Input (V_{BATT})

The V_{BATT} input allows the condition of a CMOS backup battery to be monitored. This is typically a lithium coin cell, such as a CR2032. The V_{BATT} input is accurate only for voltages greater than 1.2 V. Note that when Pin 26 is configured as a +1.2V input, voltages lower than 1.2 V are not accurately measured. Input voltage and corresponding voltage measured are shown in Figure 16.

Typically, the battery in a system is required to keep some devices powered on when the system is in a powered-off state. The V_{BATT} measurement input is designed to minimize battery drain. To reduce current drain from the battery, the lower resistor of the V_{BATT} attenuator is not connected, except when a V_{BATT} measurement is being made. The total current drain on the V_{BATT} pin is 80 nA typical (for a maximum V_{BATT} voltage = 4.0 V), so a CR2032 CMOS battery functions in a system in excess of the expected 10 years. Note that when a V_{BATT} measurement is not being made, the current drain is reduced to 16 nA typical. Under normal voltage measurement operating conditions, all measurements are made in a round-robin format, and each reading is actually the result of 16 digitally averaged measurements. However, averaging is not carried out on the V_{BATT} measurement to reduce measurement time and, therefore, reduce the current drain from the battery.

The V_{BATT} current drain when a measurement is being made is calculated by:

$$I = \frac{V_{BATT}}{100\ k\Omega} \times \frac{t_{pulse}}{t_{period}}$$

where:

t_{PULSE} is the V_{BATT} measurement time (~711 μs typical).
t_{PERIOD} is the time required to measure all analog inputs.

Monitoring cycle time depends on the ADT7462 configuration. Calculating the monitoring cycle time is described in more detail in the ADC Information section.

V_{BATT} Input Battery Protection

In addition to minimizing battery current drain, the V_{BATT} measurement circuitry is specifically designed with battery protection in mind. Internal circuitry prevents the battery from being back-biased by the ADT7462 supply or through any other path under normal operating conditions. In the unlikely event of a catastrophic ADT7462 failure, the ADT7462 includes a second level of battery protection, including a series 3 kΩ resistor to limit current to the battery, as recommended by UL (see Figure 37). Thus, it is not necessary to add a series resistor between the battery and the V_{BATT} input; the battery can be connected directly to the V_{BATT} input to improve voltage measurement accuracy.

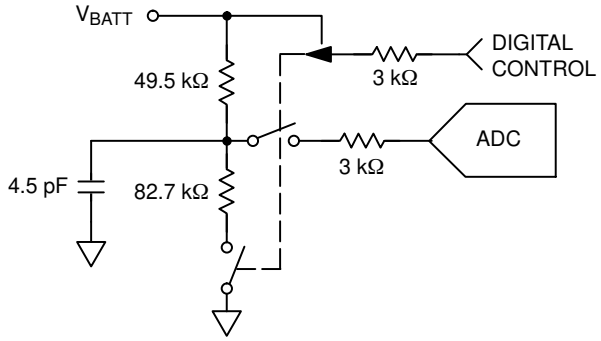


Figure 37. Equivalent V_{BATT} Input Protection Circuit

ADC Information

Round Robin

Both temperature and voltage measurements are analog inputs that are digitized using the on-board ADC. An internal multiplexer switches between the different analog inputs and digitizes them, in turn, in a round-robin manner. The total conversion time depends upon how the ADT7462 is configured. The conversion times for each measurement channel are shown in Table 18. The complete conversion time is the sum of the time for the voltage and temperature measurements.

For example, if the ADT7462 is configured as Easy Configuration Option 1, the round-robin conversion time is calculated as follows:

Total Conversion Time =
1 × (Local Conversion Time) +
3 × (Remote Conversion Time) +
4 × (Voltage Measurement Time)

The TACH is not measured using the ADC and so is not part of the round-robin monitoring cycle.

Table 18. MEASUREMENT CHANNEL CONVERSION TIMES

Channel	Conversion Time (ms)
Local Temperature	9.01
Remote Temperature	38.36
Voltage	8.53

For each ADC temperature and voltage measurement read from their value registers, 16 readings have actually been made internally and the results averaged before being placed in the value register.

Bypass Voltage Attenuators

There are up to 13 voltage measurement channels on the ADT7462. Each of these voltage measurement channels has an input structure (see Figure 36 for input structures for each of the voltage channels). Because the ADC has a voltage input range from 0 V to 2.25 V, these input circuits attenuate the voltage input using a resistor divider network to match the input range of the ADC. However, the user may occasionally want to remove the attenuators and directly apply a voltage of between 0 V and 2.25 V to the ADC. These attenuators can be disabled by setting relevant bits in the voltage attenuator configuration registers (see Table 19). This feature also allows the user to rescale the voltage inputs using an external attenuator circuit. However, when the attenuators are disabled, the user should ensure that the voltage on the pin never exceeds 2.25 V.

Table 19. VOLTAGE ATTENUATOR CONFIGURATION REGISTERS

Register Name	Register Address
Voltage Attenuator Configuration Register 1	0x18
Voltage Attenuator Configuration Register 2	0x19

Single-channel ADC Conversions

Setting Bit 2 of the EDO Enable register (0x16) places the ADT7462 into single-channel mode. In this mode, the ADT7462 can be made to convert on a single voltage or temperature channel only. The channel to be converted on is selected by writing to Bits [7:3] of the EDO (single-channel) Enable register (0x16). When the device is in single-channel mode, the pin configuration option should not be changed.

Note that when the Pin 26 voltage, which includes the V_{BATT} option, is selected in single-channel mode, this means that voltage measurements are continuously made in this mode. If a battery is connected to this input, this results in an excessive current drain on the battery. The specification of >10 years of battery life is valid only when the battery voltage is measured as part of the round robin and not in single-channel mode.

Table 20. SINGLE-CHANNEL MODE OPTIONS

Bits [7:3]	ADC Channel Selected
0000 0	+1.2V2 Voltage, Pin 26
0000 1	Remote 1 Temperature
0001 0	Remote 2 Temperature
0001 1	Remote 3 Temperature
0010 0	Local Temperature
0010 1	+12V1 Voltage, Pin 7
0011 0	+12V2 Voltage, Pin 8
0011 1	+12V3 Voltage, Pin 22
0100 0	+3.3V Voltage, Pin 13
0100 1	+2.5V/+1.8V Voltage, Pin 15
0101 0	+1.25V/+0.9V Voltage, Pin 19
0101 1	+5V Voltage, Pin 21
0110 0	+1.5V/+1.8V/+2.5V Voltage, Pin 23
0110 1	+1.5V/+1.8V/+2.5V Voltage, Pin 24
0111 0	+1.2V1/+3.3V Voltage, Pin 25
1000 0	+1.5V1 Voltage, Pin 28
1000 1	+1.5V2 Voltage, Pin 29