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ADT7463

Remote Thermal Controller and Voltage Monitor

The ADT7463 controller is a complete systems monitor and multiple PWM fan controller for noise−sensitive applications requiring active system cooling. It can monitor 12 V, 5 V, and 2.5 V CPU supply voltages, plus its own supply voltage. It can monitor the temperature of up to two remote sensor diodes, plus its own internal temperature. It can measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise. The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7463 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Monitors Up to 5 Supply Voltages
- Controls and Monitors up to 4 Fan Speeds
- 1 On−Chip and 2 Remote Temperature Sensors
- Monitors Up to 6 Processor VID Bits
- Dynamic T_{MIN} Control Mode Optimizes System Acoustics Intelligently
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 2−wire and 3−wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- This is a Pb−Free Device

Applications

- Low Acoustic Noise PCs
- Networking and Telecommunications Equipment

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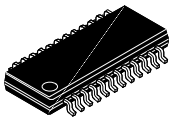
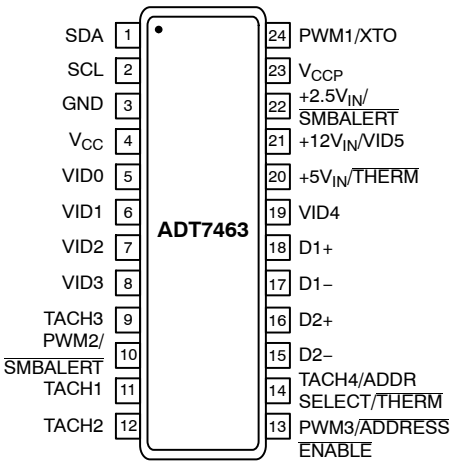


QSOP24 NB
CASE 492B

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM

ADT7463ARQZ	= Specific Device Code
#	= Pb−Free Package
YY	= Date Code
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 49 of this data sheet.

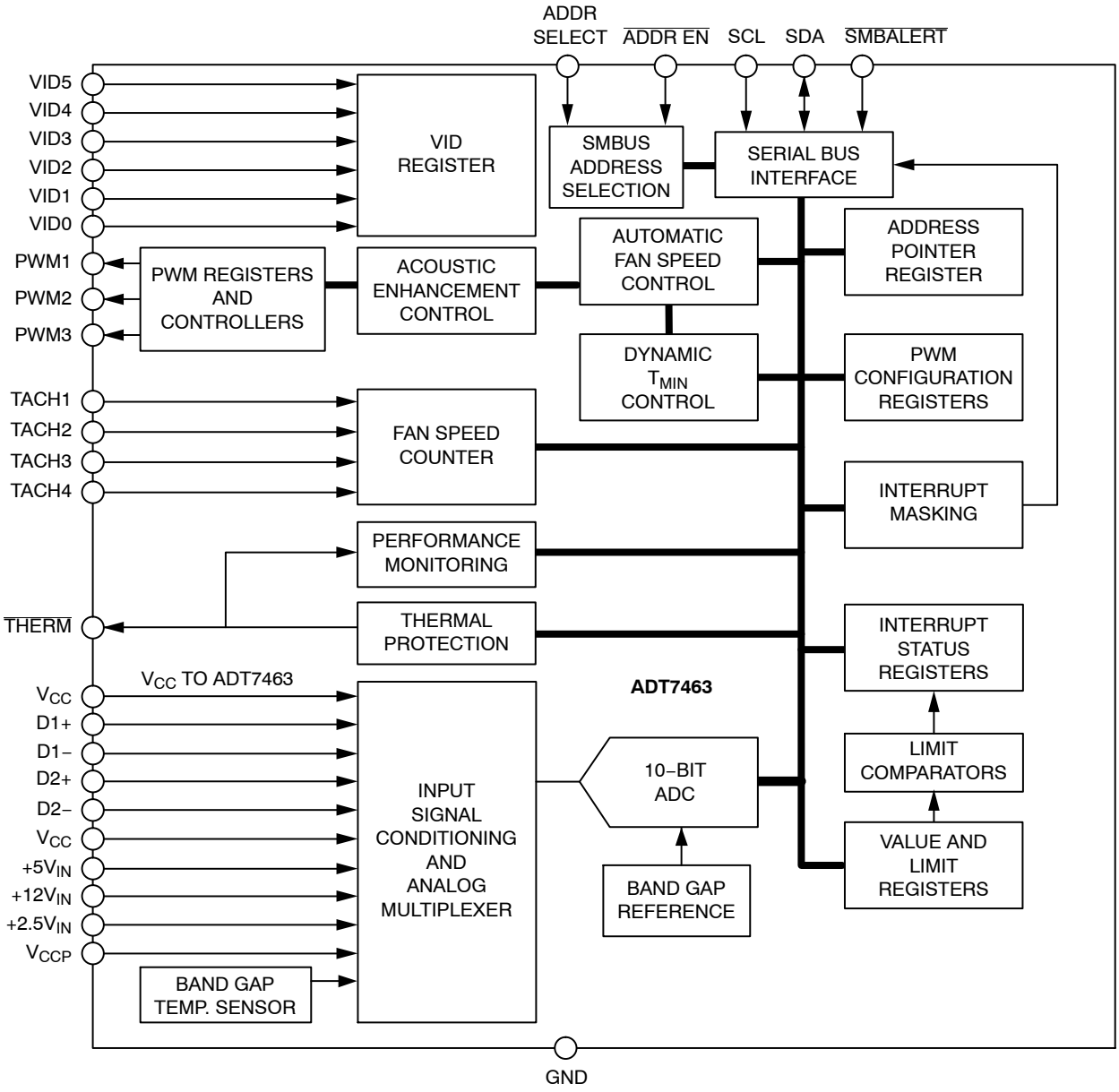


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	6.5	V
Voltage on $+12V_{IN}$ Pin	20	V
Voltage on Any Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature IR Reflow Peak Temperature for Pb−Free Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
24−lead QSOP	105	39	°C/W

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull−up.
3	GND	Ground Pin for the ADT7463.
4	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7463 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
5	VID0	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
6	VID1	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
7	VID2	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
8	VID3	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2−wire fans.
10	PWM2 $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pull−up. Pulse−width modulated output to control FAN 2 speed. Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
11	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2−wire fans.
12	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2−wire fans.
13	PWM3 $\overline{\text{ADDRESS ENABLE}}$	Digital I/O (Open Drain). Pulse−width modulated output to control Fan 3/Fan 4 speed. Requires 10 kΩ typical pull−up. If pulled low on power−up, this places the ADT7463 into address select mode, and the state of Pin 14 will determine the ADT7463's slave address.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
14	TACH4 ADDRESS SELECT $\overline{\text{THERM}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2−wire fans. If in address select mode, this pin determines the SMBus device address. Alternatively, the pin may be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
15	D2−	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1−	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
20	$+5V_{IN}$ $\overline{\text{THERM}}$	Analog Input. Monitors 5 V power supply. Alternatively, this pin may be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
21	$+12V_{IN}$ VID5	Analog Input. Monitors 12 V power supply. Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43). Supports VRM10 solutions.
22	$+2.5V_{IN}$ $\overline{\text{SMBALERT}}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage. Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
24	PWM1 XTO	Digital Output (Open Drain). Pulse−width modulated output to control Fan 1 speed. Requires 10 kΩ typical pull−up. Also functions as the output from the XOR tree in XOR test mode.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		3.0	5.0	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	− −	− −	3.0 20	mA μA
TEMPERATURE−TO−DIGITAL CONVERTER					
Local Sensor Accuracy	$0°C \le T_A \le 70°C$ $-40°C \le T_A \le +120°C$	− −	±0.5 −	±1.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Diode Sensor Accuracy	$0°C \le T_A \le 70°C$; $0°C \le T_D \le 120°C$ $0°C \le T_A \le 105°C$; $0°C \le T_D \le 120°C$ $0°C \le T_A \le 120°C$; $0°C \le T_D \le 120°C$	− − −	±0.5 − −	±1.5 ±2.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Sensor Source Current	High Level Low Level	− −	180 11	− −	μA
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE		−	−	±1.5	%
Differential Non−linearity, DNL		−	−	±1.0	LSB
Power Supply Sensitivity		−	±0.1	−	%/V
Conversion Time (Voltage Input)	Averaging Enabled	−	11.38	13	ms
Conversion Time (Local Temperature)	Averaging Enabled	−	12.09	13.50	ms
Conversion Time (Remote Temperature)	Averaging Enabled	−	25.59	28	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	− −	120.17 13.51	134.50 15	ms

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Input Resistance		100	140	200	kΩ
FAN RPM−TO−DIGITAL CONVERTER					
Accuracy	0°C ≤ T_A ≤ 70°C 0°C ≤ T_A ≤ 105°C −40°C ≤ T_A ≤ +120°C	− − −	− − −	±7 ±11 ±13	%
Full−scale Count		−	−	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	− − − −	109 329 5,000 10,000	− − − −	RPM
Internal Clock Frequency		82.8	90.0	97.2	kHz
OPEN−DRAIN DIGITAL OUTPUTS, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}		−	−	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA, V_{CC} = 3.3 V	−	−	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	1.0	μA
OPEN−DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA, V_{CC} = 3.3 V	−	−	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	1.0	μA
SMBUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	−	−	V
Input Low Voltage, V_{IL}		−	−	0.4	V
Hysteresis		−	500	−	mV
DIGITAL INPUT LOGIC LEVELS (VID0 TO VID5)					
Input High Voltage, V_{IH}	Bit 6 (THLD) Reg. 0x43 = 0 (VID Threshold = 1 V)	1.7	−	−	V
Input Low Voltage, V_{IL}	Bit 6 (THLD) Reg. 0x43 = 0 (VID Threshold = 1 V)	−	−	0.8	V
Input High Voltage, V_{IH}	Bit 6 (THLD) Reg. 0x43 = 1 (VID Threshold = 0.6 V)	0.8	−	−	V
Input Low Voltage, V_{IL}	Bit 6 (THLD) Reg. 0x43 = 1 (VID Threshold = 0.6 V)	−	−	0.4	V
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	 Maximum Input Voltage	2.0 −	− −	− 5.5	V
Input Low Voltage, V_{IL}	 Minimum Input Voltage	− −0.3	− −	+0.8 −	V
Hysteresis		−	0.5	−	V p−p
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{THERM}}$) AGTL+					
Input High Voltage, V_{IH}		−	0.75 × V_{CCP}	−	V
Input Low Voltage, V_{IL}		−	−	0.4	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	−1.0	−	−	μA
Input Low Current, I_{IL}	V_{IN} = 0	−	−	+1.0	μA
Input Capacitance, C_{IN}		−	5.0	−	pF

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING (Note 5)					
Clock Frequency, f_{SCLK}	See Figure 2	–	–	400	kHz
Glitch Immunity, t_{SW}	See Figure 2	–	–	50	ns
Bus Free Time, t_{BUF}	See Figure 2	1.3	–	–	μs
Start Setup Time, $t_{SU;STA}$	See Figure 2	0.6	–	–	μs
Start Hold Time, $t_{HD;STA}$	See Figure 2	0.6	–	–	μs
SCL Low Time, t_{LOW}	See Figure 2	1.3	–	–	μs
SCL High Time, t_{HIGH}	See Figure 2	0.6	–	50	μs
SCL, SDA Rise Time, t_R	See Figure 2	–	–	1,000	ns
SCL, SDA Fall Time, t_F	See Figure 2	–	–	300	μs
Data Setup Time, $t_{SU;DAT}$	See Figure 2	100	–	–	ns
Data Hold Time, $t_{HD;DAT}$	See Figure 2	300	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise specified.
2. Typicals are at T_A = 25°C and represent the most likely parametric norm.
3. Logic inputs accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}.
4. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.0 V for a rising edge.
5. Guaranteed by design; not production tested

NOTE: Specifications subject to change without notice.

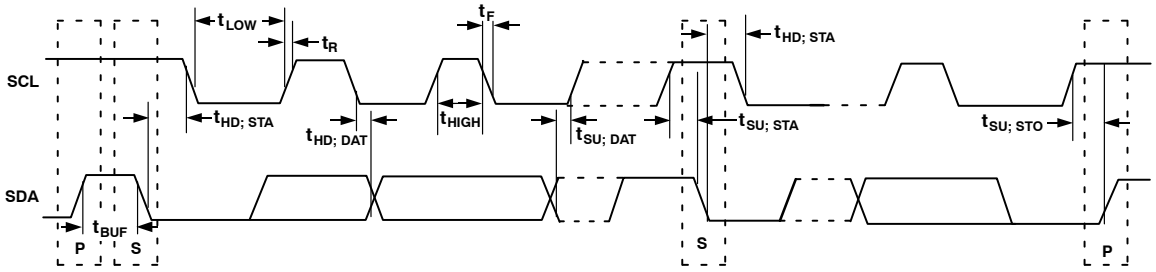


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

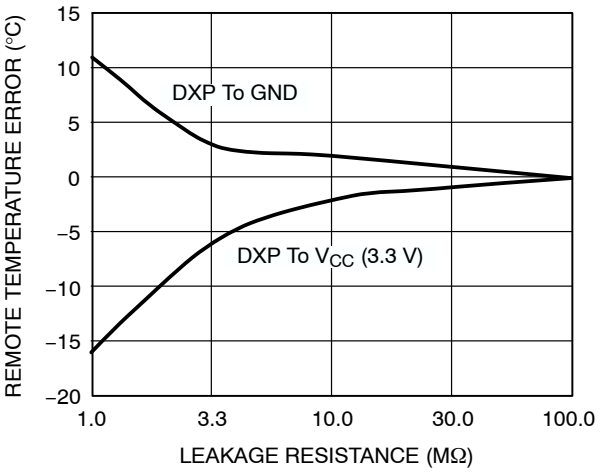


Figure 3. Remote Temperature Error vs. Leakage Resistance

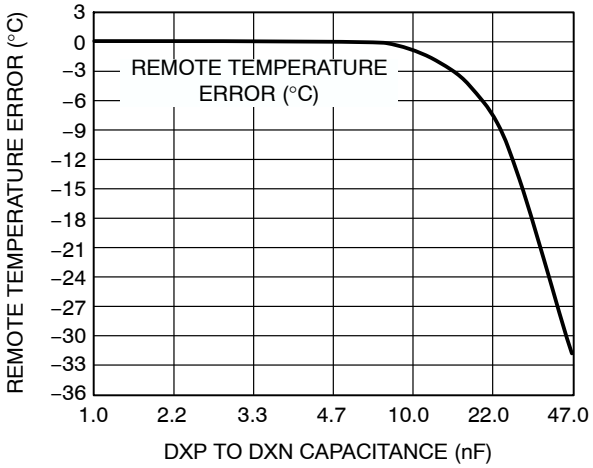


Figure 4. Remote Temperature Error vs. Capacitance between D+ and D−

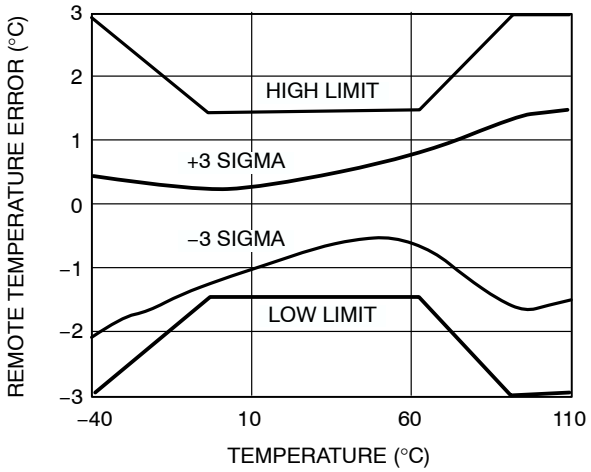


Figure 5. Remote Temperature Error vs. Actual Temperature

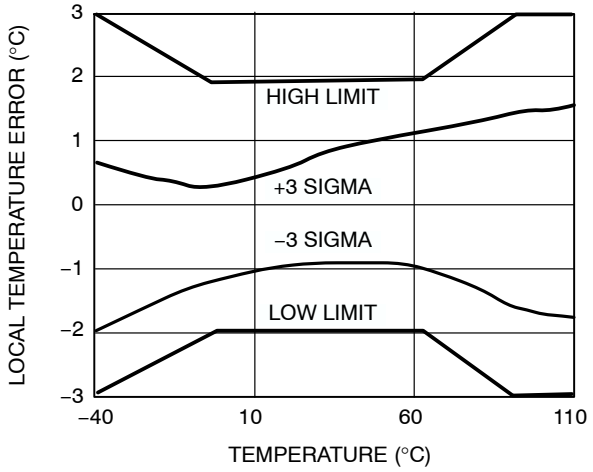


Figure 6. Local Temperature Error vs. Actual Temperature

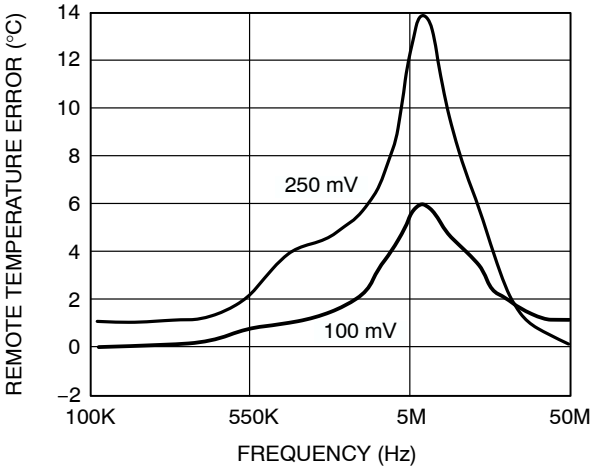


Figure 7. Remote Temperature Error vs. Power Supply Noise Frequency

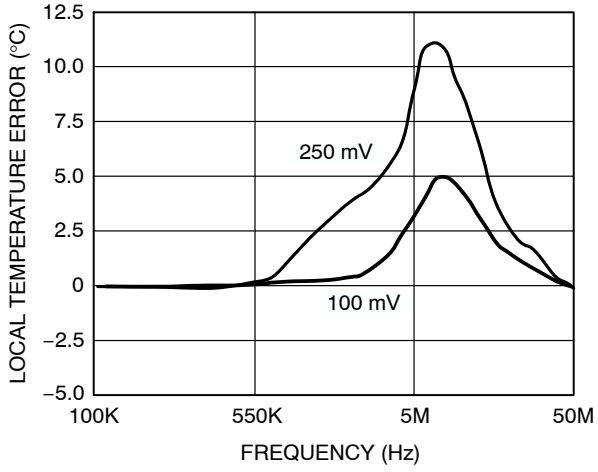


Figure 8. Local Temperature Error vs. Power Supply Noise Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

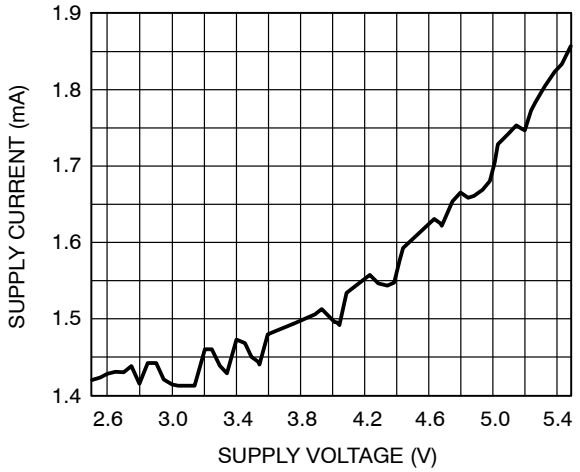


Figure 9. Supply Current vs. Supply Voltage

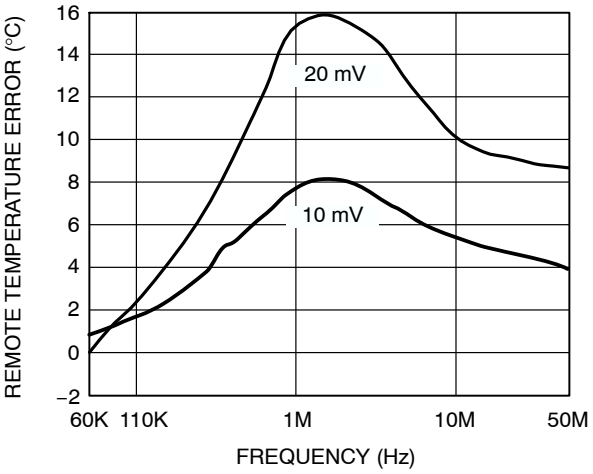


Figure 10. Remote Temperature Error vs. Differential−Mode Noise Frequency

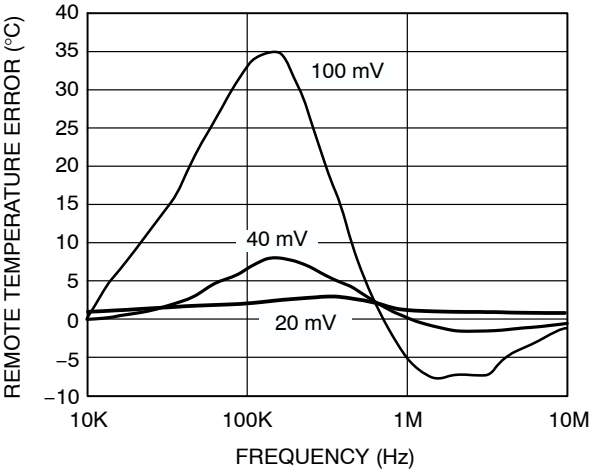


Figure 11. Remote Temperature Error vs. Common−Mode Noise Frequency

Functional Description

General Description

The ADT7463 is a complete systems monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has an optional address line for device selection (Pin 14), a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions of the ADT7463 are performed over the serial bus. In addition, two of the pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to indicate out−of−limit conditions.

Measurement Inputs

The device has six measurement inputs, four for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on−chip temperature sensor.

Pins 20 through 23 are analog inputs with on−chip attenuators, configured to monitor 5 V, 12 V, 2.5 V, and the processor core voltage (2.25 V input), respectively.

Power is supplied to the chip via Pin 4, and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5 V supply and monitor it without overranging.

Remote temperature sensing is provided by the D1± and D2± inputs, to which diode−connected, external temperature−sensing transistors, such as a 2N3904 or CPU thermal diode, may be connected.

The ADC also accepts input from an on−chip band gap temperature sensor that monitors system ambient temperature.

Sequential Measurement

When the ADT7463 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensors. Measured values from these inputs are stored in value registers. These can be read out over the serial bus or can be compared with programmed limits stored in the limit registers. The results of out−of−limit comparisons are stored in the status registers, which can be read over the serial bus to flag out−of−limit conditions.

Processor Voltage ID

Five digital inputs (VID0 to VID5 − Pins 5 to 8, 19, and 21) read the processor voltage ID code and store it in the VID register, from which it can be read out by the management system over the serial bus. The VID code monitoring function is compatible with both VRM9.x and future VRM10 solutions. Additionally, an $\overline{\text{SMBALERT}}$ can be generated to flag a change in VID code.

ADT7463 Address Selection

Pin 13 is the dual−function PWM3/$\overline{\text{ADDRESS ENABLE}}$ pin. If Pin 13 is pulled low on power−up, the ADT7463 reads the state of Pin 14 (TACH4/ADDRESS SELECT/ $\overline{\text{THERM}}$ pin) to determine the ADT7463's slave address. If Pin 13 is high on power−up, then the ADT7463 defaults to the SMBus slave Address 0x2E. This function is described in more detail later.

Internal Registers of the ADT7463

A brief description of the ADT7463's principal internal registers is given below. More detailed information on the function of each register is given in Tables X4 to X42.

Configuration Registers

The configuration registers provide control and configuration of the ADT7463, including alternate pinout functionality.

Address Pointer Register

This register contains the address that selects one of the other internal registers. When writing to the ADT7463, the first byte of data is always a register address, which is written to the address pointer register.

Status Registers

These registers provide the status of each limit comparison and are used to signal out−of−limit conditions on the temperature, voltage, or fan speed channels. If Pin 10 or Pin 22 is configured as $\overline{\text{SMBALERT}}$, then this pin asserts low whenever a status bit gets set.

Interrupt Mask Registers

These registers allow each interrupt status event to be masked when Pin 10 or Pin 22 is configured as an $\overline{\text{SMBALERT}}$ output.

VID Register

The status of the VID0 to VID5 pins of the processor can read from this register. VID code changes can also generate $\overline{\text{SMBALERT}}$ interrupts.

Value and Limit Registers

The results of analog voltage inputs, temperature, and fan speed measurements are stored in these registers, along with their limit values.

Offset Registers

These registers allow each temperature channel reading to be offset by a twos complement value written to these registers.

T_{MIN} Registers

These registers program the starting temperature for each fan under automatic fan speed control.

T_{RANGE} Registers

These registers program the temperature−to−fan speed control slope in automatic fan speed control mode for each PWM output.

Operating Point Registers

These registers define the target operating temperatures for each thermal zone when running under dynamic T_{MIN} control. This function allows the cooling solution to adjust dynamically in response to measured temperature and system performance.

Enhance Acoustics Registers

These registers allow each PWM output controlling fan to be tweaked to enhance the system's acoustics.

Recommended Implementation

Configuring the ADT7463 as in Figure 12 allows the systems designer the following features:

- Six VID Inputs (VID0 to VID5) for VRM10 Support
- Two PWM Outputs for Fan Control of Up to Three Fans (The Front and Rear Chassis Fans Are Connected in Parallel)
- Three TACH Fan Speed Measurement Inputs
- V_{CC} Measured Internally Through Pin 4
- CPU Core Voltage Measurement (V_{CORE})
- 2.5 V Measurement Input Used to Monitor CPU Current (Connected to V_{COMP} Output of ADP316x VRM Controller) This Is Used to Determine CPU Power Consumption
- 5 V Measurement Input
- VRM Temperature Uses Local Temperature Sensor
- CPU Temperature Measured Using Remote 1 Temperature Channel
- Ambient Temperature Measured Through Remote 2 Temperature Channel
- If Not Using VID5, This Pin Can Be Reconfigured as the 12 V Monitoring Input
- Bidirectional $\overline{\text{THERM}}$ Pin. Allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ Monitoring and Can Function as an Overtemperature $\overline{\text{THERM}}$ *O*utput
- $\overline{\text{SMBALERT}}$ System Interrupt Output

NOTE: See the AN−612 ADT7463 Configuration Application Note for more information and register settings for all possible configurations.

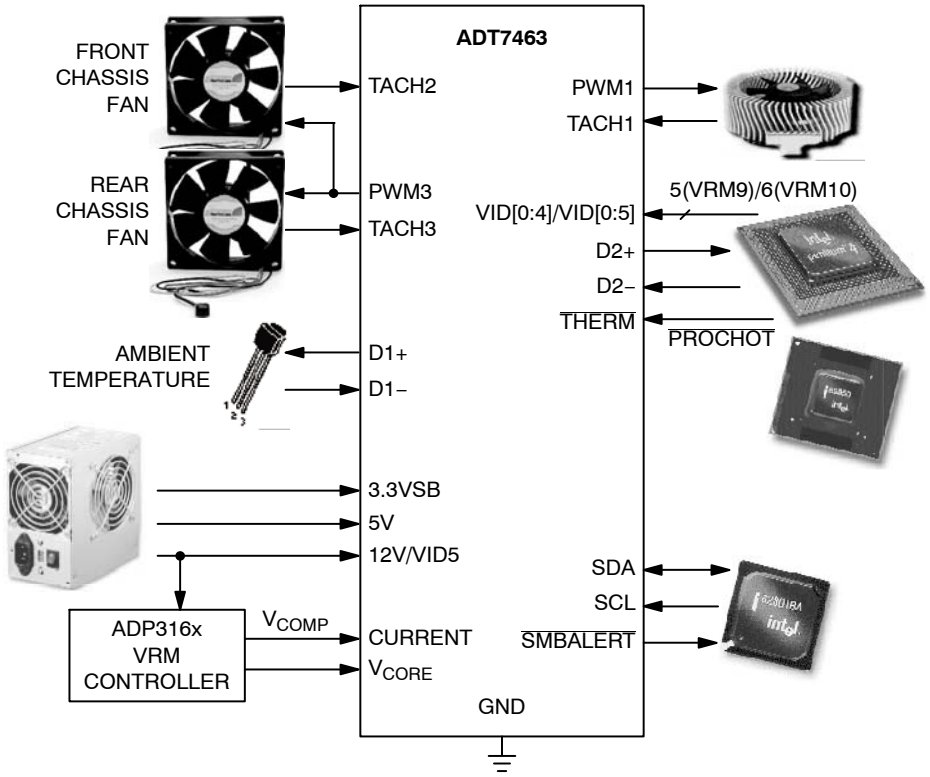


Figure 12. Recommended Implementation

Serial Bus Interface

Control of the ADT7463 is carried out using the serial system management bus (SMBus). The ADT7463 is connected to this bus as a slave device, under the control of a master controller.

The ADT7463 has a 7−bit serial bus address. When the device is powered up with Pin 13 (PWM3/ $\overline{\text{ADDRESS ENABLE}}$) high, the ADT7463 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8−bit address. If more than one ADT7463 is used in a system, then each ADT7463 should be placed in address select mode by strapping Pin 13 low on power−up. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled upon power−up.

The device address is sampled and latched on the first valid SMBus transaction, more precisely on the low−to−high transition at the beginning of the 8th SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the address enable/address select pins. Any attempted changes in the address will have no effect after this.

Table 5. ADDRESS SELECT MODE

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull−up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)

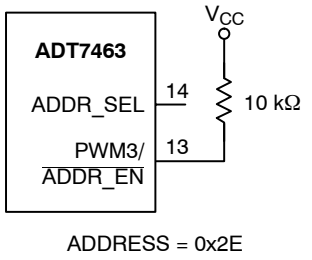


Figure 13. Default SMBus Address = 0x2E

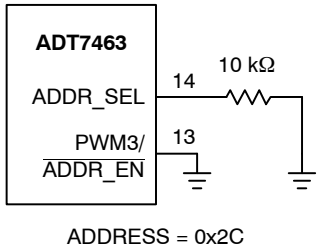


Figure 14. SMBus Address = 0x2C (Pin 14 = 0)

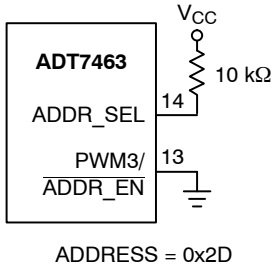
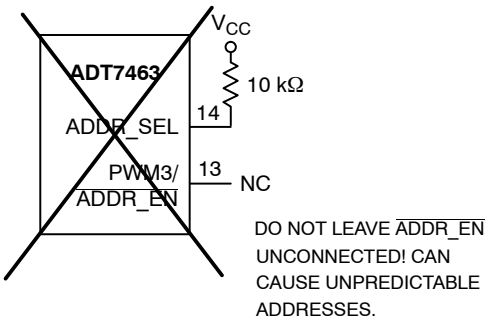


Figure 15. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/$\overline{\text{ADDR\_EN}}$) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7463 TO POWERUP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7463 IS PLACED INTO ADDRESS SELECT MODE, PINS 13 AND 14 CAN BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/$\overline{\text{THERM}}$) ONLY IF THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME.

Figure 16. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7463 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high−to−low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus a R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.
   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth

clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, then the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low−to−high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master pulls the data line high during the tenth clock pulse to assert a STOP condition. In READ mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADT7463, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 17. The device address is sent over the bus followed by R/$\overline{W}$ being set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

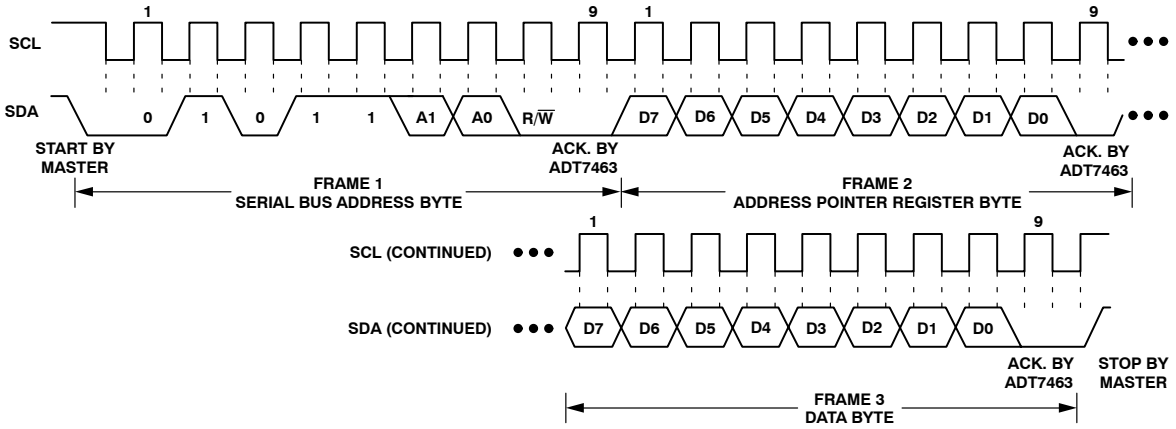


Figure 17. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

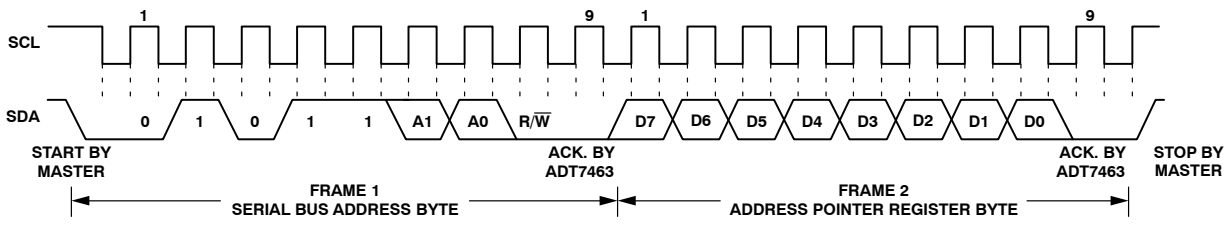


Figure 18. Writing to the Address Pointer Register Only

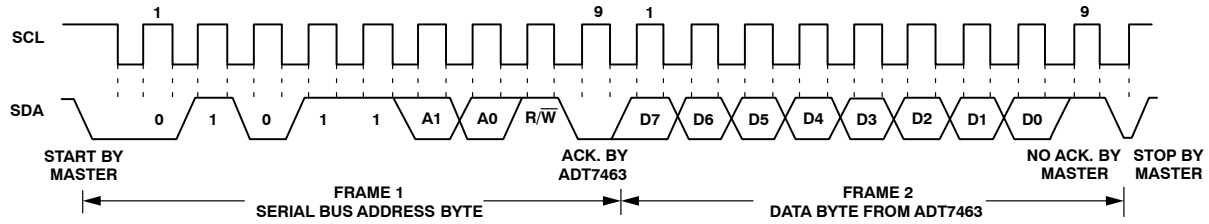


Figure 19. Reading Data from a Previously Selected Register

When reading data from a register, there are two possibilities:

1. If the ADT7463's address pointer register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7463 as before, however, only the data byte is sent and this contains the register address. This is shown in Figure 18.
   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 19.
2. If the address pointer register is already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, so Figure 18 can be omitted.

NOTES:

1. It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.
2. In Figures 17 to 19, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADT7463 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information).
4. If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

ADT7463 Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7463 are discussed below. The following abbreviations are used in the diagrams:

S – START
P – STOP
R – READ
W – WRITE
A – ACKNOWLEDGE
$\overline{A}$ – NO ACKNOWLEDGE

The ADT7463 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the write bit (low)
3. The addressed slave device asserts ACK on SDA
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master asserts a stop condition on SDA and the transaction ends

For the ADT7463, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This is illustrated in Figure 20.

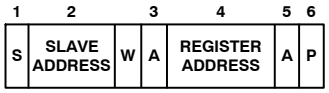


Figure 20. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the write bit (low)
3. The addressed slave device asserts ACK on SDA
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master sends a data byte
7. The slave asserts ACK on SDA
8. The master asserts a stop condition on SDA to end the transaction

This is illustrated in Figure 21.

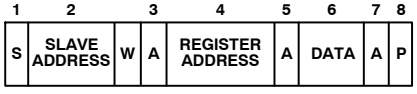


Figure 21. Single Byte Write to a Register

ADT7463 Read Operations

The ADT7463 uses the following SMBus read protocols.

Receive Byte

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the read bit (high)
3. The addressed slave device asserts ACK on SDA
4. The master receives a data byte
5. The master asserts NO ACK on SDA
6. The master asserts a stop condition on SDA and the transaction ends

In the ADT7463, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation.

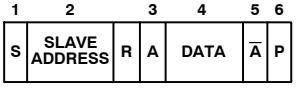


Figure 22. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as an interrupt output or can be used as an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address will have priority in accordance with normal SMBus arbitration
5. Once the ADT7463 has responded to the alert response address, the master must read the status registers and the $\overline{\text{SMBALERT}}$ will only be cleared if the error condition has gone away

SMBus Timeout

The ADT7463 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7463 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description
<6> TODIS	0: SMBus Timeout Enabled (Default)
<6> TODIS	1: SMBus Timeout Disabled

Voltage Measurement Inputs

The ADT7463 has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pins 20 to 23 are dedicated to measuring 5 V, 12 V, and 2.5 V supplies and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). Setting Bit 7 of Configuration Register 1 (Reg. 0x40) allows a 5 V supply to power the ADT7463 and be measured without overranging the V_{CC} measurement channel. The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

Analog−to−Digital Converter (ADC)

All analog inputs are multiplexed into the on−chip, successive approximation, ADC. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built−in attenuators to allow measurement of 2.5 V, 3.3 V, 5 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow for the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 23. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first−order, low−pass filter that gives the input immunity to high frequency noise.

Table 7. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x20	2.5 V Reading	0x00
0x21	V_{CCP} Reading	0x00
0x22	V_{CC} Reading	0x00
0x23	5 V Reading	0x00
0x24	12 V Reading	0x00

Associated with each voltage measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 8. VOLTAGE MEASUREMENT LIMITS REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

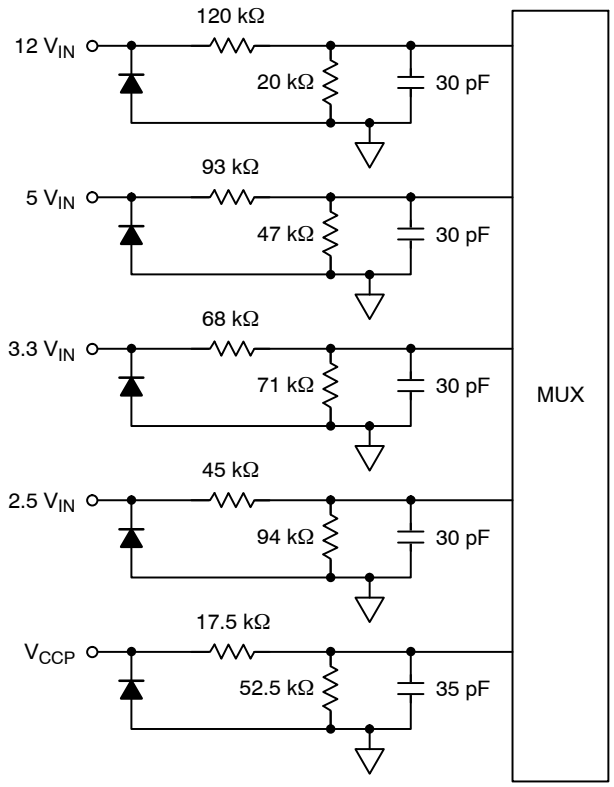


Figure 23. Structure of Analog Inputs

Table 12 shows the input ranges of the analog inputs and output codes of the 10−bit ADC.

When the ADC is running, it samples and converts a voltage input in 711 μs and averages 16 conversions to reduce noise; a measurement on each input takes nominally 11.38 ms.

VID Code Monitoring

The ADT7463 has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID register (Reg. 0x43) to determine the processor voltage required/being used in the system. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

Table 9. VID CODE REGISTER (REG. 0X43)

Bit	Description
<0> VID0	Reflects Logic State of Pin 5
<1> VID1	Reflects Logic State of Pin 6
<2> VID2	Reflects Logic State of Pin 7
<3> VID3	Reflects Logic State of Pin 8
<4> VID4	Reflects Logic State of Pin 19
<5> VID5	Reconfigurable 12 V Input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID Code Input Threshold Voltage

The switching threshold for the VID code inputs is approximately 1 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of VID register (Reg. 0x43) controls the VID input threshold voltage.

Table 10. VID CODE REGISTER (REG. 0X43)

Bit	Description
<6> THLD	0: VID Switching Threshold = 1 V, V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V 1: VID Switching Threshold = 0.6 V, V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V

Reconfiguring Pin 21 (+12V/VID5) as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10−compatible systems. Since the pin is configured as VID5, it is no longer possible to monitor a 12 V supply.

Bit 7 of the VID register (Reg. 0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or is monitoring a sixth VID input.

Table 11. VID CODE REGISTER (REG. 0X43)

Bit	Description
<7> VIDSEL	0: Pin 21 functions as a 12 V measurement input. Software can read this bit to determine that there are five VID inputs being monitored. Bit 5 of Register 0x43 (VID5) always reads back 0. Bit 0 of Status Register 2 (Reg. 0x42) reflects 12 V out−of−limit measurements. 1: Pin 21 functions as the sixth VID code input (VID5). Software can read this bit to determine that there are six VID inputs being monitored. Bit 5 of Register 0x43 reflects the logic state of Pin 21. Bit 0 of Status Register 2 (Reg. 0x42) reflects VID code changes.

Table 12. 10−BIT A/D OUTPUT CODE VS. V_{IN}

Input Voltage					A/D Output	
$+12V_{IN}$	$+5V_{IN}$	V_{CC} ($3.3V_{IN}$) (Note 1)	$+2.5V_{IN}$	$+V_{CCP}$	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156–0.0312	0.0065–0.0130	0.0042–0.0085	0.0032–0.0065	0.0293–0.0058	1	00000000 01
0.0312–0.0469	0.0130–0.0195	0.0085–0.0128	0.0065–0.0097	0.0058–0.0087	2	00000000 10
0.0469–0.0625	0.0195–0.0260	0.0128–0.0171	0.0097–0.0130	0.0087–0.0117	3	00000000 11
0.0625–0.0781	0.0260–0.0325	0.0171–0.0214	0.0130–0.0162	0.0117–0.0146	4	00000001 00
0.0781–0.0937	0.0325–0.0390	0.0214–0.0257	0.0162–0.0195	0.0146–0.0175	5	00000001 01
0.0937–0.1093	0.0390–0.0455	0.0257–0.0300	0.0195–0.0227	0.0175–0.0205	6	00000001 10
0.1093–0.1250	0.0455–0.0521	0.0300–0.0343	0.0227–0.0260	0.0205–0.0234	7	00000001 11
0.1250–0.14060	0.0521–0.0586	0.0343–0.0386	0.0260–0.0292 • • •	0.0234–0.0263	8	00000010 00
4.0000–4.0156	1.6675–1.6740	1.1000–1.1042	0.8325–0.8357 • • •	0.7500–0.7529	256 (1/4 Scale)	01000000 00
8.0000–8.0156	3.3300–3.3415	2.2000–2.2042	1.6650–1.6682 • • •	1.5000–1.5029	512 (1/2 Scale)	10000000 00
12.0000–12.0156	5.0025–5.0090	3.3000–3.3042	2.4975–2.5007 • • •	2.2500–2.2529	768 (3/4 Scale)	11000000 00
15.8281–15.8437	6.5983–6.6048	4.3527–4.3570	3.2942–3.2974	2.9677–2.9707	1013	11111101 01
15.8437–15.8593	6.6048–6.6113	4.3570–4.3613	3.2974–3.3007	2.9707–2.9736	1014	11111101 10
15.8593–15.8750	6.6113–6.6178	4.3613–4.3656	3.3007–3.3039	2.9736–2.9765	1015	11111101 11
15.8750–15.8906	6.6178–6.6244	4.3656–4.3699	3.3039–3.3072	2.9765–2.9794	1016	11111110 00
15.8906–15.9062	6.6244–6.6309	4.3699–4.3742	3.3072–3.3104	2.9794–2.9824	1017	11111110 01
15.9062–15.9218	6.6309–6.6374	4.3742–4.3785	3.3104–3.3137	2.9824–2.9853	1018	11111110 10
15.9218–15.9375	6.6374–6.4390	4.3785–4.3828	3.3137–3.3169	2.9853–2.9882	1019	11111110 11
15.9375–15.9531	6.6439–6.6504	4.3828–4.3871	3.3169–3.3202	2.9882–2.9912	1020	11111111 00
15.9531–15.9687	6.6504–6.6569	4.3871–4.3914	3.3202–3.3234	2.9912–2.9941	1021	11111111 01
15.9687–15.9843	6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	2.9941–2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

1. The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the $+5V_{IN}$ column.

VID Code Change Detect Function

The ADT7463 has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes can be detected and reported back by the ADT7463. Bit 0 of Status Register 2 (Reg. 0x42) is the 12V/VC bit and denotes a VID change when set. The VID code change bit gets set when the logic states on the VID inputs are different than they were 11 μs previously. The change of VID code can be used to generate an $\overline{\text{SMBALERT}}$ interrupt. If an $\overline{\text{SMBALERT}}$ interrupt is not required, Bit 0 of Interrupt Mask Register 2 (Reg. 0x75), when set, prevents $\overline{\text{SMBALERT}}$s from occurring on VID code changes.

Table 13. STATUS REGISTER (REG. 0X42)

Bit	Description
<0> 12V/VC	0: If Pin 21 is configured as VID5, then a Logic 0 denotes no change in VID code within last 11 μs. 1: If Pin 21 is configured as VID5, then a Logic 1 means that a change has occurred on the VID code inputs within the last 11 μs. An $\overline{\text{SMBALERT}}$ generates if this function is enabled.

Additional ADC Functions for Voltage Measurement

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility, including:

Turn−off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. There may be an instance where you would like to speed up conversions. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (Reg 0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single−channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7463 into single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read a single voltage channel only. If the internal ADT7463 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 Minimum High Byte Register (0x55).

Table 14. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<5>	1: Bypass Input Attenuators
<6>	1: Single−channel Convert Mode

Table 15. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description	
<7:5>	Selects ADC Channel for Single−channel Convert Mode	
	Value	**Channel Selected**
	000	2.5 V
	001	V_{CCP}
	010	V_{CC}
	011	5 V
	100	12 V

Temperature Measurement System

Local Temperature Measurement

The ADT7463 contains an on−chip band gap temperature sensor whose output is digitized by the on−chip 10−bit ADC. The 8−bit MSB temperature data is stored in the local temperature register (Address 26h). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 16. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside this range are not possible.

Remote Temperature Measurement

The ADT7463 can measure the temperature of two remote diode sensors or diode−connected transistors connected to Pins 15 and 16, or 17 and 18.

The forward voltage of a diode or diode−connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7463 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by

$$\Delta V_{BE} = KT/q \times \ln(N) \qquad \text{(eq. 1)}$$

where:

K is Boltzmann's constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvins.

N is the ratio of the two currents.

Figure 24 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could equally well be a discrete transistor, such as a 2N3904.

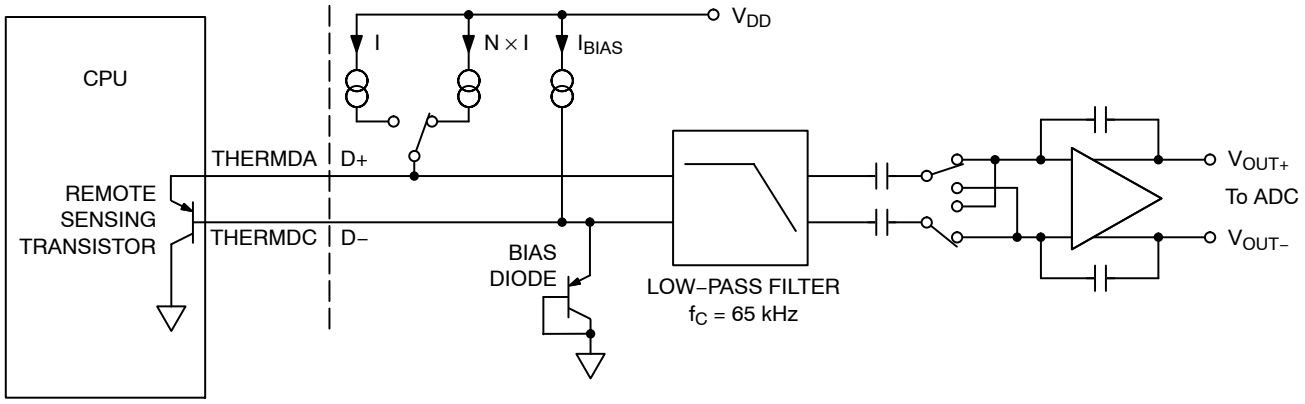


Figure 24. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector will not be grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figures 25 and 26 show how to connect the ADT7463 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D– input.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low−pass filter to remove noise and to a chopper−stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10−bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 25.5 ms. The results of remote temperature measurements are stored in 10−bit, twos complement format, as illustrated in Table 16. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

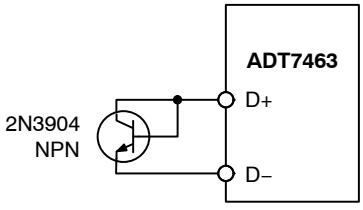


Figure 25. Measuring Temperature by Using an NPN Transistor

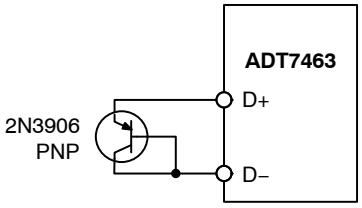


Figure 26. Measuring Temperature by Using a PNP Transistor

Table 16. TEMPERATURE DATA FORMAT

Temperature	Digital Output (10−bit) (Note 1)
−128°C	1000 0000 **00**
−125°C	1000 0011 **00**
−100°C	1001 1100 **00**
−75°C	1011 0101 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 17. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	0x80
0x26	Local Temperature	0x80
0x27	Remote 2 Temperature	0x80
0x77	Extended Resolution 2	0x00

Table 18. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS (REG. 0X77)

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Reading Temperature from the ADT7463

It is important to note that temperature can be read from the ADT7463 as an 8−bit value (with 1°C resolution) or as a 10−bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10−bit measurement is required, this involves a 2−register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its 2 LSBs are being read and vice versa.

Nulling Out Temperature Errors

As CPUs run faster, it is getting more difficult to avoid high frequency clocks when routing the D+, D− traces around a system board. Even when recommended layout guidelines are followed, there may still be temperature errors attributed to noise being coupled onto the D+/D− lines. High frequency noise generally has the effect of giving temperature measurements that are too high by a constant amount. The ADT7463 has temperature offset registers at Addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one−time calibration of the system, one can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8−bit reading to every temperature measurement. The LSBs add 0.25°C offset to the temperature reading so the 8−bit register effectively allows temperature offsets of up to ±32°C with a resolution of 0.25°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Table 19. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 20. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Registers 0x6A to 0x6C are the $\overline{\text{THERM}}$ limits. When a temperature exceeds its $\overline{\text{THERM}}$ limit, all fans run at 100% duty cycle. The fans stay running at 100% until the temperature drops below $\overline{\text{THERM}}$ – Hysteresis (this can be disabled by setting the boost bit in Configuration Register 3, Bit 2, Register 0x78). The hysteresis value for that $\overline{\text{THERM}}$ limit is the value programmed into Registers 0x6D, 0x6E (hysteresis registers). The default hysteresis value is 4°C.

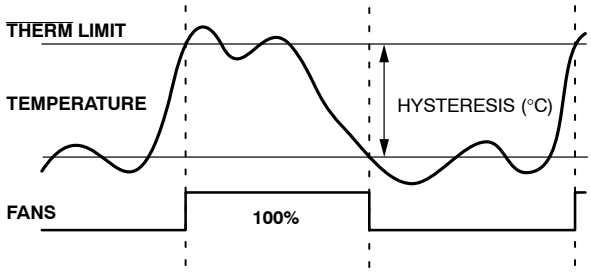


Figure 27. $\overline{\text{THERM}}$ Limit Operation

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility.

Turn−off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it may be necessary to take a very fast measurement, e.g., of CPU temperature. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This takes a reading every 13 ms. The measurement itself takes 4 ms.

Single−channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7463 into single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read a single temperature channel only. If the internal ADT7463 clock is used, the selected input is read every 1.4 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 Minimum High Byte Register (0x55).

Table 21. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<6>	1: Single−channel Convert Mode

Table 22. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description	
<7:5>	Selects ADC Channel for Single−channel Convert Mode	
	Value	Channel Selected
	101	Remote 1 Temp
	110	Local Temp
	111	Remote 2 Temp

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7463 are high and low limits. These can form the basis of system status monitoring: a status bit can be set for any out−of−limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out−of−limit conditions.

8−bit Limits

The following is a list of 8−bit limits on the ADT7463.

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64

Table 25. $\overline{\text{THERM}}$ LIMIT REGISTERS

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Limit	0x00

16−bit Limits

The fan TACH measurements are 16−bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Since fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Since fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 26. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out−of−Limit Comparisons

Once all limits are programmed, the ADT7463 can be enabled for monitoring. The ADT7463 measures all parameters in round−robin format and sets the appropriate status bit for out−of−limit conditions. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed

Low Limit: < or = Comparison Performed

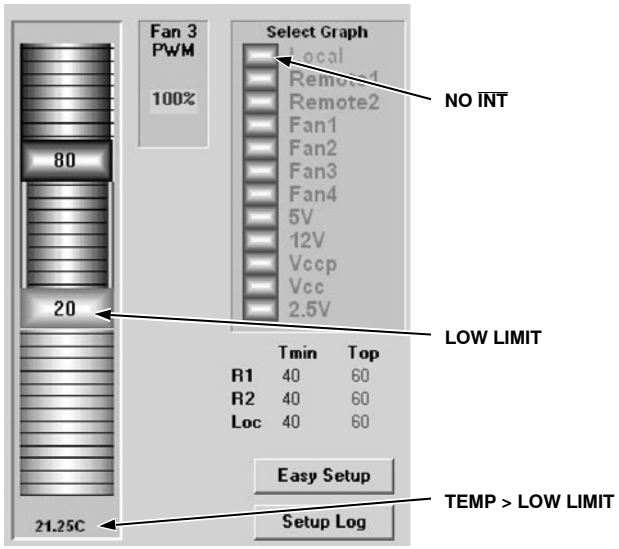


Figure 28. Temperature > Low Limit: No $\overline{INT}$

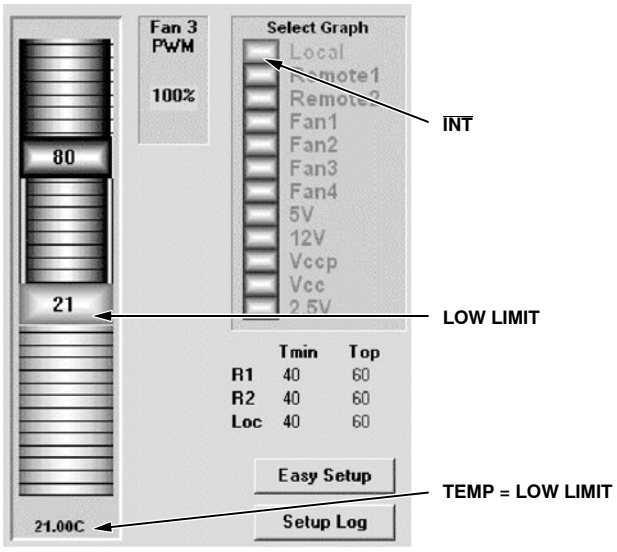


Figure 29. Temperature = Low Limit: $\overline{INT}$ Occurs

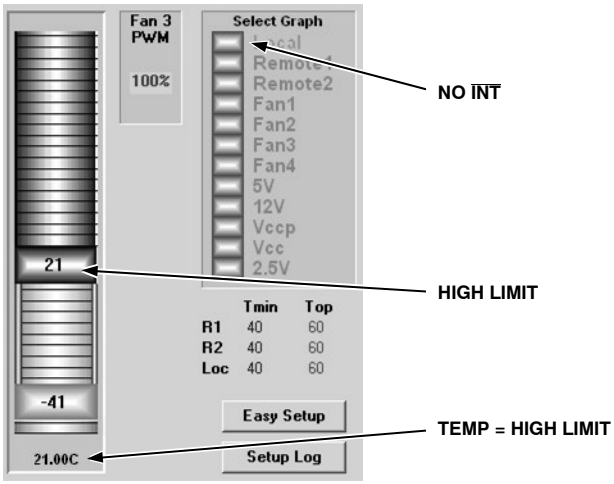


Figure 30. Temperature = High Limit: No $\overline{INT}$

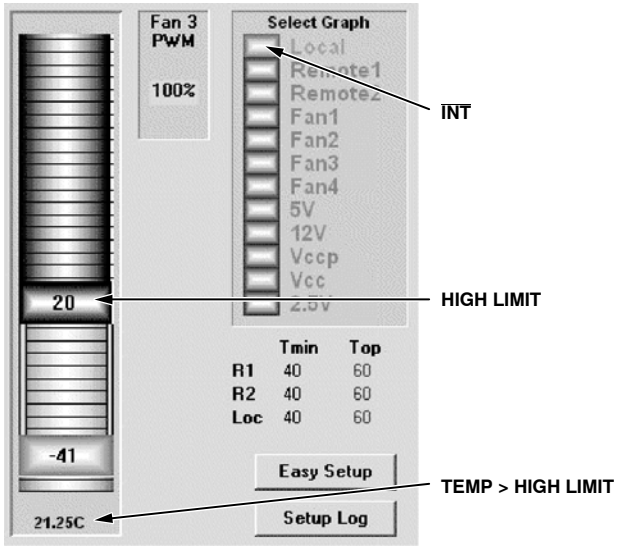


Figure 31. Temperature > High Limit: $\overline{INT}$ Occurs

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn and as each measurement is completed, the result is automatically stored in the appropriate value register. This round−robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

Because the ADC is normally left to free−run in this manner, the time taken to monitor all the analog inputs is normally not of interest, since the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it is easily calculated.

The total number of channels measured is:

- Four Dedicated Supply Voltage Inputs
- 3.3 V_{STBY} or 5 V Supply (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round−robin conversions and takes 11.38 ms for each voltage measurement, 12 ms for a local temperature reading, and 25.5 ms for each remote temperature reading.

The total monitoring cycle time for averaged voltage and temperature monitoring is therefore nominally

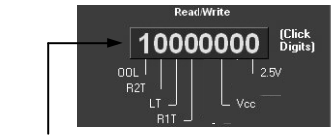
$$(5 \times 11.38) + 12\ (2 \times 25.5) = 120\ \text{ms} \quad \text{(eq. 2)}$$

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Status Registers 1 and 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out−of−limits, the corresponding status register bit is set to 1.

The state of the various measurement channels may be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Status Register 1 (Reg. 0x41), 1 means that an out−of−limit event has been flagged in Status Register 2. This means that a user need only read Status Register 2 when this bit is set. Alternatively, Pin 10 or Pin 22 can be configured as an $\overline{\text{SMBALERT}}$ output. This automatically notifies the system supervisor of an out−of−limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are “sticky.” Whenever a status bit gets set, indicating an out−of−limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out−of−limit, its associated status bit gets set in the interrupt status registers.



OOL = 1 DENOTES A PARAMETER MONITORED THROUGH STATUS REG 2 IS OUT−OF−LIMIT

Figure 32. Status Register 1

Table 27. STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1: denotes a bit in Status Register 2 is set and Status Register 2 should be read.
6	R2T	1: Remote 2 Temperature High or Low Limit has been exceeded.
5	LT	1: Local Temperature High or Low Limit has been exceeded.
4	R1T	1: Remote 1 Temperature High or Low Limit has been exceeded.
3	5V	1: 5 V High or Low Limit has been exceeded.
2	V_{CC}	1: V_{CC} High or Low Limit has been exceeded.
1	V_{CCP}	1: V_{CCP} High or Low Limit has been exceeded.
0	2.5V	1: 2.5 V High or Low Limit has been exceeded.

F4P = 1, FAN 4 OR $\overline{\text{THERM}}$ TIMER IS OUT−OF−LIMIT

Figure 33. Status Register 2

Table 28. STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D2+/D2− inputs.
5	F4P	1 indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ limit has been exceeded if the $\overline{\text{THERM}}$ function is used.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.
0	12V/VC	1 indicates that 12 V High or Low Limit has been exceeded. If the VID code change function is used, this bit indicates a change in VID code on the VID0 to VID5 inputs.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7463 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out−of−limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing Interrupt Handler software.

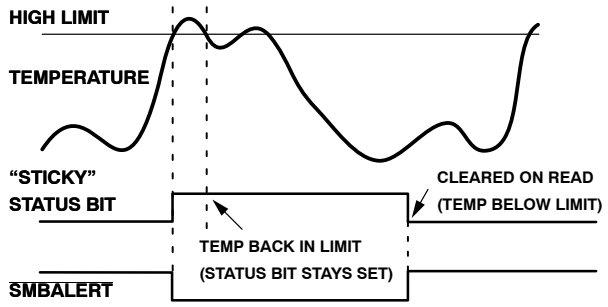


Figure 34. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

Figure 34 shows how the $\overline{\text{SMBALERT}}$ output and "sticky" status bits behave. Once a limit is exceeded, the corresponding status bit gets set to 1. The status bit remains set until the error condition subsides and the status register gets read. The status bits are referred to as sticky since they remain set until read by software. This ensures that an out−of−limit event cannot be missed if software is polling the device periodically. Note that the $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out−of−limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the Interrupt Handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 35.

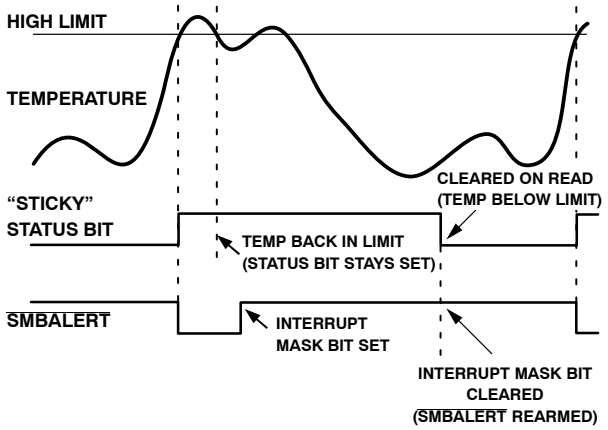


Figure 35. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent $\overline{\text{SMBALERT}}$ interrupts. Note that masking an interrupt source only prevents the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit gets set as normal.

Table 29. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Status Register 2.
6	R2T	1 masks $\overline{\text{SMBALERT}}$ for Remote 2 temperature.
5	LT	1 masks $\overline{\text{SMBALERT}}$ for Local Temperature.
4	R1T	1 masks $\overline{\text{SMBALERT}}$ for Remote 1 Temperature.
3	5V	1 masks $\overline{\text{SMBALERT}}$ for 5 V channel.
2	V_{CC}	1 masks $\overline{\text{SMBALERT}}$ for V_{CC} channel.
1	V_{CCP}	1 masks $\overline{\text{SMBALERT}}$ for V_{CCP} channel.
0	2.5V	1 masks $\overline{\text{SMBALERT}}$ for 2.5 V channel.

Table 30. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.
6	D1	1 masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.
5	FAN4	1 masks $\overline{\text{SMBALERT}}$ for Fan 4 failure. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event.
4	FAN3	1 masks $\overline{\text{SMBALERT}}$ for Fan 3.
3	FAN2	1 masks $\overline{\text{SMBALERT}}$ for Fan 2.
2	FAN1	1 masks $\overline{\text{SMBALERT}}$ for Fan 1.
1	OVT	1 masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ limits).
0	12V/VC	1 masks $\overline{\text{SMBALERT}}$ for 12 V channel or for a VID code change, depending on the function used.

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 10 or Pin 22 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out−of−limit conditions.

Table 31. CONFIGURATION PIN 22 AS $\overline{\text{SMBALERT}}$ OUTPUT (REG. 0X78)

Register	Bit Setting
Config Reg 3	<0> ALERT = 1

Table 32. CONFIGURATION PIN 22 AS $\overline{\text{SMBALERT}}$ OUTPUT (REG. 0X7D)

Register	Bit Setting
Config Reg 4	<0> AL2.5V = 1

To Assign $\overline{\text{THERM}}$ Functionality to a Pin

Pin 14 or Pin 20 can be configured as the $\overline{\text{THERM}}$ pin on the ADT7463.

To enable the $\overline{\text{THERM}}$ functionality, users must first set the $\overline{\text{THERM}}$ enable bit. The TH5V bit then determines which pin the $\overline{\text{THERM}}$ functionality is enabled on (i.e., users cannot enable $\overline{\text{THERM}}$ on two pins at once).

To configure Pin 20 as the $\overline{\text{THERM}}$ pin:

1. Set the TH5V bit (Bit 1) in the Configuration Register 4 (Address = 0x7D) = 1.
2. Set the $\overline{\text{THERM}}$ Enable Bit (Bit 1) in the Configuration Register 3 (Address = 0x78) = 1.

To configure Pin 14 as the $\overline{\text{THERM}}$ pin:

1. Set the TH5V bit (Bit 1) in the Configuration Register 4 (Address = 0x7D) = 0.
2. Set the $\overline{\text{THERM}}$ Enable Bit (Bit 1) in the Configuration Register 3 (Address = 0x78) = 1.

$\overline{\text{THERM}}$ as an Input

When configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance. See this data sheet for more information on timing $\overline{\text{THERM}}$ assertions and generating $\overline{\text{ALERT}}$s based on $\overline{\text{THERM}}$.

The user can also setup the ADT7463 so when the THERM pin is driven low externally the fans run at 100%. The fans run at 100% for the duration of the $\overline{\text{THERM}}$ pin being pulled low.

This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address = 0x78) to 1. This only works if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00 or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, then pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 36 for more information.

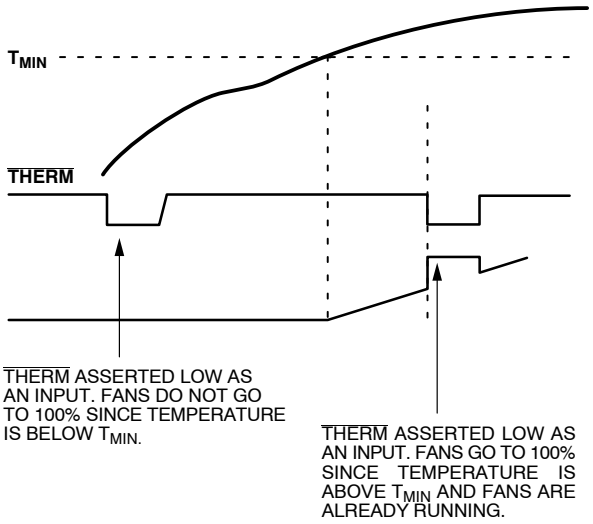


Figure 36. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7463 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input may be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium® 4 CPU and measure system performance. The $\overline{\text{THERM}}$ input may also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7463's $\overline{\text{THERM}}$ input and stopped on the negation of the pin. The timer counts $\overline{\text{THERM}}$ times cumulatively, i.e., the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8−bit $\overline{\text{THERM}}$ timer register (Reg. 0x79) is designed such that Bit 0 gets set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer gets set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms.

Figure 37 illustrates how the $\overline{\text{THERM}}$ timer behaves as the $\overline{\text{THERM}}$ input is asserted and negated. Bit 0 gets set on the first $\overline{\text{THERM}}$ assertion detected. This bit remains set until such time as the cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms. At this time, Bit 1 of the $\overline{\text{THERM}}$ timer gets set, and Bit 0 is cleared. Bit 0 now reflects timer readings with a resolution of 22.76 ms.

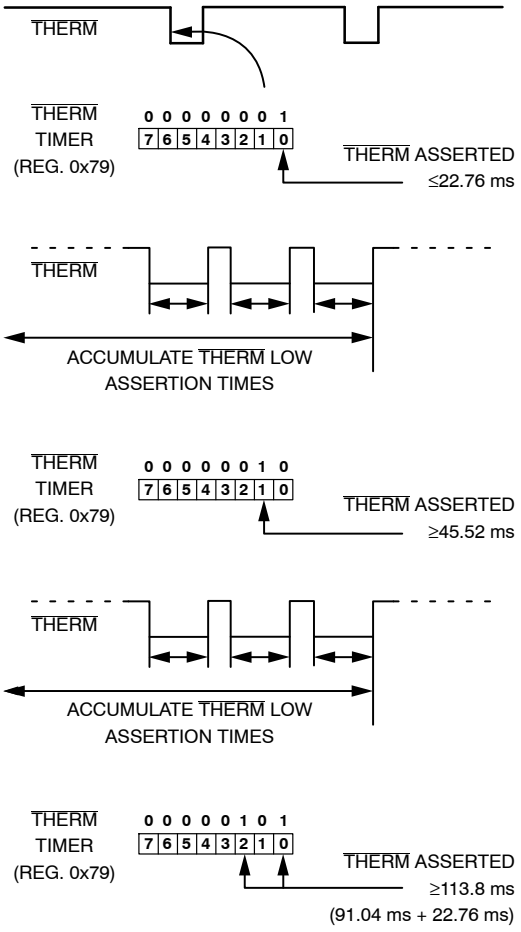


Figure 37. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

- After a THERM timer read (Reg. 0x79):
  1. The contents of the timer get cleared on read.
  2. The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming the THERM limit has been exceeded).
- If the THERM timer is read during a THERM assertion, then the following will happen:
  1. The contents of the timer are cleared.
  2. Bit 0 of the THERM timer is set to 1 (since a THERM assertion is occurring).
  3. The THERM timer increments from zero.
  4. If the THERM limit (Reg. 0x7A) = 0x00, then the F4P bit gets set.

Generating SMBALERT Interrupts from THERM Events

The ADT7463 can generate SMBALERTs when a programmable THERM limit has been exceeded. This allows the systems designer to ignore brief, infrequent THERM assertions, while capturing longer THERM events. Register 0x7A is the THERM Limit Register. This 8−bit register allows a limit from 0 seconds (first THERM assertion) to 5.825 seconds to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM limit register. If the THERM timer value exceeds the THERM limit value, then the F4P bit (Bit 5) of Status Register 2 gets set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 still gets set if the THERM limit is exceeded.

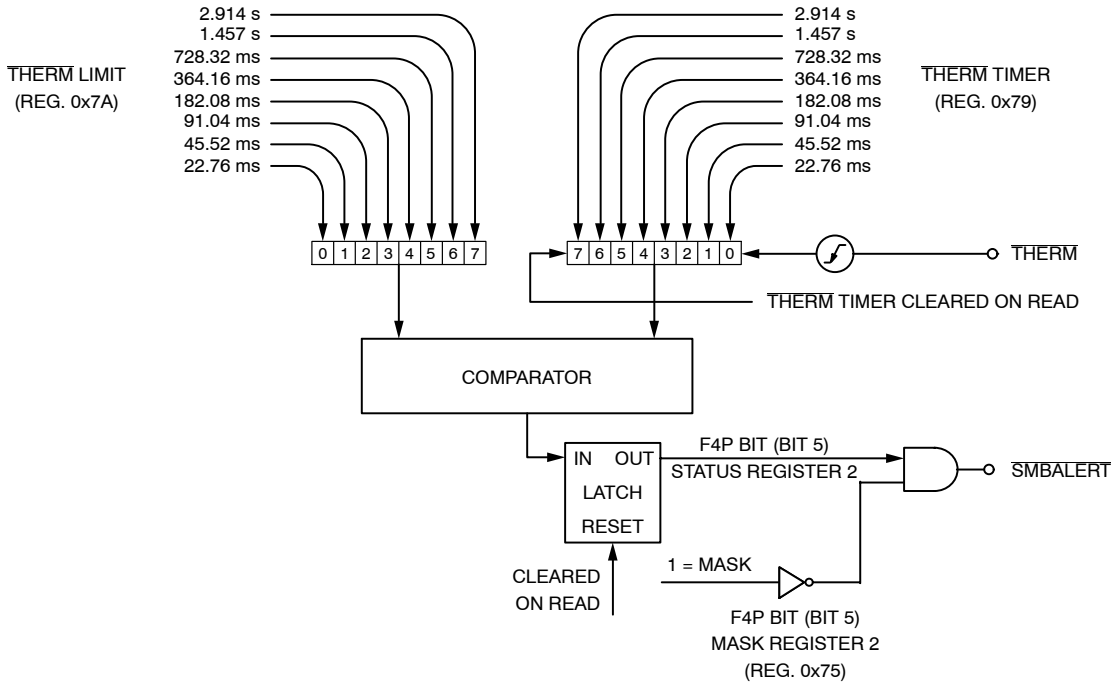


Figure 38. Functional Diagram of the ADT7463 THERM Monitoring Circuitry