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ADT7467

dbCOOL Remote Thermal Monitor and Fan Controller

The ADT7467 dbCOOL controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7467 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7467 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Controls and Monitors up to 4 Fans
- High and Low Frequency Fan Drive Signal
- 1 On-chip and 2 Remote Temperature Sensors
- Series Resistance Cancellation on the Remote Channel
- Extended Temperature Measurement Range, up to 191°C
- Dynamic T_{MIN} Control Mode Intelligently Optimizes System Acoustics
- Automatic Fan Speed Control Mode Manages System Cooling based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 2-wire, 3-wire, and 4-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- This Device is Pb-Free and is RoHS Compliant*
- Halide-Free Packages are Available

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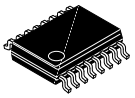
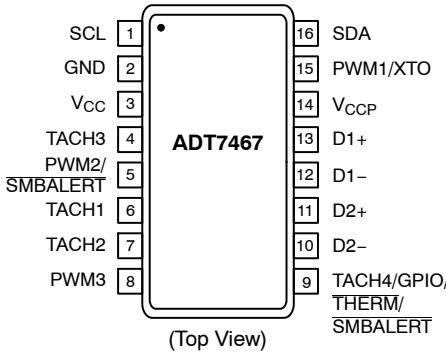


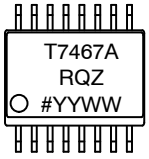
QSOP−16
CASE 492

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM



T7467ARQZ	= Specific Device Code
#	= Pb-Free Package
YY	= Date Code
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 70 of this data sheet.

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

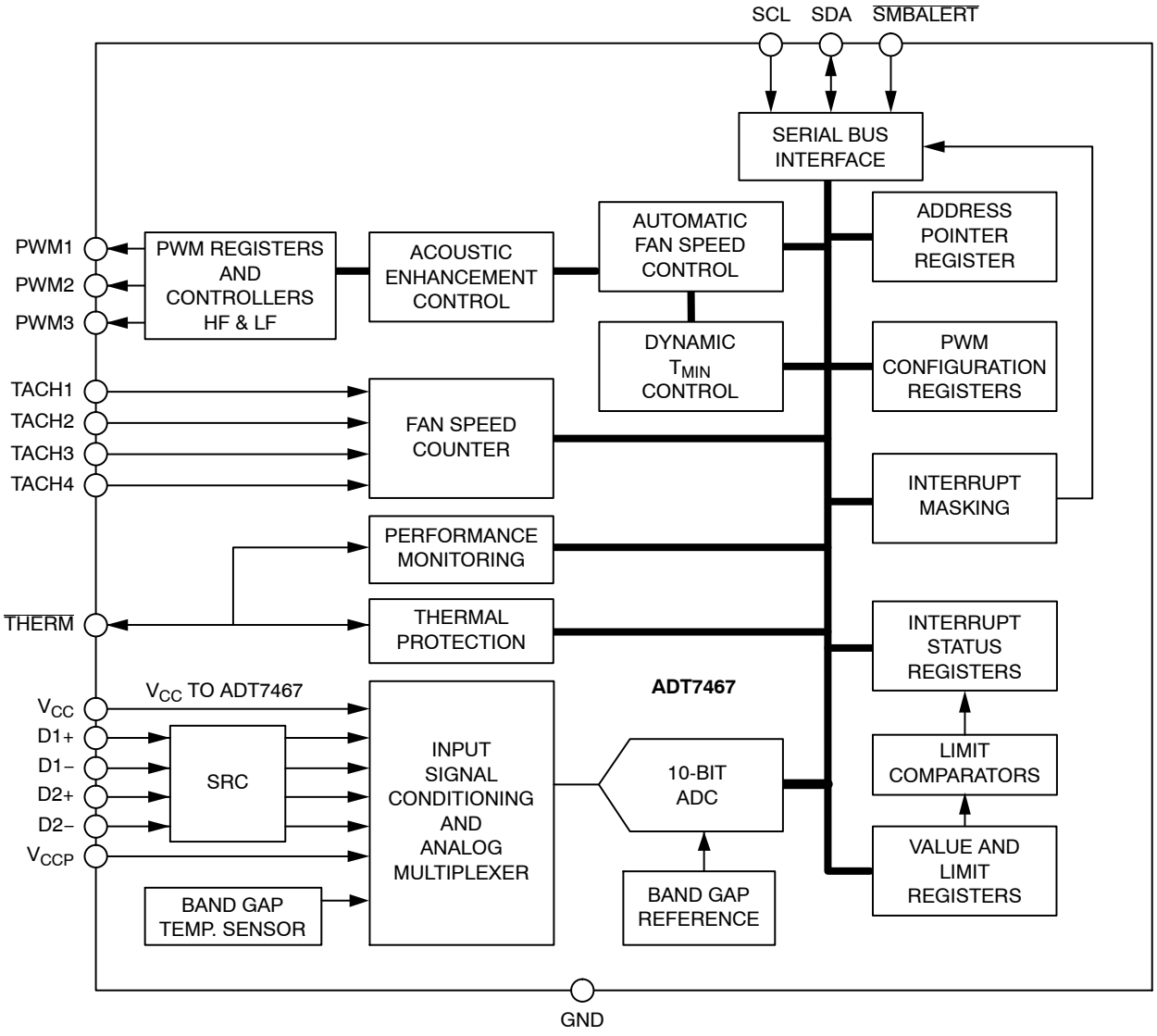


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	5.5	V
Voltage on Any Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature For Pb-Free Models Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1,000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

WARNING: Electrostatic Sensitive Device − Do not open packages or handle except at a static-free workstation.

Table 2. PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7467.
3	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7467 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans (low frequency mode only).
5	PWM2 $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control the speed of Fan 2. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans (low frequency mode only).
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans (low frequency mode only).
8	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pull-up. Can be configured as a high or low frequency drive.
9	TACH4 GPIO $\overline{\text{THERM}}$ $\overline{\text{SMBALERT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans (low frequency mode only). General-Purpose Open-Drain Digital I/O. Alternatively, the pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin, which can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, the pin can be connected to the $\overline{\text{PROCHOT}}$ output of an Intel® Pentium® 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 kΩ typical pull-up. Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pull-up.

Table 3. ELECTRICAL SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		3.0	3.3	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	– –	– –	3 20	mA μA
TEMPERATURE-TO-DIGITAL CONVERTER					
Local Sensor Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +100°C −40°C ≤ T_A ≤ +120°C	– −3.5 −4	– – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C
Remote Diode Sensor Accuracy	0°C ≤ T_A ≤ 70°C; 0°C ≤ T_D ≤ 120°C 0°C ≤ T_A ≤ 105°C; 0°C ≤ T_D ≤ 120°C −40°C ≤ T_A ≤ +120°C; 0°C ≤ T_D ≤ +120°C	– −3.5 −4.5	±0.5 – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C
Remote Sensor Source Current	First Current Second Current Third Current	– – –	6 36 96	– – –	μA
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error (TUE)		–	–	±1.5	%
Differential Nonlinearity (DNL)	8 Bits	–	–	±1	LSB
Power Supply Sensitivity		–	±0.1	–	%/V
Conversion Time (Voltage Input)	Averaging Enabled	–	11	–	ms
Conversion Time (Local Temperature)	Averaging Enabled	–	12	–	ms
Conversion Time (Remote Temperature)	Averaging Enabled	–	38	–	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	– –	145 19	– –	ms
Input Resistance	For V_{CC} Channel For All Channels other than V_{CC}	40 80	80 140	100 200	kΩ
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy	0°C ≤ T_A ≤ 70°C, 3.3 V −40°C ≤ T_A ≤ +120°C, 3.3 V −40°C ≤ T_A ≤ +120°C, 5.5 V	– – –	– – –	±5 ±7 ±10	%
Full-scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5000 10,000	– – – –	RPM
Internal Clock Frequency	0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3 V −40°C ≤ T_A ≤ +120°C, V_{CC} = 3.3 V	85.5 83.7	90 90	94.5 96.3	kHz
Internal Clock Frequency	−40°C ≤ T_A ≤ +120°C, V_{CC} = 5.5 V	81	90	99	kHz
OPEN-DRAIN DIGITAL OUTPUTS, PWM1 to PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA

Table 3. ELECTRICAL SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SMBus DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
Hysteresis		–	500	–	mV
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	Maximum Input Voltage	2.0 –	– –	– 5.5	V
Input Low Voltage, V_{IL}	Minimum Input Voltage	– –0.3	– –	0.8 –	V
Hysteresis		–	0.5	–	V p–p
DIGITAL INPUT LOGIC LEVELS ($\overline{THERM}$) ADTL+					
Input High Voltage, V_{IH}		–	0.75 × V_{CCP}	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	–1	–	–	μA
Input Low Current, I_{IL}	$V_{IN} = 0$	–	–	1	μA
Input Capacitance, C_{IN}		–	5	–	pF
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}		10	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
Start Setup Time, $t_{SU;\ STA}$		4.7	–	–	μs
Start Hold Time, $t_{HD;\ STA}$		4.0	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_r		–	–	1000	ns
SCL, SDA Fall Time, t_f		–	–	300	μs
Data Setup Time, $t_{SU;\ DAT}$		250	–	–	ns
Data Hold Time, $t_{HD;\ DAT}$		300	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typicals are at $T_A = 25°C$ and represent the most likely parametric norm. Logic inputs accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge and $V_{IH} = 2.0$ V for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

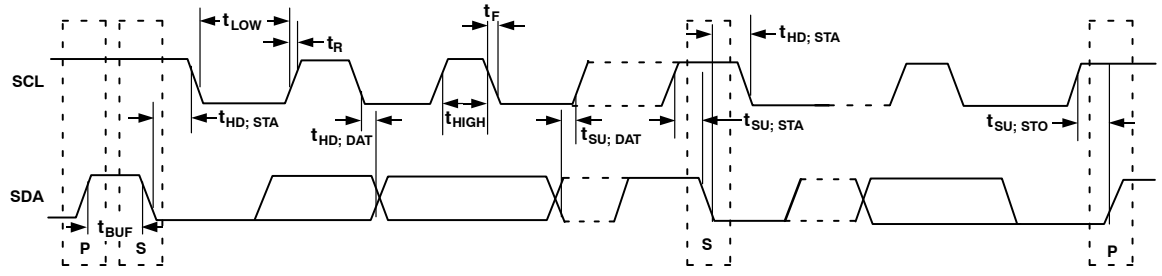


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

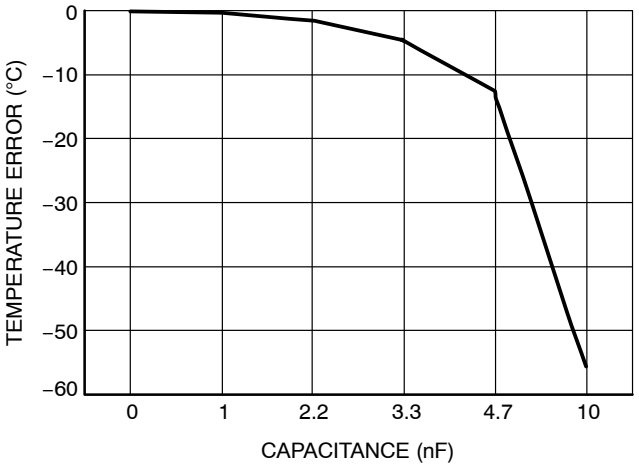


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

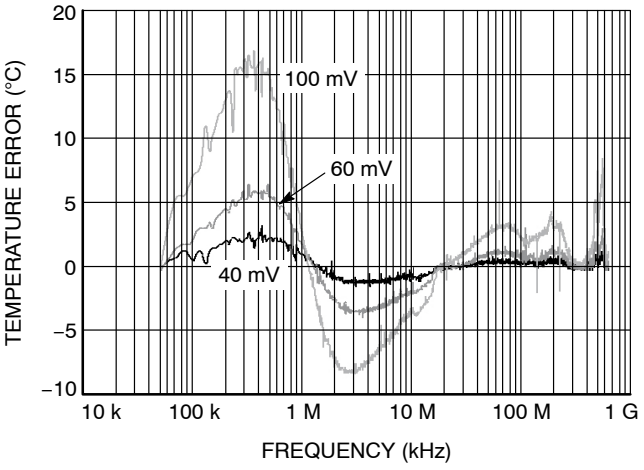


Figure 4. Remote Temperature Error vs. Common-Mode Noise Frequency

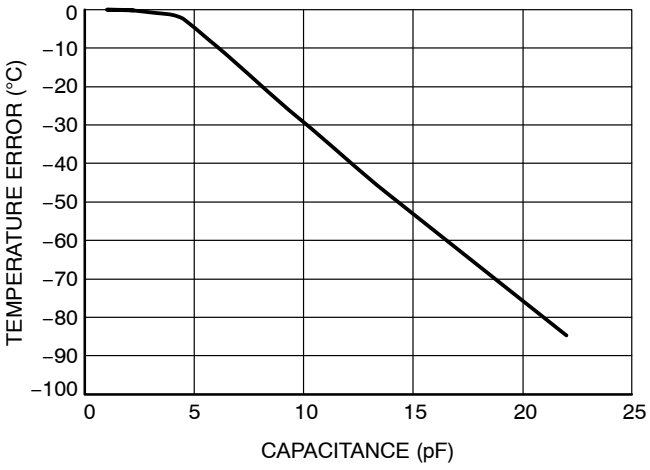


Figure 5. External Temperature Error vs. Capacitance Between D+ and D−

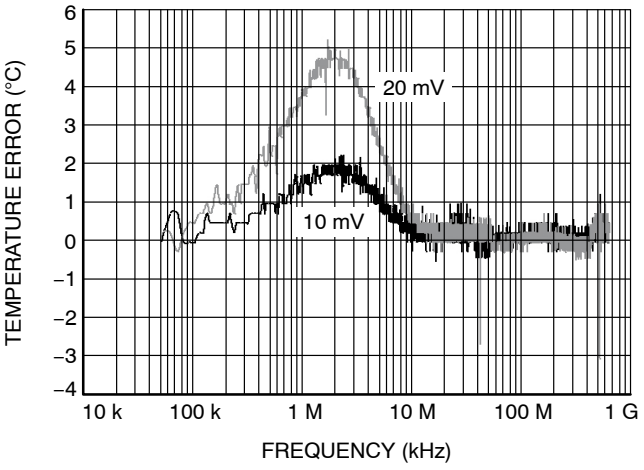


Figure 6. Remote Temperature Error vs. Differential Mode Noise Frequency

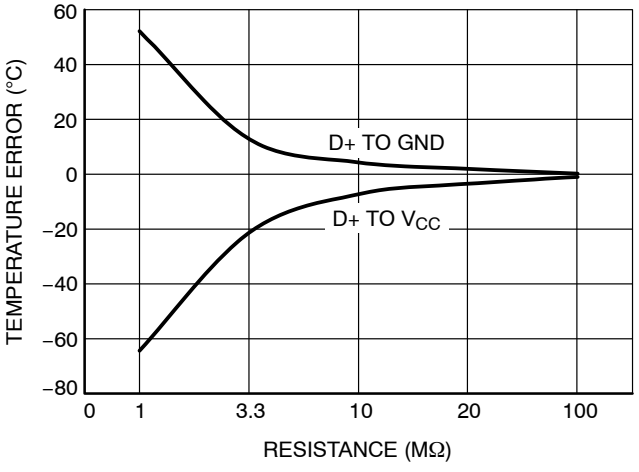


Figure 7. Temperature Error vs. PCB Resistance

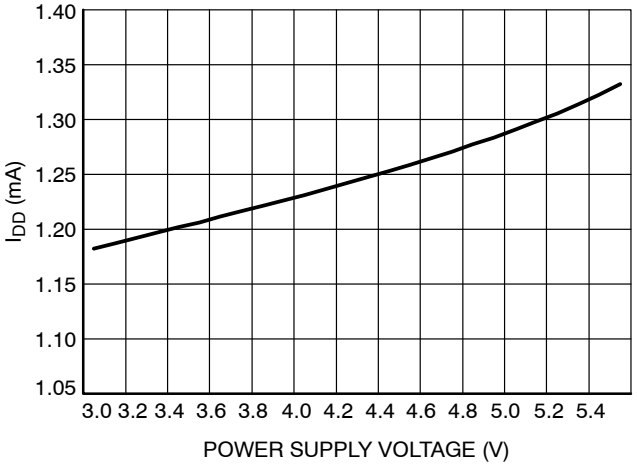


Figure 8. Normal I_{DD} vs. Power Supply

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

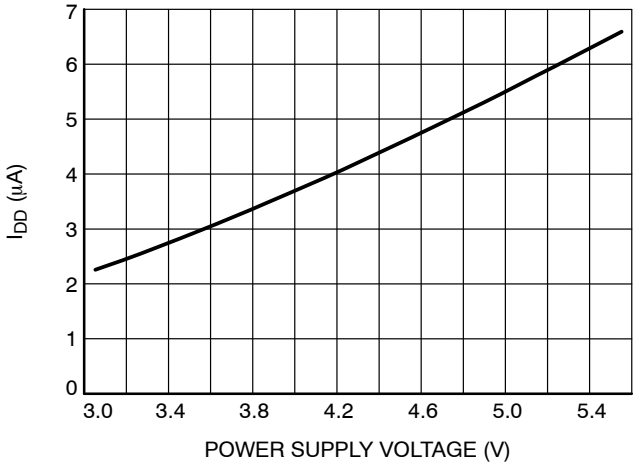


Figure 9. Shutdown I_{DD} vs. Power Supply

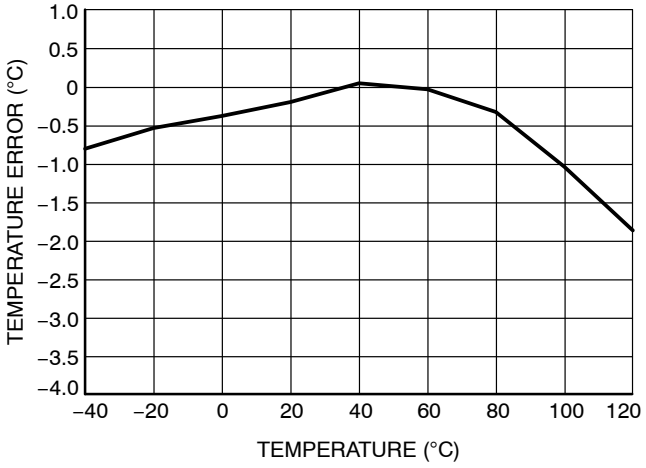


Figure 10. Internal Temperature Error vs. Temperature

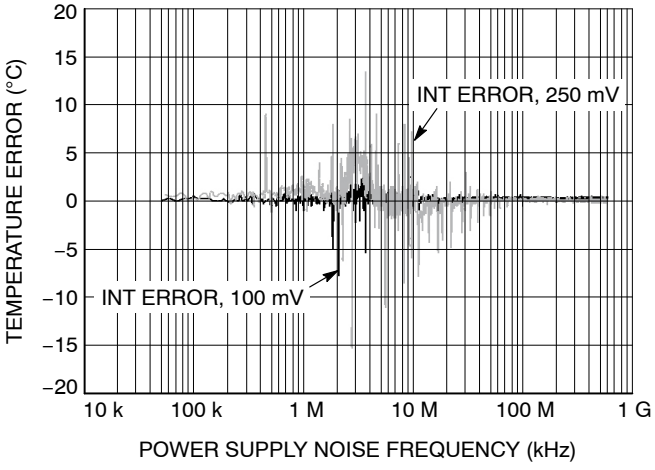


Figure 11. Internal Temperature Error vs. Power Supply Noise Frequency

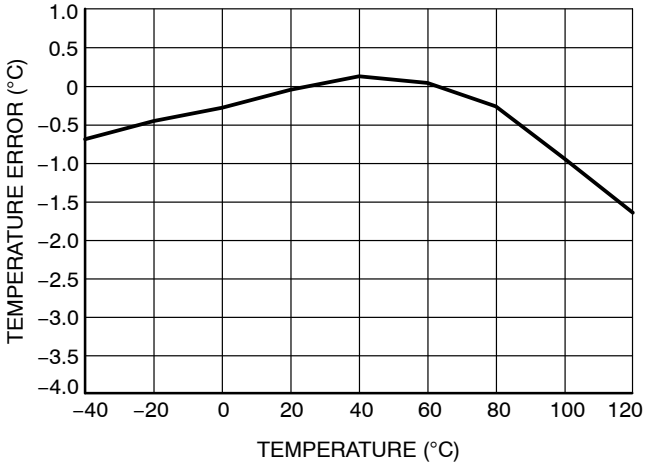


Figure 12. Remote Temperature Error vs. Temperature

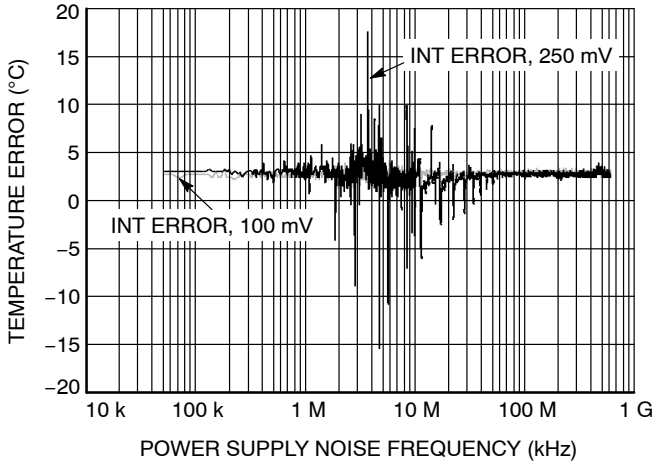


Figure 13. Remote Temperature Error vs. Power Supply Noise Frequency

Product Description

The ADT7467 is a complete thermal monitor and multiple fan controller for systems requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16) and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7467 are performed over the serial bus. In addition, one of two pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Comparison between ADT7460 and ADT7467

The ADT7467 is an upgrade from the ADT7460. The ADT7467 and ADT7460 are almost pin and register map compatible. The ADT7467 and ADT7460 have the following differences:

1. On the ADT7467, the PWM drive signals can be configured as either high frequency or low frequency drives. The low frequency option is programmable between 10 Hz and 100 Hz. The high frequency option is 22.5 kHz. On the ADT7460, only the low frequency option is available.
2. Once V_{CC} and V_{CCP} are powered up, monitoring of temperature and fan speeds is enabled on the ADT7467. If V_{CCP} is never powered up, monitoring is enabled when the first SMBus transaction with the ADT7467 is complete. On the ADT7460, the STRT bit in Configuration Register 1 must be set to enable monitoring.
3. The fans are switched off by default upon power-up of the ADT7467. On the ADT7460, the fans run at full speed upon power-up.
   Fail-safe cooling is provided on the ADT7467. If the measured temperature exceeds the $\overline{\text{THERM}}$ limit (100°C), the fans run at full speed.
   Fail-safe cooling is also provided 4.6 sec after V_{CCP} is powered up. The fans operate at full speed if the ADT7467 has not been addressed via the SMBus within 4.6 sec of when the V_{CCP} is powered up. This protects the system in the event that the SMBus fails. The ADT7467 can be programmed at any time, and it behaves as programmed. If V_{CCP} is never powered up, fail-safe cooling is effectively disabled. If V_{CCP} is disabled, writing to the ADT7467 at any time causes the ADT7467 to operate normally.
4. Series resistance cancellation (SRC) is provided on the remote temperature channels on the ADT7467, but not on the ADT7460. SRC automatically cancels linear offset introduced by a series resistance between the thermal diode and the sensor.
5. The ADT7467 has an extended temperature measurement range. The measurement range goes from −64°C to +191°C. On the ADT7460, the measurement range is from −127°C to +127°C. This means that the ADT7467 can measure higher temperatures. The ADT7467 also includes the ADT7460 temperature range; the temperature measurement range can be switched by setting Bit 0 of Configuration Register 5.
6. The ADT7467 maximum fan speed (% duty cycle) in the automatic fan speed control loop can be programmed. The maximum fan speed is 100% duty cycle on the ADT7460 and is not programmable.
7. The offset register in the ADT7467 is programmable up to ±64°C with 0.50°C resolution. The offset register of the ADT7460 is programmable up to ±32°C with 0.25°C resolution.
8. V_{CCP} is monitored on Pin 14 of the ADT7467 and can be used to set the threshold for $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$) (2/3 of V_{CCP}). 2.5 V is monitored on Pin 14 of the ADT7460. The threshold for $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$) is set at V_{IH} = 1.7 V and V_{IL} = 0.8 V on the ADT7460.
9. On the ADT7460, Pin 14 could be reconfigured as $\overline{\text{SMBALERT}}$. This is not available on the ADT7467. $\overline{\text{SMBALERT}}$ can be enabled instead on Pin 9.
10. A GPIO can also be made available on Pin 9 on the ADT7467. This is not available on the ADT7460. Set the GPIO polarity and direction in Configuration Register 5. The GPIO status bit is Bit 5 of Status Register 2 (it is shared with TACH4 and $\overline{\text{THERM}}$ because only one can be enabled at a time).
11. The ADT7460 has three possible SMBus addresses, which are selectable using the address select and address enable pins. The ADT7467 has one SMBus address available at Address 0x2E.

Due to the inclusion of extra functionality, the register map has changed, including an additional configuration register, Configuration Register 5 at Address 0x7C.

Configuration Register 5

Bit 0: If Bit 0 is set to 1, the ADT7467, in terms of temperature, is backward compatible with the ADT7460. Measurements, including T_{MIN} calibration circuit and fan control, work in the range −127°C to +127°C. In addition, care should be taken in reprogramming the temperature limits (T_{MIN}, operating point, $\overline{\text{THERM}}$) to their desired twos complement value, because the power-on default for them is at Offset 64. The extended temperature range is −64°C to 191°C. The default is 1, which is in the −64°C to +191°C temperature range.

Bit 1 = 0 is the high frequency (22.5 kHz) fan drive signal.

Bit 1 = 1 switches the fan drive to low frequency PWM, programmable between 10 Hz and 100 Hz, the same as the ADT7460. The default is 0, or HF PWM.

Bit 2 sets the direction for the GPIO: 0 = input, 1 = output. Bit 3 sets the GPIO polarity: 0 = active low, 1 = active high.

Setting the Functionality of Pin 9

Pin 9 on the ADT7467 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 4. PIN 9 SETTINGS

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

Recommended Implementation

Configuring the ADT7467 as in Figure NO TAG allows the system designer to use the following features:

- Two PWM Outputs for Fan Control of Up to Three Fans (The Front and Rear Chassis Fans are Connected in Parallel)
- Three TACH Fan Speed Measurement Inputs
- V_{CC} Measured Internally through Pin 3
- CPU Temperature Measured Using the Remote 1 Temperature Channel
- Ambient Temperature Measured through the Remote 2 Temperature Channel
- Bidirectional $\overline{\text{THERM}}$ Pin. This Feature Allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ Monitoring and Can Function as an Overtemperature $\overline{\text{THERM}}$ Output. Alternatively, it Can be Programmed as an $\overline{\text{SMBALERT}}$ System Interrupt Output

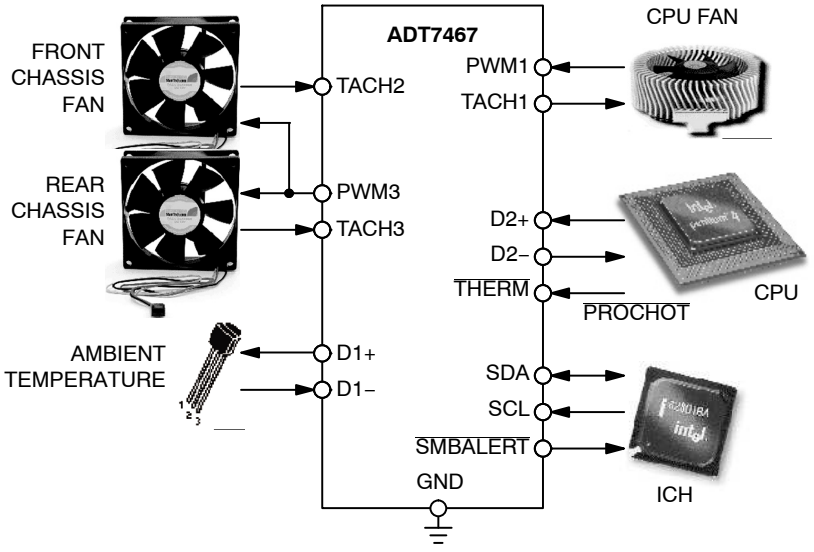


Figure 14. ADT7467 Implementation

Serial Bus Interface

On PCs and servers, control of the ADT7467 is carried out using the serial system management bus (SMBus). The ADT7467 is connected to this bus as a slave device under the control of a master controller, which is usually (but not necessarily) the ICH.

The ADT7467 has a fixed 7-bit serial bus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address (01011100 or 0x5C). Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition might be interpreted as a stop signal when the clock is high. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is only limited by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. It is not possible to mix a read and a write in one operation, however, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7467, write operations contain either one or two bytes, and read operations contain one byte. To write data to a device data register or read data from it, the address pointer register must first be set. The first byte of a write operation always contains an address, which is stored in the address pointer register, and the second byte, if there is a second byte, is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 15. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register, and the second data byte is the data written to that internal data register.

When reading data from a register, there are two possibilities:

1. If the address pointer register value of the ADT7467 is unknown or not the desired value, it must be set to the correct value before data can be read from the desired data register. This is achieved by writing a data byte containing the register address to the ADT7467. This is shown in Figure 16. A read operation is then performed consisting of the serial bus address and the R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 17.
2. If the address pointer register is known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 17.

If the address pointer register is already at the correct value, it is possible to read a data byte from the data register without first writing to the address pointer register. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7467 also supports the read byte protocol. (See the Intel *System Management Bus Specifications Rev. 2* for more information.)

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

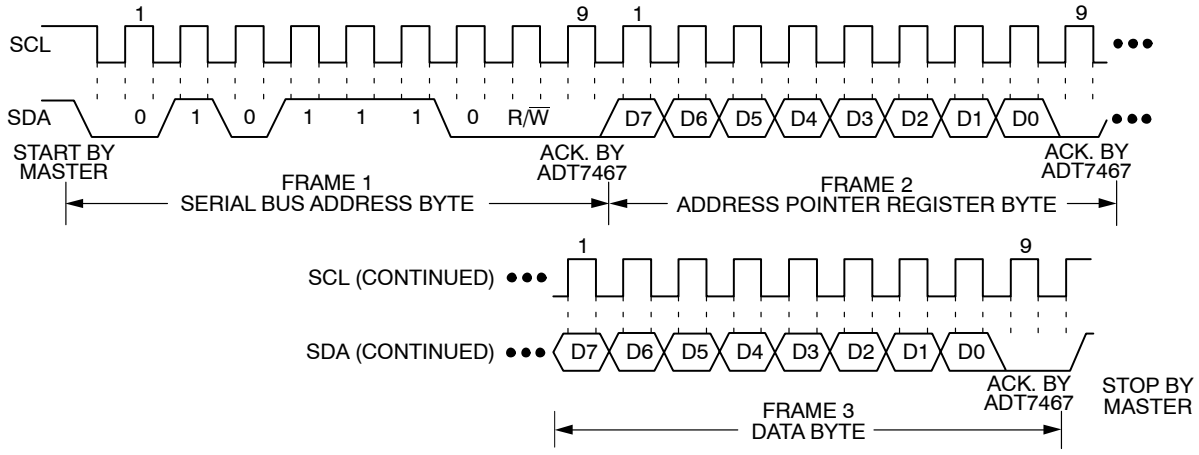


Figure 15. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

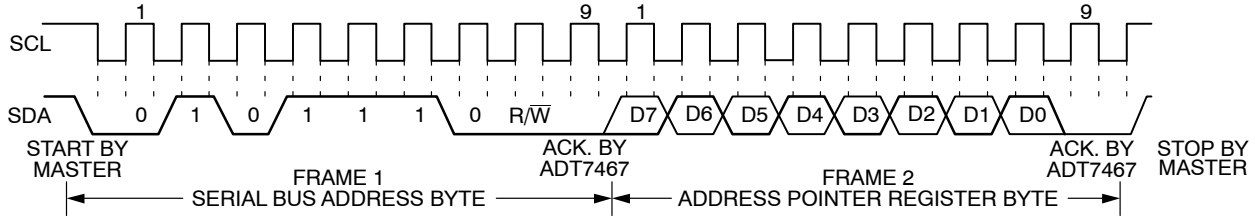


Figure 16. Writing to the Address Pointer Register Only

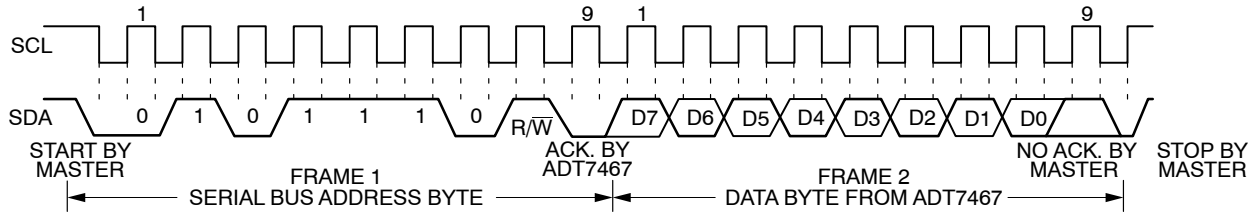


Figure 17. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7467 are discussed here. The following abbreviations are used in Figure 18 through Figure 20:

S = start
P = stop
R = read
W = write
A = acknowledge
$\overline{A}$ = no acknowledge

The ADT7467 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7467, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is illustrated in Figure 18.

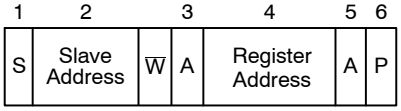


Figure 18. Setting a Register Address for Subsequent Read

If the master is required to read data from the register directly after setting up the address, it can assert a repeat start condition immediately after the final acknowledge and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

This operation is illustrated in Figure 19.

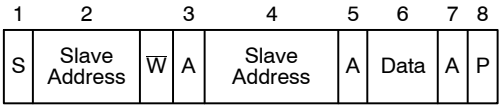


Figure 19. Single Byte Write to a Register

Read Operations

The ADT7467 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts a no acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7467, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 20.

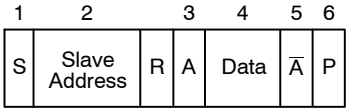


Figure 20. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the

device is now known and can be interrogated in the usual way.

4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7467 has responded to the alert response address, the master must read the status registers. The $\overline{\text{SMBALERT}}$ is cleared only if the error condition is absent.

SMBus Timeout

The ADT7467 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7467 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus in anticipation of receiving data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (0x40)

<6> TODIS = 0, SMBus timeout enabled (default)

<6> TODIS = 1, SMBus timeout disabled

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter, which has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hexadecimal) for the nominal input voltage and, therefore, has adequate headroom to deal with overvoltages.

Voltage Measurement Input

The ADT7467 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). Setting Bit 7 of Configuration Register 1 (0x40) allows a 5 V supply to power the ADT7467 and be measured without overranging the V_{CC} measurement channel. The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 21. The input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first-order low-pass filter that gives the input immunity to high frequency noise.

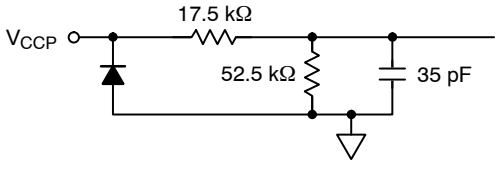


Figure 21. Structure of Analog Inputs

Voltage Measurement Registers

Register 0x21 V_{CCP} reading = 0x00 default

Register 0x22 V_{CC} reading = 0x00 default

V_{CCP} Limit Registers

Associated with the V_{CCP} and V_{CC} measurement channels is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Register 0x46 V_{CCP} low limit = 0x00 default

Register 0x47 V_{CCP} high limit = 0xFF default

Register 0x48 V_{CC} low limit = 0x00 default

Register 0x49 V_{CC} high limit = 0xFF default

Table 6 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings are made internally, the results of which are averaged and then placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This produces a reading that is 16 times faster (0.7 ms), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7467 into single−channel ADC conversion mode. In this mode, the ADT7467 can be made to read a single voltage channel only. If the internal ADT7467 clock is used, the selected input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 5. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits <7:5>, Register 0x55	Channel Selected
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

<4> = 1, Averaging Off

<5> = 1, Bypass Input Attenuators

<6> = 1, Single-channel Conversion Mode

TACH1 Minimum High Byte (0x55)

<7:5> Selects ADC Channel for Single-channel Convert Mode

Table 6. 10-BIT ANALOG-TO-DIGITAL OUTPUT CODE VS. V_{IN}

Input Voltage			A/D Output	
V_{CC} (5 V_{IN})	V_{CC} (3.3 V_{IN})	V_{CCP}	Decimal	Binary (10 Bits)
<0.0065	<0.0042	<0.00293	0	00000000 00
0.0065 to 0.0130	0.0042 to 0.0085	0.0293 to 0.0058	1	00000000 01
0.0130 to 0.0195	0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0195 to 0.0260	0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0260 to 0.0325	0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0325 to 0.0390	0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0390 to 0.0455	0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0455 to 0.0521	0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0521 to 0.0586	0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
			…	
1.6675 to 1.6740	1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
			…	
3.330 to 3.3415	2.200 to 2.2042	1.5000 to 1.5029	512 (1/2 scale)	10000000 00
			…	
5.0025 to 5.0090	3.300 to 3.3042	2.2500 to 2.2529	768 (3/4 scale)	11000000 00
			…	
6.5983 to 6.6048	4.3527 to 4.3570	2.9677 to 2.9707	1013	11111101 01
6.6048 to 6.6113	4.3570 to 4.3613	2.9707 to 2.9736	1014	11111101 10
6.6113 to 6.6178	4.3613 to 4.3656	2.9736 to 2.9765	1015	11111101 11
6.6178 to 6.6244	4.3656 to 4.3699	2.9765 to 2.9794	1016	11111110 00
6.6244 to 6.6309	4.3699 to 4.3742	2.9794 to 2.9824	1017	11111110 01
6.6309 to 6.6374	4.3742 to 4.3785	2.9824 to 2.9853	1018	11111110 10
6.6374 to 6.4390	4.3785 to 4.3828	2.9853 to 2.9882	1019	11111110 11
6.6439 to 6.6504	4.3828 to 4.3871	2.9882 to 2.9912	1020	11111111 00
6.6504 to 6.6569	4.3871 to 4.3914	2.9912 to 2.9941	1021	11111111 01
6.6569 to 6.6634	4.3914 to 4.3957	2.9941 to 2.9970	1022	11111111 10
>6.6634	>4.3957	>2.9970	1023	11111111 11

Temperature Measurement

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from each device.

The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 23 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (the recommended maximum value is 1,000 pF). However, a better option in noisy environments is to add a filter as described in the Noise Filtering section.

Local Temperature Measurement

The ADT7467 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 7 and Table 8. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C (or −64°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, preventing local temperature measurements outside the ADT7467 operating temperature range.

Remote Temperature Measurement

The ADT7467 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from each device and thus requires individual calibration; therefore, the technique is unsuitable for mass production. The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. This is given by:

$$\Delta V_{BE} = kT/q \times \ln(N) \quad \text{(eq. 1)}$$

where:

k is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvins.
N is the ratio of the two currents.

Figure 22 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

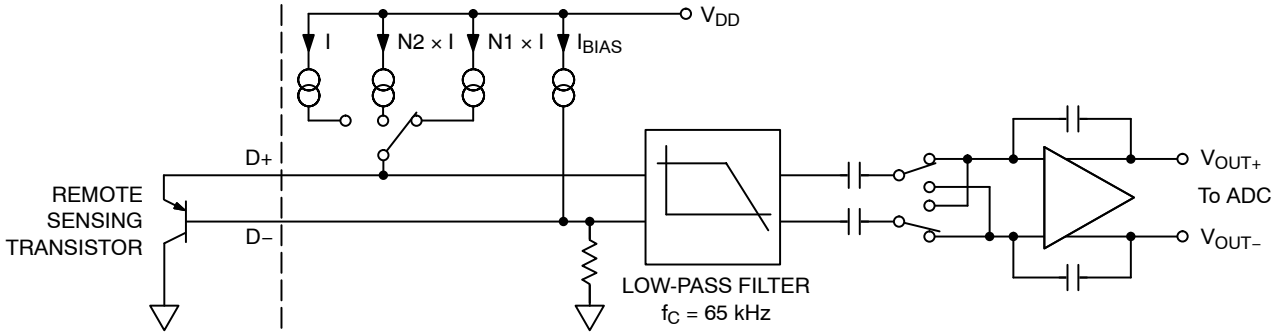


Figure 22. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter is connected to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base is connected to the D+ input. Figure 24 and Figure 25 show how to connect the ADT7467 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. Shown in Figure 22, N1 × I and N2 × I are different multiples of the current I. The currents through the temperature diode are switched between I and N1 × I, resulting in ΔV_{BE1}; then

they are switched between I and N2 × I, resulting in ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then sent to a chopper-stabilized amplifier that amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10-bit twos complement format, as listed in Table 7. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This produces temperature readings with a resolution of 0.25°C.

Series Resistance Cancellation

Parasitic resistance to the ADT7467 D+ and D− inputs (seen in series with the remote diode) is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per 1 Ω of parasitic resistance in series with the remote diode.

The ADT7467 automatically cancels the effect of this series resistance on the temperature reading, providing a more accurate result without the need for user characterization of this resistance. The ADT7467 is designed to automatically cancel, typically up to 3 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the Noise Filtering section for details.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice involved placing a capacitor across the D+ and D− pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF. A capacitor of this value reduces the noise but does not eliminate it, making use of the sensor difficult in a very noisy environment.

The ADT7467 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the device. The effect of filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7467 and the remote temperature sensor to operate in noisy environments. Figure 23 shows a low-pass R-C-R filter with the following values:

R = 100 Ω, C = 1 nF

This filtering reduces both common-mode noise and differential noise.

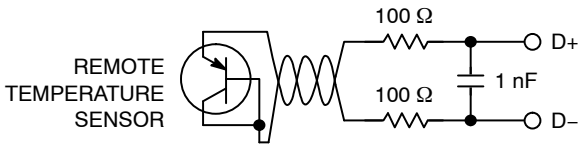


Figure 23. Filter Between Remote Sensor and ADT7467

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7467 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7467 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T (°C), when using a transistor whose n_f does not equal 1.008. See the processor's data sheet for the n_f values.
  $\Delta T = (n_f - 1.008)/1.008 \times (273.15\ K + T)$
- To correct for this error, the user can write the ΔT value to the offset register, and the ADT7467 automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7467, I_{HIGH}, is 96 μA, and the low level current, I_{LOW}, is 6 μA. If the ADT7467 current levels do not match the current levels specified by the CPU manufacturer, it may be necessary to remove an offset. The CPU's data sheet should provide information relating to n_f to compensate for differences. An offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7467, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage is greater than 0.25 V at 6 μA with the highest operating temperature.
- Base-emitter voltage is less than 0.95 V at 100 μA with the lowest operating temperature.
- Base resistance is less than 100 Ω.
- There is a small variation in h_{FE} (for example, 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors such as 2N3904, 2N3906, or equivalents in SOT−23 packages are suitable devices to use.

Table 7. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−128°C	1000 0000 **00**
−125°C	1000 0011 **00**
−100°C	1001 1100 **00**
−75°C	1011 0101 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 8. OFFSET 64 TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−64°C	0000 0000 **00**
−1°C	0011 1111 **00**
0°C	0100 0000 **00**
+1°C	0100 0001 **00**
+10°C	0100 1010 **00**
+25°C	0101 1001 **00**
+50°C	0111 0010 **00**
+75°C	1000 1001 **00**
+100°C	1010 0100 **00**
+125°C	1011 1101 **00**
+191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in Extended Resolution Register 2 (0x77) with 0.25°C resolution.

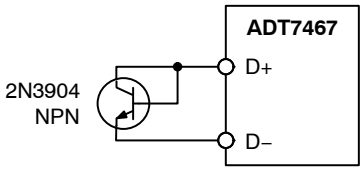


Figure 24. Measuring Temperature by Using an NPN Transistor

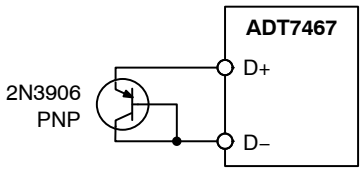


Figure 25. Measuring Temperature by Using a PNP Transistor

Nulling Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors may still be attributed to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7467 has temperature offset registers at Address 0x70 and Address 0x72 for the Remote 1 and Remote 2 temperature channels, respectively. By performing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it using the offset registers. The offset registers automatically add an Offset 64/twos complement 8-bit reading to every temperature measurement. The LSBs add 0.5°C offset to the temperature reading; therefore, the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of 0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Temperature Offset Registers

Register 0x70 Remote 1 Temperature Iffset = 0x00 (0°C Default)

Register 0x71 Local Temperature Offset = 0x00 (0°C Default)

Register 0x72 Remote 2 Temperature Offset = 0x00 (0°C Default)

ADT7460/ADT7467 Backwards-compatible Mode

By setting Bit 1 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature value registers (Register 0x25, Register 0x26, and Register 0x27) in twos complement format in the range −128°C to +127°C. (The ADT7468 makes calculations based on the Offset 64 extended range and clamps the results if necessary.) The temperature limits must be reprogrammed in twos complement format. If a twos complement

temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, whereas the fault condition is represented by −64°C = 0000 0000 in the extended temperature range (−64°C to +191°C).

Table 9. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	0x01
0x26	Local Temperature	0x01
0x27	Remote 2 Temperature	0x01
0x77	Extended Resolution 2	0x00

Table 10. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Temperature Measurement Limit Registers

High and low limit registers are associated with each temperature measurement channel. Exceeding the programmed high or low limit sets the appropriate status bit and can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 11. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7467

It is important to note that temperature can be read from the ADT7467 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (0x77) should be read first. Then all temperature reading registers freeze until all temperature reading registers are read. This prevents updating of an MSB reading while its two LSBs are read and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings are made internally, the results of which are averaged and then placed into the value register. Sometimes it is necessary to perform a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off.

Table 12. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time
Voltage Channels	0.7 ms
Remote Temperature 1	7 ms
Remote Temperature 2	7 ms
Local Temperature	1.3 ms

Table 13. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time
Voltage Channels	11 ms
Remote Temperature	39 ms
Local Temperature	12 ms

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7467 into single-channel ADC conversion mode. In this mode, users can read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 14. CHANNEL SELECTION

Bits <7:5>, Register 0x55	Channel Selected
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

<4> = 1, Averaging Off

<6> = 1, Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

<7:5> Selects ADC Channel for Single-channel Convert Mode

Overtemperature Events

Overtemperature events on a temperature channel can be automatically detected and dealt with in automatic fan speed control mode. Register 0x6A to Register 0x6C contain the $\overline{\text{THERM}}$ temperature limits. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (0x38, 0x39, 0x3A); therefore, fans run at the fastest speed allowed and continue running at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. (This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2, Register 0x78.) The hysteresis value for that $\overline{\text{THERM}}$ temperature limit is the value programmed into Register 0x6D and Register 0x6E (hysteresis registers). The default hysteresis value is 4°C.

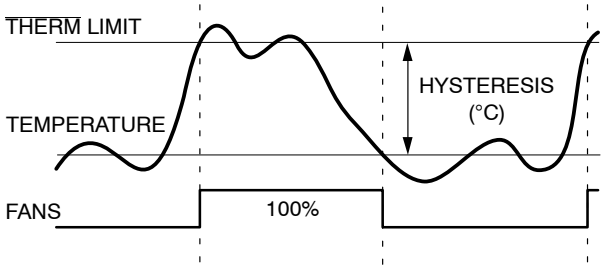


Figure 26. $\overline{\text{THERM}}$ Temperature Limit Operation

Limits, Status Registers, and Interrupts

Limit Values

High and low limits are associated with each measurement channel on the ADT7467. These limits form the basis of system-status monitoring in that a status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-bit Limits

The following is a list of 8-bit limits on the ADT7467.

Table 15. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF

Table 16. $\overline{\text{THERM}}$ TIMER LIMIT REGISTERS

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Timer Limit	0x00

Table 17. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0xA4
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0xA4
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0xA4

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because slow or stalled fans are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is measured, exceeding the limit indicates a slow or stalled fan.

Table 18. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits are programmed, the ADT7467 can be enabled for monitoring. The ADT7467 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently, depending on whether the measured value is being compared to a high or low limit.

High limit: > comparison performed

Low limit: ≤ comparison performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). By default, the ADT7463 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time to monitor all analog inputs is normally not of interest because the most recently measured value of an input can be read at any time.

For applications where the monitoring cycle time is important, it can be calculated easily. The total number of channels measured is

- One Dedicated Supply Voltage Input (V_{CCP})
- One Supply Voltage (V_{CC} Pin)
- One Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round-robin conversions. The total monitoring cycle time for averaged voltage and temperature monitoring is 145 ms. The total monitoring cycle time for voltage and temperature monitoring with averaging disabled is 19 ms. The ADT7467 is a derivative of the ADT7468. As a result, the total conversion time for the ADT7467 and ADT7468 are the same, even though the ADT7467 has less monitored channels.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out of limit, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), 1 means that an out-of-limit event has been flagged in Interrupt Status Register 2. This means that the user also should read Interrupt Status Register 2. Alternatively, Pin 5 or Pin 9 can be configured as an $\overline{\text{SMBALERT}}$ output. This hardware interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit if the error condition that caused the interrupt is absent. Status register bits are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set until read, even if the event that caused it is absent. The only way to clear the status bit is to read the status register after the event is absent. Interrupt mask registers (0x74 and 0x75) allow masking of individual interrupt sources to prevent an $\overline{\text{SMBALERT}}$. However, if a masked interrupt source goes out of limit, its associated status bit is set in the interrupt status registers.

Table 19. STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1 denotes a bit in Status Register 2 is set and Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 temperature high or low limit has been exceeded.
5	LT	1 indicates that the Local temperature high or low limit has been exceeded.
4	R1T	1 indicates that the Remote 1 temperature high or low limit has been exceeded.
2	V_{CC}	1 indicates that the V_{CC} high or low limit has been exceeded.
1	V_{CCP}	1 indicates that the V_{CCP} high or low limit has been exceeded.

Table 20. STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D2+/D2− inputs.
5	F4P	1 indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ timer limit has been exceeded if the $\overline{\text{THERM}}$ timer function is used.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.

Interrupts

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7467 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

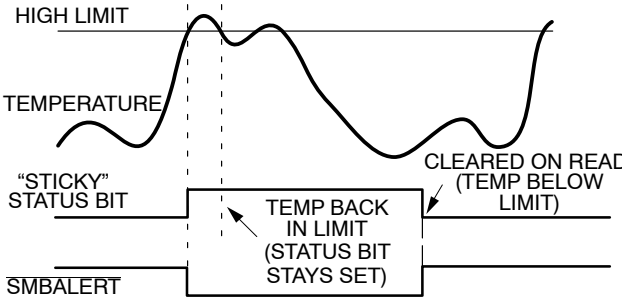


Figure 27. SMBALERT and Status Bit Behavior

Figure 27 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low both for the duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up with servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Register 0x74 and Register 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 28.

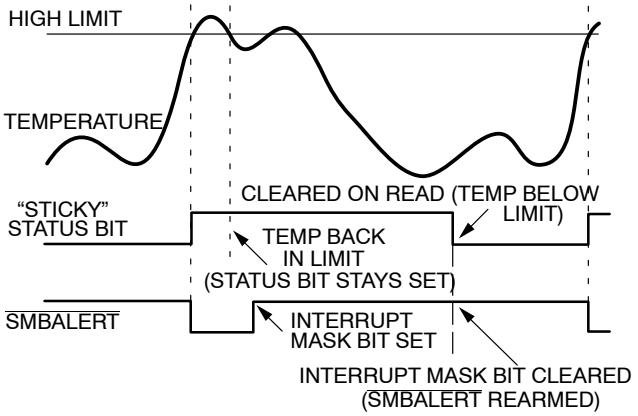


Figure 28. Effect of Masking the Interrupt Source on SMBALERT Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Address 0x74 and Address 0x75, respectively, and allow individual interrupt sources to be masked to prevent SMBALERT interrupts. Note that masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

Table 21. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature channel.
5	LT	1 masks SMBALERT for local temperature channel.
4	R1T	1 masks SMBALERT for Remote 1 temperature channel.
2	V_{CC}	1 masks SMBALERT for the V_{CC} channel.
0	V_{CCP}	1 masks SMBALERT for the V_{CCP} channel.

Table 22. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).

Enabling the SMBALERT Interrupt Output

The SMBALERT interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Table 23. CONFIGURING PIN 5 AS SMBALERT OUTPUT

Register	Bit Setting
Configuration Register 3 (0x78)	<0> ALERT Enable = 1

Assigning THERM Functionality to a Pin

Pin 9 on the ADT7467 has four possible functions: SMBALERT, THERM, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 24. CONFIGURING PIN 9

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

Once Pin 9 is configured as $\overline{\text{THERM}}$, it must be enabled (Bit 1, Configuration Register 3 at Address 0x78).

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the ADT7467 so that when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This only works if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, externally pulling $\overline{\text{THERM}}$ low has no effect. See Figure 29 for more information.

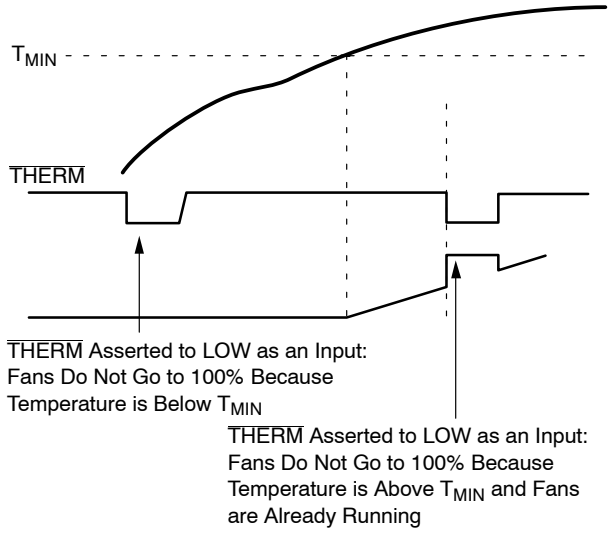


Figure 29. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7467 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium® 4 CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is deasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared upon a read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer register (0x79) is designed such that Bit 0 is set to 1 upon the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 30).

It is important to be aware of the following when using the $\overline{\text{THERM}}$ timer.

After a $\overline{\text{THERM}}$ timer is read (Register 0x79), the following occurs:

- The contents of the timer are cleared upon a read.
- The F4P bit (Bit 5) of Interrupt Status Register 2 must be cleared, assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded.

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, the following occurs:

- The contents of the timer are cleared.
- Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 because a $\overline{\text{THERM}}$ assertion is occurring.
- The $\overline{\text{THERM}}$ timer increments from 0.
- If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) is 0x00, the F4P bit is set.

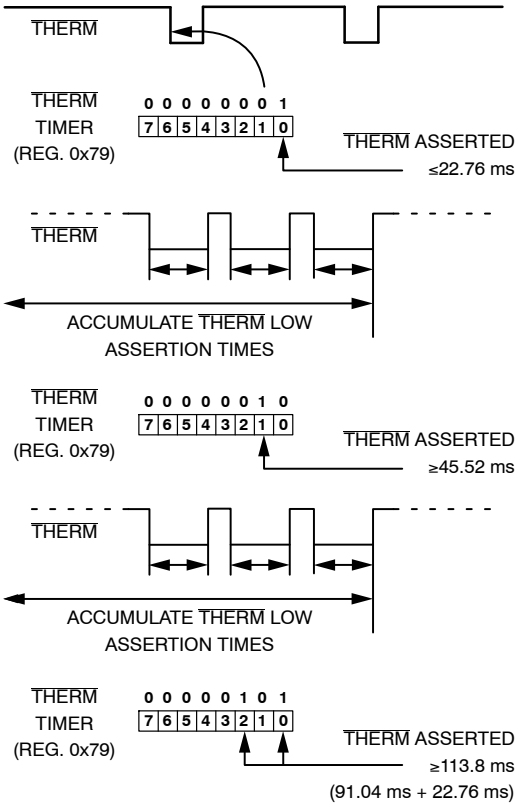


Figure 30. Understanding the $\overline{\text{THERM}}$ Timer

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7467 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 sec (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit, the F4P bit (Bit 5) of Interrupt Status Register 2 is set and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks SMBALERT if this bit is set to 1; however, the F4P bit of Interrupt Status Register 2 remains set if the THERM timer limit is exceeded.

Figure 31 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes SMBALERT to be generated upon the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.

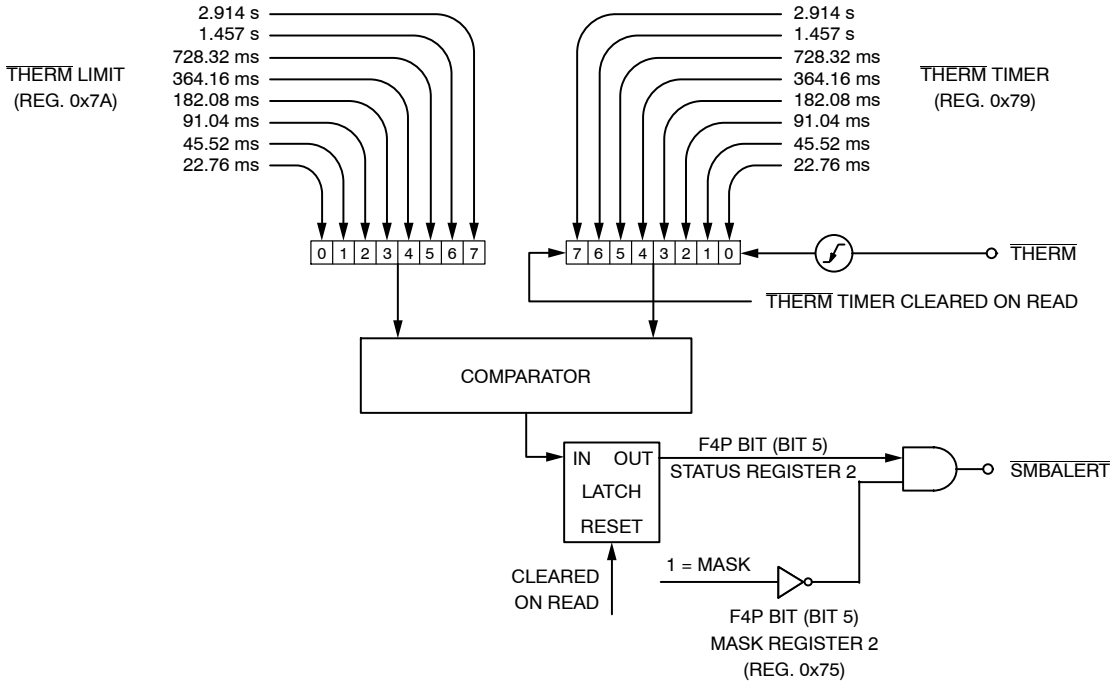


Figure 31. Functional Diagram of THERM Monitoring Circuitry

Configuring THERM Behavior

1. Configure the relevant pin as the THERM timer input:
   Setting Bit 1 (THERM timer enable) of Configuration Register 3 (0x78) enables the THERM timer monitoring functionality. This is disabled on Pin 9 by default.
   Setting Bit 0 and Bit 1 (Pin 9 Func) of Configuration Register 4 (0x7D) enables THERM timer/output functionality on Pin 9 (Bit 1, THERM, of Configuration Register 3 must also be set). Pin 9 can also be used as TACH4.
2. Select the desired fan behavior for THERM timer events:
   Assuming that the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (0x78) causes all fans to run at 100% duty cycle whenever THERM is asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by THERM events. If the fans are not already running when THERM is asserted, the fans do not run to full speed.
3. Select whether THERM timer events should generate SMBALERT interrupts:
   When set, Bit 5 (F4P) of Mask Register 2 (0x75) masks SMBALERTs when the THERM timer limit value is exceeded. This bit should be cleared if SMBALERT based on THERM events are required.
4. Select a suitable THERM limit value:
   This value determines whether an SMBALERT is generated upon the first THERM assertion, or if only a cumulative THERM assertion time limit is exceeded. A value of 0x00 causes an SMBALERT to be generated upon the first THERM assertion.
5. Select a THERM monitoring time:
   This value specifies how often OS or BIOS level software checks the THERM timer. For example,

BIOS could read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >2.914 sec in Hour 3, this can indicate that system performance is degrading significantly, because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

Alternatively, OS or BIOS level software can timestamp when the system is powered on. If an $\overline{\text{SMBALERT}}$ is generated because the $\overline{\text{THERM}}$ timer limit has been exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ timer limit. For example, if it takes one week for a $\overline{\text{THERM}}$ timer limit of 2.914 sec to be exceeded and the next time it takes only 1 hour, this is an indication of a serious degradation in system performance.

Configuring the $\overline{\text{THERM}}$ Pin as an Output

In addition to monitoring $\overline{\text{THERM}}$ as an input, the ADT7467 can optionally drive $\overline{\text{THERM}}$ low as an output. In cases where $\overline{\text{PROCHOT}}$ is bidirectional, $\overline{\text{THERM}}$ can be used to throttle the processor by asserting $\overline{\text{PROCHOT}}$. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, it is guaranteed to remain low for at least one monitoring cycle after $\overline{\text{THERM}}$ is asserted.

The $\overline{\text{THERM}}$ pin can be configured to assert low if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables the $\overline{\text{THERM}}$ output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 32 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

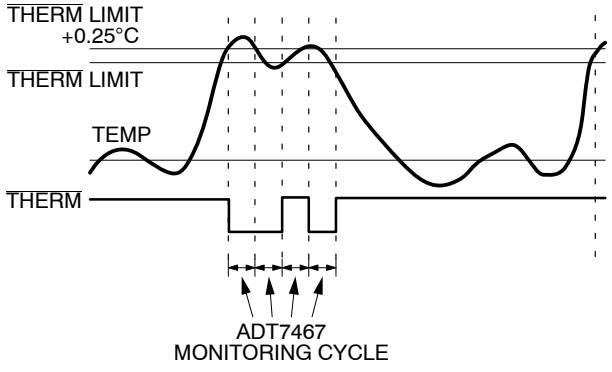


Figure 32. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to −64°C or less in Offset 64 mode, or to −128°C or less in twos complement mode; therefore, for $\overline{\text{THERM}}$ temperature limit values less than −64°C or −128°C, respectively, $\overline{\text{THERM}}$ is disabled.

Active Cooling

Driving the Fan using PWM Control

The ADT7467 uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive may need only a pull-up resistor. In many cases, the 4-wire fan PWM input has a built-in pull-up resistor.

The ADT7467 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are usually used for 2-wire and 3-wire fans, and the high frequency option is usually used for 4-wire fans.

For 2-wire or 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA; therefore, SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET have a gate voltage drive of V_{GS} < 3.3 V for direct interfacing to the PWMx pin. V_{GS} can be greater than 3.3 V as long as the pull-up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 33 shows how to drive a 3-wire fan using PWM control.

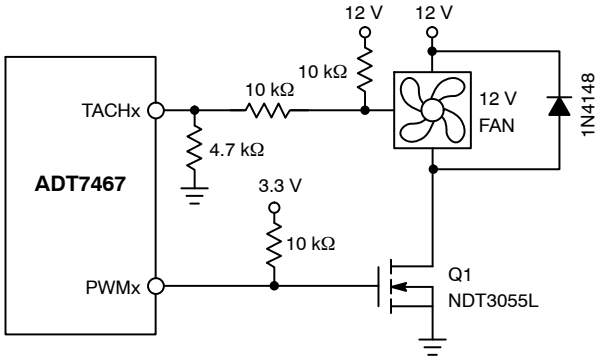


Figure 33. Driving a 3-wire Fan Using an N-channel MOSFET

Figure 33 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5 V maximum to prevent damaging the ADT7467. If in doubt as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 34 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. Although these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

Because 4-wire fans are powered continuously, the fan speed is not switched on or off as with previous PWM driven/powered fans. This enables it to perform better than 3-wire fans, especially for high frequency applications. Figure 35 shows a typical drive circuit for 4-wire fans.

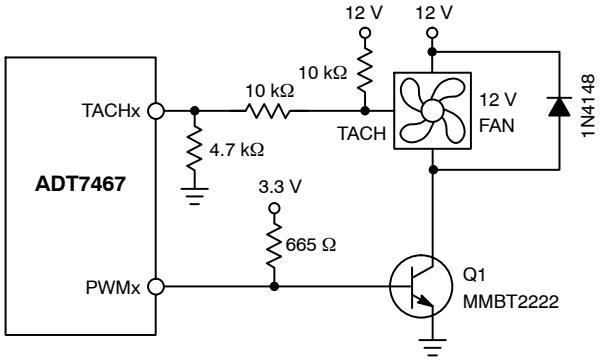


Figure 34. Driving a 3-wire Fan Using an NPN Transistor

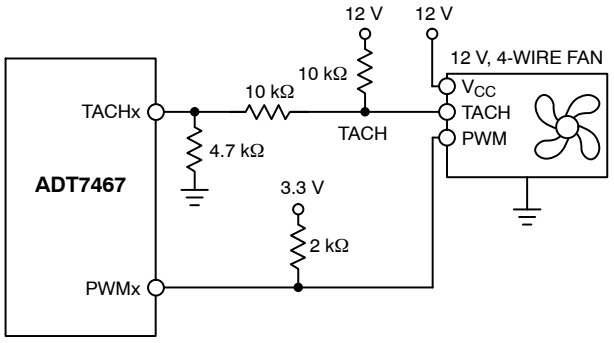


Figure 35. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7467 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 36 shows how to drive two fans in parallel using low cost NPN transistors. Figure 37 shows the equivalent circuit using a MOSFET.

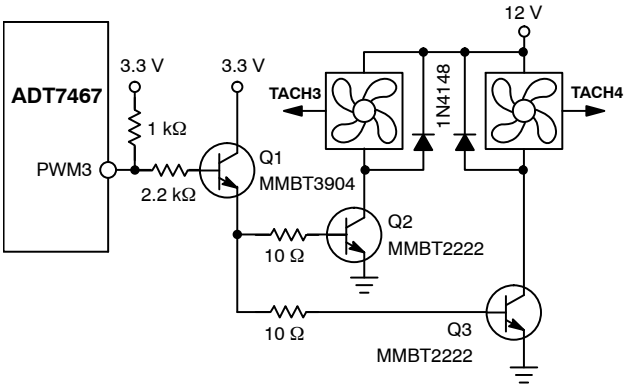


Figure 36. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

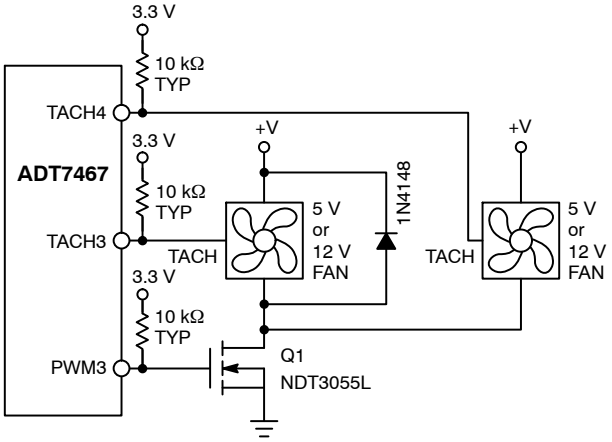


Figure 37. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-channel MOSFET

Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current and that they sink less than the 5 mA maximum current specified on the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3; therefore, PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry is as shown in Figure 36 and Figure 37. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4-wire fans.

Table 25. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM3.

Driving 2-wire Fans

The ADT7467 can only support 2-wire fans when low frequency PWM mode is selected in Configuration Register 5, Bit 2. If this bit is not set to 1, the ADT7467 cannot measure the speed of 2-wire fans.

Figure 38 shows how a 2-wire fan can be connected to the ADT7467. This circuit allows the speed of a 2-wire fan to be measured, even though the fan has no dedicated TACH signal. A series resistor, R_{SENSE}, in the fan circuit converts the fan commutation pulses into a voltage, which is ac-coupled into the ADT7467 through the 0.01 μF capacitor. On-chip signal conditioning allows accurate monitoring of fan speed. The value of R_{SENSE} depends on the programmed input threshold and the current drawn by the fan. For fans drawing approximately 200 mA, a 2 Ω R_{SENSE} value is suitable when the threshold is programmed as 40 mV.

For fans that draw more current, such as larger desktop or server fans, R_{SENSE} can be reduced for the same programmed threshold. The smaller the threshold programmed, the better, because more voltage is developed across the fan and the fan spins faster. Figure 39 shows a typical plot of the sensing waveform at the TACHx pin.

Note that when the voltage spikes (either negative going or positive going) are more than 40 mV in amplitude, the fan speed can be reliably determined.

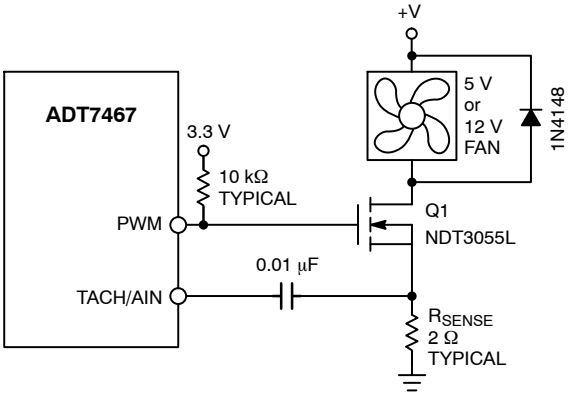


Figure 38. Driving a 2-wire Fan

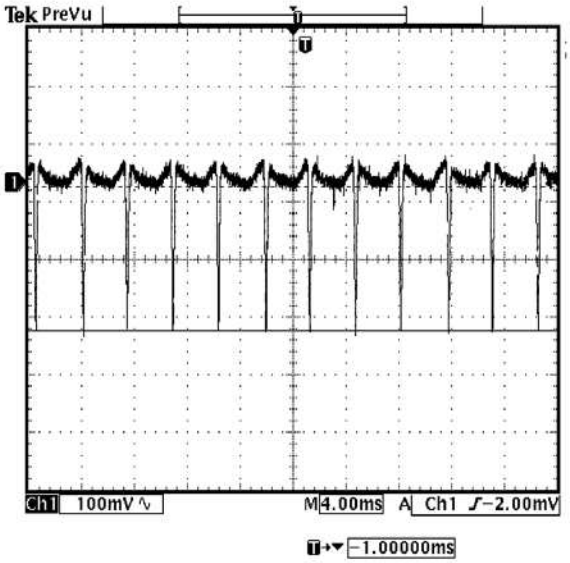


Figure 39. Fan Speed Sensing Waveform at TACHx Pin

Laying Out 2-wire and 3-wire Fans

Figure 40 shows how to lay out a common circuit arrangement for 2-wire and 3-wire fans. Some components are not populated, depending on whether a 2-wire or 3-wire fan is used.

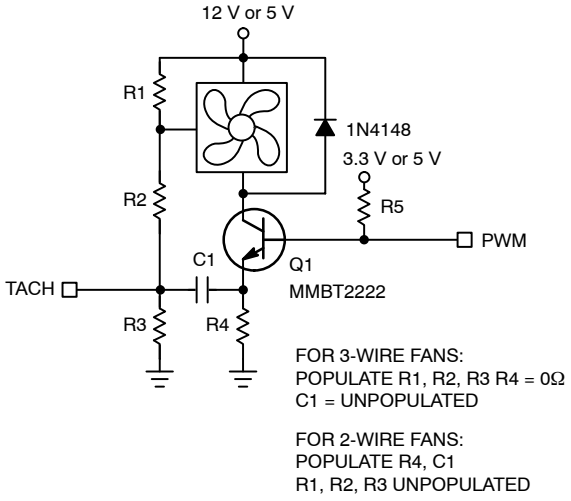


Figure 40. Planning for 2-wire or 3-wire Fans on a PCB