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ADT7473

Remote Thermal Monitor and Fan Control

The ADT7473/ADT7473−1 controller is a thermal monitor and multiple PWM fan controller for noise sensitive or power sensitive applications requiring active system cooling. The ADT7473/ADT7473−1 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans so they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7473/ADT7473−1 also provide critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Controls and Monitors Up to 4 Fans
- High and Low Frequency Fan Drive Signal
- 1 On-Chip and 2 Remote Temperature Sensors
- Series Resistance Cancellation on the Remote Channel
- Extended Temperature Measurement Range, Up to 191°C
- Dynamic T_{MIN} Control Mode Intelligently Optimizes System Acoustics
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 3-wire and 4-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

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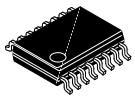
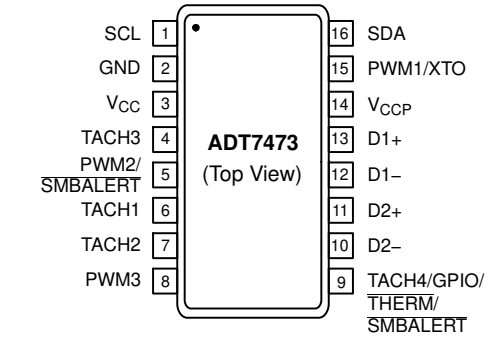
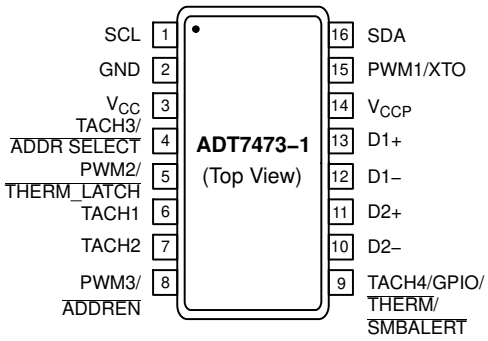


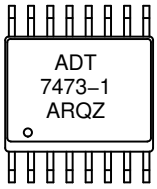
QSOP−16
CASE 492

PIN ASSIGNMENTS





TOP MARKING



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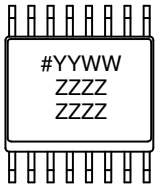


ADT7473−1ARQZ = Specific Device Code
# = Pb-Free Package
YYWW = Date Code
ZZZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 72 of this data sheet.

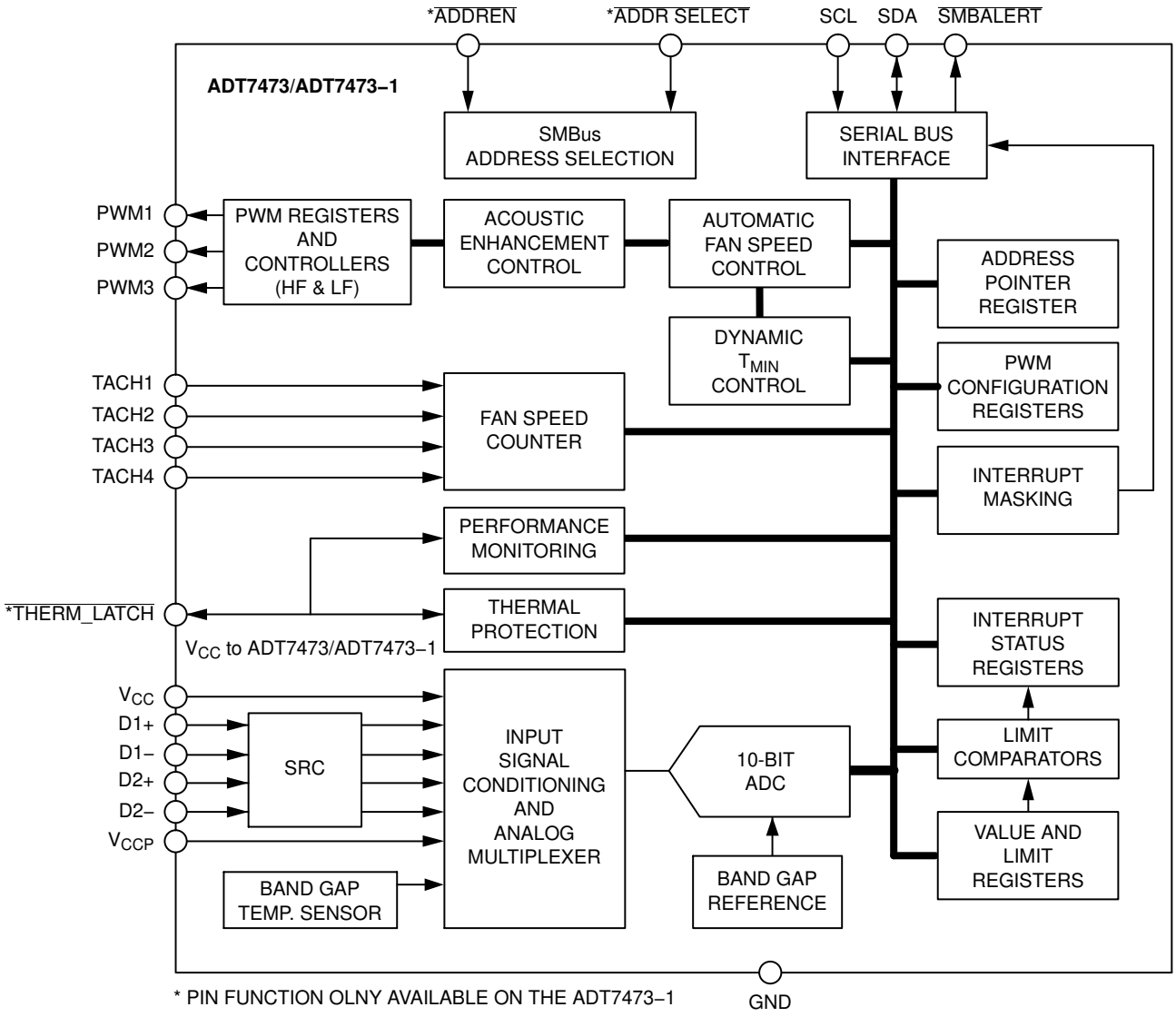


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Voltage on any Input or Output Pin	–0.3 to +3.6	V
Input Current at any Pin	±5.0	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	–65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Lead Temperature (Soldering, 10 sec)	 260 300	°C
ESD Rating	1,500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
16-lead QSOP	150	39	°C/W

NOTE: θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
2	GND	Ground Pin.
3	V_{CC}	Power Supply. Powered by 3.3 V.
4	TACH3 $\overline{\text{ADDR SELECT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. If in address select mode, the logic state of this pin defines the SMBus device address.
5	PWM2 $\overline{\text{SMBALERT}}$ $\overline{\text{THERM\_LATCH}}$	Digital Output (Open Drain). ADT7473 default pin function is PWM2. Requires 10 kΩ typical pullup. Pulse-width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. On the ADT7473, this pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions. ADT7473−1 default pin function. $\overline{\text{THERM\_LATCH}}$ is a thermal event alert signal when an overtemperature condition occurs.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.
8	PWM3 $\overline{\text{ADDREN}}$	Digital I/O (Open Drain). Pulse-width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pullup. Can be configured as a high or low frequency drive. If pulled low on powerup, the ADT7473−1 enters address select mode, and the state of Pin 4 ($\overline{\text{ADDR SELECT}}$) determines the ADT7473−1 slave address.
9	TACH4 GPIO $\overline{\text{THERM}}$ $\overline{\text{SMBALERT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. General Purpose Open Drain Digital I/O. Bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input as well as to assert when an ADT7473 $\overline{\text{THERM}}$ overtemperature limit is exceeded. For example, the pin can be connected to the $\overline{\text{PROCHOT}}$ output of an Intel® Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3.0 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse-width modulated output to control Fan 1 speed. Requires 10 kΩ typical pullup. Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pullup.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface Inactive, ADC Active	–	1.5	3.0	mA
Temperature-to-Digital Converter					
Local Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +125°C	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Diode Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ +125°C	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Sensor Source Current	First Current Second Current Third Current	– – –	6 36 96	– – –	μA
Analog-to-Digital Converter (Including MUX and Attentuators)					
Total Unadjusted Error (TUE)		–	–	±1.5	%
Differential Nonlinearity (DNL)	8 Bits	–	–	±1.0	LSB
Power Supply Sensitivity		–	±0.1	–	%/V
Conversion Time (Voltage Input)	Averaging Enabled	–	11	–	ms
Conversion Time (Local Temperature)	Averaging Enabled	–	12	–	ms
Conversion Time (Remote Temperature)	Averaging Enabled	–	38	–	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	– –	145 19	– –	ms
Input Resistance	For V_{CCP} Channel	70	120	–	kΩ
Fan RPM-to-Digital Converter					
Accuracy	0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ +120°C	– –	– –	±6.0 ±10	%
Full-scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5,000 10,000	– – – –	RPM
Open-Drain Digital Outputs, PWM1 to PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = –8.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	20	μA
Open-Drain Serial Data Bus Output (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = –4.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	1.0	μA
Digital Output Logic Levels, ADT7473–1 ($\overline{\text{THERM\_LATCH}}$) ADTL+					
Output High Voltage, V_{OH}		0.75 × V_{CC}	–	–	V
Output Low Voltage, V_{OL}		–	–	0.4	V
SMBus Digital Inputs (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
Hysteresis		–	500	–	mV

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Digital Input Logic Levels (TACH Inputs)					
Input High Voltage, V_{IH}	Maximum Input Voltage	2.0 –	– –	– 3.6	V
Input Low Voltage, V_{IL}	Minimum Input Voltage	– –0.3	– –	0.8 –	V
Hysteresis		–	0.5	–	V p-p
Digital Input Logic Levels ($\overline{\text{THERM}}$) ADTL+					
Input High Voltage, V_{IH}		$0.75 \times V_{CC}$	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Input High Voltage, V_{IH}		–	–	–	
Input Low Voltage, V_{IL}	$V_{IN} = V_{CC}$	–	±1	–	μA
Input Low Current, I_{IL}	$V_{IN} = 0$	–	±1	–	μA
Input Capacitance, C_{IN}		–	5.0	–	pF
Serial Bus Timing (Note 2) (See Figure 2)					
Clock Frequency, f_{SCLK}		10	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_r		–	–	1,000	ns
SCL, SDA Fall Time, t_f		–	–	300	μs
Data Setup Time, $t_{SU;\,DAT}$		250	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise noted. Typicals are at $T_A = 25°C$ and represent most likely parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge and $V_{IH} = 2.0$ V for a rising edge.
2. Serial management bus (SMBus) timing specifications are guaranteed by design and are not production tested.

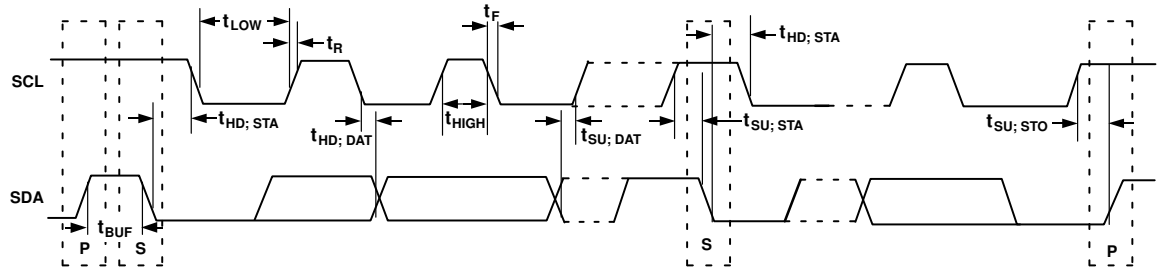


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

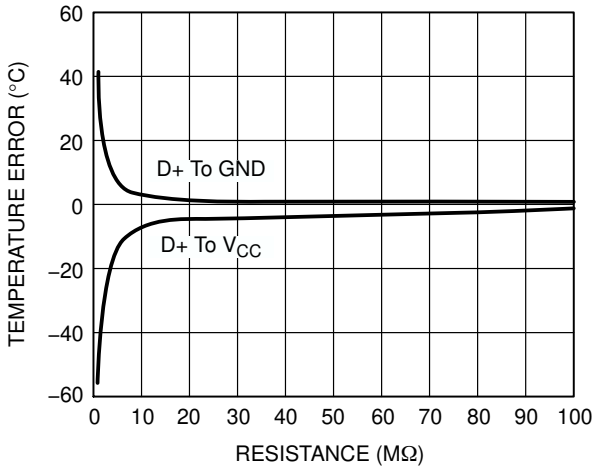


Figure 3. Remote Temperature Error vs. PCB Resistance

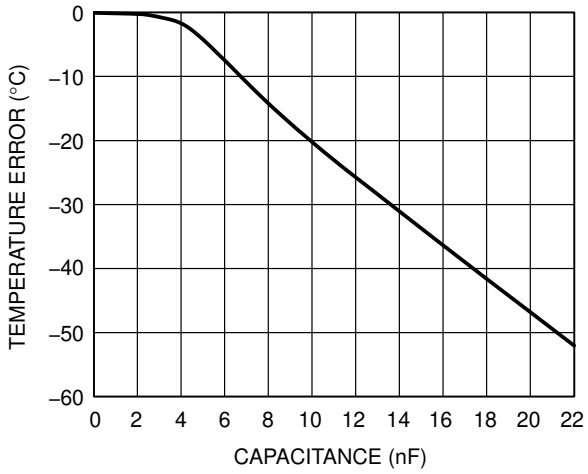


Figure 4. Temperature Error vs. Capacitance Between D+ and D–

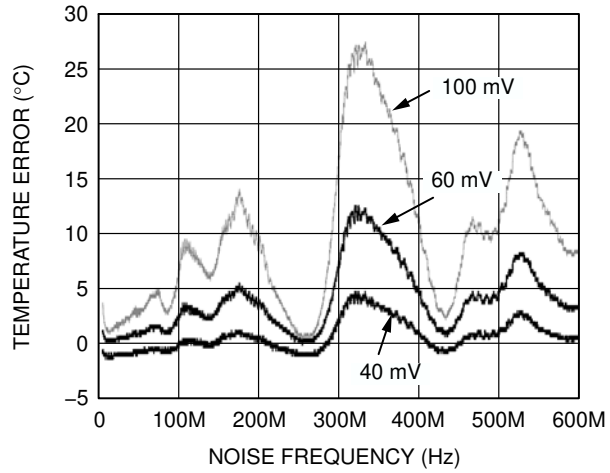


Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

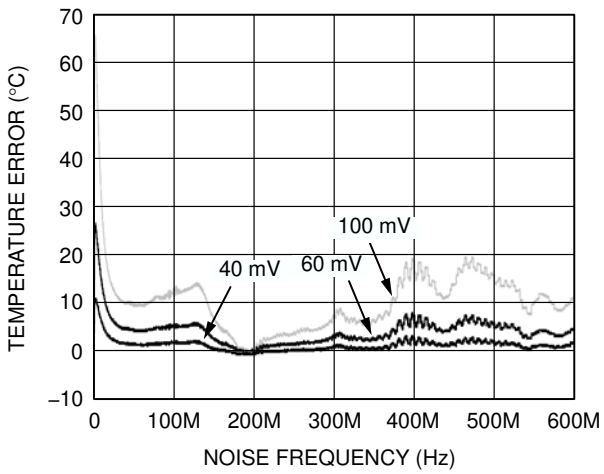


Figure 6. Remote Temperature Error vs. Common-Mode Noise Frequency

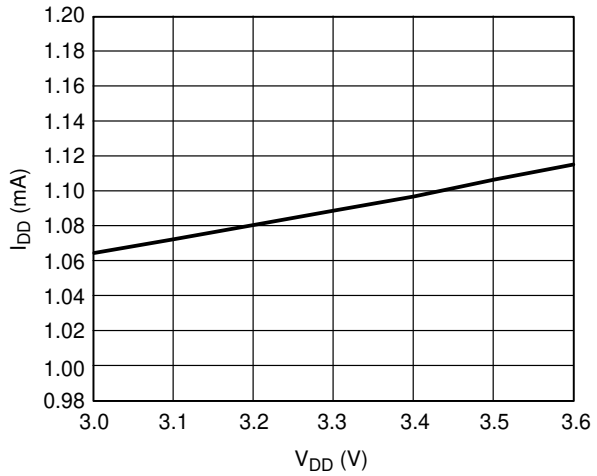


Figure 7. Normal I_{DD} vs. Power Supply

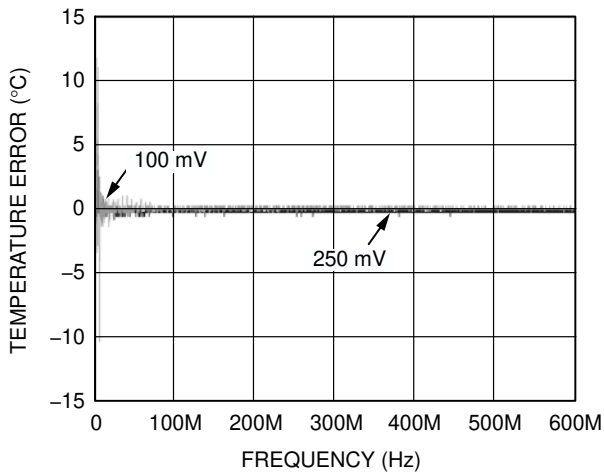


Figure 8. Internal Temperature Error vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

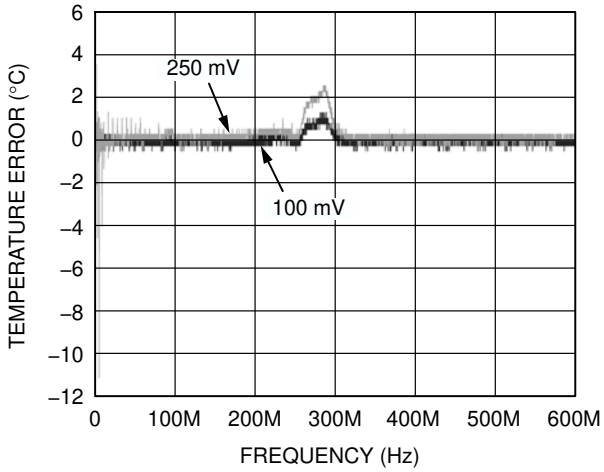


Figure 9. Remote Temperature Error vs. Power Supply Noise Frequency

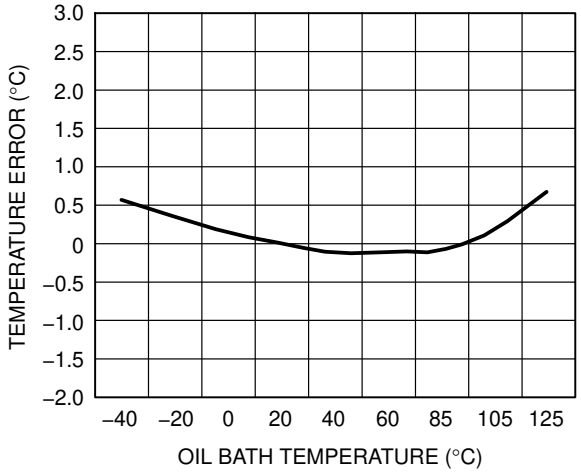


Figure 10. Internal Temperature Error vs. Temperature

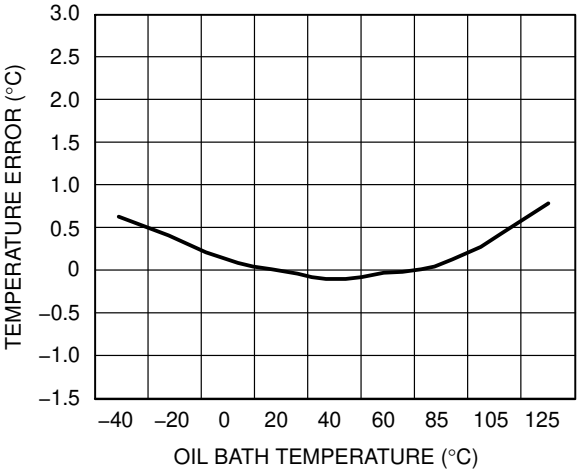


Figure 11. Remote Temperature Error vs. Temperature

Product Description

The ADT7473/ADT7473−1 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7473/ADT7473−1 are performed over the serial bus. Additionally, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 5 illustrates the differences between the ADT7473 and the ADT7473−1.

Table 5. ADT7473/ADT7473−1 DEVICE COMPARISON

Feature	ADT7473	ADT7473−1
Pin 5	Default: PWM2	Default: $\overline{\text{THERM\_LATCH}}$
SMBus Address	Fixed Address	Address selectable
Remote Ch. 2 Therm Limit	= 100°C	= 136°C
Register 0x30, 0x31, 0x32	Default: 0x00	Default: 0xFF
Register 0x3F Revision Reg	Default: 0x68	Default: 0x69
Register 0x40, Bit 7	Reserved	(R/W) 1 = Reset Latch (Lockable)
Register 0x42, Bit 0	Reserved	(Read-only) 1 = $\overline{\text{THERM}}$ Limit Latched
Registers 0x5C, 0x5D, 0x5E	Default: 0x82	Default: 0x62
Register 0x7C, Bit 4	Reserved	$\overline{\text{THERM}}$ Output Hysteresis
Register 0x7D, Bit 4	Reserved	$\overline{\text{THERM\_LATCH}}$ Configuration 0 = Remote Channel 2 1 = Remote Channel 1 and Remote Channel 2

Comparison Between ADT7467 and ADT7473/ADT7473−1

The following list shows some comparisons between the ADT7467 and the ADT7473/ADT7473−1:

- The ADT7473/ADT7473−1 can be powered via a 3.3 V supply only, and does not support 5.0 V operation, while the ADT7467 does. Violating this specification results in irreversible damage to the ADT7473/ADT7473−1. See the Specifications section for more information.
- A high frequency PWM drive can be independently selected for each PWM channel on the ADT7473/ADT7473−1. This is not available on the ADT7467.
- The range and resolution of the temperature offset register can be changed from a ±64°C range at 0.5°C resolution to a ±128°C range at 1°C resolution. This is not available on the ADT7467.
- $\overline{\text{THERM}}$ overtemperature events can be disabled/enabled individually on each temperature channel. This is not available on the ADT7467.
- Bit 7 of Configuration Register 1 is no longer supported because the ADT7473/ADT7473−1 cannot be powered via a 5.0 V supply.
- Bit 0 of Configuration Register 1 (0x40) remains writable after the lock bit is set. This bit enables monitoring.
- 2-wire fan speed measurement is not supported on the ADT7473/ADT7473−1.

How to Set the Functionality of Pin 9

Pin 9 on the ADT7473/ADT7473−1 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 (0x7D).

Table 6. PIN 9 SETTINGS

Bit 0	Bit 1	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	GPIO
1	1	$\overline{\text{SMBALERT}}$

Recommended Implementation

Configuring the ADT7473 as shown in Figure 12 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans. (The front and rear chassis fans are connected in parallel.)
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU temperature measured using Remote 1 temperature channel.
- Ambient temperature measured through Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

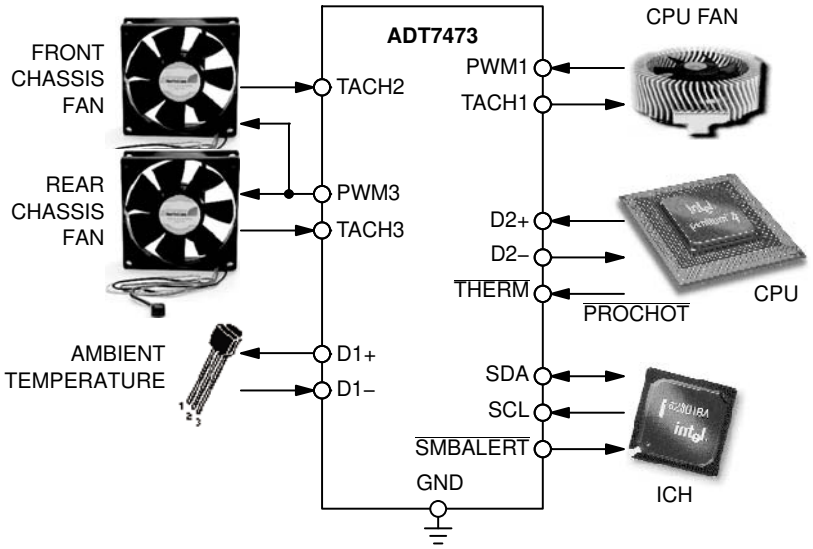


Figure 12. ADT7473 Configuration

Serial Bus Interface

On PCs and servers, control of the ADT7473/ADT7473−1 is carried out using the SMBus. The ADT7473/ADT7473−1 is connected to this bus as a slave device, under the control of a master controller, which is usually (but not necessarily) the ICH.

The ADT7473 has a fixed 7-bit serial bus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address (01011100 or 0x5C). When the ADT7473−1 is powered up with Pin 8 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7473−1 has a default SMBus address of 0101110 or 0x2E. If more than one ADT7473−1 is used in a system, each ADT7473−1 is placed in $\overline{\text{ADDR SELECT}}$ mode by strapping Pin 8 low on powerup. The logic state of Pin 4 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is sampled on powerup and latched on the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDREN}}$ pin/$\overline{\text{ADDR SELECT}}$ pin. Any attempted change in the address has no effect after this.

Table 7. HARDWIRING THE ADT7473−1 SMBUS DEVICE ADDRESS

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pullup)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E)

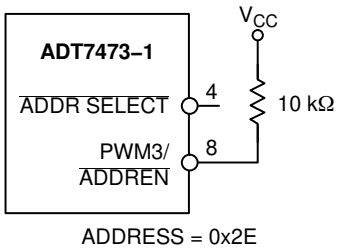


Figure 13. Default SMBus Address = 0x2E

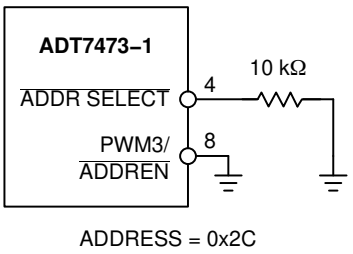


Figure 14. SMBus Address = 0x2C (Pin 4 = 0)

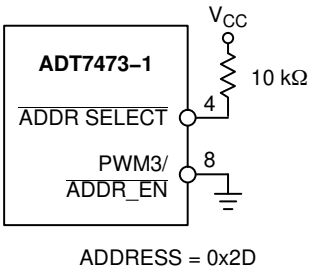
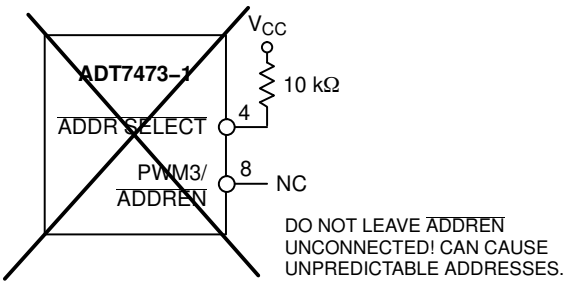


Figure 15. SMBus Address = 0x2D (Pin 4 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 8 (PWM3/ADDREN) IS EITHER TIED HIGH OR LOW. LEAVING PIN 8 FLOATING COULD CAUSE THE ADT7473−1 TO POWER UP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7473−1 IS PLACED INTO ADDR SELECT MODE, PINS 8 AND 4 CAN BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/THERM) UNLESS THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME OR DESIGNED TO HANDLE THESE DUAL FUNCTIONS.

Figure 16. Unpredictable SMBus Address if Pin 8 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7473−1 is used in a system.

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7473/ADT7473−1, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so the correct data register is addressed, and then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 17. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7473/ADT7473−1's address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7473/ADT7473−1, but only the data byte containing the register address is sent, because no data is written to the register. This is shown in Figure 18.
   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 19.
2. If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 19.

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7473/ADT7473−1 also supports the read byte protocol. (See System Management Bus (SMBus) Specifications Version 2 for more information; this document is available from Intel.)

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

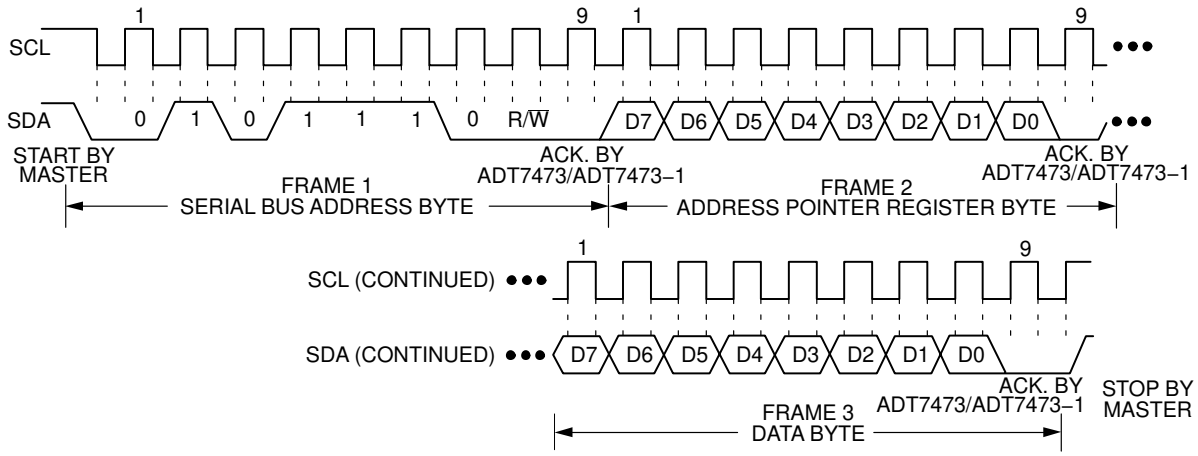


Figure 17. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

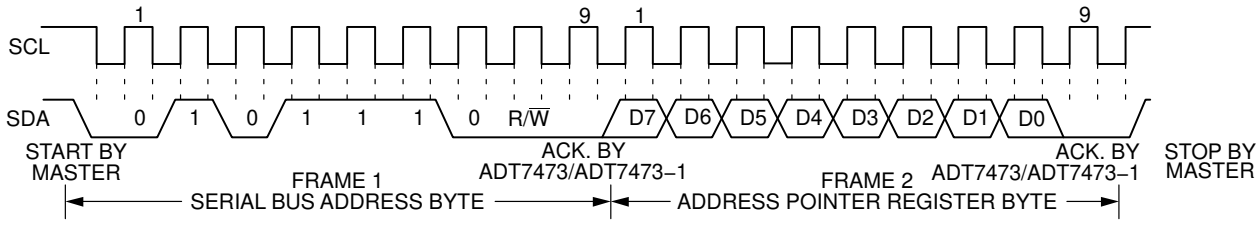


Figure 18. Writing to the Address Pointer Register Only

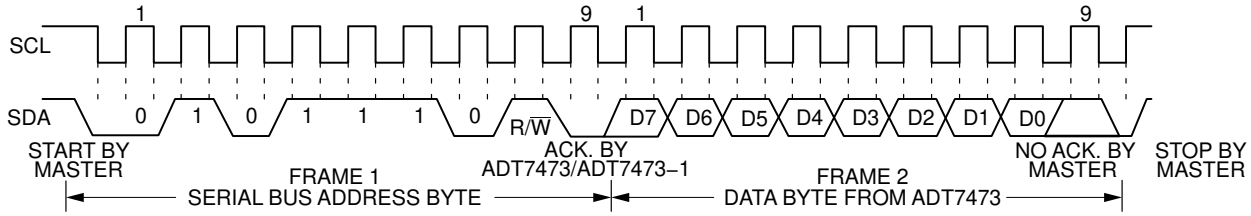


Figure 19. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for various read and write operations. The ADT7473/ADT7473−1 uses the following SMBus write protocols. The following abbreviations are used in the diagrams:

S – Start
P – Stop
R – Read
W – Write
A – Acknowledge
$\overline{A}$ – No Acknowledge

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (active low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADT7473/ADT7473−1, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 20.

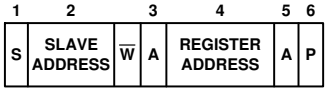


Figure 20. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single-byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (active low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

The single byte write operation is illustrated in Figure 21.

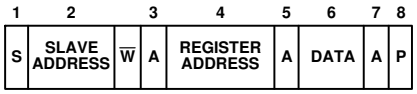


Figure 21. Single-byte Write to a Register

Read Operations

The ADT7473/ADT7473−1 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must have been previously set up. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7473/ADT7473−1, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 22.

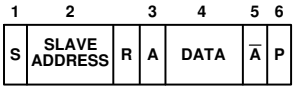


Figure 22. Single-byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

- $\overline{\text{SMBALERT}}$ is pulled low.
- The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
- The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
- If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.

Once the ADT7473/ADT7473−1 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition is gone.

SMBus Timeout

The ADT7473/ADT7473−1 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7473/ADT7473−1 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.

Table 8. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description
<6> TODIS	0: SMBus Timeout Enabled (Default) 1: SMBus Timeout Disabled

Voltage Measurement Input

The ADT7473/ADT7473−1 has one external voltage measurement channel and can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. (ADC) This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (768 decimal or 300 hexadecimal) for the nominal input voltage and thus has adequate headroom to deal with overvoltages.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 23. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first order low-pass filter that provides the input immunity to high frequency noise.

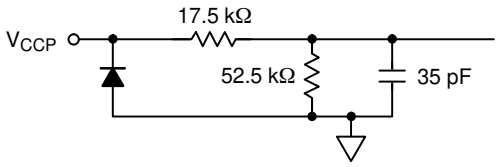


Figure 23. Structure of Analog Inputs

Table 9. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x21	V_{CCP} Reading	0x00
0x22	V_{CCP} Reading	0x00

V_{CCP} Limit Registers

Associated with the V_{CCP} measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 10. V_{CCP} LIMIT REGISTERS

Register	Description	Default
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF

Table 13 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 711 μs and averages 16 conversions to reduce noise; a measurement takes nominally 11.38 ms.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7473/ADT7473−1 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. When faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7473/ADT7473−1 into single-channel ADC conversion mode. In this mode, the ADT7473/ADT7473−1 can be made to read a single voltage channel only. If the internal ADT7473/ADT7473−1 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 11. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits <7:5>, Register 0x55	Channel Selected
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Table 12. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<5>	1: Bypass Input Attenuators
<6>	1: Single-channel Convert Mode

TACH1 Minimum High Byte Register (0x55)

Bits <7:5> select ADC channel for single-channel convert mode.

Table 13. 10-BIT ADC OUTPUT CODE VS. V_{IN}

ADC Output			
V_{CC} (3.3 V_{IN}) (Note 1)	**V_{CCP}**	**Decimal**	**Binary (10 Bits)**
<0.0042	<0.00293	0	00000000 00
0.0042 to 0.0085	0.0293 to 0.0058	1	00000000 01
0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
–	–	–	–
1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
–	–	–	–
2.200 to 2.2042	1.5000 to 1.5029	512 (1/2 scale)	10000000 00
–	–	–	–
3.300 to 3.3042	2.2500 to 2.2529	768 (3/4 scale)	11000000 00
–	–	–	–
4.3527 to 4.3570	2.9677 to 2.9707	1013	11111101 01
4.3570 to 4.3613	2.9707 to 2.9736	1014	11111101 10
4.3613 to 4.3656	2.9736 to 2.9765	1015	11111101 11
4.3656 to 4.3699	2.9765 to 2.9794	1016	11111110 00
4.3699 to 4.3742	2.9794 to 2.9824	1017	11111110 01
4.3742 to 4.3785	2.9824 to 2.9853	1018	11111110 10
4.3785 to 4.3828	2.9853 to 2.9882	1019	11111110 11
4.3828 to 4.3871	2.9882 to 2.9912	1020	11111111 00
4.3871 to 4.3914	2.9912 to 2.9941	1021	11111111 01
4.3914 to 4.3957	2.9941 to 2.9970	1022	11111111 10
>4.3957	>2.9970	1023	11111111 11

1. The V_{CC} output codes listed assume that V_{CC} is 3.3 V.

Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null out the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADT7473/ADT7473−1 measures the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 24 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (recommended maximum value 1,000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

Local Temperature Measurement

The ADT7473/ADT7473−1 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 14 and Table 15. Theoretically, the temperature sensor and ADC can measure temperatures from −63°C to +127°C (or −63°C to +191°C in the extended temperature range) with a resolution of +0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7473/ADT7473−1 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7473/ADT7473−1 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7473/ADT7473−1 is to measure the change in V_{BE} when the device is operated at three different currents. This is given by:

$$\Delta V_{BE} = kT/q \times \ln(N) \quad \text{(eq. 1)}$$

where:
k is Boltzmann's constant.
T is the absolute temperature in Kelvin.
q is the charge on the carrier.
N is the ratio of the two currents.

Figure 24 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

Table 14. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−128°C	1000 0000 **00** (Diode Fault)
−63°C	1100 0001 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25.5°C	0001 1001 **10**
50.75°C	0011 0010 **11**
75°C	0100 1011 **00**
100°C	0110 0100 **00**
125°C	0111 1101 **00**
127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (Register 0x77) with 0.25°C resolution.

Table 15. EXTENDED RANGE, TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−64°C	0000 0000 **00** (Diode Fault)
−63°C	0000 0001 **00**
−1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (Register 0x77) with 0.25°C resolution.

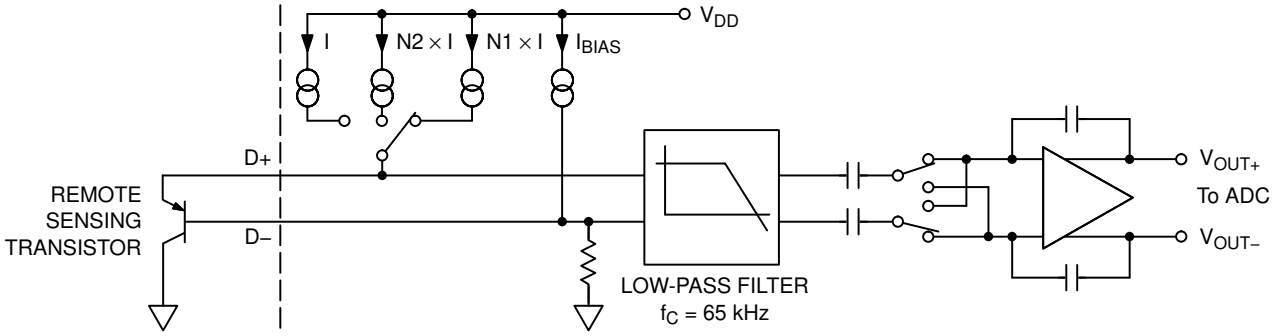


Figure 24. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter is connected to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base is connected to the D+ input. Figure 25 and Figure 26 show how to connect the ADT7473/ADT7473−1 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

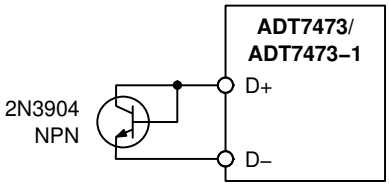


Figure 25. Measuring Temperature by Using an NPN Transistor

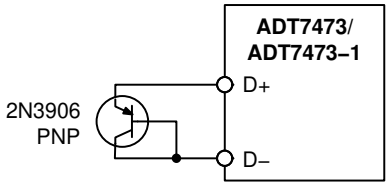


Figure 26. Measuring Temperature by Using a PNP Transistor

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. N1 × I and N2 × I are different multiples of the current I, as shown in Figure 24. The currents through the temperature diode are switched between I and N1 × I, giving ΔV_{BE1}, and then between I and N2 × I, giving ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10-bit, twos complement format, as listed in Table 10. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and the D− pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF. This capacitor reduces the noise, but does not eliminate it, making use of the sensor difficult in a very noisy environment.

The ADT7473/ADT7473−1 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7473/ADT7473−1 and the remote temperature sensor to operate in noisy environments. Figure 27 shows a low-pass R-C filter with the following values:

$$R = 100\ \Omega,\ C = 1\ nF \qquad \text{(eq. 1)}$$

This filtering reduces both common-mode noise and differential noise.

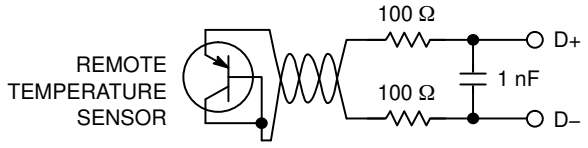


Figure 27. Filter Between Remote Sensor and ADT7473/ADT7473−1

Series Resistance Cancellation

Parasitic resistance to the ADT7473/ADT7473−1 D+ and D− inputs (seen in series with the remote diode) is caused by a variety of factors including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per Ω of parasitic resistance in series with the remote diode.

The ADT7473/ADT7473−1 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result without the need for user characterization of this resistance. The ADT7473/ADT7473−1 is designed to automatically cancel up to 3 kΩ of resistance, typically. This is transparent to the user by using an advanced temperature measurement method. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the Noise Filtering section for details.

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7473/ADT7473−1 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7473/ADT7473−1 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T(°C), when using a transistor whose n_f does not equal 1.008. Refer to the data sheet for the related CPU to obtain the n_f values.

$$\Delta T = (n_f - 1.008)/1.008 \times (273.15\ K + T) \qquad \text{(eq. 2)}$$

  To factor this in, the user can write the ΔT value to the offset register. Then, the ADT7473/ADT7473−1 automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7473/ADT7473−1, I_{HIGH}, is 96 μA and the low level current, I_{LOW}, is 6 μA. If the ADT7473/ADT7473−1 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that, if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7473/ADT7473−1, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 6 μA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 100 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (such as 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT−23 packages, are suitable devices to use.

Nulling Out Temperature Errors

As CPUs run faster, it becomes more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors can still be attributable to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7473/ADT7473−1 has temperature offset registers at Register 0x70 and Register 0x72 for the Remote 1 and Remote 2 temperature channels. By performing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement, 8-bit reading to every temperature measurement. The LSBs add +0.5°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of +0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Table 16. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

ADT7460/ADT7473/ADT7473−1 Backwards-compatible Mode

By setting Bit 1 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature value registers (Register 0x25, Register 0x26, and Register 0x27) in twos complement, in the range −63°C to +127°C. (The ADT7473/ADT7473−1 still makes calculations based on the Offset 64 extended range and clamps the results, if necessary.) The temperature limits

must be reprogrammed in twos complement. If a twos complement temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, while in the extended temperature range (−64°C to +191°C), the fault condition is represented by −64°C = 0000 0000.

Table 17. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	–
0x26	Local Temperature	–
0x27	Remote 2 Temperature	–
0x77	Extended Resolution 2	0x00

Table 18. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 19. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7473/ADT7473−1

It is important to note that the temperature can be read from the ADT7473/ADT7473−1 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, a 2-register read for each measurement is used. The extended resolution register (Register 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read, and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7473/ADT7473−1 to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off.

Table 20. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channel	0.7
Remote 1 Temperature	7
Remote 2 Temperature	7
Local Temperature	1.3

Table 21. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)
Voltage Channel	11
Remote Temperature	39
Local Temperature	12

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7473/ADT7473−1 into single-channel ADC conversion mode. In this mode, the ADT7473/ADT7473−1 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 22. PROGRAMMING SINGLE-CHANNEL ADC MODE FOR TEMPERATURES

Channel Selected	Bits <7:4>, Register 0x55
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

Bit <4> = 1, Averaging Off.

Bit <6> = 1, Single-channel Convert Mode.

TACH1 Minimum High Byte Register (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in

automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ limits. When a temperature exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs run at 100% duty cycle or the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A) if Bit 3 of Configuration Register 4 (0x7D) is set. The fans remain running at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis; this can be disabled by setting the boost bit in Configuration Register 3 (0x78), Bit 2. The hysteresis value for that $\overline{\text{THERM}}$ limit is the value programmed into the hysteresis registers (Register 0x6D and Register 0x6E). The default hysteresis value is 4°C.

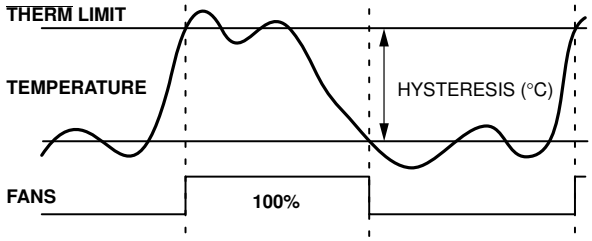


Figure 28. $\overline{\text{THERM}}$ Limit Operation

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7473/ADT7473−1 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-bit Limits

The following is a list of 8-bit limits on the ADT7473/ ADT7473−1.

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0xFF
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0xA4
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0xFF
0x6B	Local $\overline{\text{THERM}}$ Temperature Limit	0xA4
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0xFF
0x6C	Remote 2 $\overline{\text{THERM}}$ Temp. Limit	0xA4

Table 25. $\overline{\text{THERM}}$ LIMIT REGISTER

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Timer Limit	0x00

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 26. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7473/ ADT7473−1 can be enabled for monitoring. The ADT7473/ ADT7473−1 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High limit > comparison performed
Low limit ≤ comparison performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). By default, the ADT7473/ADT7473−1 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated. The total number of channels measured is:

- One Dedicated Supply Voltage Input (V_{CCP})
- Supply Voltage (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round-robin conversions. The total monitoring cycle time for averaged voltage and temperature monitoring is 146 ms. The total monitoring cycle time for voltage and temperature monitoring with averaging disabled is 19 ms. The ADT7473/ ADT7473−1 is a derivative of the ADT7467. As a result, the total conversion time in the ADT7473/ ADT7473−1 is the same as the total conversion time of the ADT7467, even though the ADT7473/ADT7473−1 has fewer monitored channels.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Interrupt Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out of limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (Reg. 0x41), a 1 means an out-of-limit event has been flagged in Interrupt Status Register 2. This means the user needs only to read Interrupt Status Register 2 when this bit is set. Alternatively, Pin 5 or Pin 9 on the ADT7473 can be configured as an $\overline{\text{SMBALERT}}$ output, while only Pin 9 can be configured to be an $\overline{\text{SMBALERT}}$ on the ADT7473−1. This automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits (except OVT) are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt mask registers (Register 0x74 and Register 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out of limit, its associated status bit is set in the interrupt status registers. OVT clears automatically.

Table 27. INTERRUPT STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1 denotes a bit in Interrupt Status Register 2 is set and Interrupt Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 Temperature High or Low Limit has been exceeded.
5	LT	1 indicates that the Local Temperature High or Low Limit has been exceeded.
4	R1T	1 indicates that the Remote 1 Temperature High or Low Limit has been exceeded.
3	–	Unused
2	V_{CC}	1 indicates that the V_{CC} High or Low Limit has been exceeded.
1	V_{CCP}	1 indicates that the V_{CCP} High or Low Limit has been exceeded.
0	–	Unused

Table 28. INTERRUPT STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D1+/D1− inputs.
5	F4P	1 indicates that Fan 4 has dropped below the minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ timer limit has been exceeded if the $\overline{\text{THERM}}$ timer function is used.
4	FAN3	1 indicates that Fan 3 has dropped below the minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below the minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below the minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.
0	$\overline{\text{THERM}}$ Limit Latch	1 indicates that a Remote Channel 2 latch.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT747/ADT7473−1 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

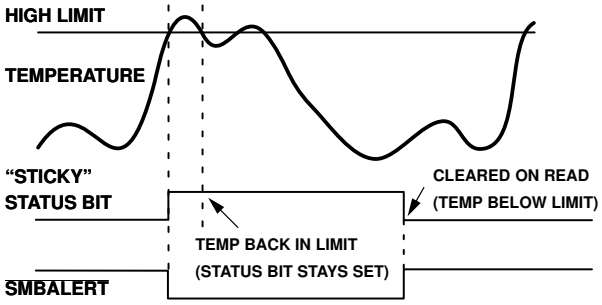


Figure 29. SMBALERT and Status Bit Behavior

Figure 29 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The interrupt status bit remains set until the error condition subsides and the interrupt status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low for the entire duration that a reading is out of limit and until the interrupt status register has been read. This has implications on how software handles the interrupt.

Note that THERM overtemperature events are not sticky, resetting immediately after the overtemperature condition ceases. This also applies to SMBALERT if associated with an OVT event.

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommended to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Register 0x74 and Register 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.

Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 30.

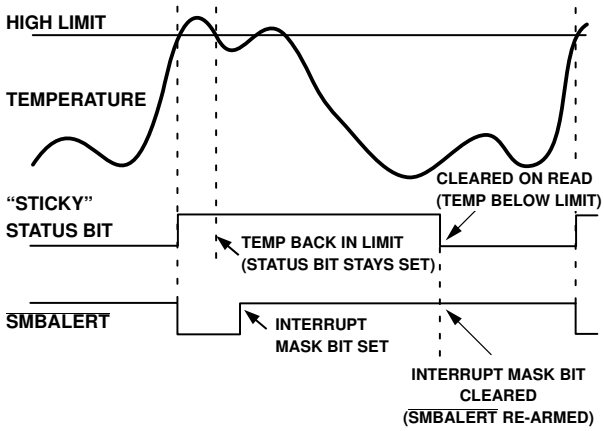


Figure 30. How Masking the Interrupt Source Affects SMBALERT Output

Masking Interrupt Sources

Register 0x74, Interrupt Mask Register 1

Register 0x75, Interrupt Mask Register 2

These registers allow individual interrupt sources to be masked out to prevent SMBALERT interrupts. Masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

Table 29. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	0 when one or more alerts are generated in Interrupt Status Register 2, assuming all the mask bits in the Interrupt Mask Register 2 (0x75) = 1; SMBALERT is still asserted. 1 when one or more alerts are generated in Interrupt Status Register 2, assuming all the mask bits in the Interrupt Mask Register 2 (0x75) = 1; SMBALERT is not asserted.
6	R2T	1 masks SMBALERT for Remote 2 temperature.
5	LT	1 masks SMBALERT for Local temperature.
4	R1T	1 masks SMBALERT for Remote 1 temperature.
3	–	Unused
2	V_{CC}	1 masks SMBALERT for the V_{CC} channel.
1	V_{CCP}	1 masks SMBALERT for the V_{CCP} channel.
0	–	Unused

Table 30. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.
6	D1	1 masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.
5	FAN4	1 masks $\overline{\text{SMBALERT}}$ for Fan 4 failure. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event.
4	FAN3	1 masks $\overline{\text{SMBALERT}}$ for Fan 3.
3	FAN2	1 masks $\overline{\text{SMBALERT}}$ for Fan 2.
2	FAN1	1 masks $\overline{\text{SMBALERT}}$ for Fan 1.
1	OVT	1 masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ limits).
0	–	Unused

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions. ($\overline{\text{SMBALERT}}$ function is available only on Pin 9 of ADT7473−1.)

Table 31. ADT7473 CONFIGURING PIN 5 AS $\overline{\text{SMBALERT}}$ OUTPUT

Register	Bit Setting
Configuration Register 3 (Register 0x78)	<0> $\overline{\text{ALERT}}$ = 1

The ADT7473−1 $\overline{\text{THERM\_LATCH}}$ function latches and asserts when temperature rises 0.25°C above the $\overline{\text{THERM}}$ limit for the selected remote channel. Due to a $\overline{\text{THERM}}$ event, the fans spin at full speed. This can be disabled by setting Bit 2 in Configuration Register 0x7D.

Pin 5 remains latched until temperature falls below $\overline{\text{THERM}}$ limit for the selected zone, Remote Channel D1 or Remote Channel D2, and Bit 0 in Status Register 2 is cleared. By default on the ADT7473−1, the $\overline{\text{THERM}}$ limit is set as 136°C for Remote Channel 2 and 100°C for Remote Channel 1.

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 9 on the ADT7473/ADT7473−1 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 (0x7D).

Table 32. CONFIGURATION REGISTER 4 (REG. 0X7D)

Bit 1	Bit 0	Function
0	1	TACH4
0	0	$\overline{\text{THERM}}$
1	1	SMBusALERT
1	0	GPIO

Once Pin 9 is configured as $\overline{\text{THERM}}$, it must be enabled by setting Bit 1 of Configuration Register 3 (0x78).

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the ADT7473/ADT7473−1 can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance. See the $\overline{\text{THERM}}$ Timer section for more information.

The user can also set up the ADT7473/ADT7473−1 so that, when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, then pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 31 for more information.

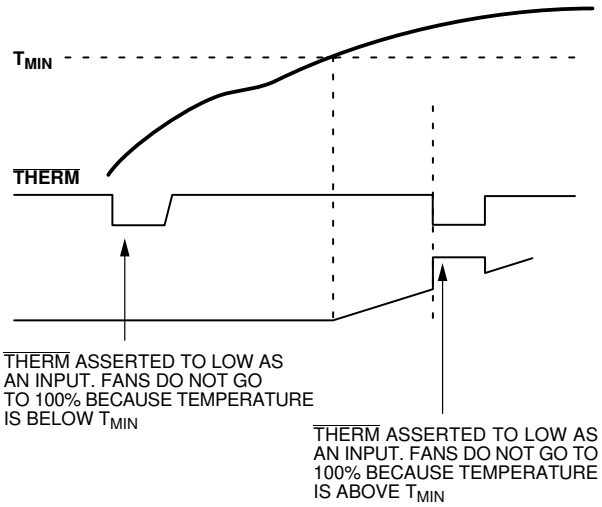


Figure 31. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7473/ADT7473−1 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium® 4 CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7473/ADT7473−1 $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is deasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively; that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer status register (0x79) is designed so that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded

45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 32).

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (0x79):

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded).

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, then the following happens:

1. The contents of the timer are cleared.
2. Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 (because a $\overline{\text{THERM}}$ assertion is occurring).
3. The $\overline{\text{THERM}}$ timer increments from 0.
4. If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) = 0x00, the F4P bit is set.

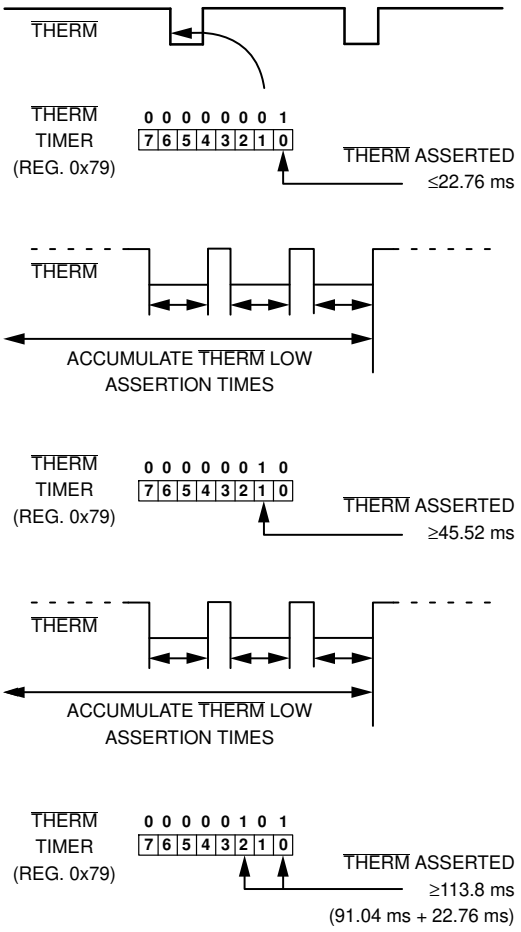


Figure 32. Understanding the $\overline{\text{THERM}}$ Timer

Generating $\overline{\text{SMBALERT}}$ Interrupts from $\overline{\text{THERM}}$ Timer Events

The ADT7473/ADT7473−1 can generate an $\overline{\text{SMBALERT}}$ when a programmable $\overline{\text{THERM}}$ timer limit is exceeded. This allows the system designer to ignore brief, infrequent $\overline{\text{THERM}}$ assertions, while capturing longer $\overline{\text{THERM}}$ timer events. Register 0x7A is the $\overline{\text{THERM}}$ timer limit register. This 8-bit register allows a limit from 0 sec (first $\overline{\text{THERM}}$ assertion) to 5.825 sec to be set before an $\overline{\text{SMBALERT}}$ is generated. The $\overline{\text{THERM}}$ timer value is compared with the contents of the $\overline{\text{THERM}}$ timer limit register. If the $\overline{\text{THERM}}$ timer value exceeds the $\overline{\text{THERM}}$ timer limit value, the F4P bit (Bit 5) of Interrupt Status Register 2 is set and an $\overline{\text{SMBALERT}}$ is generated. The F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks out the $\overline{\text{SMBALERT}}$ if this bit is set to 1; however, the F4P bit of Interrupt Status Register 2 still is set if the $\overline{\text{THERM}}$ timer limit is exceeded.

Figure 33 is a functional block diagram of the $\overline{\text{THERM}}$ timer, limit, and associated circuitry. Writing a value of 0x00 to the $\overline{\text{THERM}}$ timer limit register (0x7A) causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion. A $\overline{\text{THERM}}$ timer limit value of 0x01 generates an $\overline{\text{SMBALERT}}$ once cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms.

Configuring the $\overline{\text{THERM}}$ Behavior

1. Configure Pin 9 as a $\overline{\text{THERM}}$ timer input. Setting Bit 1 ($\overline{\text{THERM}}$ timer enable) of Configuration Register 3 (0x78) enables the $\overline{\text{THERM}}$ timer monitoring functionality. This is disabled on Pin 9 by default. Setting Bit 0 and Bit 1 (PIN9FUNC) of Configuration Register 4 (0x7D) enables $\overline{\text{THERM}}$ timer/output functionality on Pin 9 (Bit 1 of Configuration Register 3, $\overline{\text{THERM}}$, must also be set). Pin 9 can also be used as TACH4. Setting Bit 5, Bit 6, and Bit 7 of Configuration Register 5 (0x7C) makes $\overline{\text{THERM}}$ bidirectional. This means that if the appropriate temperature channel exceeds the $\overline{\text{THERM}}$ temperature limit, the $\overline{\text{THERM}}$ output asserts. If the ADT7473 is not pulling $\overline{\text{THERM}}$ low, but $\overline{\text{THERM}}$ is pulled low by an external device (such as a CPU overtemperature signal), the $\overline{\text{THERM}}$ timer also times $\overline{\text{THERM}}$ assertions. If Bit 5, Bit 6, and Bit 7 of Configuration Register 5 (0x7C) are set to 0, $\overline{\text{THERM}}$ is set as a timer input only.
2. Select the desired fan behavior for $\overline{\text{THERM}}$ timer events. Assuming the fans are running, setting Bit 2 (BOOST) of Configuration Register 3 (0x78) causes all fans to run at 100% duty cycle whenever $\overline{\text{THERM}}$ is asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by $\overline{\text{THERM}}$ events. If the fans are not already running when $\overline{\text{THERM}}$ is asserted, the fans do not run at full speed.
3. Select whether $\overline{\text{THERM}}$ timer events should generate $\overline{\text{SMBALERT}}$ interrupts. Bit 5 (F4P) of Interrupt Mask Register 2 (0x75), when set, masks out the $\overline{\text{SMBALERT}}$ when the $\overline{\text{THERM}}$ timer limit value is exceeded. This bit should be cleared if $\overline{\text{SMBALERT}}$is based on $\overline{\text{THERM}}$ events required.

4. Select a suitable $\overline{\text{THERM}}$ limit value. This value determines whether an $\overline{\text{SMBALERT}}$ is generated on the first $\overline{\text{THERM}}$ assertion, or only if a cumulative $\overline{\text{THERM}}$ assertion time limit is exceeded. A value of 0x00 causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion.
5. Select a $\overline{\text{THERM}}$ monitoring time. This value specifies how often OS or BIOS level software checks the $\overline{\text{THERM}}$ timer. For example, BIOS could read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >5.825 sec in Hour 3, this can indicate that system performance is degrading significantly because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

Alternatively, OS- or BIOS-level software can timestamp when the system is powered on. If an $\overline{\text{SMBALERT}}$ is generated due to the $\overline{\text{THERM}}$ timer limit being exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ timer limit time. For example, if it takes one week for a $\overline{\text{THERM}}$ timer limit of 2.914 seconds to be exceeded and the next time it takes only one hour, this is an indication of a serious degradation in system performance.

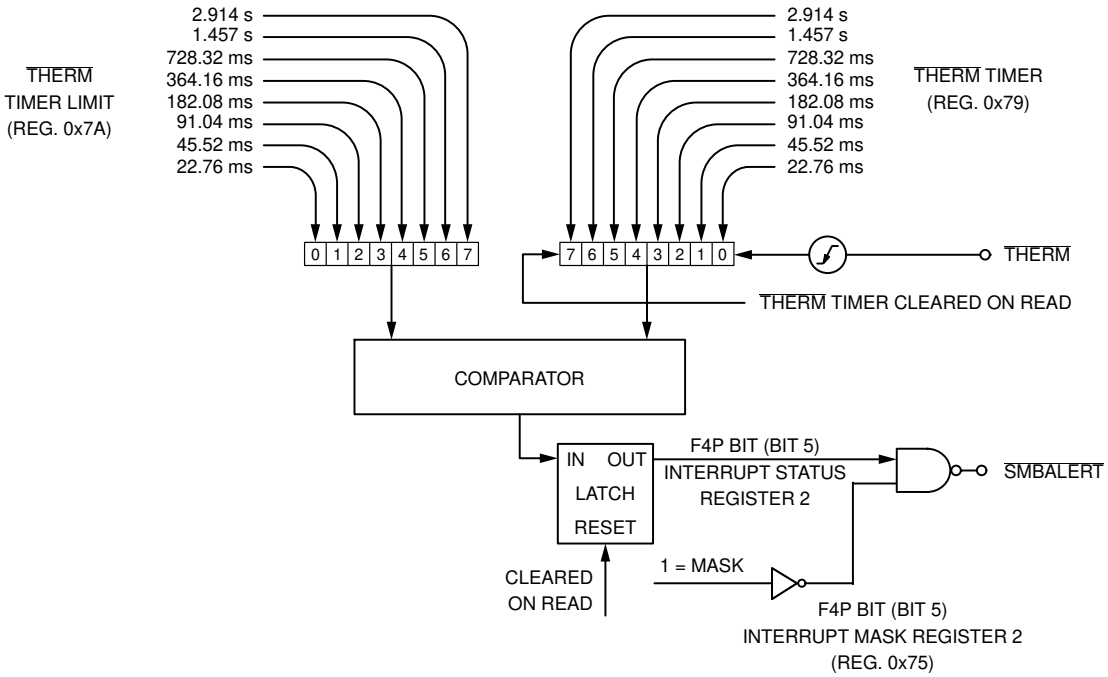


Figure 33. Functional Diagram of the ADT7473 $\overline{\text{THERM}}$ Monitoring Circuitry

Configuring the $\overline{\text{THERM}}$ Pin as Bidirectional

In addition to monitoring $\overline{\text{THERM}}$ as an input, the ADT7473/ADT7473−1 can optionally drive $\overline{\text{THERM}}$ low as an output. When $\overline{\text{PROCHOT}}$ is bidirectional, $\overline{\text{THERM}}$ can be used to throttle the processor by asserting $\overline{\text{PROCHOT}}$. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle after $\overline{\text{THERM}}$ asserts, it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low, if the Remote 1, Local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bit 5, Bit 6, and Bit 7 of Configuration Register 5 (0x7C) makes $\overline{\text{THERM}}$ bidirectional for the Remote 1, Local, and Remote 2 temperature channels, respectively. Figure 34 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to –64°C or less in Offset 64 mode, or −128°C or less in twos complement mode; that is, for $\overline{\text{THERM}}$ temperature limit values less than –63°C or –128°C, respectively, $\overline{\text{THERM}}$ is disabled. $\overline{\text{THERM}}$ can also be disabled by setting Bit 1 of Configuration Register 3 (0x78) to 0.

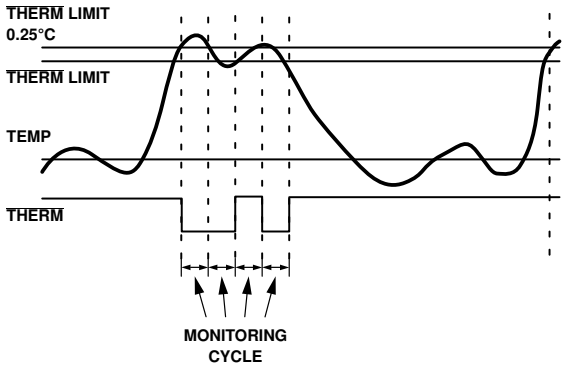


Figure 34. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

Fan Drive Using PWM Control

The ADT7473/ADT7473−1 uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive might need only a pullup resistor. In many cases, the 4-wire fan PWM input has a built-in pullup resistor.

The ADT7473/ADT7473−1 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are usually used for 3-wire fans, while the high frequency option is usually used with 4-wire fans.

Note that care must be taken to ensure that the PWM or TACH pins are not connected to a pullup supply greater than 3.6 V.

Many fans have internal pullups connected to the TACH/PWM pins to a supply greater than 3.6 V. Clamping or dividing down the voltage on these pins must be done where necessary. Clamping these pins with a Zener diode can also help prevent back-EMF related noise from being coupled into the system.

For 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA; therefore, SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM output. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 35 shows how to drive a 3 wire fan using PWM control.

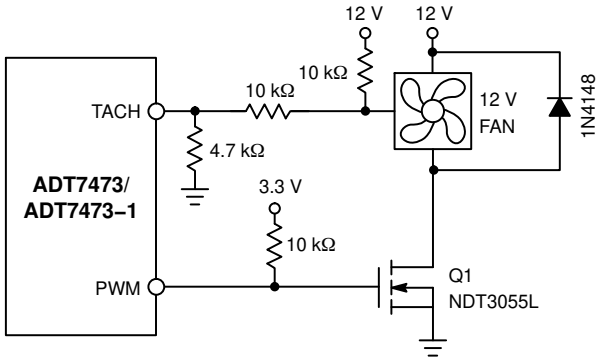


Figure 35. Driving a 3-wire Fan Using an N-channel MOSFET

Figure 35 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 3.6 V maximum to prevent damaging the ADT7473/ADT7473−1. If uncertain as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 36 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

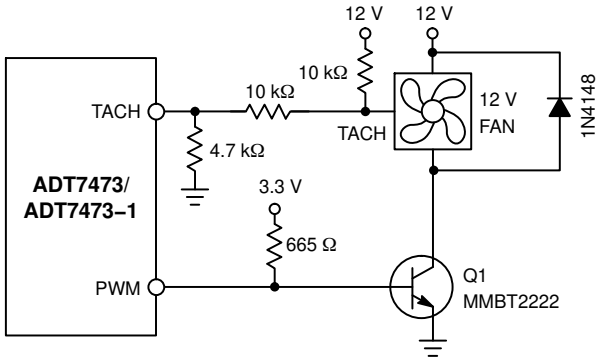


Figure 36. Driving a 3-wire Fan Using an NPN Transistor

Because 4-wire fans are powered continuously, the fan speed is not switched on or off as with previous PWM driven/powered fans. This enables it to perform better than 3-wire fans, especially for high frequency applications.

Figure 37 shows a typical drive circuit for 4-wire fans. As the PWM input on 4-wire fans is usually internally pulled up to a voltage greater than 3.6 V (the maximum voltage allowed on the ADT7473/ADT7473−1 PWM output), the PWM output should be clamped to 3.3 V using a Zener diode.