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ADT7476

Remote Thermal Controller and Voltage Monitor

The ADT7476 controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7476 can drive a fan using either a low or high frequency drive signal and can monitor the temperature of up to two remote sensor diodes plus its own internal temperature. The part also measures and controls the speed of up to four fans, so the fans operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7476 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Monitors Up to Five Voltages
- Controls and Monitors Up to Four Fans
- High and Low Frequency Fan Drive Signal
- One On-Chip and Two Remote Temperature Sensors
- Extended Temperature Measurement Range Up to 191°C
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 3-wire and 4-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

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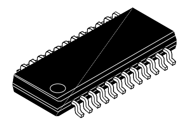
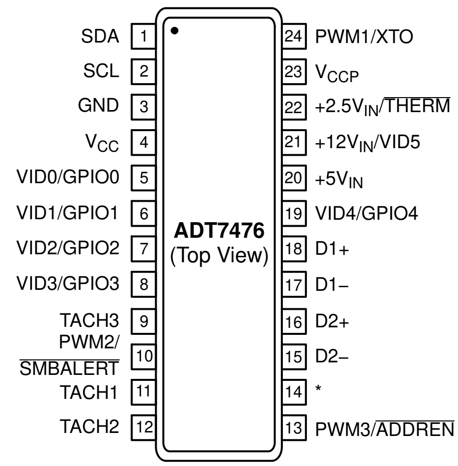


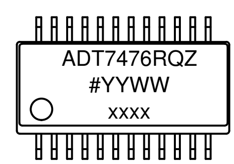
QSOP−24 NB
CASE 492B

PIN ASSIGNMENT



*TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/GPIO6/$\overline{\text{ADDR SELECT}}$

MARKING DIAGRAMS



ADT7476RQZ	= Specific Device Code
#	= Pb-Free Package
YYWW	= Date Code
xxxx	= Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 67 of this data sheet.

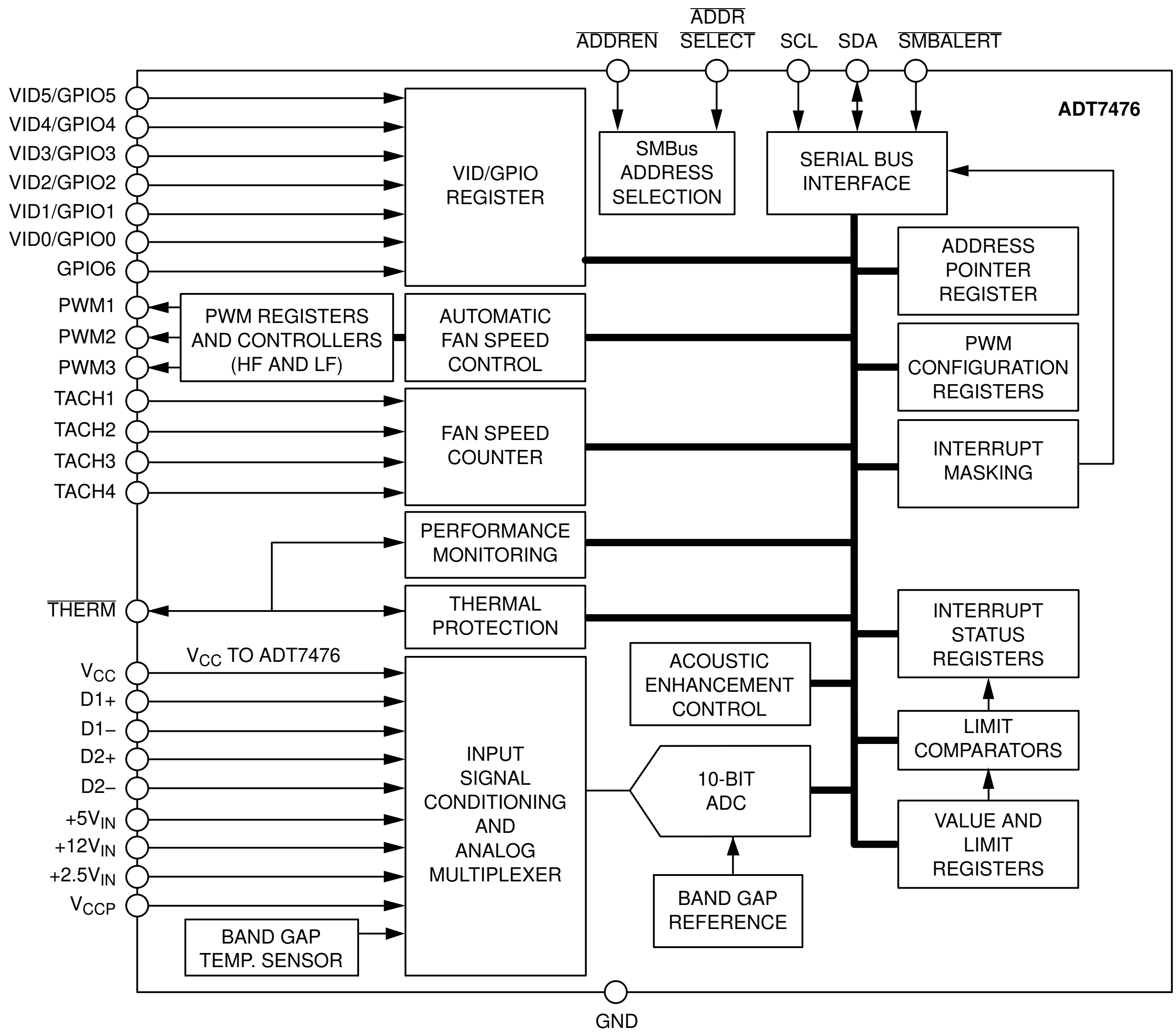


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Maximum Voltage on +12 V_{IN} Pin	16	V
Maximum Voltage on +5.0 V_{IN} Pin	6.25	V
Maximum Voltage on All Open-Drain Outputs	3.6	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	–65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Pb-Free Peak Temperature Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1,500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS (Note 1)

Package Type	θ_{JA}	θ_{JC}	Unit
24-lead QSOP	122	31.25	°C/W

1. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pullup.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
3	GND	Ground Pin.
4	V_{CC}	Power Supply. Powered by 3.3 V standby, if monitoring in low power states is required. V_{CC} is also monitored through this pin.
5	VID0/ GPIO0	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
6	VID1/ GPIO1	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
7	VID2/ GPIO2	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
8	VID3/ GPIO3	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
10	PWM2/ $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.
12	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.
13	PWM3 $\overline{\text{ADDREN}}$	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pullup. Can be configured as a high or low frequency drive. If pulled low on powerup, the ADT7476 enters address select mode, and the state of Pin 14 ($\overline{\text{ADDR SELECT}}$) determines the ADT7476's slave address.
14	TACH4/ $\overline{\text{THERM}}$/ $\overline{\text{SMBALERT}}$/ GPIO6/ $\overline{\text{ADDR SELECT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Alternatively, the pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Times and monitors assertions on the $\overline{\text{THERM}}$ input. For example, it can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions. General-Purpose Open Drain Digital I/O. If in address select mode, the logic state of this pin defines the SMBus device address.
15	D2–	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1–	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4/ GPIO4	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
20	+5.0 V_{IN}	Analog Input. Monitors 5.0 V power supply.
21	+12 V_{IN}/ VID5	Analog Input. Monitors 12 V power supply. Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43).
22	+2.5 V_{IN}/ $\overline{\text{THERM}}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage. Alternatively, this pin can be reconfigured as a bidirectional/omnidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3.0 V).
24	PWM1/ XTO	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 kΩ typical pullup. Also functions as the output from the XOR tree in XOR test mode.

Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface Inactive, ADC Active	–	1.5	3.0	mA
Temperature-to-Digital Converter					
Local Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Diode Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Sensor Source Current	Low Level High Level	– –	11 180	– –	μA
Analog-to-Digital Converter (Including MUX and Attentuators)					
Total Unadjusted Error (TUE)	For 12 V Channel For All Other Channels	– –	– –	±2 ±1.5	%
Differential Non-linearity (DNL)	8 Bits	–	–	±1	LSB
Power Supply Sensitivity		–	±0.1	–	%/V
Conversion Time Voltage Input Local Temperature Remote Temperature	Averaging Enabled	 – – –	 11 12 38	 – – –	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	– –	145 19	– –	ms
Input Resistance	For V_{CCP} channel For all other channels	70 70	120 114	– –	kΩ
Fan RPM-to-Digital Converter					
Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +120°C	– –	– –	±6 ±10	%
Full-Scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5,000 10,000	– – – –	RPM
Open-Drain Digital Outputs, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	20	μA
Open-Drain Serial Data Bus Output (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA
SMBus Digital Inputs (SCL, SDA) (Note 2)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
Digital Input Logic Levels (TACH Inputs)					
Input High Voltage, V_{IH}	Maximum Input Voltage	2.0	–	3.6	V
Input Low Voltage, V_{IL}	Minimum Input Voltage	−0.3	–	0.8	V
Hysteresis		–	0.5	–	V p-p

Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Digital Input Logic Levels (THERM) ADTL+					
Input High Voltage, V_{IH}		0.75 x V_{CCP}	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Digital Input Current					
Input High Current, I_{IH}	V_{IN} = V_{CC}	–	±1	–	μA
Input Low Current, I_{IL}	V_{IN} = 0 V	–	±1	–	μA
Input Capacitance, C_{IN}		–	5.0	–	pF
Serial Bus Timing (See Figure 2)					
Clock Frequency, f_{SCLK}		10	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_r		–	–	1,000	ns
SCL, SDA Fall Time, t_f		–	–	300	μs
Data Setup Time, $t_{SU;DAT}$		250	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge.
2. SMBus timing specifications are guaranteed by design and are not production tested.

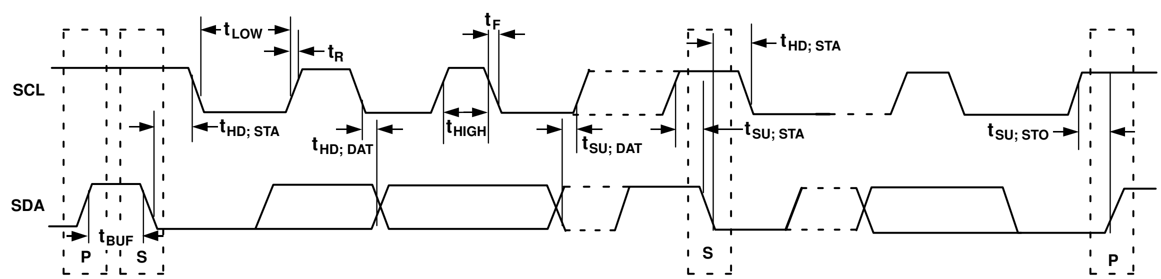


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

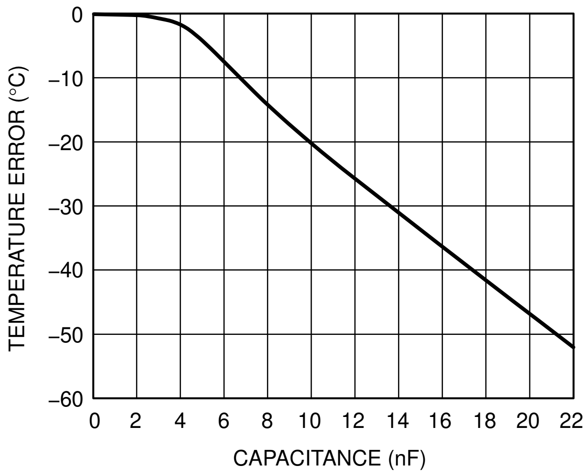


Figure 3. Temperature Error vs. Capacitance Between D+ and D–

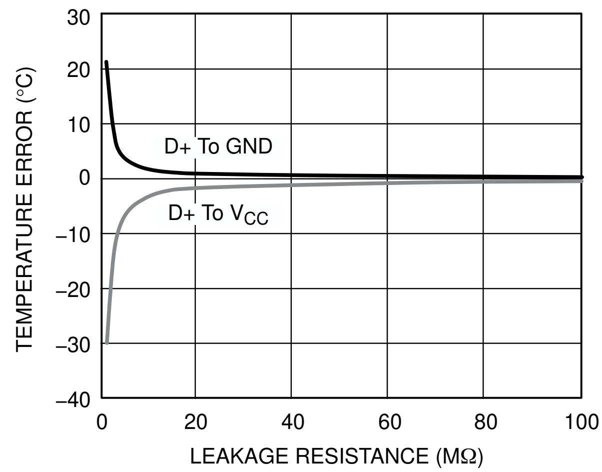


Figure 4. Remote Temperature Error vs. PCB Resistance

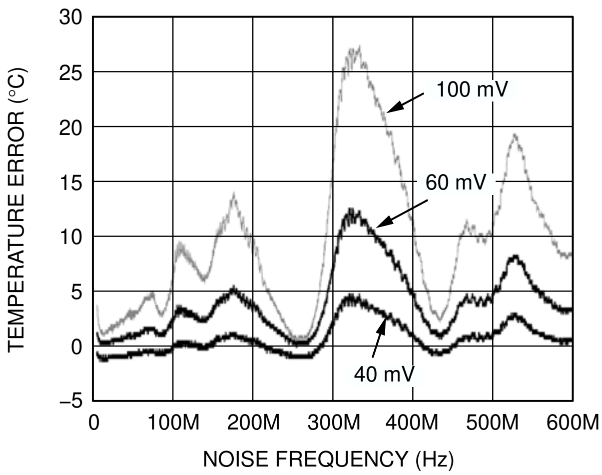


Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

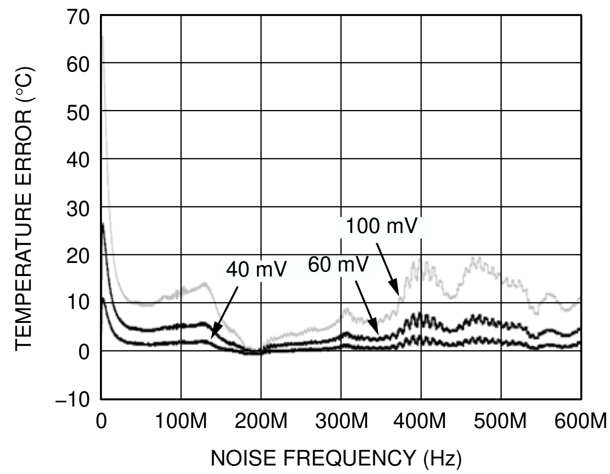


Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

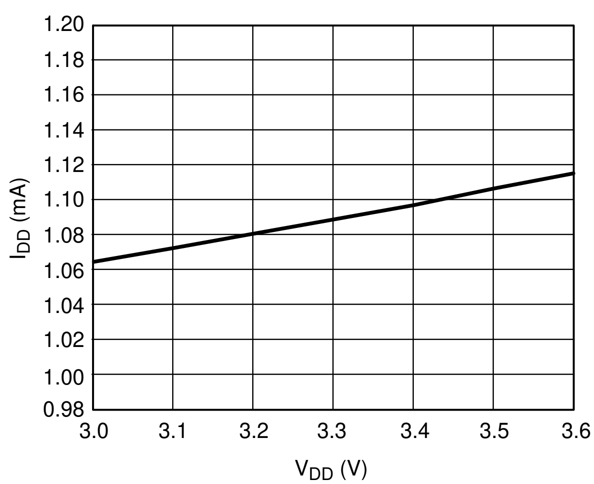


Figure 7. Normal I_{DD} vs. Power Supply

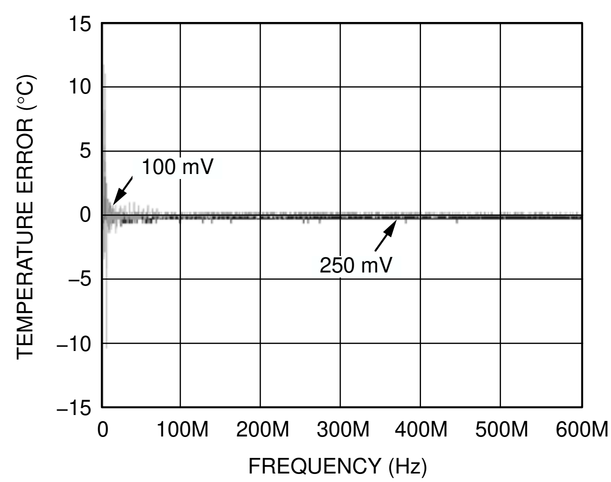


Figure 8. Internal Temperature Error vs. Power Supply Noise

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

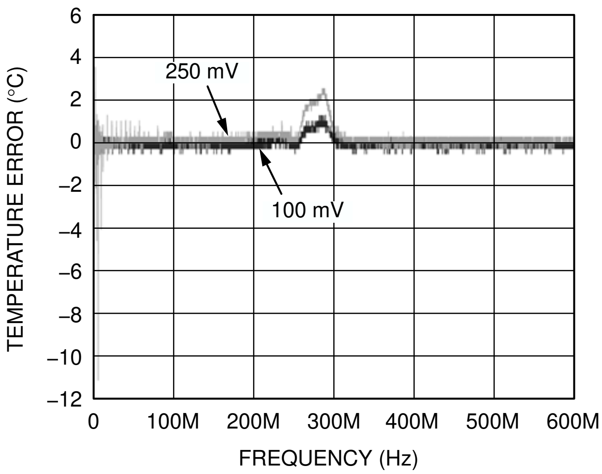


Figure 9. Remote Temperature Error vs. Power Supply Noise Frequency

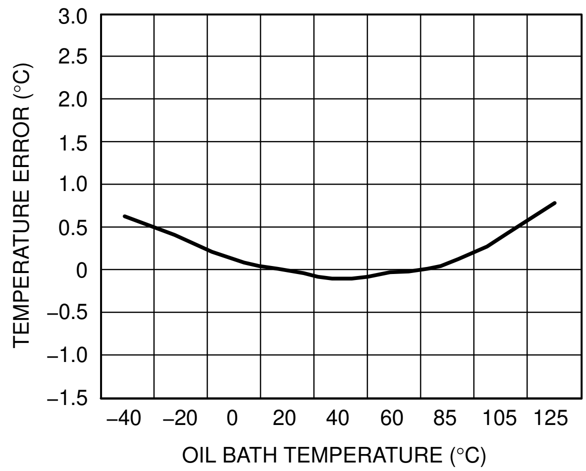


Figure 10. Internal Temperature Error vs. Temperature

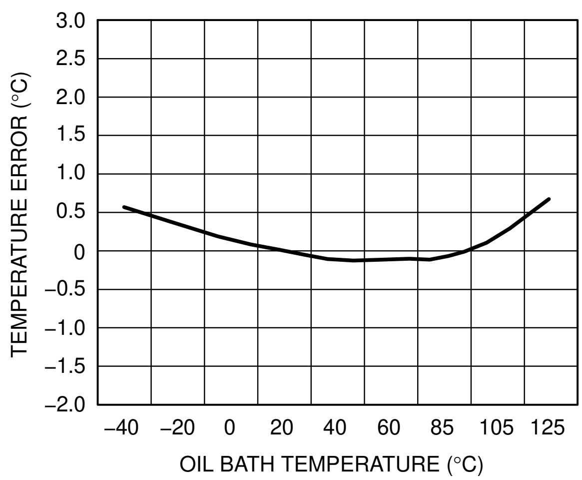


Figure 11. Remote Temperature Error vs. Temperature

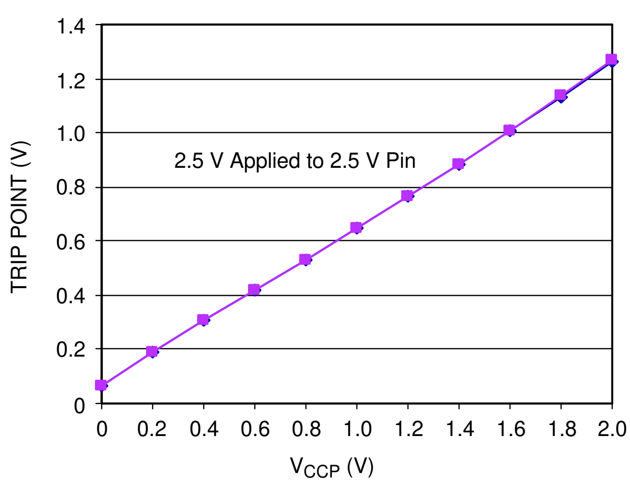


Figure 12. $\overline{\text{THERM}}$ Input Threshold vs. V_{CCP} Voltage

Product Description

The ADT7476 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7476 are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Feature Comparisons Between ADT7476 and ADT7468

- Dynamic T_{MIN}, dynamic operating point, and associated registers are no longer available in the ADT7476. The following related registers are gone:
  - Calibration Control 1 (0x36)
  - Calibration Control 2 (0x37)
  - Operating Point (0x33, 0x34, and 0x35)
- Previously (in the ADT7468), T_{RANGE} defined the slope of the automatic fan control algorithm. T_{RANGE} now defines a true temperature range (in the ADT7476).
- Acoustic filtering is now assigned to temperature zones, not to fans. Available smoothing times have been increased for better acoustic performance.
- Temperature measurements are now made with two switching currents instead of three. SRC is not available in the ADT7476.
- High frequency PWM can now be enabled/disabled on each PWM output individually.
- $\overline{\text{THERM}}$ can now be enabled/disabled on each temperature channel individually.
- The ADT7476 does not support full shutdown mode.
- The ADT7476 offers increased temperature accuracy on all temperature channels.
- The ADT7476 defaults to twos complement temperature measurement mode.
- Some pins have swapped/added functions.
- The powerup routine for the ADT7476 is simplified.
- The ADT7476 has a higher maximum input voltage TACH/PWM spec, supporting a wider range of fans.
- $V_{CORE\_LOW\_ENABLE}$ has been reallocated to Bit 7 of Configuration Register 1 (0x40).

Recommended Implementation

Configuring the ADT7476 as shown in Figure 13 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU temperature measured using Remote 1 temperature channel.
- Remote temperature zone measured through Remote 2 temperature channel.
- Local temperature zone measured through the internal temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

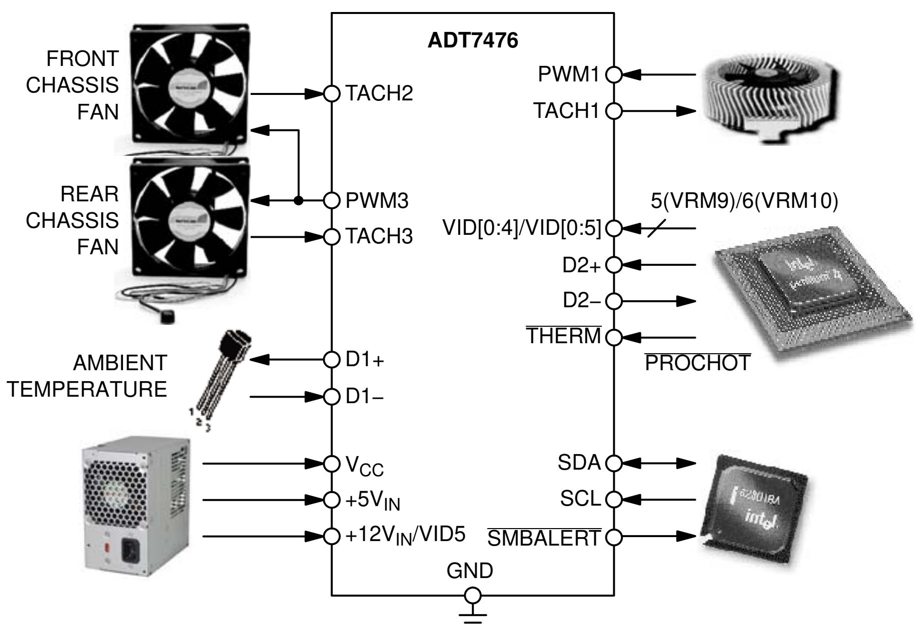


Figure 13. ADT7476 Configuration

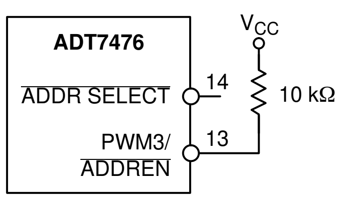
Serial Bus Interface

Control of the ADT7476 is carried out using the serial system management bus (SMBus). The ADT7476 is connected to this bus as a slave device, under the control of a master controller. The ADT7476 has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/ADDREN) high, the ADT7476 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address. If more than one ADT7476 is to be used in a system, each ADT7476 is placed in ADDR SELECT mode by strapping Pin 13 low on powerup. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is sampled on powerup and latched on the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the ADDREN pin/ADDR SELECT pin. Any attempted changes in the address have no effect after this.

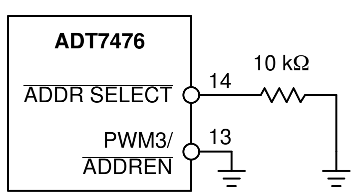
Table 5. HARDWIRING THE ADT7476 SMBUS DEVICE ADDRESS

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pullup)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E)



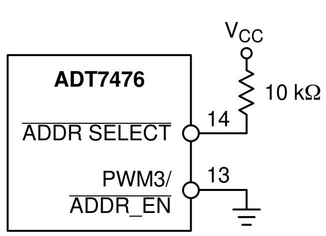
ADDRESS = 0x2E

Figure 14. Default SMBus Address = 0x2E



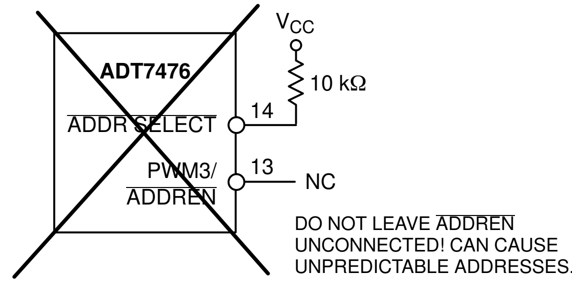
ADDRESS = 0x2C

Figure 15. SMBus Address = 0x2C (Pin 14 = 0)



ADDRESS = 0x2D

Figure 16. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/ADDREN) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7476 TO POWER UP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7476 IS PLACED INTO ADDR SELECT MODE, PINS 13 AND 14 CANNOT BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/THERM) UNLESS THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME OR DESIGNED TO HANDLE THESE DUAL FUNCTIONS.

Figure 17. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7476 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first), plus a R/W bit, which determine the direction of the data transfer, that is, whether data is written to or read from the slave device.
   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master writes to the slave device. If the R/W bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period. A low-to-high transition, when the clock is high, can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10^{th} clock

pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10^{th} clock pulse, and then high during the 10^{th} clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. However, it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In the ADT7476, write operations contain either one or two bytes, and read operations contain one byte.

To write data to one of the device data registers or read data from it, the address pointer register must be set so the correct data register is addressed. Then, data can be written into that register or read from it. The first byte of a write operation always contains an address stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 18. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7476's address pointer register value is unknown, or not the desired value, then it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7476 as before, but only the data byte containing the register address is sent, because no data is written to the register (see Figure 19).
   A read operation is then performed consisting of the serial bus address; R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register (see Figure 20.)
2. If the address pointer register is already known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 20).

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7476 also supports the read byte protocol. See Intel's System Management Bus Specifications Revision 2 for more information.

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

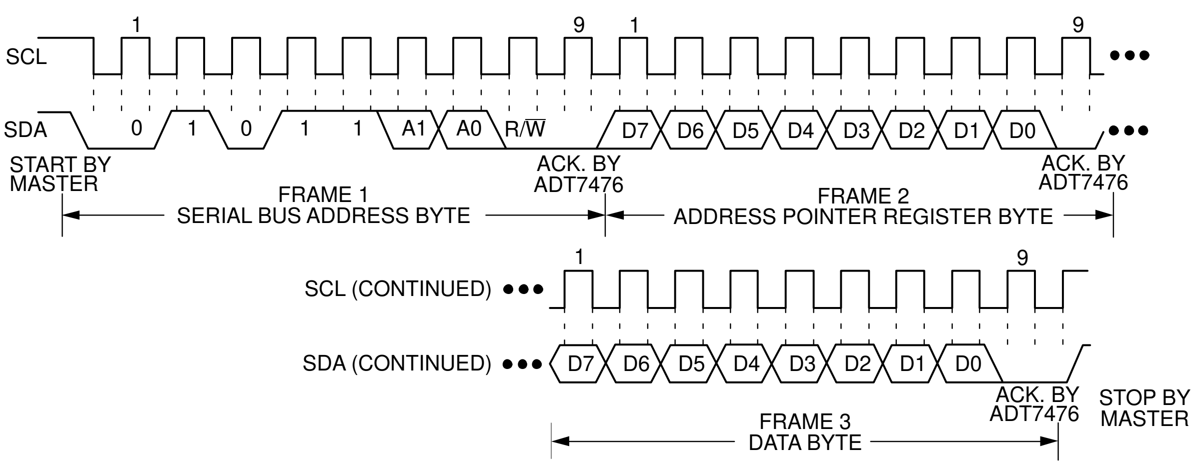


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

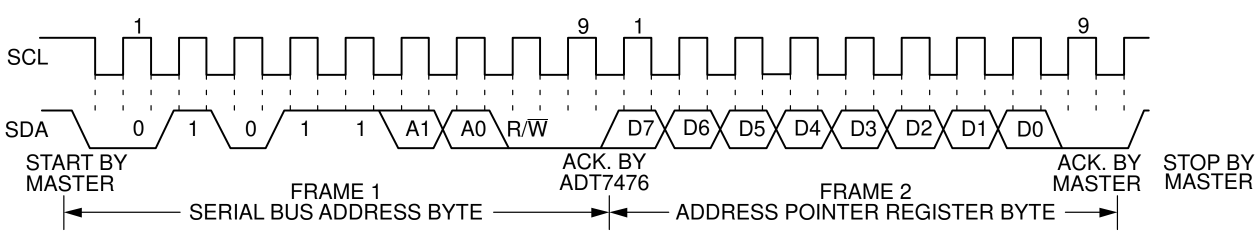


Figure 19. Writing to the Address Pointer Register Only

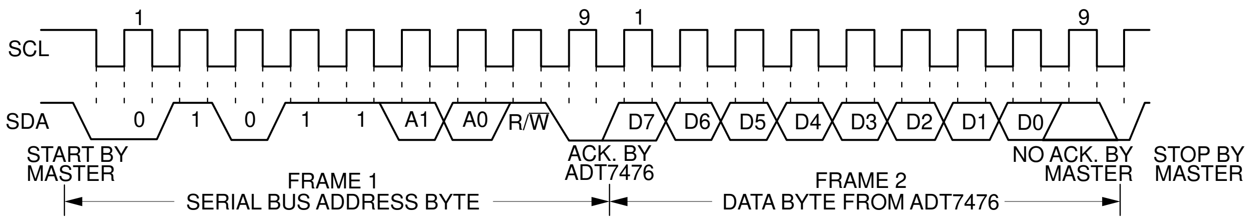


Figure 20. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7476 are discussed below. The following abbreviations are used in the diagrams:

- S – START
- P – STOP
- R – READ
- $\overline{\text{W}}$ – WRITE
- A – ACKNOWLEDGE
- $\overline{\text{A}}$ – NO ACKNOWLEDGE

The ADT7476 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7476, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 21.

1	2		3	4	5	6
S	SLAVE ADDRESS	W	A	REGISTER ADDRESS	A	P

Figure 21. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

This operation is illustrated in Figure 22.

1	2		3	4	5	6	7	8
S	SLAVE ADDRESS	W	A	REGISTER ADDRESS	A	DATA	A	P

Figure 22. Single-byte Write to a Register

Read Operations

The ADT7476 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address is set up beforehand. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7476, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 23.

1	2		3	4	5	6
S	SLAVE ADDRESS	R	A	DATA	$\overline{\text{A}}$	P

Figure 23. Single-byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices, allowing an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of this device is now known and can be interrogated per usual.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7476 responds to the alert response address, the master must read the status registers, and $\overline{\text{SMBALERT}}$ is cleared only if the error condition goes away.

SMBus Timeout

The ADT7476 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7476 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so if necessary, it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description
[6] TODIS	0: SMBus Timeout Enabled (Default) 1: SMBus Timeout Disabled

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7476 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7476 is powered down and powered up again. For more information on which registers are locked see Table 49.

Voltage Measurement Input

The ADT7476 has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}. Pin 20 to Pin 23 can measure 5.0 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive-approximation, analog-to-digital converter, which has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built−in attenuators to allow measurement of 2.5 V, 3.3 V, 5.0 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 dec or 300 hex) for the nominal input voltage, giving it adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 24 The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives input immunity to high frequency noise.

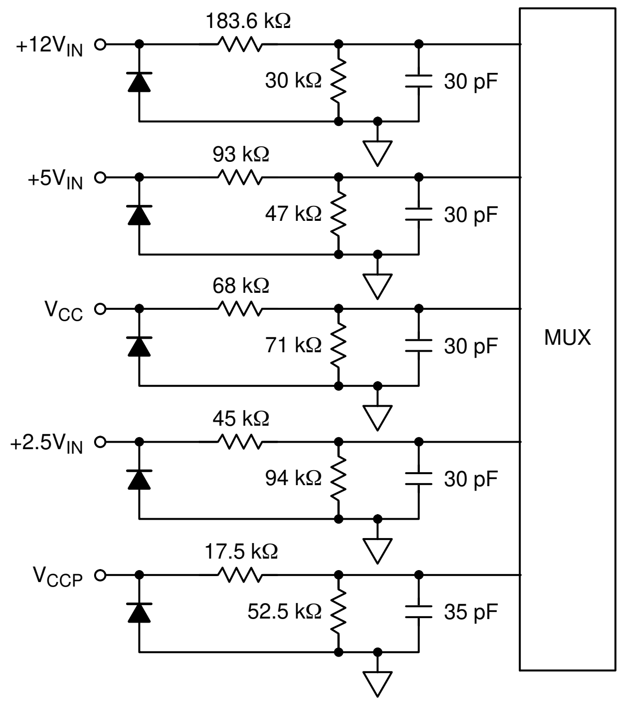


Figure 24. Structure of Analog Inputs

Table 7. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x20	2.5 V Reading	0x00
0x21	V_{CCP} Reading	0x00
0x22	V_{CC} Reading	0x00
0x23	5.0 V Reading	0x00
0x24	12 V Reading	0x00

Voltage Limit Registers

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 8. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5.0 V Low Limit	0x00
0x4B	5.0 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 13 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x76 and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x20 to 0x24) is locked until their data is read. That is, if extended resolution is required, then the extended resolution register must be read first, immediately followed by the appropriate voltage measurement register.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7476 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage/temperature measurement read from a value register, 16 readings have been made internally and the results averaged before being placed into the value register. When faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster but the reading can be noisier. The default round robin cycle time takes 146.5 ms.

Table 9. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round robin cycle time increases to 240 ms.

Bypass All Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5.0 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Bypass Individual Voltage Input Attenuators

Bits [7:4] of Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 10. BYPASSING INDIVIDUAL VOLTAGE INPUT ATTENUATORS

Configuration Register 4 (0x7D)	
Bit No.	**Channel Attenuated**
[4]	Bypass 2.5 V Attenuator
[5]	Bypass V_{CCP} Attenuator
[6]	Bypass 5.0 V Attenuator
[7]	Bypass 12 V Attenuator

Table 11. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
[4]	1: Averaging Off
[5]	1: Bypass Input Attenuators
[6]	1: Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

[7:5] Selects ADC channel for single-channel convert mode.

Single-channel ADC Conversion

While single-channel mode is intended as a test mode that can be used to increase sampling times for a specific channel, and therefore helps to analyze that channel's performance in greater detail, it can also have other applications.

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7476 into single-channel ADC conversion mode. In this mode, the ADT7476 can only read a single voltage channel. The selected voltage input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 12. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits [7:4], Register 0x55	**Channel Selected** (Note 1)
000	2.5 V
001	V_{CCP}
010	V_{CC}
011	5.0 V
100	12 V
101	Remote 1 temperature
110	Local temperature
111	Remote 2 temperature

1. In the process of configuring single-channel ADC conversion mode, the TACH1 minimum high byte is also changed, possibly trading off TACH1 minimum high byte functionality with single-channel mode functionality.

Table 13. 10-BIT ADC OUTPUT CODE VS. V_{IN}

Input Voltage						ADC Output	
12 V_{IN}	5.0 V_{IN}	V_{CC} (3.3 V_{IN})	2.5 V_{IN}	V_{CCP}	V_{TT}/I_{MON}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	<0.00220	0	00000000 00
0.0156 to 0.0312	0.0065 to 0.0130	0.0042 to 0.0085	0.0032 to 0.0065	0.0293 to 0.0058	0.00220 to 0.00440	1	00000000 01
0.0312 to 0.0469	0.0130 to 0.0195	0.0085 to 0.0128	0.0065 to 0.0097	0.0058 to 0.0087	0.00440 to 0,00660	2	00000000 10
0.0469 to 0.0625	0.0195 to 0.0260	0.0128 to 0.0171	0.0097 to 0.0130	0.0087 to 0.0117	0,00660 to 0.00881	3	00000000 11
0.0625 to 0.0781	0.0260 to 0.0325	0.0171 to 0.0214	0.0130 to 0.0162	0.0117 to 0.0146	0.00881 to 0.01100	4	00000001 00
0.0781 to 0.0937	0.0325 to 0.0390	0.0214 to 0.0257	0.0162 to 0.0195	0.0146 to 0.0175	0.01100 to 0.01320	5	00000001 01
0.0937 to 0.1093	0.0390 to 0.0455	0.0257 to 0.0300	0.0195 to 0.0227	0.0175 to 0.0205	0.01320 to 0.01541	6	00000001 10
0.1093 to 0.1250	0.0455 to 0.0521	0.0300 to 0.0343	0.0227 to 0.0260	0.0205 to 0.0234	0.01541 to 0.01761	7	00000001 11
0.1250 to 0.14060	0.0521 to 0.0586	0.0343 to 0.0386	0.0260 to 0.0292	0.0234 to 0.0263	0.01761 to 0.01981	8	00000010 00
–	–	–	–	–	–	–	–
4.0000 to 4.0156	1.6675 to 1.6740	1.1000 to 1.1042	0.8325 to 0.8357	0.7500 to 0.7529	0.5636 to 0.5658	256 (1/4 scale)	01000000 00
–	–	–	–	–	–	–	–
8.0000 to 8.0156	3.3300 to 3.3415	2.2000–2.2042	1.6650 to 1.6682	1.5000 to 1.5029	1.1272 to 1.1294	512 (1/2 scale)	10000000 00
–	–	–	–	–	–	–	–
12.0000 to 12.0156	5.0025 to 5.0090	3.3000 to 3.3042	2.4975 to 2.5007	2.2500 to 2.2529	1.6809 to 1.6930	768 (3/4 scale)	11000000 00
–	–	–	–	–	–	–	–
15.8281 to 15.8437	6.5983 to 6.6048	4.3527 to 4.3570	3.2942 to 3.2974	2.9677 to 2.9707	2.2301 to 2.2323	1013	11111101 01
15.8437 to 15.8593	6.6048 to 6.6113	4.3570 to 4.3613	3.2974 to 3.3007	2.9707 to 2.9736	2.2323 to 2.2346	1014	11111101 10
15.8593 to 15.8750	6.6113 to 6.6178	4.3613 to 4.3656	3.3007 to 3.3039	2.9736 to 2.9765	2.2346 to 2.2368	1015	11111101 11
15.8750 to 15.8906	6.6178 to 6.6244	4.3656 to 4.3699	3.3039 to 3.3072	2.9765 to 2.9794	2.2368 to 2.23899	1016	11111110 00
15.8906 to 15.9062	6.6244 to 6.6309	4.3699 to 4.3742	3.3072 to 3.3104	2.9794 to 2.9824	2,23899 to 2.2412	1017	11111110 01
15.9062 to 15.9218	6.6309 to 6.6374	4.3742 to 4.3785	3.3104 to 3.3137	2.9824 to 2.9853	2.2412 to 2.2434	1018	11111110 10
15.9218 to 15.9375	6.6374 to 6.4390	4.3785 to 4.3828	3.3137 to 3.3169	2.9853 to 2.9882	2.2434 to 2.2456	1019	11111110 11
15.9375 to 15.9531	6.6439 to 6.6504	4.3828 to 4.3871	3.3169 to 3.3202	2.9882 to 2.9912	2.2456 to 2.2478	1020	11111111 00
15.9531 to 15.9687	6.6504 to 6.6569	4.3871 to 4.3914	3.3202 to 3.3234	2.9912 to 2.9941	2.2478 to 2.25	1021	11111111 01
15.9687 to 15.9843	6.6569 to 6.6634	4.3914 to 4.3957	3.3234 to 3.3267	2.9941 to 2.9970	2.25 to 2.2522	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	>2.2522	1023	11111111 11

VID Code Monitoring

The ADT7476 has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID/GPIO register (0x43) to determine the processor voltage required or the system being used. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

VID/GPIO Register (0x43)

[0] = VID0, reflects logic state of Pin 5.

[1] = VID1, reflects logic state of Pin 6.

[2] = VID2, reflects logic state of Pin 7.

[3] = VID3, reflects logic state of Pin 8.

[4] = VID4, reflects logic state of Pin 19.

[5] = VID5, reconfigurable 12 V input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID Code Input Threshold Voltage

The switching threshold for the VID code inputs is approximately 1.0 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of the VID/GPIO register (0x43) controls the VID input threshold voltage.

VID/GPIO Register (0x43)

[6] THLD = 0, VID switching threshold = 1.0 V,
V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V.

[6] THLD = 1, VID switching threshold = 0.6 V,
V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V.

Reconfiguring Pin 21 as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10 compatible systems. Because the pin is configured as VID5, it is not possible to monitor a 12 V supply.

Bit 7 of the VID/GPIO register (0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or a sixth VID input.

VID/GPIO Register (0x43)

[7] VIDSEL = 0, Pin 21 functions as a 12 V measurement input. Software can read this bit to determine that there are five VID inputs being monitored. Bit 5 of VID/GPIO Register (0x43) always reads back 0. Bit 0 of Interrupt Status Register 2 (0x42) reflects 12 V out-of-limit measurements.

[7] VIDSEL = 1, Pin 21 functions as the sixth VID code input (VID5). Software can read this bit to determine that there are six VID inputs being monitored. Bit 5 of Register 0x43 reflects the logic state of Pin 21. Bit 0 of Interrupt Status Register 2 (0x42) reflects VID code changes.

VID Code Change Detect Function

The ADT7476 has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes are detected and reported back by the ADT7476. Bit 0 of Interrupt Status Register 2 (0x42) is the 12 V/VC bit and denotes a VID change when set. The VID code change bit is set when the logic states on the VID inputs are different than they were 11 μs previously. The change of VID code is used to generate an $\overline{\text{SMBALERT}}$ interrupt. If an $\overline{\text{SMBALERT}}$ interrupt is not required, Bit 0 of Interrupt Mask Register 2 (0x75), when set, prevents $\overline{\text{SMBALERT}}$s from occurring on VID code changes.

Interrupt Status Register 2 (0x42)

[0] 12 V/VC = 0, if Pin 21 is configured as VID5, Logic 0 denotes no change in VID code within the last 11 μs.

[0] 12 V/VC = 1, if Pin 21 is configured as VID5, Logic 1 means that a change has occurred on the VID code inputs within the last 11 μs. An $\overline{\text{SMBALERT}}$ is generated, if this function is enabled.

Programming the GPIOs

The ADT7476 follows an upgrade path from the ADM1027 to the ADT7476. In order to maintain consistency between versions, it is necessary to omit references to GPIO5. As a result, there are six GPIOs as follows: GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO6.

Setting Bit 4 of Configuration Register 5 (0x7C) to 1 enables GPIO functionality. This turns all pins configured as VID inputs into general-purpose outputs. Writing to the corresponding VID bit in the VID/GPIO register (0x43) sets the polarity for the corresponding GPIO. GPIO6 can be programmed independently as, for example, an input or output, using Bits [3:2] of Configuration Register 5 (0x7C).

Temperature Measurement Method

Local Temperature Measurement

The ADT7476 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (Addresses 0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 14 and Table 15. Theoretically, the temperature sensor and ADC can measure temperatures from −63°C to +127°C (or −61°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7476 operating temperature range are not possible.

Table 14. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
–128°C	1000 0000 **00** (Diode Fault)
–50°C	1100 1110 **00**
–25°C	1110 0111 **00**
–10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSB of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 15. EXTENDED RANGE, TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-Bit) (Note 1)
–64°C	0000 0000 **00** (Diode Fault)
–1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSB of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Remote Temperature Measurement

The ADT7476 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 17 and Pin 18, or Pin 15 and Pin 16.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out. As a result, this technique is unsuitable for mass production. The technique used in the ADT7476 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = \frac{kT}{q} \times \ln(N) \qquad \text{(eq. 1)}$$

where:

k is the Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

Figure 25 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, which is provided on some microprocessors for temperature monitoring. It could also be a discrete transistor such as a 2N3904/2N3906.

If a discrete transistor is used, the collector is not grounded and is linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figure 26 and Figure 27 show how to connect the ADT7476 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

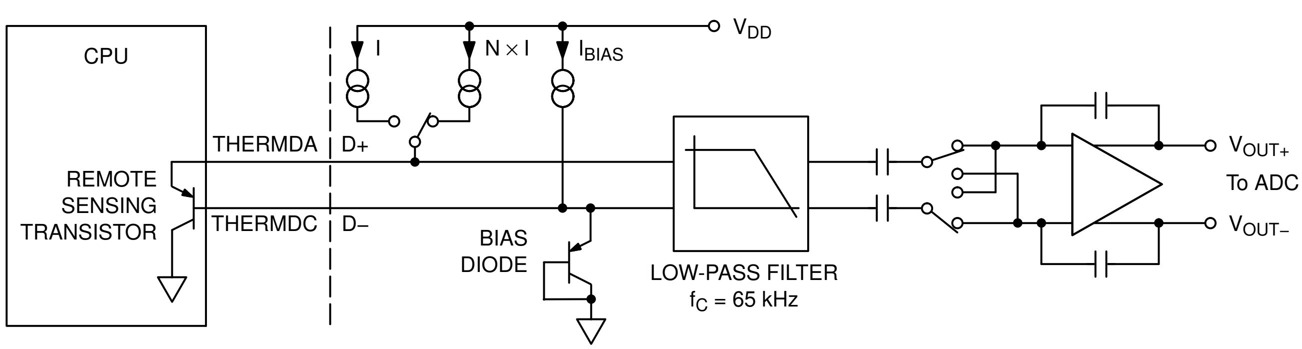


Figure 25. Signal Conditioning for Remote Diode Temperature Sensors

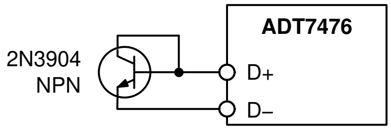


Figure 26. Measuring Temperature by Using an NPN Transistor

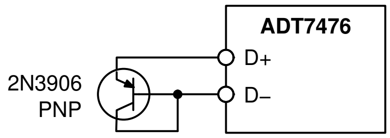


Figure 27. Measuring Temperature by Using a PNP Transistor

To measure ΔV_{BE}, the sensor switches between operating currents of I and $N \times I$. The resulting waveform passes through a 65 kHz low-pass filter to remove noise and through a chopper-stabilized amplifier. The amplifier performs the amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

A remote temperature measurement takes nominally 38 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 10. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice placed a capacitor across the D+ pin and the D– pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

This capacitor reduces the noise but does not eliminate it, which makes using the sensor difficult in a very noisy environment. In most cases, a capacitor is not required because differential inputs by their very nature have a high immunity to noise.

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7476 is designed to work with substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D–. If a PNP transistor is used, the collector and base are connected to D– and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7476 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C), when using a transistor whose n_f does not equal 1.008 (see the processor's data sheet for the n_f values):

$$\Delta T = (nf - 1.008) \times (273.15\ K + T) \qquad \text{(eq. 2)}$$

  To factor this in, the user can write the ΔT value to the offset register. The ADT7476 then automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7476, I_{HIGH}, is 180 μA, and the low level current, I_{LOW}, is 11 μA. If the ADT7476 current levels do not match the current levels specified by the CPU manufacturer, it could be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, then the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7476, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 11 μA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 180 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in the current gain, h_{FE}, (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT–23 packages, are suitable devices to use.

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D– traces around a system board. Even when recommended layout guidelines are followed, some temperature errors can still be attributable to noise coupled onto the D+/D– lines. Constant high frequency noise usually attenuates, or increases, temperature measurements by a linear, constant value.

The ADT7476 has temperature offset registers (0x70 and 0x72) for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement.

Changing Bit 1 of Configuration Register 5 (0x7C) changes the resolution and therefore, the range of the temperature offset as either having a −63°C to +127°C range with a resolution of 1°C or having a −63°C to +64°C range with a resolution of 0.5°C. This temperature offset can be used to compensate for linear temperature errors introduced by noise.

Table 16. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

ADT7463/ADT7476 Backwards Compatible Mode

By setting Bit 0 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature reading registers (0x25, 0x26, and 0x27) in twos complement in the −63°C to +127°C range. The temperature limits must be reprogrammed in twos complement.

If a twos complement temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, while in the extended temperature range (−63°C to +191°C), the fault condition is represented by −64°C = 0000 0000.

Table 17. TEMPERATURE READING REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	–
0x26	Local Temperature	–
0x27	Remote 2 Temperature	–
0x77	Extended Resolution 2	0x00

Table 18. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
[7:6]	TDM2	Remote 2 Temperature LSBs
[5:4]	LTMP	Local Temperature LSBs
[3:2]	TDM1	Remote 1 Temperature LSBs

Temperature Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Table 19. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7476

It is important to note that temperature can be read from the ADT7476 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. Extended Resolution Register 2 (0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7476 to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. The default round robin cycle time takes 146.5 ms.

Table 20. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round robin cycle time increases to 240 ms.

Table 21. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature	39
Local Temperature	12

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7476 into single-channel ADC conversion mode. In this mode, the ADT7476 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 22. PROGRAMMING SINGLE-CHANNEL ADC MODE FOR TEMPERATURES

Bits [7:5], Register 0x55	Channel Selected
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Table 23. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
[4]	1: Averaging Off
[6]	1: Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

[7:5] selects ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the THERM temperature limits. When a temperature exceeds its THERM temperature limit, all PWM outputs run at the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A). This effectively runs the fans at the fastest allowed speed.

The fans run at this speed until the temperature drops below THERM minus hysteresis. This can be disabled by setting Bit 2, the boost bit, in Configuration Register 3 (0x78). The hysteresis value for the THERM temperature limit is the value programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

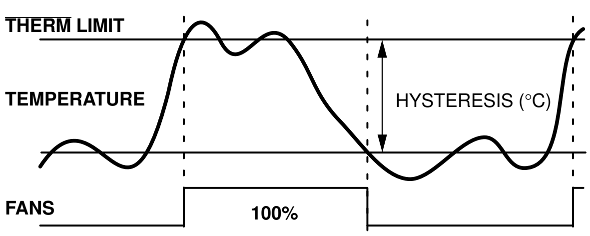


Figure 28. THERM Temperature Limit Operation

THERM can be disabled on specific temperature channels using Bits [7:5] of Configuration Register 5 (0x7C). THERM can also be disabled by:

- Writing −64°C to the appropriate THERM temperature limit in Offset 64 mode.
- Writing −128°C to the appropriate THERM temperature limit in twos complement mode.

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7476 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, SMBALERT interrupts can be generated to flag out-of-limit conditions to a processor or microcontroller.

8-bit Limits

The following is a list of 8-bit limits on the ADT7476.

Table 24. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5.0 V Low Limit	0x00
0x4B	5.0 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 25. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 THERM Temp. Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local THERM Temperature Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 THERM Temp. Limit	0x64

Table 26. THERM TIMER LIMIT REGISTER

Register	Description	Default
0x7A	THERM Timer Limit	0x00

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 27. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7476 can be enabled for monitoring. The ADT7476 measures all voltage and temperature measurements in round robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed
Low Limit: ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). The ADC measures each analog input in turn, and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

- Four Dedicated Supply Voltage Inputs
- Supply Voltage (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally:

$$(5 \times 11) + 12 + (2 \times 39) = 145 \text{ ms} \quad \text{(eq. 3)}$$

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out-of-limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), 1 means an out-of-limit event has been flagged in Interrupt Status Register 2. This means the user also needs to read Interrupt Status Register 2. Alternatively, Pin 10 or Pin 14 can be configured as an SMBALERT output. This hard interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the status bit is to read the status register after the event has gone away. Interrupt mask registers (0x74 and 0x75) allow individual interrupt sources to be masked from causing an SMBALERT. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the status registers.

Table 28. INTERRUPT STATUS REGISTER 1 (0X41)

Bit	Mnemonic	Description
7	OOL	1 denotes a bit in Interrupt Status Register 2 is set and Interrupt Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 Temperature High or Low limit has been exceeded.
5	LT	1 indicates that the Local Temperature High or Low Limit has been exceeded.
4	R1T	1 indicates that the Remote 1 Temperature High or Low Limit has been exceeded.
3	5.0 V	1 indicates that the 5.0 V High or Low Limit has been exceeded.
2	V_{CC}	1 indicates that the V_{CC} High or Low Limit has been exceeded.
1	V_{CCP}	1 indicates that the V_{CCP} High or Low Limit has been exceeded.
0	2.5 V	1 indicates that the 2.5 V High or Low Limit has been exceeded. If the 2.5 V input is configured as THERM, this bit represents the status of THERM.

Table 29. INTERRUPT STATUS REGISTER 2 (0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D1+/D1− inputs.
5	F4P	1 indicates Fan 4 has dropped below minimum speed. Alternatively, indicates that the THERM limit has been exceeded, if the THERM function is used. Alternatively, indicates the status of GPIO6.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a THERM overtemperature limit has been exceeded.
0	12 V/VC	1 indicates a 12 V high or low limit has been exceeded. If the VID code change function is used, this bit indicates a change in VID code on the VID0 to VID4 inputs.

SMBALERT Interrupt Behavior

The ADT7476 can be polled for status, or an SMBALERT interrupt can be generated for out-of-limit conditions. It is important to note how the SMBALERT output and status bits behave when writing interrupt handler software.

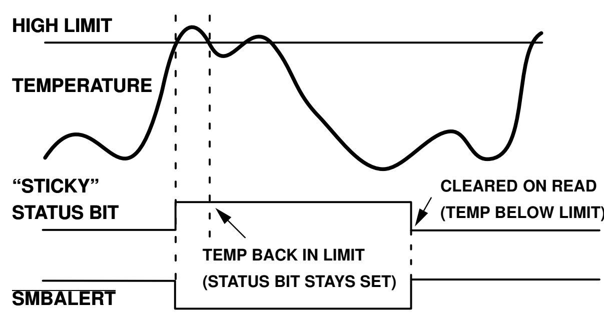


Figure 29. SMBALERT and Status Bit Behavior

Figure 29 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if the software is periodically polling the device.

Note that:

- The SMBALERT output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.
- THERM overtemperature events are not *sticky*. They reset immediately after the overtemperature condition ceases.

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74 and 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 30.

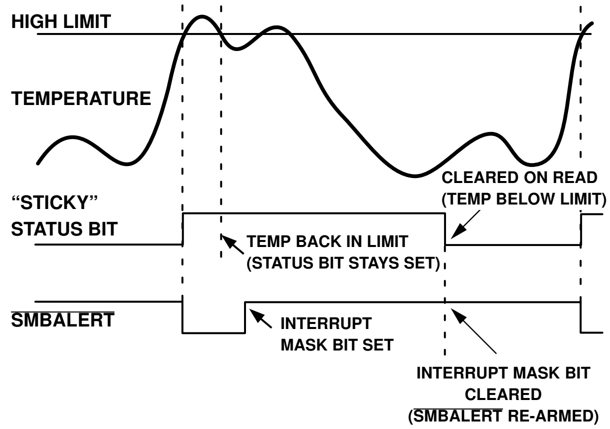


Figure 30. How Masking the Interrupt Source Affects SMBALERT Output

Masking Interrupt Sources

Interrupt Mask Register 1 (0x74) and Interrupt Mask Register 2 (0x75) allow individual interrupt sources to be masked to prevent SMBALERT interrupts.

NOTE: Masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

Table 30. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Interrupt Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature.
5	LT	1 masks SMBALERT for Local temperature.
4	R1T	1 masks SMBALERT for Remote 1 temperature.
3	5.0 V	1 masks SMBALERT for the 5.0 V channel.
2	V_{CC}	1 masks SMBALERT for the V_{CC} channel.
1	V_{CCP}	1 masks SMBALERT for the V_{CCP} channel.
0	2.5 V	1 masks SMBALERT for the 2.5 V_{IN}/THERM channel.

Table 31. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event. If the TACH4 pin is being used as GPIO6, setting this bit masks interrupts related to GPIO6.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).
0	12 V/VC	1 masks SMBALERT for 12 V channel or for a VID code change, depending on the function used.

Enabling the SMBALERT Interrupt Output

The SMBALERT interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Table 32. CONFIGURING PIN 10 AS SMBALERT OUTPUT

Register	Bit Setting
Configuration Register 3 (0x78)	[1] Pin 10 = SMBALERT [0] Pin 10 = PWM2

Assigning THERM Functionality to a Pin

Pin 14 on the ADT7476 has four possible functions: SMBALERT, THERM, GPIO6, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 (0x7D).

If THERM is enabled on Bit 1, Configuration Register 3 (0x78):

- Pin 22 becomes THERM.
- If Pin 14 is configured as THERM on Bit 0 and Bit 1 of Configuration Register 4 (0x7D), THERM is enabled on this pin.

If THERM is not enabled:

- Pin 22 becomes a 2.5 V measurement input.
- If Pin 14 is configured as THERM, then THERM is disabled on this pin.

Table 33. CONFIGURING PIN 14

Bit 1	Bit 0	Function
0	0	TACH4
0	1	THERM
1	0	SMBALERT
1	1	GPIO6

THERM as an Input

When THERM is configured as an input, the user can time assertions on the THERM pin. This can be useful for connecting to the PROCHOT output of a CPU to gauge system performance.

When the THERM pin is driven low externally, the user can also set up the ADT7476 to run the fans at 100%. The fans run at 100% for the duration of time that the THERM pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This works only if the fan is already running, for example, in manual mode, when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}.

If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the THERM low externally has no effect. See Figure 31 for more information.

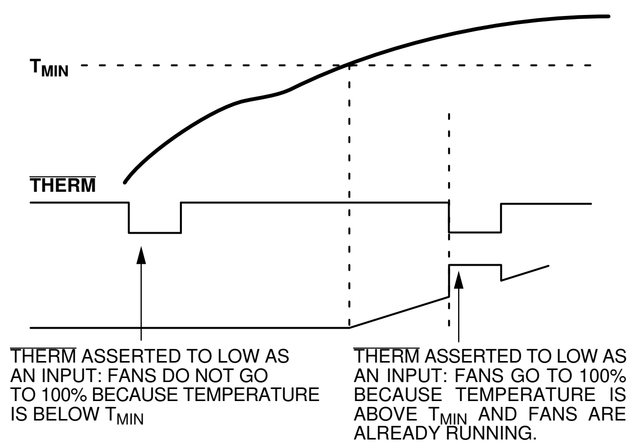


Figure 31. Asserting THERM Low as an Input in Automatic Fan Speed Control Mode

THERM Timer

The ADT7476 has an internal timer to measure THERM assertion time. For example, the THERM input can be connected to the PROCHOT output of a Pentium® 4 CPU to measure system performance. The THERM input can also be connected to the output of a trip-point temperature sensor.

The timer is started on the assertion of the ADT7476's THERM input and stopped when THERM is de-asserted. The timer counts THERM times cumulatively; that is, the timer resumes counting on the next THERM assertion. The THERM timer continues to accumulate THERM assertion times until the timer is read (where it is cleared), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit THERM timer status register (0x79) is designed so that Bit 0 is set to 1 on the first THERM assertion. Once the cumulative THERM assertion time has exceeded 45.52 ms, Bit 1 of the THERM timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 32).

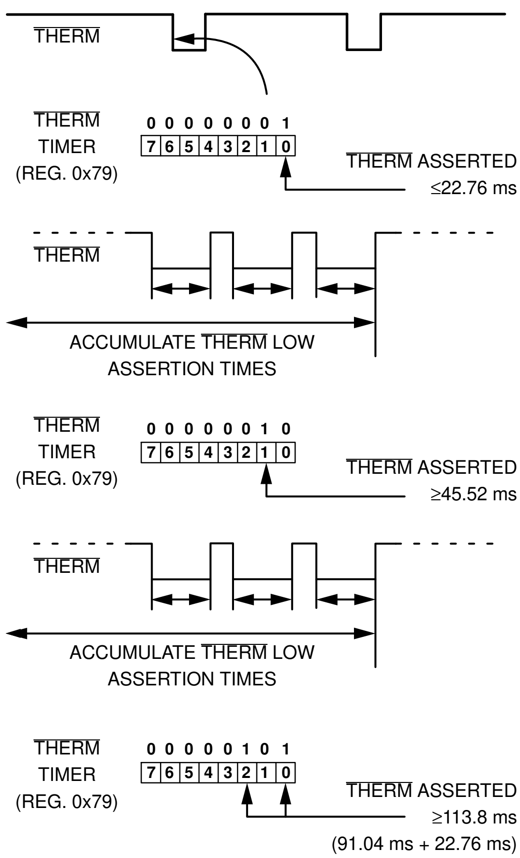


Figure 32. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

After a THERM timer read (0x79)

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following occurs:

1. The contents of the timer are cleared.
2. Bit 0 of the THERM timer is set to 1, because a THERM assertion is occurring.
3. The THERM timer increments from zero.
4. If the THERM timer limit register (0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7476 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 sec (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit value, then the F4P bit (Bit 5) of Interrupt Status Register 2 is set and an SMBALERT is generated.

NOTE: Depending on which pins are configured as a THERM timer, setting the F4P bit (Bit 5) of Mask Register 2 (0x75) or Bit 0 of Mask Register 1 (0x74) masks out SMBALERT; although the F4P bit of Interrupt Status Register 2 is still set if the THERM timer limit is exceeded.

Figure 33 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes an SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.