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ADT7490

Remote Thermal Monitor and Fan Controller with PECI Interface

The ADT7490 is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7490 includes a local temperature sensor, two remote temperature sensors including series resistance cancellation, and monitors CPU temperature with a PECI interface. The ADT7490 can drive a fan using either a low or high frequency drive signal, and measure and control the speed of up to four fans so they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature using the PECI, remote, or local temperature information. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7490 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$ pin as an output to prevent system or component overheating.

Features

- Temperature Measurement
  - 1 Local On-Chip Temperature Sensor
  - 2 Remote Temperature Sensors
  - 3 Current External Temperature Sensors with Series Resistance Cancellation (SRC)
  - PECI Interface for CPU Thermal Information and Support of Up to 4 PECI Inputs on 1 Pin
- Fan Drive and Fan Speed Control
  - 3 High Frequency or Low Frequency PWM Outputs for Use with 3-wire or 4-wire Fans
  - 4 TACH Inputs to Measure Fan Speed
  - OS Independent Automatic Fan Speed Control Based on Thermal Information
  - Dynamic T_{MIN} Control Mode to Optimize System Acoustics
  - Default Startup at 100% PWM for All Fans for Robust Operation
- Bidirectional $\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$ Pin to Flag Out-of-Limit and Overtemperature Conditions
- GPIO Functionality to Support Extra Features
  - Can be Used for Loadline Setting for Voltage Regulation, LED Control, or Other Functions
- I_{MON} Monitoring for CPU Current and Power Information
- Footprint and Register Compatible with ADT7473/ADT7475/ ADT7476/ADT7476A Family of Fan Controllers
- SMBus Interface with Addressing Capability for Up to 3 Devices

Applications

- Personal Computers
- Servers

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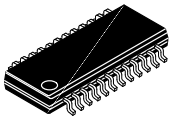
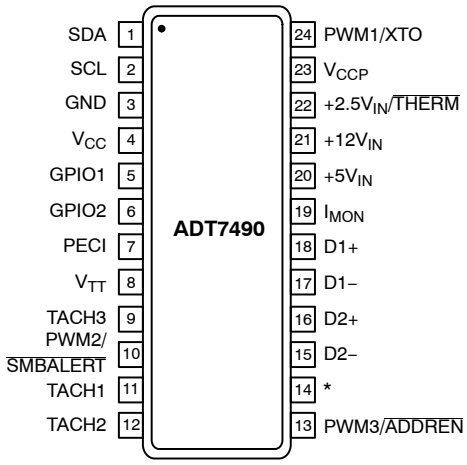


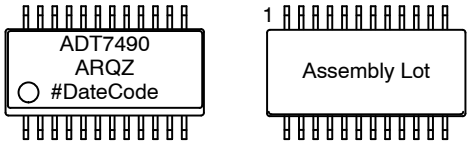
QSOP−24 NB
CASE 492B

PIN ASSIGNMENT



*TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/ADDR SELECT

MARKING DIAGRAMS



TOP MARKING **BOTTOM MARKING**

= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 74 of this data sheet.

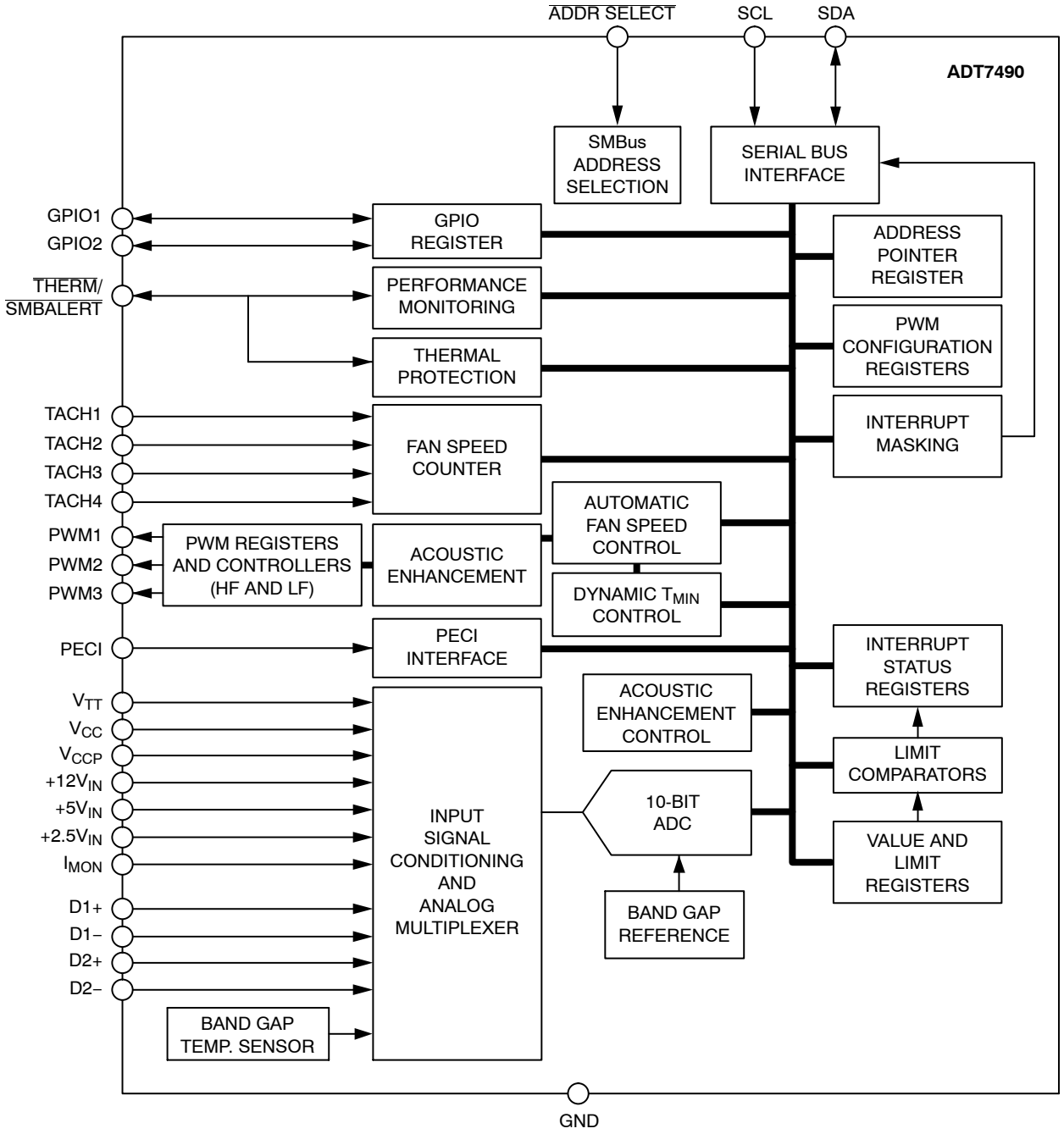


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Maximum Voltage on +12 V_{IN} Pin	16	V
Maximum Voltage on +5 V_{IN} Pin	6.25	V
Maximum Voltage on All Open-drain Outputs (excluding PWM pins)	3.6	V
Maximum Voltage on TACHx/PWMx Pins	+5.5	V
Voltage on Remaining Input or Output Pins	−0.3 to +4.2	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Pb-Free Peak Temperature Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating HBM FICDM	 2 0.5	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS (Note 1)

Package Type	θ_{JA}	θ_{JC}	Unit
24-lead QSOP	122	31.25	°C/W

1. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface Inactive, ADC Active	–	1.5	5.0	mA
Temperature-to-Digital Converter					
Local Sensor Accuracy Resolution	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +125°C$	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Diode Sensor Accuracy	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +125°C$	– – –	±0.5 – 0.25	±1.5 ±2.5 –	°C
Remote Sensor Source Current	Mid Level Low Level High Level	– – –	12 72 192	– – –	μA
Series Resistance Cancellation (Note 2)	The ADT7490 Cancels Up to 2 kΩ in Series with the Remote Thermal Sensor	–	–	1.5	kΩ

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Analog-to-Digital Converter (Including MUX and Attentuators)					
Total Unadjusted Error (TUE)	For All Channels: −40°C ≤ T_A ≤ +125°C For All Other Channels Except +12 V_{IN}: 0°C ≤ T_A ≤ +125°C	– –	– –	±2 ±1.5	%
Differential Non-linearity (DNL)	8 Bits	–	–	±1	LSB
Power Supply Sensitivity		–	±0.1	–	%/V
Conversion Times (Note 2)	Averaging Enabled, All Channels Excluding V_{TT} (Note 3)				ms
Voltage Inputs V_{TT} Voltage Input (Note 3) Local Temperature Remote Temperature	Averaging Enabled Averaging Enabled Averaging Enabled Averaging Enabled	– – – –	11 12 12 38	13 14 14 43	
Total Monitoring Cycle Time	 Averaging disabled	– –	169 19	193 –	ms
Input Resistance	For +12 V_{IN} Channel For All Other Channels	150 70	200 100	– –	kΩ
Fan RPM-to-Digital Converter					
Accuracy	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ +125°C	– –	– –	±10 ±14	%
Full-scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5,000 10,000	– – – –	RPM
Open-Drain Digital Outputs, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	20	μA
Open-Drain Serial Data Bus Output (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA
SMBus Digital Inputs (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
Digital I/O (PECI Pin) (Note 2)					
V_{TT}, Supply Voltage		0.95	–	1.26	V
Input High Voltage, V_{IH}		0.55 × V_{TT} (Note 3)	–	–	V
Input Low Voltage, V_{IL}		–	–	0.5 × V_{TT} (Note 3)	V
Hysteresis (Note 2)	Hysteresis between Input Switching Levels	0.1 × V_{TT} (Note 3)	–	–	mV
High Level Output Source Current, I_{SOURCE}	V_{OH} = 0.75 × V_{TT}	–	–	6.0	mA
Low Level Output Sink Current, I_{SINK}	V_{OL} = 0.25 × V_{TT}	0.5	–	1.0	mA
Signal Noise Immunity, V_{NOISE}	Noise Glitches from 10 MHz to 100 MHz, Width Up to 50 ns	300	–	–	mV p-p

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Digital Input Logic Levels (TACH1 to TACH3)					
Input High Voltage, V_{IH}	 Maximum Input Voltage	2.0 –	– –	– 5.5	V
Input Low Voltage, V_{IL}	 Minimum Input Voltage	– −0.3	– –	0.8 –	V
Hysteresis		–	0.5	–	V p-p
Digital Input Logic Levels ($\overline{\text{THERM}}$)					
Input High Voltage, V_{IH}		0.75 × V_{CCP}	–	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
Digital Input Current					
Input High Current, I_{IH}	V_{IN} = V_{CC}	–	±1	–	μA
Input Low Current, I_{IL}	V_{IN} = 0	–	±1	–	μA
Input Capacitance, C_{IN}		–	5.0	–	pF
Serial Bus Timing (Note 2) (See Figure 2)					
Clock Frequency, f_{SCLK}		10	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_r		–	–	1,000	ns
SCL, SDA Fall Time, t_f		–	–	300	μs
Data Setup Time, $t_{SU;DAT}$		250	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge.
2. Guaranteed by design, not production tested.
3. V_{TT} is the voltage input on Pin 8. The V_{TT} voltage is determined by the processor installed on the system.

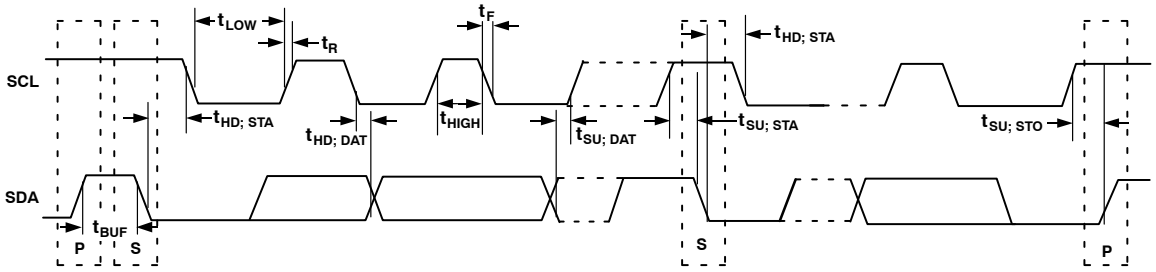


Figure 2. Serial Bus Timing Diagram

Table 4. PIN ASSIGNMENT

Pin No.	Mnemonic	Type	Description
1	SDA	Digital I/O	SMBus Bidirectional Serial Data. Open drain, requires SMBus pullup.
2	SCL	Digital Input	SMBus Serial Clock Input. Open drain, requires SMBus pullup.
3	GND	Ground	Ground Pin.
4	V_{CC}	Power Supply	3.3 V ±10%.
5	GPIO1	Digital Input/Output	General-purpose Open-drain Digital Input/Output. Frequently used for switching load line resistors into VR load line circuitry or for switching LEDs using external FETs.
6	GPIO2	Digital Input/Output	General-purpose Open-drain Digital Input/Output. Frequently used for switching load line resistors into VR load line circuitry or for switching LEDs using external FETs.
7	PECI	Digital Input/Output	PECI Input to Report CPU Thermal Information. PECI voltage level is referenced on the V_{TT} input.
8	V_{TT}	Analog Input	Voltage Reference for PECI. This is the supply voltage for the PECI interface and must be present to measure temperature over the PECI interface. This voltage is also monitored and presented in Register 0x1E.
9	TACH3	Digital Input	Fan Tachometer Input to Measure Speed of Fan 3 (Open-drain Digital Input).
10	PWM2/$\overline{\text{SMBALERT}}$	Digital Output	Pulse-width Modulated Output to Control Fan 2 Speed. Open drain requires 10 kΩ typical pullup. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input	Fan Tachometer Input to Measure Speed Of Fan 1 (Open-drain Digital Input).
12	TACH2	Digital Input	Fan Tachometer Input To Measure Speed Of Fan 2 (Open-drain Digital Input).
13	PWM3/ $\overline{\text{ADDREN}}$	Digital Output	Pulse-width Modulated Output to Control Fan 3 Speed. Open drain requires 10 kΩ typical pullup. If pulled low on powerup, the ADT7490 enters address select mode, and the state of Pin 14 ($\overline{\text{ADDR SELECT}}$) determines the ADT7490 slave address.
14	TACH4/$\overline{\text{THERM}}$/ $\overline{\text{SMBALERT}}$/ $\overline{\text{ADDR SELECT}}$	Digital Input/Output	Fan Tachometer Input to Measure Speed of Fan 4 (Open-drain Digital Input). May be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the processor, to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. Active Low Digital Output. The $\overline{\text{SMBALERT}}$ pin is used to signal out-of-limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus alert. Can also be used at device powerup to assign SMBus address.
15	D2−	Analog Input	Negative Connection for Remote Temperature Sensor 2.
16	D2+	Analog Input	Positive Connection to Remote Temperature Sensor 2.
17	D1−	Analog Input	Negative Connection for Remote Temperature Sensor 1.
18	D1+	Analog Input	Positive Connection to Remote Temperature Sensor 1.
19	I_{MON}	Analog Input	Monitors Current Output of Analog Devices ADP319x family of VRD10/VRD11 controllers.
20	+5 V_{IN}	Analog Input	Monitors 5.0 V Supply Using Internal Resistor Dividers.
21	+12 V_{IN}	Analog Input	Monitors 12 V Supply Using Internal Resistor Dividers.
22	+2.5 V_{IN}/$\overline{\text{THERM}}$	Analog Input	Monitors 2.5 V Supply Using Internal Resistor Dividers. Alternatively, this pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes.
23	V_{CCP}	Analog Input	Monitors CPU V_{CC} Voltage (to maximum of 3.0 V). All voltage inputs can have their resistor dividers removed allowing for full-scale input of 2.25 V of the ADC channel.
24	PWM1/XTO	Digital Output	Pulse-width Modulated Output to Control Fan 1 Speed. Open drain requires 10 kΩ typical pullup. Also functions as the output for the XNOR tree test enable mode.

Table 5. COMPARISON OF ADT7490 AND ADT7476A CONFIGURATIONS

Pin No.	ADT7490	ADT7476A
1	SDA	SDA
2	SCL	SCL
3	GND	GND
4	V_{CC}	V_{CC}
5	GPIO1	VID0/GPIO0
6	GPIO2	VID1/GPIO1
7	PECI	VID2/GPIO2
8	V_{TT}	VID3/GPIO3
9	TACH3	TACH3
10	PWM2/$\overline{\text{SMBALERT}}$	PWM2/$\overline{\text{SMBALERT}}$
11	TACH1	TACH1
12	TACH2	TACH2
13	PWM3/$\overline{\text{ADDREN}}$	PWM3/$\overline{\text{ADDREN}}$
14	TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/ADDR SELECT	TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/GPIO6/ADDR SELECT
15	D2−	D2−
16	D2+	D2+
17	D1−	D1−
18	D1+	D1+
19	I_{MON}	VID4/GPIO4
20	+5 V_{IN}	+5 V_{IN}
21	+12 V_{IN}	+12 V_{IN}/VID5
22	+2.5 V_{IN}/ $\overline{\text{THERM}}$	+2.5 V_{IN}/ $\overline{\text{THERM}}$
23	V_{CCP}	V_{CCP}
24	PWM1/XTO	PWM1/XTO

TYPICAL PERFORMANCE CHARACTERISTICS

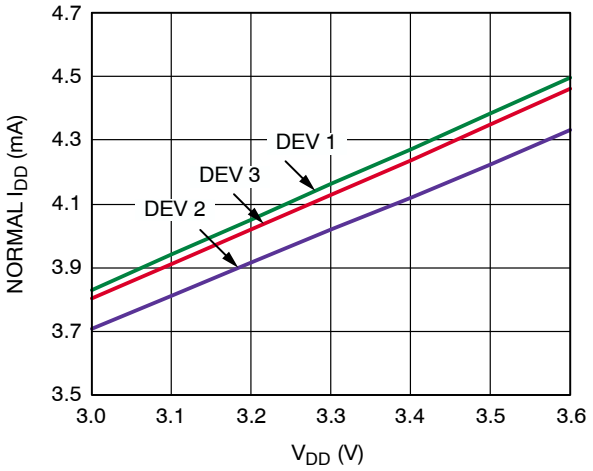


Figure 3. Supply Current vs. Supply Voltage

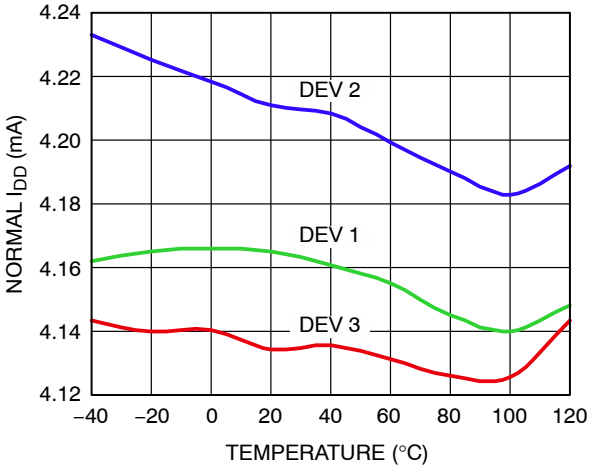


Figure 4. Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

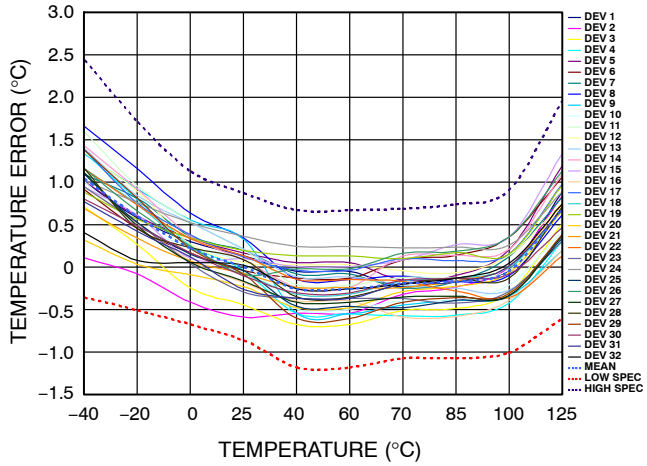


Figure 5. Local Temperature Sensor Error

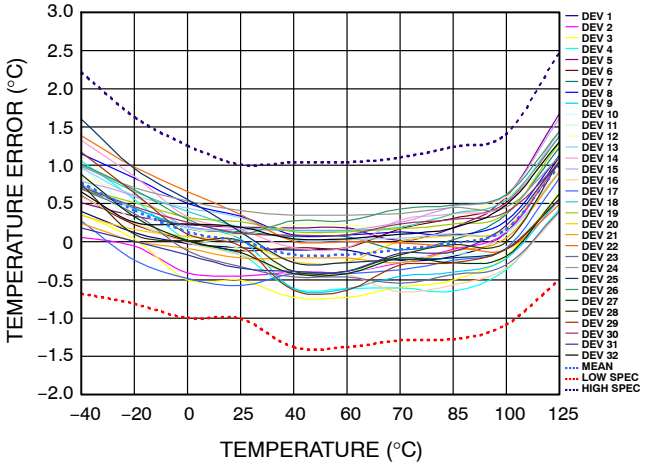


Figure 6. Remote 1 Temperature Sensor Error

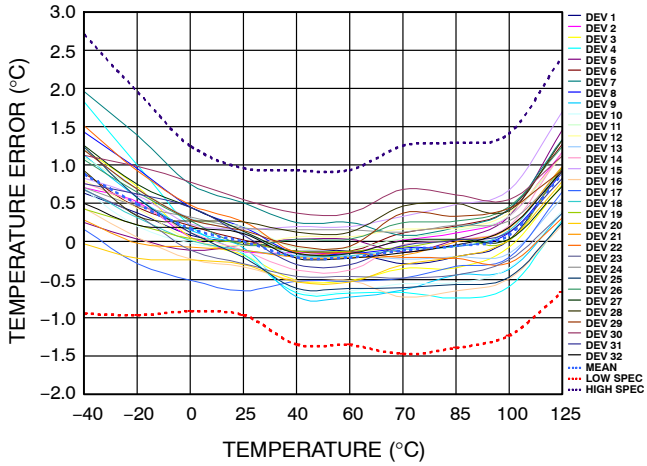


Figure 7. Remote 2 Temperature Sensor Error

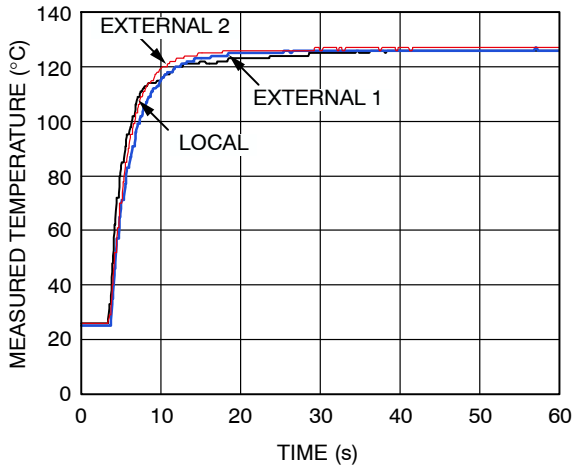


Figure 8. ADT7490 Response to Thermal Shock

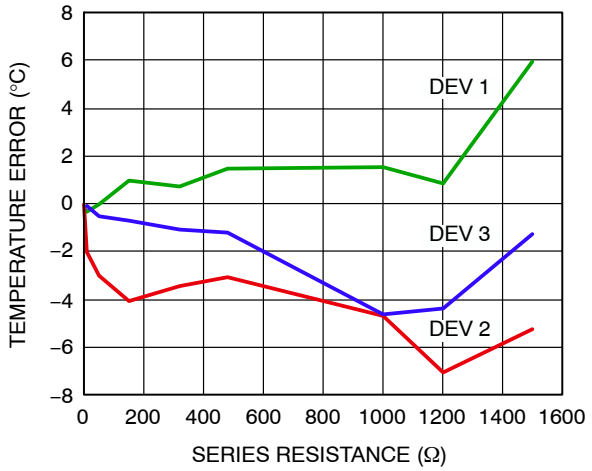


Figure 9. Temperature Error vs. Series Resistance

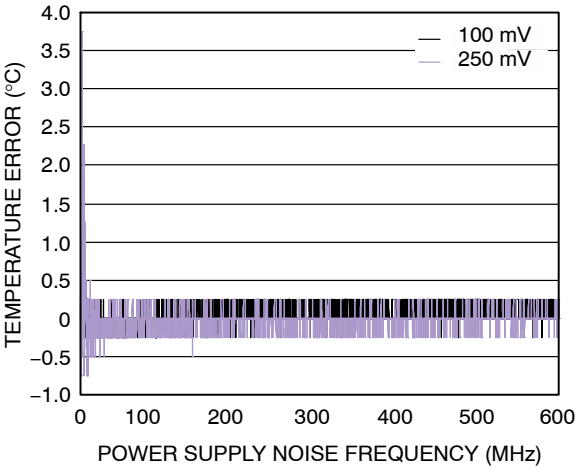


Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

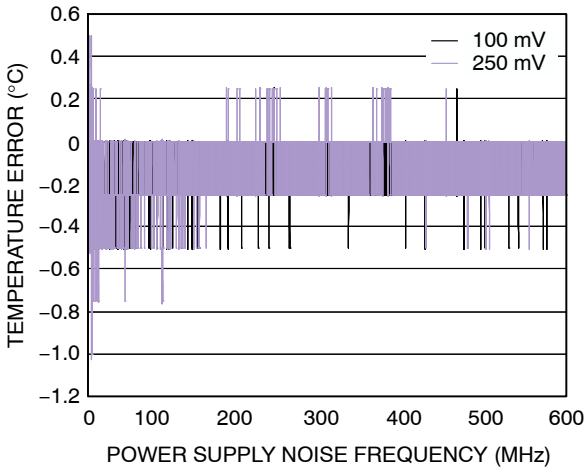


Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

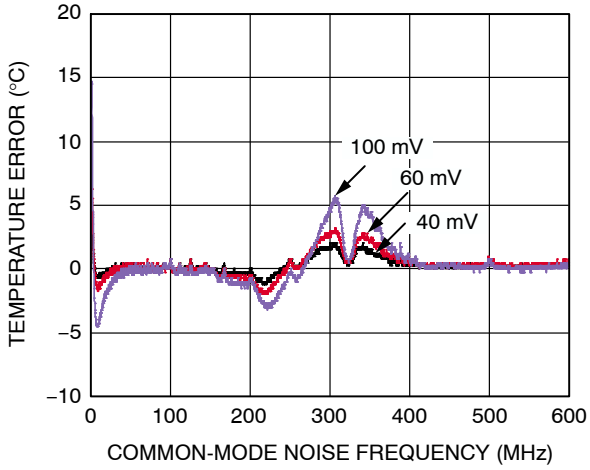


Figure 12. Temperature Error vs. Common-Mode Noise Frequency

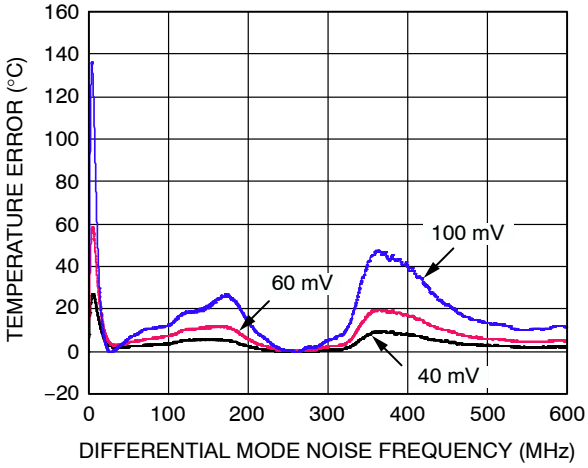


Figure 13. Temperature Error vs. Differential Mode Noise Frequency

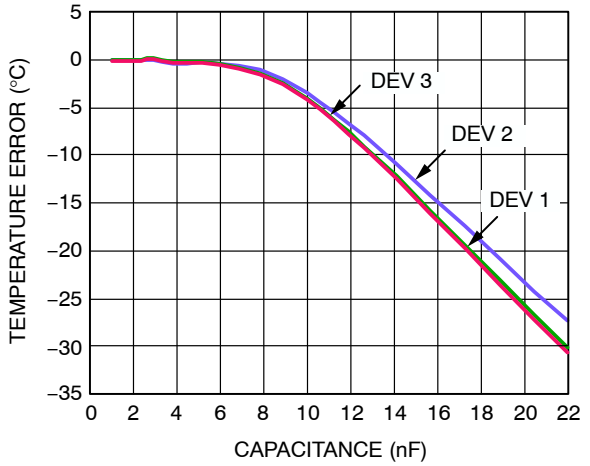


Figure 14. Temperature Error vs. Capacitance Between D+ and D–

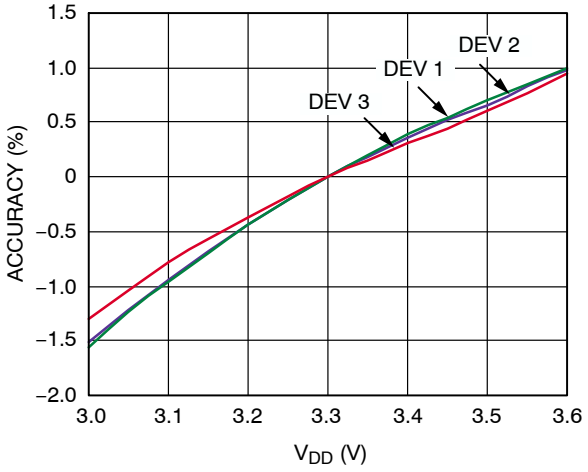


Figure 15. TACH Accuracy vs. Supply Voltage

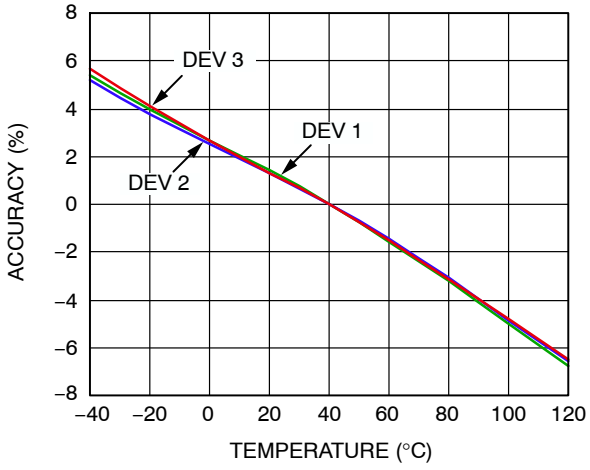


Figure 16. TACH Accuracy vs. Temperature

Theory of Operation

The ADT7490 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7490 are performed over the serial bus. In addition, Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Feature Comparisons Between the ADT7490 and ADT7476A

The ADT7490 is pin and register map compatible with the ADT7476A. The new or additional features are detailed in the following sections.

PECI Input

CPU thermal information is provided through the PECI input. The ADT7490 has PECI master capabilities and can read the CPU thermal information through the PECI interface. Each CPU address can have up to two PECI domains. The ADT7490 has the ability to record four PECI temperature readings corresponding to the four PECI addresses of 0x30 to 0x33. The hotter of the two domains at any given address is stored in the PECI value registers. A PECI reading is a negative value, in degrees Celsius, which represents the offset from the thermal control circuit (T_{CC}) activation temperature. PECI information is not converted to absolute temperature reading. PECI information is in a 16-bit twos complement value; however, the ADT7490 records the sign bit as well as the bits from 12:6 in the 16-bit PECI payload. See the Platform Environment Control Interface (PECI) Specification from Intel® for more details on the PECI data format. The PECI format is represented in Table 6.

Table 6. PECI DATA FORMAT

MSB Upper Nibble				MSB Lower Nibble			
S	x	x	x	x	x	x	x
Sign Bit				Integer Value (0°C to 127°C)			

There are associated high and low limits for each PECI reading that can be programmed. The limit values take the same format as the PECI reading. Therefore, the programmed limits are not absolute temperatures but a relative offset in degrees Celsius from the T_{CC} activation temperature. An out-of-limit event is recorded as follows:

High Limit > Comparison Performed
Low Limit ≤ Comparison Performed

An out-of-limit event is recorded in the associated status register and can be used to assert the $\overline{\text{SMBALERT}}$ pin.

Temperature Data REPLACE Mode

The REPLACE mode is configured by setting Bit 4 of Register 0x36. In this mode, the data in the existing Remote 1 registers are replaced by PECI0 data and vice versa. This is a legacy mode that allows the thermal data from CPU1 to be stored in the same registers as in the ADT7476A. This reduces the software changes in systems transitioning from CPUs with thermal diodes to CPUs with a PECI interface. See the PECI Temperature Measurement section for more details.

Fan Control Using PECI Information

The CPU thermal information from PECI can be used in the existing automatic fan control algorithms. This temperature reading remains relative to T_{CC} activation temperature and the associated AFC control parameters are programmed in relative temperatures as opposed to absolute temperatures, and are in the same format as detailed in Table 6. $PECI_{MIN}$, T_{RANGE}, and $T_{CONTROL}$ are user defined.

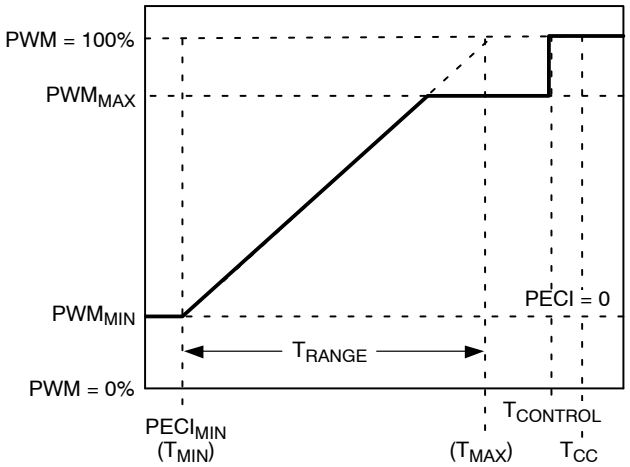


Figure 17. Overview of Automatic Fan Speed Control Using PECI Thermal Information

Dynamic T_{MIN} Fan Control Mode

The automatic fan speed control incorporates a feature called dynamic T_{MIN} control. This intelligent fan control feature reduces the design effort required to program the automatic fan speed control loop and improves the system acoustics.

V_{TT} Input

The V_{TT} voltage is monitored on Pin 8. This voltage is also used as the reference voltage for the PECI interface. The V_{TT} voltage must be connected to the ADT7490 in order for the PECI interface to be operational.

I_{MON} Monitoring

The I_{MON} input on Pin 19 can be used to monitor the I_{MON} output of ON Semiconductor's VR10/VR11.1 controllers. I_{MON} is a voltage representation of the CPU current. Using

the I_{MON} value and the measured V_{CCP} value on Pin 23, the CPU power consumption can be calculated. See the appropriate Analog Devices flex mode data sheet for calculations. The I_{MON} information can be considered as an early indication of an increase in CPU temperature.

Startup Operation

At startup, the ADT7490 turns the fans on to 100% PWM. This allows the most robust operation at turn-on.

Serial Bus Interface

Control of the ADT7490 is carried out using the serial system management bus (SMBus). The ADT7490 is connected to this bus as a slave device, under the control of a master controller. The ADT7490 has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7490 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to obtain the 8-bit address. If more than one ADT7490 is to be used in a system, each ADT7490 is placed in address select mode by strapping Pin 13 low on powerup. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is monitored from powerup but not latched until the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDREN}}$/ADDR SELECT pins. Any attempted changes in the address have no effect after this.

Table 7. HARD-WIRING THE ADT7490 SMBus DEVICE ADDRESS

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pullup)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E)

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as no acknowledge. The master takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7490, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation must contain a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 18. The device address is sent over the bus, and then R/$\overline{\text{W}}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7490 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7490 as before, but only the data byte containing the register address is sent because no data is written to the register. This is shown in Figure 19.
   A read operation is then performed consisting of the serial bus address, R/$\overline{\text{W}}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 20.
2. If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 20.

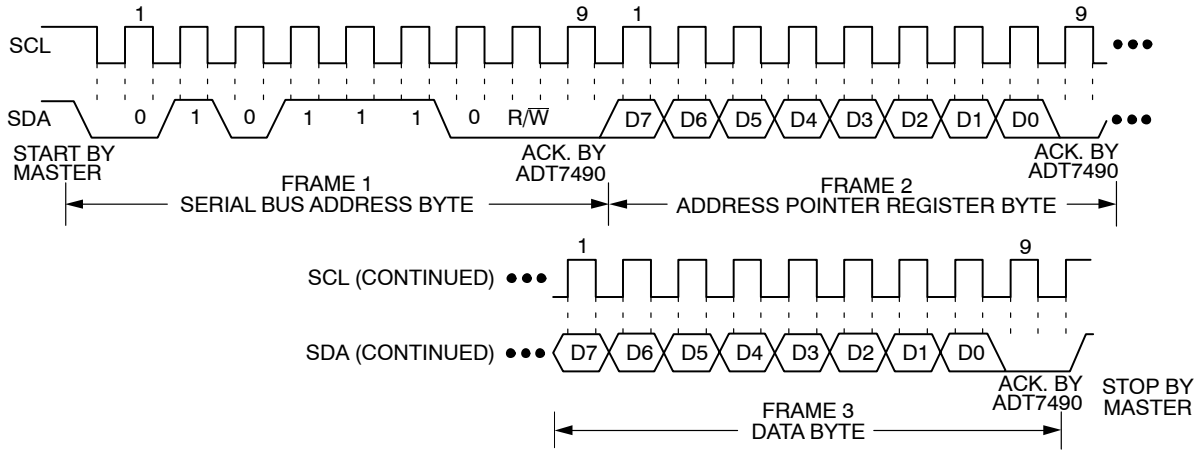


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

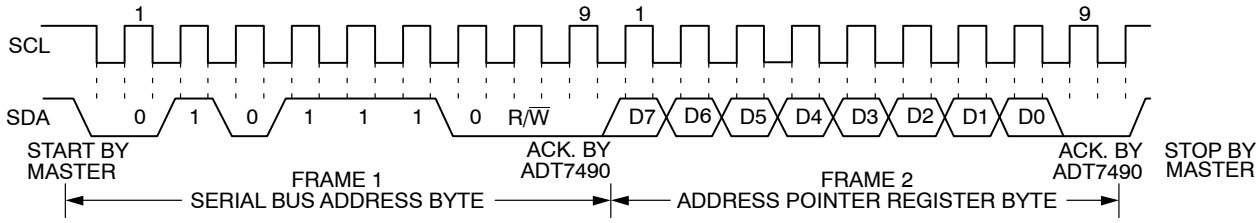


Figure 19. Writing to the Address Pointer Register Only

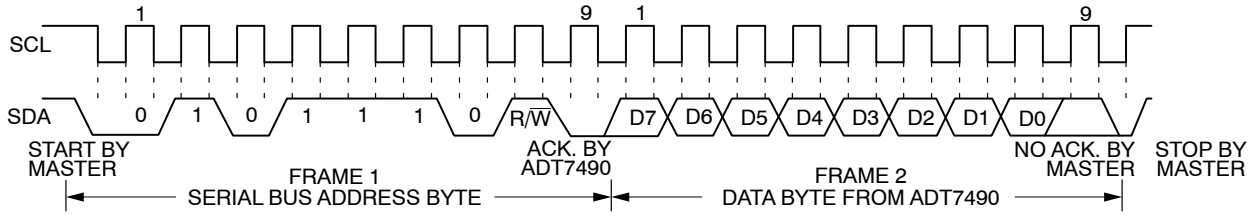


Figure 20. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7490 also supports the read byte protocol (see System Management Bus Specifications Rev. 2 for more information; this document is available from the SMBus organization).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7490 are discussed here. The following abbreviations are used in the diagrams:

- S: Start
- P: Stop
- R: Read
- $\overline{W}$: Write
- A: Acknowledge
- $\overline{A}$: No acknowledge

The ADT7490 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADT7490, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 21.

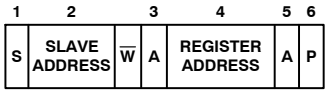


Figure 21. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single-byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

The byte write operation is illustrated in Figure 22.

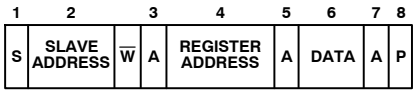


Figure 22. Single-byte Write to a Register

Read Operations

The ADT7490 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be previously set up. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7490, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 23.

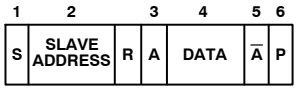


Figure 23. Single-byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7490 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition is gone.

SMBus Timeout

The ADT7490 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7490 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.

Configuration Register 7 (Register 0x11)

Bit 4 (TODIS) = 0, SMBus Timeout Enabled (Default)

Bit 4 (TODIS) = 1, SMBus Timeout Disabled

Voltage Measurement Input

The ADT7490 has six external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pin 20 to Pin 23 can measure 5.0 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3.0 V input). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). Pin 8 measures the V_{TT} voltage of the processor and is the dedicated reference voltage for the PECI circuitry. The I_{MON} input on Pin 19 can be used to monitor the I_{MON}

output of ON Semiconductor's VR11.1 controllers. I_{MON} is a voltage representation of the CPU current.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This ADC has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of 2.5 V, 3.3 V, 5.0 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 decimal or 0x300 hexadecimal) for the nominal input voltage, and therefore, has adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 24 . The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives input immunity to high frequency noise.

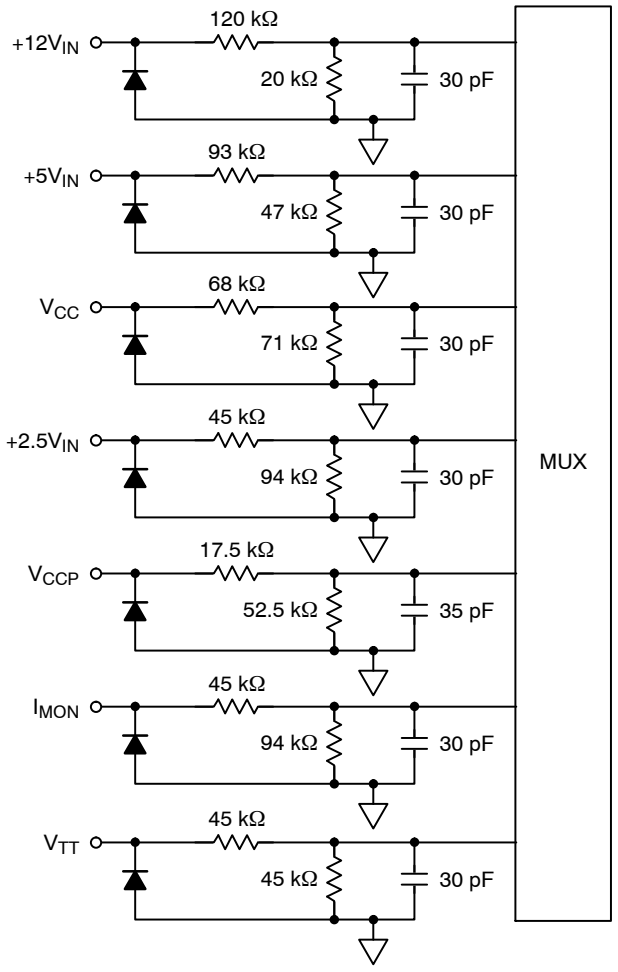


Figure 24. Analog Inputs Structure

Table 8. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x1D	I_{MON} Reading	0x00
0x1E	V_{TT} Reading	0x00
0x20	+2.5 V_{IN} Reading	0x00
0x21	V_{CCP} Reading	0x00
0x22	V_{CC} Reading	0x00
0x23	+5 V_{IN} Reading	0x00
0x24	+12 V_{IN} Reading	0x00

Voltage Limit Registers

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 9. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x85	I_{MON} Low Limit	0x00
0x87	I_{MON} High Limit	0xFF
0x84	V_{TT} Low Limit	0x00
0x86	V_{TT} High Limit	0xFF
0x44	+2.5 V_{IN} Low Limit	0x00
0x45	+2.5 V_{IN} High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	+5.0 V_{IN} Low Limit	0x00
0x4B	+5.0 V_{IN} High Limit	0xFF
0x4C	+12 V_{IN} Low Limit	0x00
0x4D	+12 V_{IN} High Limit	0xFF

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x1F, 0x76, and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x1D, 0x1E, and 0x20 to 0x24) is locked until their data is read. That is, if extended resolution is required, the extended resolution register must be read first, immediately followed by the appropriate voltage measurement register.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7490 to offer the system designer increased flexibility. The functions described in the following sections are enabled by setting the appropriate bit in Configuration Register 2.

Configuration Register 2 (Register 0x73)

Bit 4 (AVG) = 1, Averaging Off.

Bit 5 (ATTN) = 1, Bypass Input Attenuators.

Bit 6 (CONV) = 1, Single-channel Convert Mode.

Turn-off Averaging

For each voltage/temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. When faster conversions are needed, setting Bit 4 (AVG) of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading that is 16 times faster, but the reading can be noisier. The default round-robin cycle time takes 146.5 ms.

Table 10. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 (ExtraSlow) of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to 240 ms.

Bypass All Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the 2.5 V_{IN}, V_{CCP}, V_{CC}, 5 V_{IN}, and 12 V_{IN} inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Bypass Individual Voltage Input Attenuators

Bits [7:4] of Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 11. BYPASSING INDIVIDUAL VOLTAGE INPUT ATTENUATORS

Configuration Register 4 (0x7D)	
Bit No.	**Channel Attenuated**
[4]	Bypass +2.5 V_{IN} Attenuator
[5]	Bypass V_{CCP} Attenuator
[6]	Bypass +5 V_{IN} Attenuator
[7]	Bypass +12 V_{IN} Attenuator

Single-channel ADC Conversion

While single-channel mode is intended as a test mode that can be used to increase sampling times for a specific channel, therefore helping to analyze that channel's performance in greater detail, it can also have other applications.

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7490 into single-channel ADC conversion mode. In this mode, the ADT7490 can read a single voltage channel only. The selected voltage input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits [7:4] of the TACH1 minimum high byte register (0x55).

Table 12. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits [7:4], Register 0x55	**Channel Selected** (Note 1)
0000	+2.5 V_{IN}
0001	V_{CCP}
0010	V_{CC}
0011	+5 V_{IN}
0100	+12 V_{IN}
0101	Remote 1 Temperature
0110	Local Temperature
0111	Remote 2 Temperature
1000	V_{TT}
1001	I_{MON}

1. In the process of configuring single-channel ADC conversion mode, the TACH1 minimum high byte is also changed, possibly trading off TACH1 minimum high byte functionality with single-channel mode functionality.

Table 13. 10-BIT ADC OUTPUT CODE VS. V_{IN}

Input Voltage						ADC Output	
+12 V_{IN}	+5 V_{IN}	V_{CC} (3.3 V_{IN})	+2.5 V_{IN}	V_{CCP}	V_{TT}/I_{MON}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	<0.00220	0	00000000 00
0.0156 to 0.0312	0.0065 to 0.0130	0.0042 to 0.0085	0.0032 to 0.0065	0.0293 to 0.0058	0.00220 to 0.00440	1	00000000 01
0.0312 to 0.0469	0.0130 to 0.0195	0.0085 to 0.0128	0.0065 to 0.0097	0.0058 to 0.0087	0.00440 to 0,00660	2	00000000 10
0.0469 to 0.0625	0.0195 to 0.0260	0.0128 to 0.0171	0.0097 to 0.0130	0.0087 to 0.0117	0,00660 to 0.00881	3	00000000 11
0.0625 to 0.0781	0.0260 to 0.0325	0.0171 to 0.0214	0.0130 to 0.0162	0.0117 to 0.0146	0.00881 to 0.01100	4	00000001 00
0.0781 to 0.0937	0.0325 to 0.0390	0.0214 to 0.0257	0.0162 to 0.0195	0.0146 to 0.0175	0.01100 to 0.01320	5	00000001 01
0.0937 to 0.1093	0.0390 to 0.0455	0.0257 to 0.0300	0.0195 to 0.0227	0.0175 to 0.0205	0.01320 to 0.01541	6	00000001 10
0.1093 to 0.1250	0.0455 to 0.0521	0.0300 to 0.0343	0.0227 to 0.0260	0.0205 to 0.0234	0.01541 to 0.01761	7	00000001 11
0.1250 to 0.14060	0.0521 to 0.0586	0.0343 to 0.0386	0.0260 to 0.0292	0.0234 to 0.0263	0.01761 to 0.01981	8	00000010 00
–	–	–	–	–	–	–	–
4.0000 to 4.0156	1.6675 to 1.6740	1.1000 to 1.1042	0.8325 to 0.8357	0.7500 to 0.7529	0.5636 to 0.5658	256 (1/4 scale)	01000000 00
–	–	–	–	–	–	–	–
8.0000 to 8.0156	3.3300 to 3.3415	2.2000–2.204 2	1.6650 to 1.6682	1.5000 to 1.5029	1.1272 to 1.1294	512 (1/2 scale)	10000000 00
–	–	–	–	–	–	–	–
12.0000 to 12.0156	5.0025 to 5.0090	3.3000 to 3.3042	2.4975 to 2.5007	2.2500 to 2.2529	1.6809 to 1.6930	768 (3/4 scale)	11000000 00
–	–	–	–	–	–	–	–
15.8281 to 15.8437	6.5983 to 6.6048	4.3527 to 4.3570	3.2942 to 3.2974	2.9677 to 2.9707	2.2301 to 2.2323	1013	11111101 01
15.8437 to 15.8593	6.6048 to 6.6113	4.3570 to 4.3613	3.2974 to 3.3007	2.9707 to 2.9736	2.2323 to 2.2346	1014	11111101 10
15.8593 to 15.8750	6.6113 to 6.6178	4.3613 to 4.3656	3.3007 to 3.3039	2.9736 to 2.9765	2.2346 to 2.2368	1015	11111101 11
15.8750 to 15.8906	6.6178 to 6.6244	4.3656 to 4.3699	3.3039 to 3.3072	2.9765 to 2.9794	2.2368 to 2.23899	1016	11111110 00
15.8906 to 15.9062	6.6244 to 6.6309	4.3699 to 4.3742	3.3072 to 3.3104	2.9794 to 2.9824	2,23899 to 2.2412	1017	11111110 01
15.9062 to 15.9218	6.6309 to 6.6374	4.3742 to 4.3785	3.3104 to 3.3137	2.9824 to 2.9853	2.2412 to 2.2434	1018	11111110 10
15.9218 to 15.9375	6.6374 to 6.4390	4.3785 to 4.3828	3.3137 to 3.3169	2.9853 to 2.9882	2.2434 to 2.2456	1019	11111110 11
15.9375 to 15.9531	6.6439 to 6.6504	4.3828 to 4.3871	3.3169 to 3.3202	2.9882 to 2.9912	2.2456 to 2.2478	1020	11111111 00
15.9531 to 15.9687	6.6504 to 6.6569	4.3871 to 4.3914	3.3202 to 3.3234	2.9912 to 2.9941	2.2478 to 2.25	1021	11111111 01
15.9687 to 15.9843	6.6569 to 6.6634	4.3914 to 4.3957	3.3234 to 3.3267	2.9941 to 2.9970	2.25 to 2.2522	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	>2.2522	1023	1111111111 1

Temperature Measurement

The ADT7490 has four temperature measurement channels: one local, two remote thermal diodes, and a PECI. The local and thermal diode readings are analog temperature measurements, whereas PECI is a digital temperature reading.

PECI Temperature Measurement

The PECI interface is a dedicated thermal interface. The CPU temperature measurement is carried out internally in the CPU. This information is digitized and transferred to the ADT7490 via the PECI interface. The ADT7490 is a PECI host device and therefore, polls the CPU for thermal information.

The PECI measurement differs from traditional thermal diode temperature measurements in that the measurement is a relative value instead of an absolute value. The PECI reading is a negative value that indicates how close the CPU temperature is from the thermal throttling or T_{CC} point of the CPU.

The ADT7490 records and uses the PECI measurement for fan control in its relative format. Therefore, care must be taken in programming the relevant limits and fan control parameters in the PECI format. Refer to the PECI Input section and Table 6 for further PECI information.

PECI monitoring is enabled on the ADT7490 by setting the PECI monitoring bit in Configuration Register 1 (Register 0x40, Bit 4). The ADT7490 can measure the temperature of up to four dual-core CPUs. The number of CPUs in the system that provide PECI information is set in Bits [7:6] of Register 0x88. Each CPU is distinguished by the PECI address. The number of domains, or domain count, per CPU address must also be programmed into the ADT7490. The ADT7490 reads the temperature of both domains per CPU, however, only the PECI value of the hottest domain is recorded in the PECI value register.

PECI0 domains: Register 0x36, Bit 3

PECI1 domains: Register 0x88, Bit 5

PECI2 domains: Register 0x88, Bit 4

PECI3 domains: Register 0x88, Bit 3

PECI Reading Registers

Register 0x33, PECI0: PECI Reading from CPU Address 0x30

Register 0x1A, PECI1: PECI Reading from CPU Address 0x31

Register 0x1B, PECI2: PECI Reading from CPU Address 0x32

Register 0x1C, PECI3: PECI Reading from CPU Address 0x33

PECI Limit Registers

Each PECI measurement shares the same high and low limits.

Register 0x34, PECI Low Limit = 0x81 Default

Register 0x35, PECI High Limit = 0x00 Default

PECI Offset Registers

Each PECI reading has a dedicated offset register to calibrate the PECI measurement and account for errors in the temperature reading. The LSBs add a 1°C offset to the temperature reading so that the 8-bit register effectively allows temperature offsets of up to ±128°C with a resolution of 1°C.

Register 0x94, PECI0 Offset

Register 0x95, PECI1 Offset

Register 0x96, PECI2 Offset

Register 0x97, PECI3 Offset

PECI Data Smoothing

The PECI smoothing interval is programmed in PECI Configuration Register 1 (0x36). Bits [2:0] of Register 0x36 set the duration over which the PECI data being read by the ADT7490 is averaged. These bits set the duration over which smoothing is carried out on the PECI data read. The refresh rate in the PECI value registers is the same as the smoothing interval programmed.

The smoothing interval is calculated using the following formula:

$$\text{Smoothing Interval} = \#\text{reads} \times \left(t_{BIT} \times 67 \times \#\text{CPU} + t_{IDLE}\right) \quad \text{(eq. 1)}$$

where:

#reads is the number of readings defined in Register 0x36, Bits [2:0]

t_{BIT} is the negotiated bit rate.

67 is the number of bits in each PECI reading.

#CPU is the number of CPUs providing PECI data (1 to 4).

t_{IDLE} = 14 μs, the delay between consecutive reads.

For example,

#reads = 4096

t_{BIT} = 1 μs (1 MHz speed)

#CPU = 1

Smoothing Interval = 331 ms = PECI reading refresh rate

PECI Error Codes

There are two different error conditions for PECI data, PECI data errors, and PECI bus communications errors. Table 14 describes the two different error conditions. If the ADT7490 reads an error code (0x8000 to 0x8003) from the CPU over the PECI interface, Bit 1 is set in Interrupt Status 3 register (0x43), indicating a data error. The value of the error code is not included in the PECI value averaging sum. This means that a value of 0x00 is added to the PECI sum when an error code is recorded. The error code is not reported in the appropriate PECI value register. If an invalid FCS is recorded by the ADT7490, Bit 2 is set in the Interrupt Status 3 register (0x43), indicating a communications error. An alert is generated on the $\overline{\text{SMBALERT}}$ pin when either or both of these status bits are asserted.

Table 14. PECI ERROR INDICATORS

PECI Data	Description	Action
0x8000 to 0x8003	PECI Data Error	Bit 1 of Register 0x43 is set to 1
Invalid FCS	PECI Communications Error	Bit 2 of Register 0x43 is set to 1

Each PECI channel also has an associated status bit to indicate if the PECI high or low limits have been exceeded. An alert is generated on the $\overline{\text{SMBALERT}}$ pin when these status bits are asserted.

Table 15. PECI STATUS BITS

Channel	Register	Bit
PECI0	0x43	0
PECI1	0x81	3
PECI2	0x81	4
PECI3	0x81	5

Temperature Data REPLACE Mode

The REPLACE mode is configured by setting Bit 4 of Register 0x36. In this mode, the data in the existing Remote 1 registers are replaced by PECI0 data. This is a legacy mode that allows the thermal data from CPU1 to be stored in the same registers as in the ADT7476A. This reduces the software changes in systems transitioning from CPUs with thermal diodes to CPUs with a PECI interface. However, note that even though the associated registers are swapped, the correct data format (PECI vs. absolute temperature, see Table 6) must be written to and interpreted from these registers.

Notes

In Table 16, registers listed under the Remote 1 Default column are in absolute temperature format by default and are in PECI format in REPLACE mode. Registers listed under the PECI0 Default column are in PECI format by default and in absolute temperature format in REPLACE mode.

Table 16. REPLACE MODE TEMPERATURE REGISTERS

Register Name	Remote 1 Default	PECI0 Default
Value Register	Reg. 0x25	Reg. 0x33
Low Limit	Reg. 0x4E	Reg. 0x34
High Limit	Reg. 0x4F	Reg. 0x35
T_{MIN}	Reg. 0x67	Reg. 0x3B
T_{RANGE}	Reg. 0x5F, Bits [7:4]	Reg. 0x3C, Bits [7:4]
Enhanced Acoustics	Reg. 0x62, Bits [2:0]	Reg. 0x3C, Bits [2:0]
Enhanced Acoustics Enable	Reg. 0x62, Bit 3	Reg. 0x3C, Bit 3
$\overline{\text{THERM}}$ $T_{CONTROL}$	Reg. 0x6A	Reg. 0x3D
T_{MIN} Hysteresis	Reg. 0x6D, Bits [7:4] Reg. 0x6D, Bits [3:0] (Note 1)	Reg. 0x6E, Bits [3:0] Reg. 0x6E, Bits [7:4] (Note 1)
Temperature offset	Reg. 0x70	Reg. 0x94
Operating Point for Dynamic T_{MIN}	Reg. 0x8B	Reg. 0x8A

1. In REPLACE mode, the Remote 2 and local temperature hysteresis values are swapped.

In REPLACE mode, the temperature zone controlling the relevant PWM output are also swapped from Remote 1 to PECI0. The swap of control only occurs if the default behavior setting for Register 0x5C Bits [7:5], Register 0x5D Bits [7:5] or Register 0x5E Bits [7:5] is 000.

Local Temperature Measurement

The ADT7490 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 17 and Table 18. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C (or −64°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7490 operating temperature range are not possible.

Table 17. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
–128°C	1000 0000 **00** (Diode Fault)
–63°C	1100 0001 **00**
–50°C	1100 1110 **00**
–25°C	1110 0111 **00**
–10°C	1111 0110 **00**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25.5°C	0001 1001 **10**
50.75°C	0011 0010 **11**
75°C	0100 1011 **00**
100°C	0110 0100 **00**
125°C	0111 1101 **00**
127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution 2 register (Register 0x77) with 0.25°C resolution.

Table 18. OFFSET 64 DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
–64°C	0000 0000 **00** (Diode Fault)
–63°C	0000 0001 **00**
–1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution 2 register (Register 0x77) with 0.25°C resolution.

Thermal Diode Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null out the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADT7490 is to measure the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 28 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor, such as a 2N3904/2N3906.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figure 25 and Figure 26 show how to connect the ADT7490 to an NPN or PNP transistor for temperature measurement.

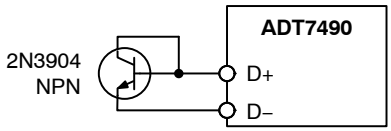


Figure 25. Measuring Temperature by Using an NPN Transistor

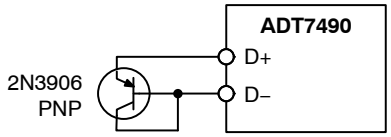


Figure 26. Measuring Temperature by Using a PNP Transistor

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input. C1 can optionally be added as a noise filter (recommended maximum value of 1,000 pF). However, a better option in noisy environments is to add a filter, as described in the section.

Remote Temperature Measurement

The ADT7490 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11, or Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out. Therefore, the technique is unsuitable for mass production. The technique used in the ADT7490 is to measure the change in V_{BE} when the device is operated at three different currents. This is given by:

$$\Delta V_{BE} = \frac{kT}{q} \times \ln(N) \qquad \text{(eq. 2)}$$

where:

k is the Boltzmann constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvin.

N is the ratio of the two currents.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. N1 × I and N2 × I are different multiples of the current I, as shown in Figure 27. The currents through the temperature diode are

switched between I and N1 × I, giving ΔV_{BE1}, and then between I and N2 × I, giving ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10-bit, twos complement format, as listed in Table 17. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

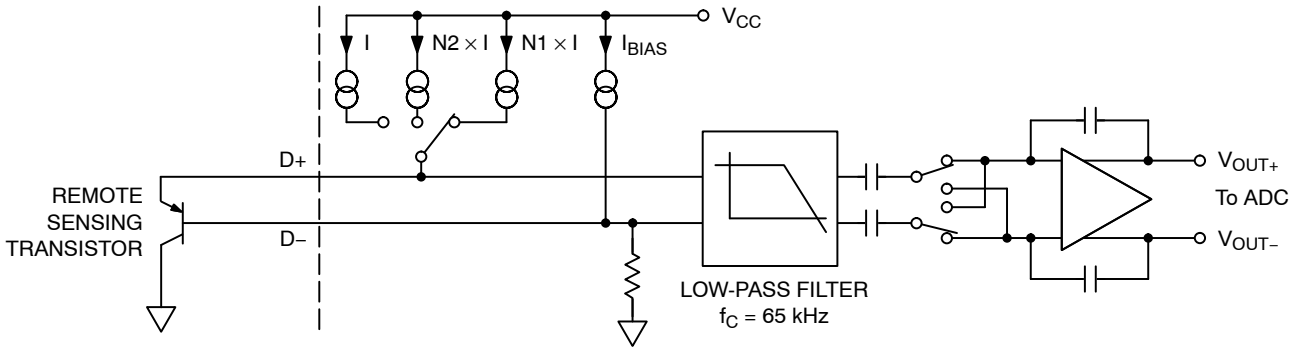


Figure 27. Signal Conditioning for Remote Diode Temperature Sensors

Series Resistance Cancellation

Parasitic resistance to the ADT7490 D+ and D− inputs (seen in series with the remote diode) is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The ADT7490 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result without the need for user characterization of this resistance. The ADT7490 is designed to automatically cancel, typically up to 1.5 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and the D− pin to help combat the effects of noise. However, large capacitance affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF. This capacitor reduces the noise, but does not eliminate it, which makes using the sensor difficult in a very noisy environment.

The ADT7490 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7490 and the remote temperature sensor to operate in noisy environments. Figure 28 shows a low-pass RC filter with the following values:

$$R = 100\ \Omega, C = 1\ nF \qquad \text{(eq. 3)}$$

This filtering reduces both common-mode noise and differential noise.

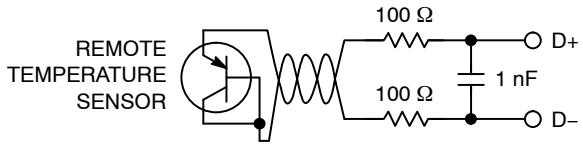


Figure 28. Filter between Remote Sensor and ADT7490

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7490 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7490 is trimmed for an n_f value of 1.008. Use

the following equation to calculate the error introduced at a temperature T (°C) when using a transistor whose n_f does not equal 1.008. Refer to the data sheet for the related CPU to obtain the n_f values.

$$\Delta T = (nf - 1.008)/1.008 \times (273.15\ K + T) \quad \text{(eq. 4)}$$

To factor this in, the user can write the ΔT value to the offset register. The ADT7490 automatically adds it to or subtracts it from the temperature measurement.

- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7490, I_{HIGH}, is 192 μA and the low level current, I_{LOW}, is 12 μA. If the ADT7490 current levels do not match the current levels specified by the CPU manufacturer, it may be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7490, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 12 μA at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 192 μA at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (such as 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT−23 packages, are suitable devices to use.

Reading Temperature from the ADT7490

It is important to note that temperature can be read from the ADT7490 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, it involves a 2-register read for each measurement. The Extended Resolution 2 register (0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

Nulling Out Temperature Errors

As CPUs run faster, it becomes more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors may still be attributable to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7490 has temperature offset registers at Address 0x70, Address 0x71, and Address 0x72 for the Remote 1, local, and Remote 2 temperature channels, respectively. By performing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement.

The temperature offset range and resolution is selected by setting Bit 1 of Register 0x7C. This ensures that the readings in the temperature measurement registers are as accurate as possible. Setting this bit to 0 means the LSBs add 0.5°C offset to the temperature reading, so the 8-bit register effectively allows temperature offsets from −63°C to +64°C with a resolution of 0.5°C. Setting this bit to 1 means the LSBs add 1°C offset to the temperature reading, so the 8-bit register effectively allows temperature offsets of up to −63°C to +127°C with a resolution of 1°C. For the PECI offset registers, the resolution is always 1°C.

Table 19. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)
0x94	PECI0 Temperature Offset	0x00 (0°C)
0x95	PECI1 Temperature Offset	0x00 (0°C)
0x96	PECI2 Temperature Offset	0x00 (0°C)
0x97	PECI3 Temperature Offset	0x00 (0°C)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7490 to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. The default round-robin cycle time with averaging off is a maximum of 23 ms.

Table 20. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to a maximum of 193 ms.

Table 21. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature	39
Local Temperature	12

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Register 0x73) places the ADT7490 into single-channel ADC conversion mode. In this mode, the ADT7490 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:4] of the TACH1 Minimum High Byte register (0x55).

Table 22. PROGRAMMING SINGLE-CHANNEL ADC MODE FOR TEMPERATURES

Bits [7:4], Register 0x55	Channel Selected
Remote 1 Temperature	0101
Local Temperature	0110
Remote 2 Temperature	0111

Configuration Register 2 (Register 0x73)

Bit 4 (AVG) = 1, Averaging Off.

Bit 6 (CONV) = 1, Single-channel Convert Mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limits for the local and remote diode temperature channels. The equivalent PECI limit is $T_{CONTROL}$ in Register 0x3D. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at 100% duty cycle (default). This can be changed to maximum PWM duty cycle as programmed in Register 0x38, Register 0x39, and Register 0x3A, by setting Bit 3 of Register 0x7D.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2 (0x78). The hysteresis value for the $\overline{\text{THERM}}$ temperature limit is the value programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

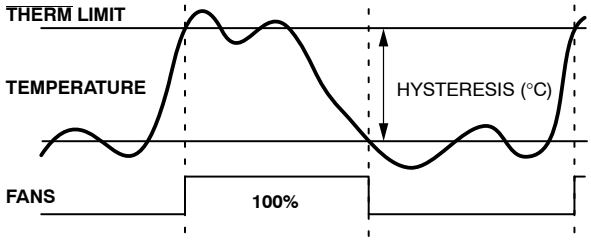


Figure 29. $\overline{\text{THERM}}$ Temperature Limit Operation

$\overline{\text{THERM}}$ can be disabled by setting Bit 2 of Configuration Register 4 (0x7D). $\overline{\text{THERM}}$ can also be disabled by:

- In Offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
- In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7490 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag out-of-limit conditions to a processor or micro-controller.

8-bit Limits

The following is a list of 8-bit limits on the ADT7490:

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	+2.5 V_{IN} Low Limit	0x00
0x45	+2.5 V_{IN} High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	+5 V_{IN} Low Limit	0x00
0x4B	+5 V_{IN} High Limit	0xFF
0x4C	+12 V_{IN} Low Limit	0x00
0x4D	+12 V_{IN} High Limit	0xFF
0x84	V_{TT} Low Limit	0x00
0x86	V_{TT} High Limit	0xFF
0x85	I_{MON} Low Limit	0x00
0x87	I_{MON} High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Temp. Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Temperature Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Temp. Limit	0x64
0x34	PECI Low Limit	0x81
0x35	PECI High Limit	0x00
0x3D	PECI $T_{CONTROL}$ Limit	0x00

Table 25. $\overline{\text{THERM}}$ TIMER LIMIT REGISTER

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Timer Limit	0x00

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Only high limits exist for fan TACHs because fans running under speed or stalled are normally the only conditions of interest. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 26. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7490 can be enabled for monitoring. The ADT7490 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit to indicate out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit > Comparison Performed
Low Limit ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time. For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured consists of

- Six Dedicated Supply Voltage Inputs
- Supply Voltage (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round-robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally

$$(7 \times 11) + 12 + (2 \times 39) = 167 \text{ ms} \quad \text{(eq. 5)}$$

Fan TACH measurements and PECI thermal measurements are made in parallel and are not synchronized with the analog measurements in any way.

Interrupt Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 to Interrupt Status Register 4. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding interrupt status register bit is cleared to 0. If the measurement is out of limit, the corresponding interrupt status register bit is set to 1.

The state of the various measurement channels can be polled by reading the interrupt status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), a Logic 1 indicates an out-of-limit event has been flagged in Interrupt Status Register 2. This means the user also needs to read Interrupt Status Register 2. There is a similar OOL bit in Interrupt Status Register 2 and Interrupt Status Register 3, indicating an out-of-limit event in the next status register.

Alternatively, Pin 10 or Pin 14 can be configured as an $\overline{\text{SMBALERT}}$ output. This hard interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the interrupt status registers clears the appropriate status bit as long as the error condition that caused the

interrupt has cleared. Interrupt status register bits are sticky. Whenever an interrupt status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the interrupt status bit is to read the interrupt status register after the event has gone away. Interrupt status mask registers allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$ on the dedicated alert pin. However, if one of these masked interrupt sources goes out of limit, its associated interrupt status bit is set in the interrupt status registers.

Full details of the Interrupt Status and Interrupt Mask registers associated with each measurement channels are detailed in the Table 27 and in the full register map in the Register Tables section.

Table 27. INTERRUPT STATUS AND INTERRUPT MASK REGISTER ADDRESS AND BIT ASSIGNMENTS

Interrupt Status Register	Interrupt Mask Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	0x74	OOL	R2T	LT	R1T	+5 V_{IN}	V_{CC}	V_{CCP}	+2.5 V_{IN}/$\overline{\text{THERM}}$
0x42	0x75	D2 FAULT	D1 FAULT	FAN4/$\overline{\text{THERM}}$	FAN3	FAN2	FAN1	OOL	+12 V_{IN}
0x43	0x82	OOL	RES	RES	RES	OVT	COM M	DATA	PECI0
0x81	0x83	V_{TT}	I_{MON}	PECI3	PECI2	PECI1	RES	RES	RES

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7490 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

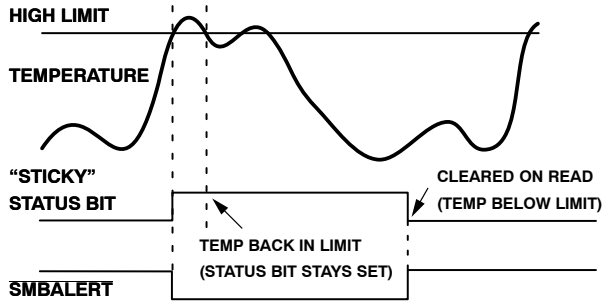


Figure 30. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

Figure 30 shows how the $\overline{\text{SMBALERT}}$ output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky, because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically.

Note that the $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74, 0x75, 0x82, and 0x83).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 31.

Masking Interrupt Sources

The interrupt mask registers allow individual interrupt sources to be masked out to prevent $\overline{\text{SMBALERT}}$ interrupts. Note that masking an interrupt source prevents only the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit is set normally (see Figure 31). Full details of the status and mask registers associated with each measurement channel are detailed in Table 27 and Table 44.

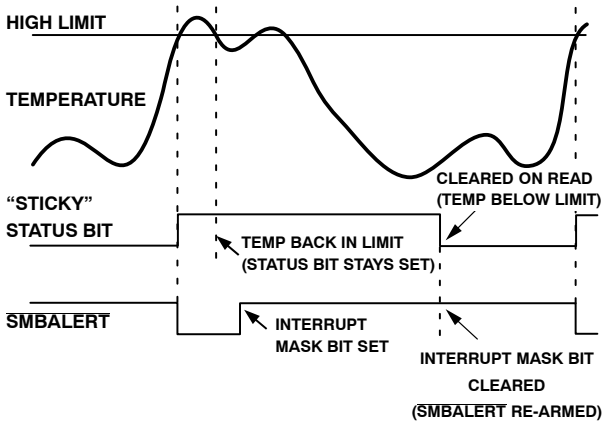


Figure 31. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 28. CONFIGURING PIN 10 AS $\overline{\text{SMBALERT}}$ OUTPUT

Register	Bit Setting
Configuration Register 3 (Register 0x78), Bit 0	[1] Pin 10 = $\overline{\text{SMBALERT}}$ [0] Pin 10 = PWM2 (Default)

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 14 on the ADT7490 has three possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

If $\overline{\text{THERM}}$ is enabled (Bit 1, Configuration Register 3 at Address 0x78),

- Pin 22 becomes $\overline{\text{THERM}}$.
- If Pin 14 is configured as $\overline{\text{THERM}}$ (Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D), $\overline{\text{THERM}}$ is enabled on this pin.

If $\overline{\text{THERM}}$ is not enabled,

- Pin 22 becomes a 2.5 V_{IN} measurement input.
- If Pin 14 is configured as $\overline{\text{THERM}}$, $\overline{\text{THERM}}$ is disabled on this pin.

Table 29. CONFIGURING PIN 14 IN REGISTER 0x7D

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	Reserved

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the ADT7490 so that the fans run at 100% when the $\overline{\text{THERM}}$ pin is driven low externally. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}.

If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 32 for more information.

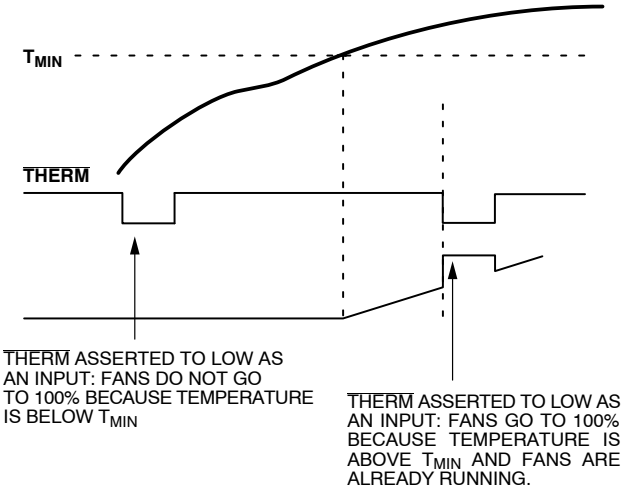


Figure 32. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7490 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7490 $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is deasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer status register (0x79) is designed so that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 33).