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SPI-/I²C-Compatible, Temperature Sensor, 4-Channel ADC and Quad Voltage Output

ADT7516/ADT7517/ADT7519

FEATURES

ADT7516: four 12-bit DACs
ADT7517: four 10-bit DACs
ADT7519: four 8-bit DACs
Buffered voltage output
Guaranteed monotonic by design over all codes
10-bit temperature-to-digital converter
10-bit 4-channel ADC
DC input bandwidth
Input range: 0 V to 2.28 V
Temperature range: −40°C to +120°C
Temperature sensor accuracy: ±0.5°C typ
Supply range: 2.7 V to 5.5 V
DAC output range: 0 V to 2 V_{REF}
Power-down current: <10 µA
Internal 2.28 V_{REF} option
Double-buffered input logic
Buffered reference input
Power-on reset to 0 V DAC output
Simultaneous update of outputs (LDAC function)
On-chip, rail-to-rail output buffer amplifier
SPI®, I²C®, QSPI™, MICROWIRE™, and DSP compatible
4-wire serial interface
SMBus packet error checking (PEC) compatible
16-lead QSOP package

APPLICATIONS

Portable battery-powered instruments
Personal computers
Smart battery chargers
Telecommunications systems
Electronic text equipment
Domestic appliances
Process control

PIN CONFIGURATION

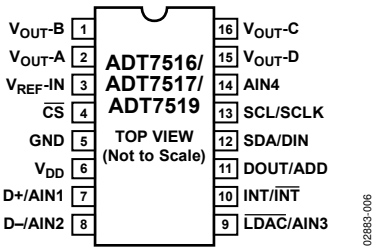

Figure 1.

GENERAL DESCRIPTION

The ADT7516/ADT7517/ADT7519[1] combine a 10-bit temperature-to-digital converter, a 10-bit 4-channel ADC, and a quad 12-/10-/8-bit DAC, respectively, in a 16-lead QSOP package. The parts also include a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C.

The ADT7516/ADT7517/ADT7519 operate from a single 2.7 V to 5.5 V supply. The input voltage range on the ADC channels is 0 V to 2.28 V, and the input bandwidth is dc. The reference for the ADC channels is derived internally. The output voltage of the DAC ranges from 0 V to V_{DD}, with an output voltage settling time of 7 µs typical.

The ADT7516/ADT7517/ADT7519 provide two serial interface options: a 4-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards, and a 2-wire SMBus/I²C interface. They feature a standby mode that is controlled through the serial interface.

The reference for the four DACs is derived either internally or from a reference pin. The outputs of all DACs can be updated simultaneously using the software LDAC function or the external $\overline{\text{LDAC}}$ pin. The ADT7516/ADT7517/ADT7519 incorporate a power-on reset circuit, ensuring that the DAC output powers up to 0 V and remains there until a valid write takes place.

The wide supply voltage range, low supply current, and SPI-/I²C-compatible interface of the ADT7516/ADT7517/ADT7519 make them ideal for a variety of applications, including personal computers, office equipment, and domestic appliances.

[1] Protected by U.S. Patent Numbers: 6,169,442; 5,867,012; and 5,764,174.

Rev. B

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Deleted ADT7518
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7/03—Initial Version: Rev. 0

SPECIFICATIONS

Temperature range is as follows: A version: −40°C to +120°C, V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.25 V, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DAC DC PERFORMANCE[2, 3]					
ADT7519					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic over all codes
ADT7517					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic over all codes
ADT7516					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.02	±0.9	LSB	Guaranteed monotonic over all codes
Offset Error		±0.4	±2	% of FSR	
Gain Error		±0.3	±2	% of FSR	
Lower Deadband		20	65	mV	Lower deadband exists only if offset error is negative, see Figure 40
Upper Deadband		60	100	mV	Upper deadband exists if $V_{REF} = V_{DD}$ and off-set plus gain error is positive, see Figure 41
Offset Error Drift[4]		−12		ppm of FSR/°C	
Gain Error Drift[4]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[4]		−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[4]		200		µV	See Figure 5
ADC DC ACCURACY					Maximum V_{DD} = 5 V
Resolution			10	Bits	
Total Unadjusted Error (TUE)		2	3	% of FSR	V_{DD} = 2.7 V to 5.5 V
Total Unadjusted Error (TUE)			2	% of FSR	V_{DD} = 3.3 V ±10%
Offset Error			±0.5	% of FSR	
Gain Error			±2	% of FSR	
ADC BANDWIDTH			DC	Hz	
ANALOG INPUTS					
Input Voltage Range	0		2.28	V	AIN1 to AIN4, C4 = 0 in Control Configuration 3
	0		V_{DD}	V	AIN1 to AIN4, C4 = 0 in Control Configuration 3
DC Leakage Current			±1	µA	
Input Capacitance		5	20	pF	
Input Resistance		10		MΩ	
THERMAL CHARACTERISTICS					
Internal Temperature Sensor					Internal reference used, averaging on
Accuracy @ V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C
		±0.5	±3	°C	T_A = 0°C to +85°C
		±2	±5	°C	T_A = −40°C to +120°C
Accuracy @ V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C
		±3	±5	°C	T_A = −40°C to +120°C
Resolution			10	Bits	Equivalent to 0.25°C
Long-Term Drift		0.25		°C	Drift over 10 years if part is operated at 55°C

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
External Temperature Sensor					External transistor = 2N3906
Accuracy @ V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C
			±3	°C	T_A = 0°C to +85°C
			±5	°C	T_A = −40°C to +120°C
Accuracy @ V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C
		±3	±5	°C	T_A = −40°C to +120°C
Resolution			10	Bits	Equivalent to 0.25°C
Output Source Current		180		µA	High level
		11		µA	Low level
Thermal Voltage Output					
8-Bit DAC Output					
Resolution	1			°C	
Scale Factor		8.97		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		17.58		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C
10-Bit DAC Output					
Resolution	0.25			°C	
Scale Factor		2.2		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		4.39		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C
CONVERSION TIMES					Single channel mode
Slow ADC					
V_{DD}/AIN		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
Internal Temperature		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
External Temperature		24.22		ms	Averaging (16 samples) on
		1.51		ms	Averaging off
Fast ADC					
V_{DD}/AIN		712		µs	Averaging (16 samples) on
		44.5		µs	Averaging off
Internal Temperature		2.14		ms	Averaging (16 samples) on
		134		µs	Averaging off
External Temperature		14.25		ms	Averaging (16 samples) on
		890		µs	Averaging off
ROUND ROBIN UPDATE RATE[5]					Time to complete one measurement cycle through all channels
Slow ADC @ 25°C					
Averaging On		79.8		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging Off		4.99		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging On		94.76		ms	D+ and D– are selected on Pin 7 and Pin 8
Averaging Off		9.26		ms	D+ and D– are selected on Pin 7 and Pin 8
Fast ADC @ 25°C					
Averaging On		6.41		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging Off		400.84		µs	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging On		21.77		ms	D+ and D– are selected on Pin 7 and Pin 8
Averaging Off		3.07		ms	D+ and D– are selected on Pin 7 and Pin 8
DAC EXTERNAL REFERENCE INPUT[4]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference
V_{REF} Input Impedance		>10		MΩ	Buffered reference and power-down mode
Reference Feedthrough		−90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
ON-CHIP REFERENCE					
Reference Voltage[4]	2.2662	2.28	2.2938	V	
Temperature Coefficient[4]		80		ppm/°C	
OUTPUT CHARACTERISTICS[4]					
Output Voltage[6]	0.001		V_{DD} − 0.1	V	This is a measure of the minimum and maximum drive capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5		µs	Coming out of power-down mode, V_{DD} = 3.3 V
DIGITAL INPUTS[4]					
Input Current			±1	µA	V_{IN} = 0 V to V_{DD}
V_{IL}, Input Low Voltage			0.8	V	
V_{IH}, Input High Voltage	1.89			V	
Pin Capacitance		3	10	pF	All digital inputs
SCL, SDA Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
$\overline{LDAC}$ Pulse Width	20			ns	Edge triggered input
DIGITAL OUTPUT					
Digital High Voltage, V_{OH}	2.4			V	I_{SOURCE} = I_{SINK} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 3 mA
Output High Current, I_{OH}			1	mA	V_{OH} = 5 V
Output Capacitance, C_{OUT}			50	pF	
INT/$\overline{INT}$ Output Saturation Voltage			0.8	V	I_{OUT} = 4 mA
I^2C TIMING CHARACTERISTICS[7, 8]					
Serial Clock Period, t_1	2.5			µs	Fast mode I^2C, see Figure 2
Data In Setup Time to SCL High, t_2	50			ns	
Data Out Stable after SCL Low, t_3	0			ns	See Figure 2
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	See Figure 2
SDA High Hold Time after SCL High (Stop Condition), t_5	50			ns	See Figure 2
SDA and SCL Fall Time, t_6			300	ns	See Figure 2
SDA and SCL Rise Time, t_7			300[9]	ns	See Figure 2
SPI TIMING CHARACTERISTICS[4, 10]					
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	See Figure 3
SCLK High Pulse Width, t_2	50			ns	See Figure 3
SCLK Low Pulse Width, t_3	50			ns	See Figure 3
Data Access Time after SCLK Falling Edge, t_4[11]			35	ns	
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	See Figure 3
Data Hold Time after SCLK Rising Edge, t_6	0			ns	See Figure 3
$\overline{CS}$ to SCLK Hold Time, t_7	0			µs	See Figure 3
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	See Figure 3
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of its final voltage level
I_{DD} (Normal Mode)[12]			3	mA	V_{DD} = 3.3 V, V_{IH} = V_{DD}, and V_{IL} = GND
		2.2	3	mA	V_{DD} = 5 V, V_{IH} = V_{DD}, and V_{IL} = GND

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
I_{DD} (Power-Down Mode)			10	µA	V_{DD} = 3.3 V, V_{IH} = V_{DD}, and V_{IL} = GND
			10	µA	V_{DD} = 5 V, V_{IH} = V_{DD}, and V_{IL} = GND
Power Dissipation			10	mW	V_{DD} = 3.3 V, normal mode
			33	µW	V_{DD} = 3.3 V, shutdown mode

[1] See the Terminology section.
[2] DC specifications are tested with the outputs unloaded.
[3] Linearity is tested using a reduced code range: ADT7516 (Code 115 to 4095); ADT7517 (Code 28 to 1023); ADT7519 (Code 8 to 255).
[4] Guaranteed by design and characterization, not production tested.
[5] Round robin is the continuous sequential measurement of the following channels: V_{DD}, internal temperature, external temperature (AIN1, AIN2), AIN3, and AIN4.
[6] For the amplifier output to reach its minimum voltage, the offset error must be negative. For the amplifier output to reach its maximum voltage (V_{REF} = V_{DD}), the offset plus gain error must be positive.
[7] The SDA and SCL timing is measured with the input filters turned on to meet the fast mode I^2C specification. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[8] Guaranteed by design, not production tested. All I^2C timing specifications are for fast mode operation but the interface is still capable of handling the slower standard rate specifications.
[9] The interface is also capable of handling the I^2C standard mode rise time specification of 1000 ns.
[10] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}), and timed from a voltage level of 1.6 V.
[11] Measured with the load circuit shown in Figure 4.
[12] The I_{DD} specification is valid for all DAC codes and full-scale analog input voltages. Interface inactive. All DACs and ADCs active. Load currents excluded.

DAC AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 4.7 kΩ to GND, C_L = 200 pF to GND, 4.7 kΩ to V_{DD}, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Min	Typ[3]	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V_{REF} = V_{DD} = 5 V
ADT7519		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0)
ADT7517		7	9	µs	1/4 scale to 3/4 scale change (0x100 to 0x300)
ADT7516		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ±0.1 V p-p
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ±0.1 V p-p; frequency = 10 kHz

[1] See the Terminology section.
[2] Guaranteed by design and characterization, not production tested.
[3] At 25°C.

TIMING DIAGRAMS

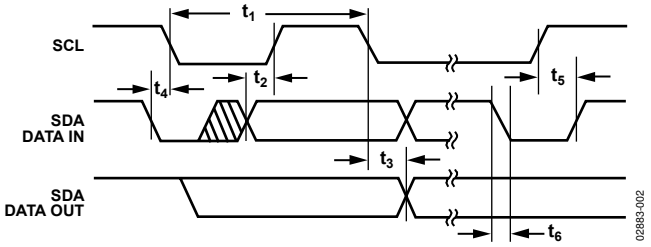

Figure 2. I²C Bus Timing Diagram

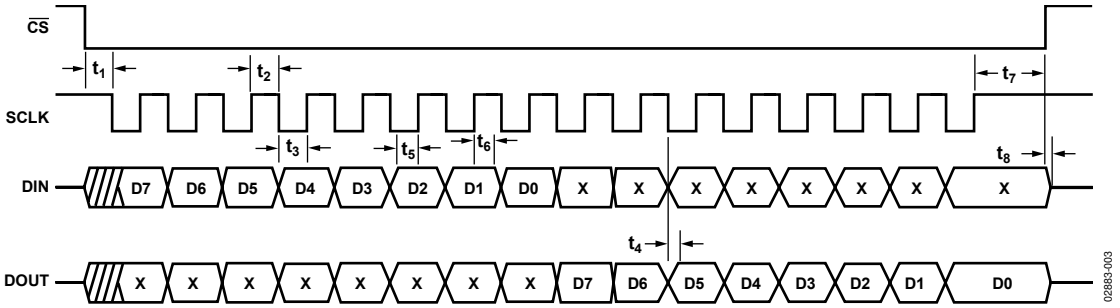

Figure 3. SPI Bus Timing Diagram

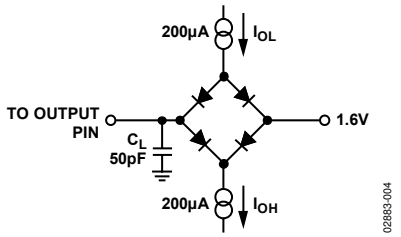

Figure 4. Load Circuit for Access Time and Bus Relinquish Time

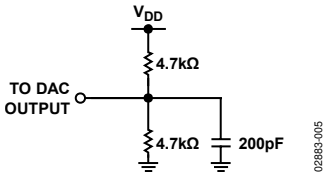

Figure 5. Load Circuit for DAC Outputs

FUNCTIONAL BLOCK DIAGRAM

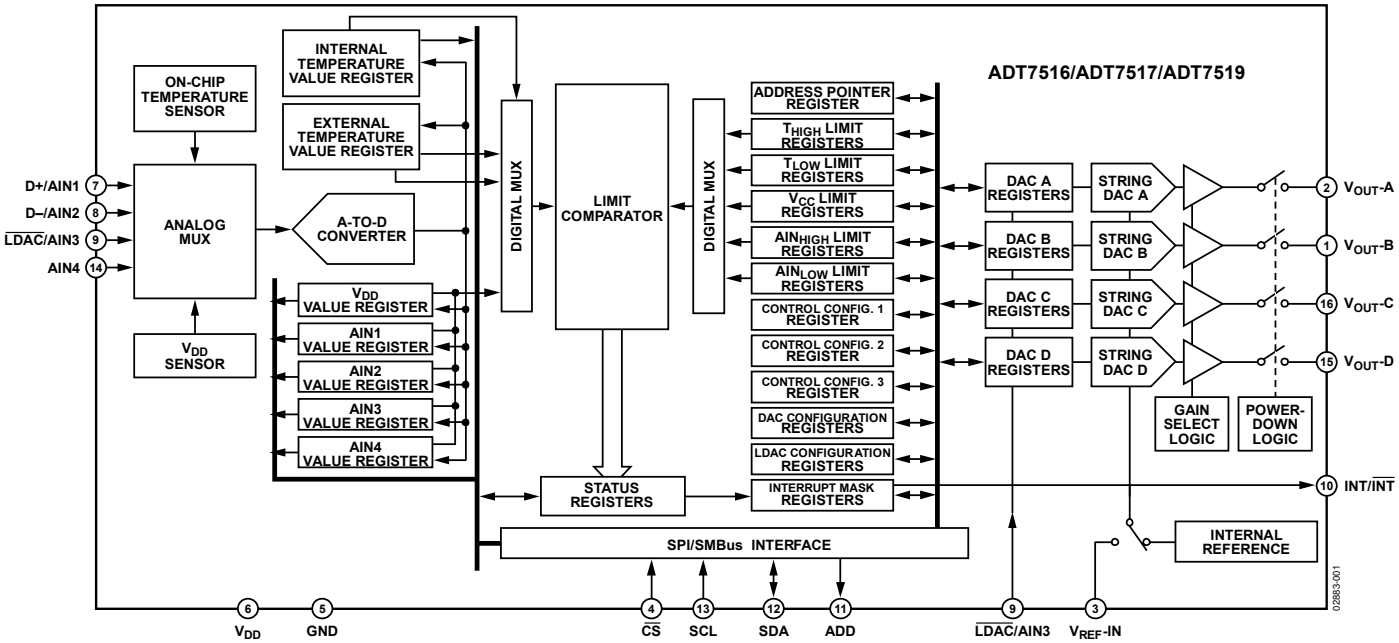

Figure 6. Functional Block Diagram for the ADT7516/ADT7517/ADT7519

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +120°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Power Dissipation[1]	(T_J max – T_A)/θ_{JA}
Thermal Impedance[2]	
θ_{JA} Junction-to-Ambient	105.44°C/W
θ_{JC} Junction-to-Case	38.8°C/W
IR Reflow Soldering	
Peak Temperature	220°C (0°C/5°C)
Time at Peak Temperature	10 sec to 20 sec
Ramp-Up Rate	3°C/sec maximum
Ramp-Down Rate	–6°C/sec maximum
Time 25°C to Peak Temperature	6 min maximum
IR Reflow Soldering (Pb-Free Package)	
Peak Temperature	260°C (+0°C)
Time at Peak Temperature	20 sec to 40 sec
Ramp-Up Rate	3°C/sec maximum
Ramp-Down Rate	–6°C/sec maximum
Time 25°C to Peak Temperature	8 min maximum

[1] Values relate to the package being used on a 4-layer board.
[2] Junction-to-case resistance is applicable to components featuring a preferential flow direction, for example, components mounted on a heat sink. Junction-to-ambient resistance is more useful for air cooled PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. I²C Address Selection

ADD Pin	I²C Address
Low	1001 000
Float	1001 010
High	1001 011

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

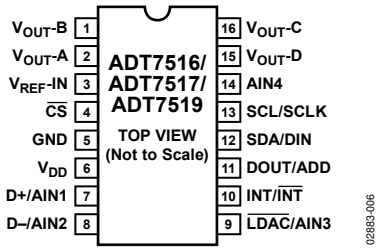

Figure 7. Pin Configuration (QSOP Package)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}-B	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V_{OUT}-A	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V_{REF}-IN	Reference Input Pin for All Four DACs. This input is buffered and has an input range from 1 V to V_{DD}.
4	$\overline{CS}$	SPI Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register, and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V_{DD} when operating the serial interface in I^2C mode.
5	GND	Ground Reference Point. Ground reference point for all circuitry on the part. Analog and digital ground.
6	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
7	D+/AIN1	D+: Positive Connection to External Temperature Sensor. AIN1: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
8	D–/AIN2	D–: Negative Connection to External Temperature Sensor. AIN2: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
9	$\overline{LDAC}$/AIN3	$\overline{LDAC}$: Active Low Control Input. Transfers the contents of the input registers to their respective DAC registers. A falling edge on this pin forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20 ns must be applied to the $\overline{LDAC}$ pin to ensure proper loading of a DAC register. This allows simultaneous update of all DAC outputs. Bit C3 of the Control Configuration 3 register enables the $\overline{LDAC}$ pin. Default is with the $\overline{LDAC}$ pin controlling the loading of the DAC registers. AIN3: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
10	INT/$\overline{INT}$	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature, V_{DD}, or AIN limits are exceeded. The default is active low. Open-drain output, needs a pull-up resistor.
11	DOUT/ADD	DOUT: SPI Serial Data Output. Logic output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open-drain output, needs a pull-up resistor. ADD: I^2C Serial Bus Address Selection Pin. Logic input. A low on this pin gives the Address 1001 000; leaving it floating gives the Address 1001 010; and setting it high gives the address 1001 011. The I^2C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent change on this pin has no effect on the I^2C serial bus address.
12	SDA/DIN	SDA: I^2C Serial Data Input/Output. I^2C serial data to be loaded into the registers of the part and read from these registers is provided on this pin. Open-drain configuration, needs a pull-up resistor. DIN: SPI Serial Data Input. Serial data to be loaded into the part's registers is provided on this pin. Data is clocked into a register on the rising edge of SCLK. Open-drain configuration, needs a pull-up resistor.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7516/ADT7517/ADT7519, and also to clock data into any register that can be written to. Open-drain configuration, needs a pull-up resistor.
14	AIN4	Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
15	V_{OUT}-D	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V_{OUT}-C	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

TYPICAL PERFORMANCE CHARACTERISTICS

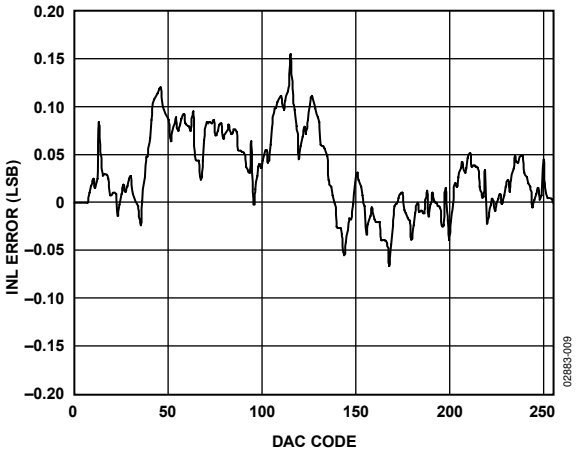

Figure 8. ADT7519 Typical DAC INL Plot

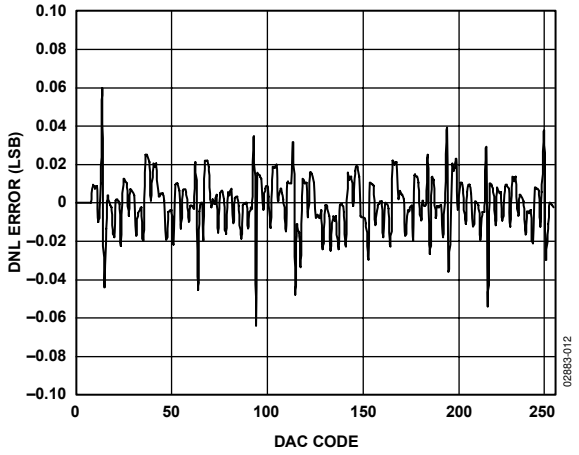

Figure 11. ADT7519 Typical DAC DNL Plot

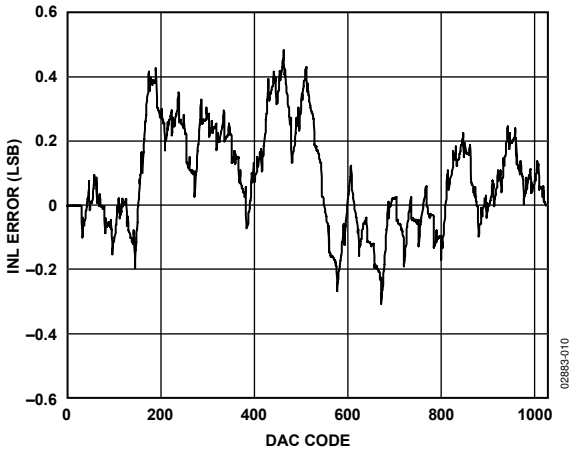

Figure 9. ADT7517 Typical DAC INL Plot

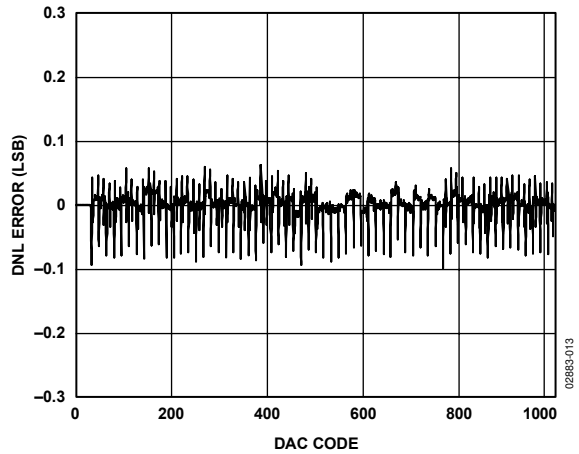

Figure 12. ADT7517 Typical DAC DNL Plot

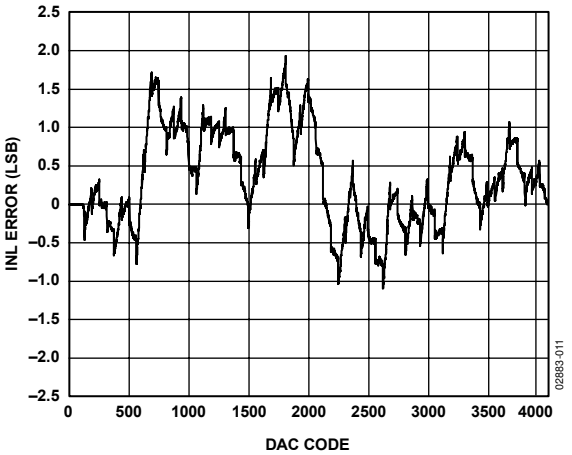

Figure 10. ADT7516 Typical DAC INL Plot

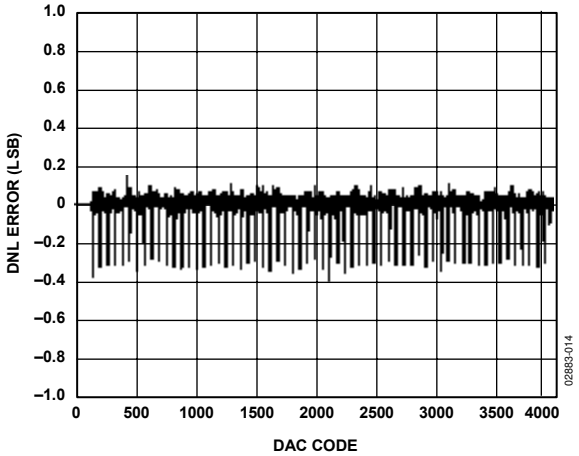

Figure 13. ADT7516 Typical DAC DNL Plot

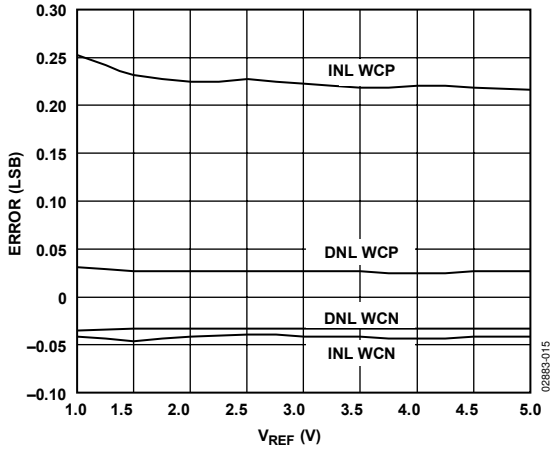

Figure 14. ADT7519 DAC INL and DNL Error vs. V_{REF}

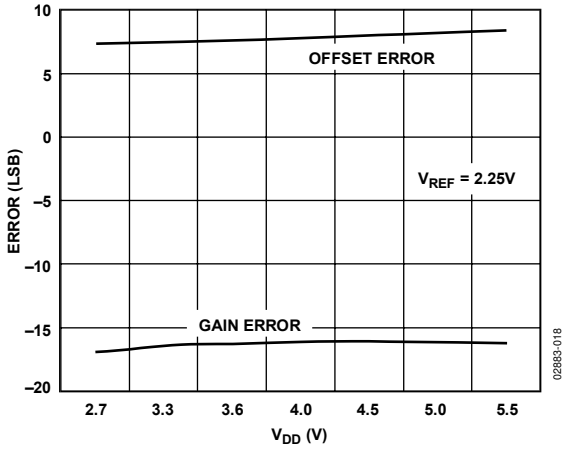

Figure 17. DAC Offset Error and Gain Error vs. V_{DD}

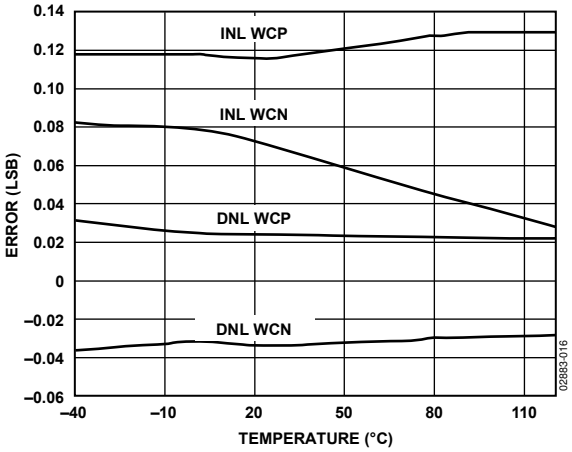

Figure 15. ADT7519 DAC INL Error and DNL Error vs. Temperature

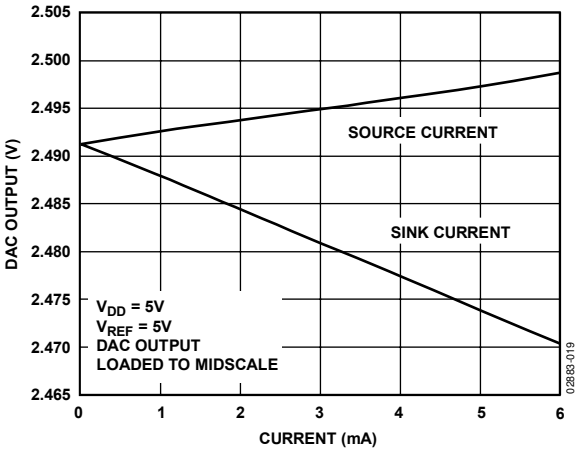

Figure 18. DAC V_{OUT} Source and Sink Current Capability

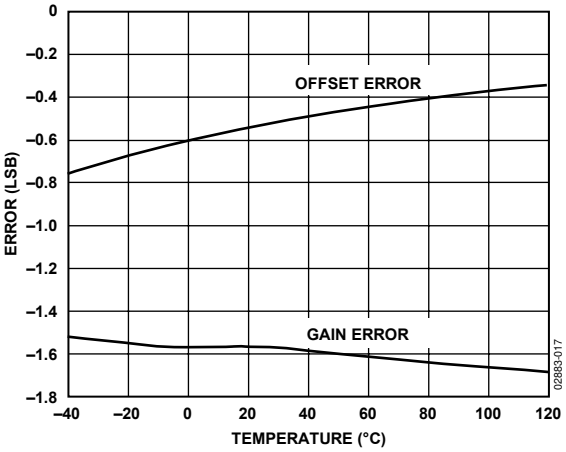

Figure 16. DAC Offset Error and Gain Error vs. Temperature

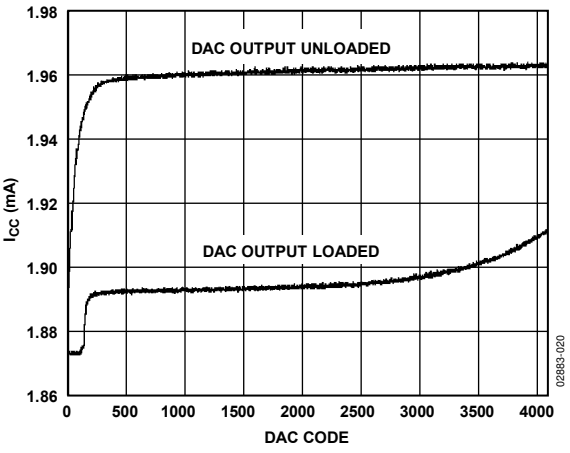

Figure 19. Supply Current vs. DAC Code

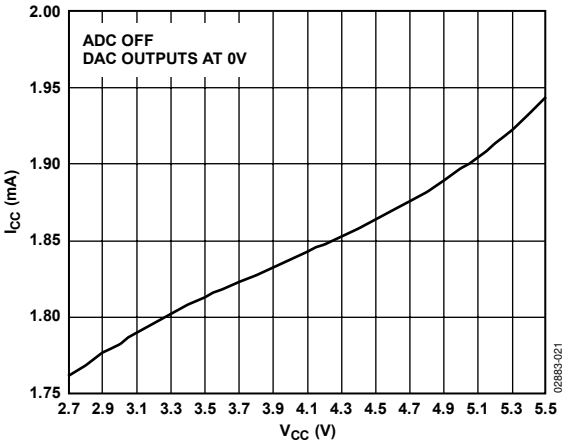

Figure 20. Supply Current vs. Supply Voltage @ 25°C

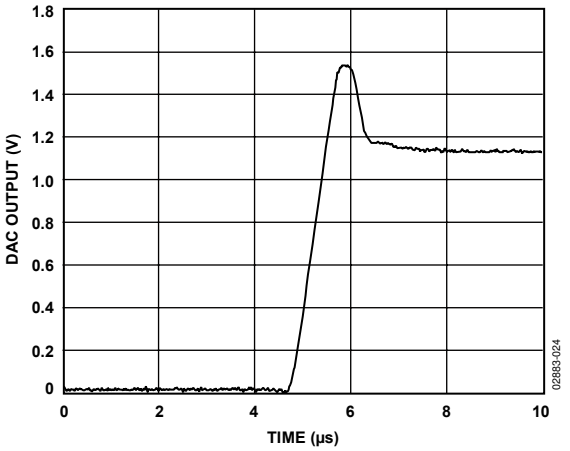

Figure 23. Exiting Power-Down to Midscale

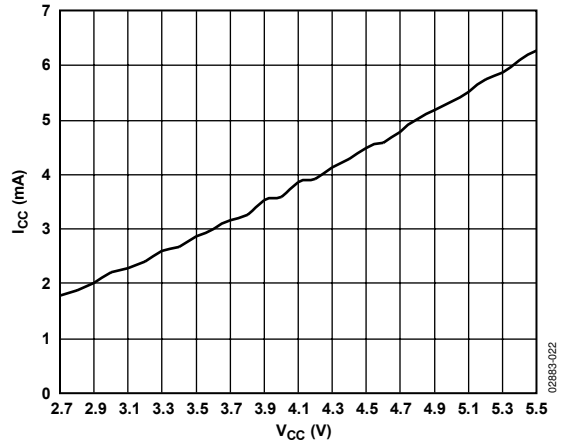

Figure 21. Power-Down Current vs. Supply Voltage @ 25°C

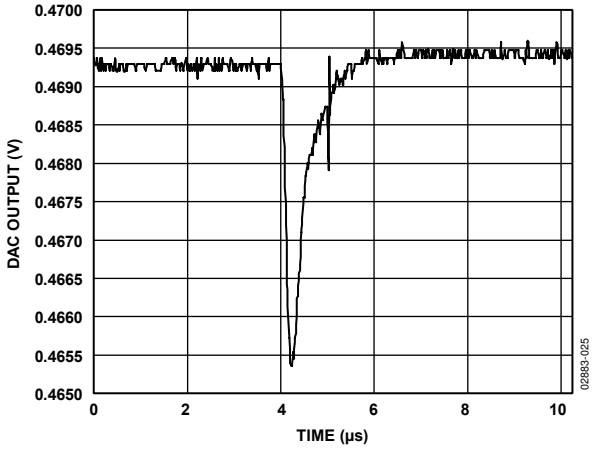

Figure 24. ADT7516 DAC Major Code Transition Glitch Energy; 011…11 to 100...00

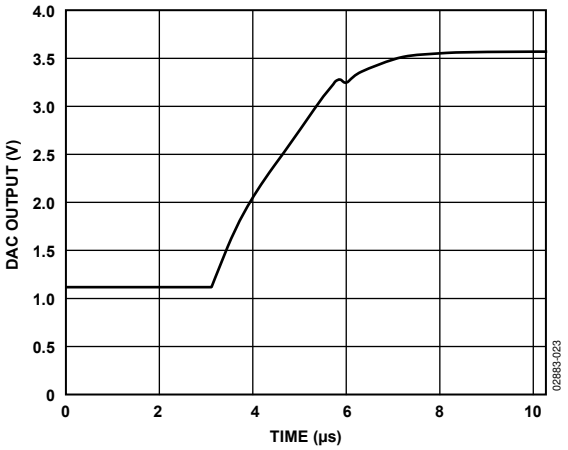

Figure 22. DAC Half-Scale Settling (1/4 to 3/4 Scale Code Change)

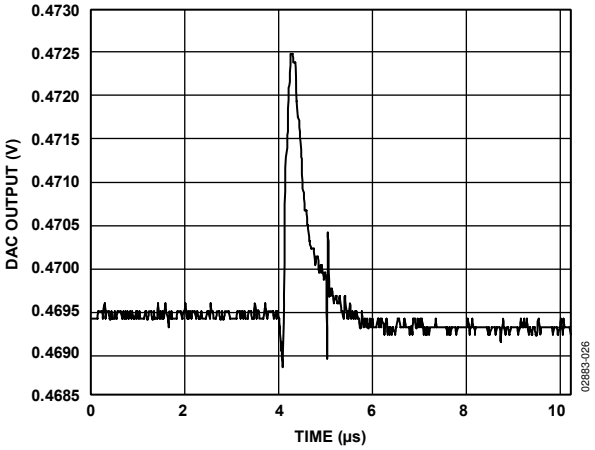

Figure 25. ADT7516 DAC Major Code Transition Glitch Energy; 100…00 to 011…11

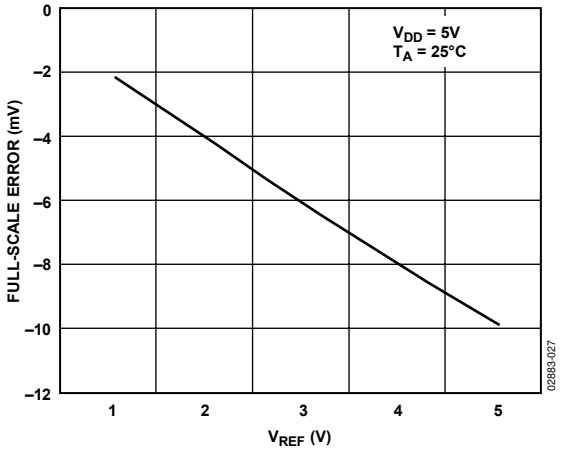

Figure 26. DAC Full-Scale Error vs. V_{REF}

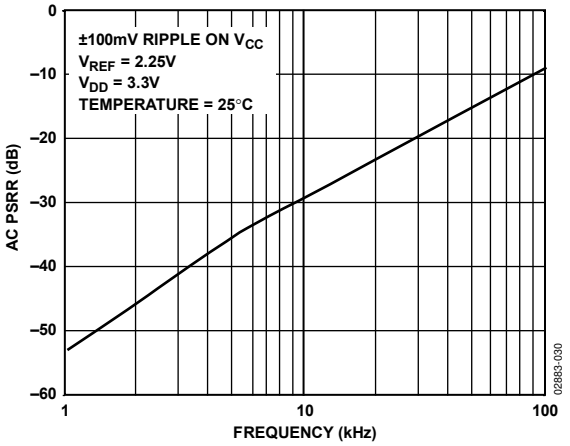

Figure 29. PSRR vs. Supply Ripple Frequency

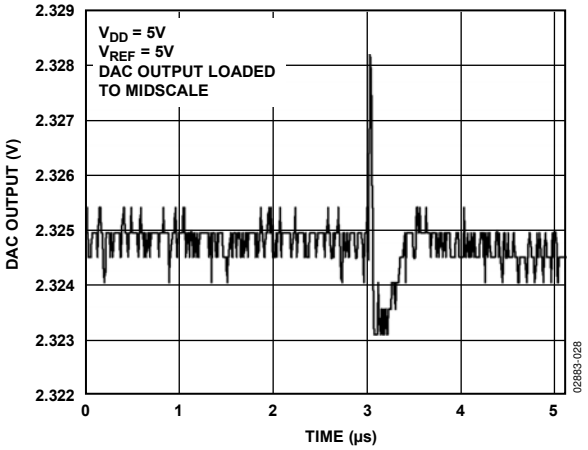

Figure 27. DAC-to-DAC Crosstalk

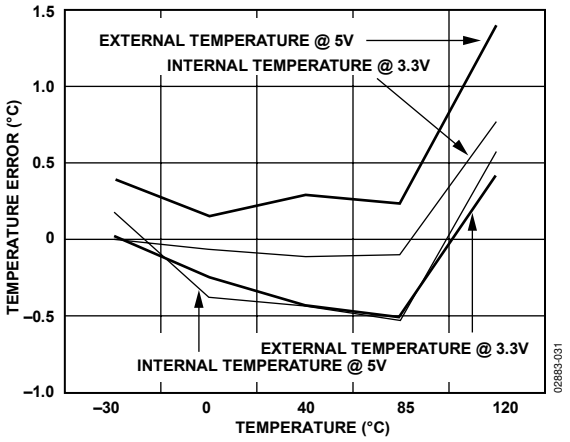

Figure 30. Internal Temperature Error @ 3.3 V and 5 V

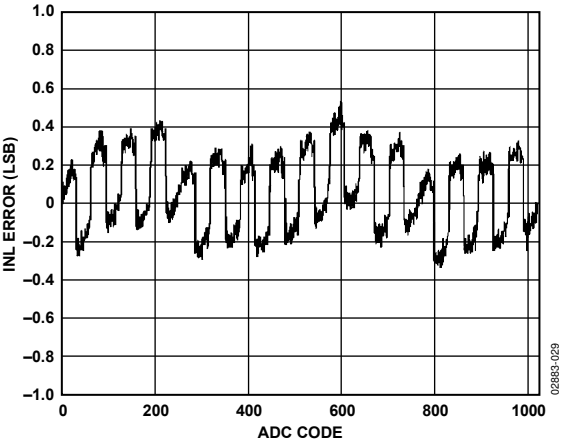

Figure 28. ADC INL with $V_{REF} = V_{DD}$ (3.3 V)

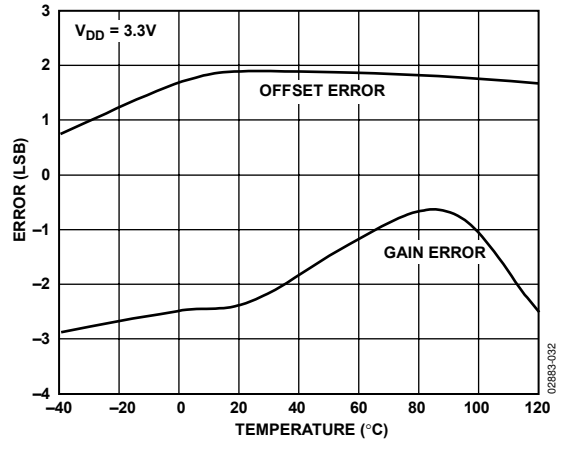

Figure 31. ADC Offset Error and Gain Error vs. Temperature

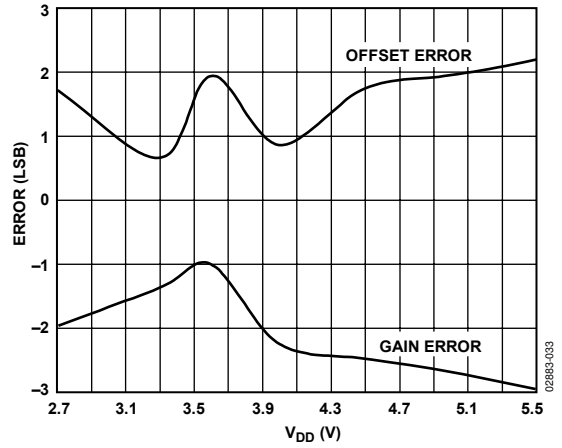

Figure 32. ADC Offset Error and Gain Error vs. V_{DD}

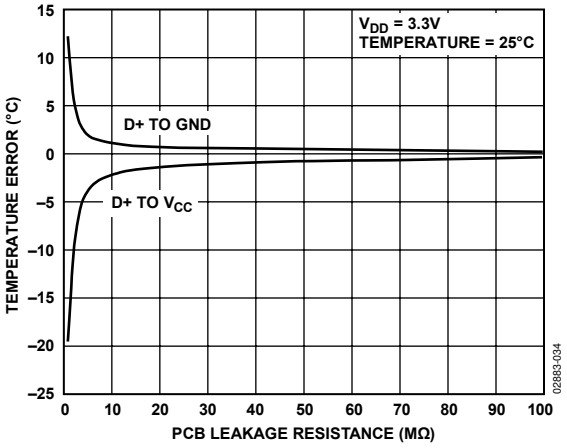

Figure 33. External Temperature Error vs. PCB Leakage Resistance

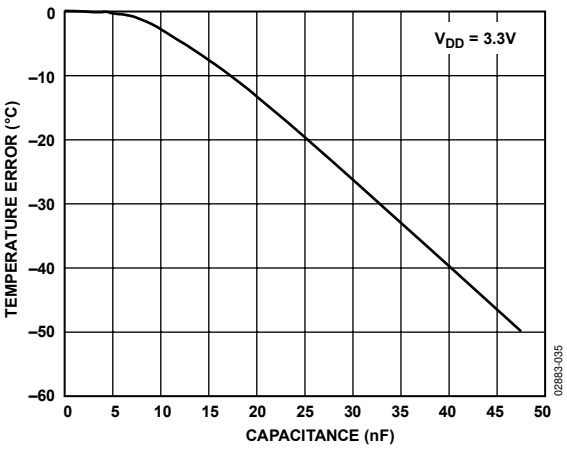

Figure 34. External Temperature Error vs. Capacitance Between D+ and D–

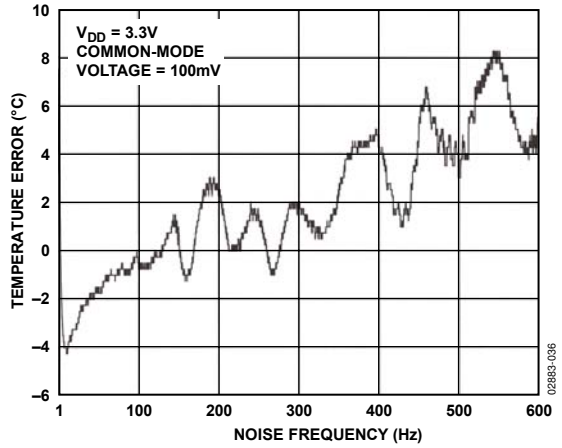

Figure 35. External Temperature Error vs. Common-Mode Noise Frequency

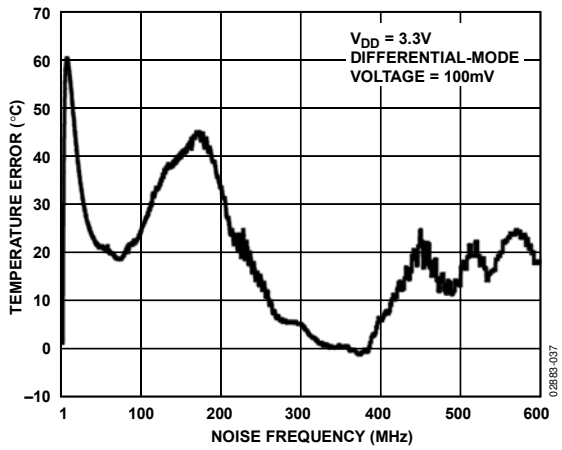

Figure 36. External Temperature Error vs. Differential-Mode Noise Frequency

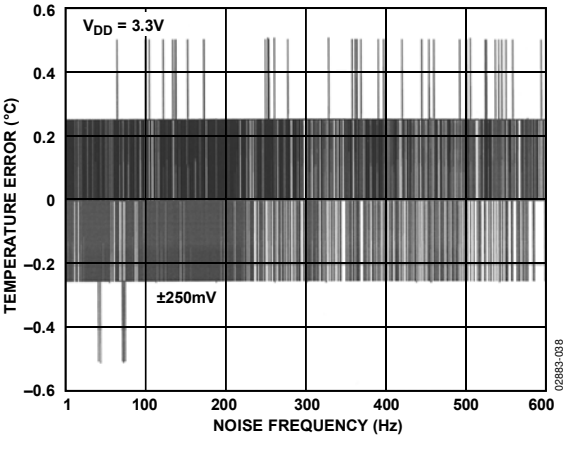

Figure 37. Internal Temperature Error vs. Power Supply Noise Frequency

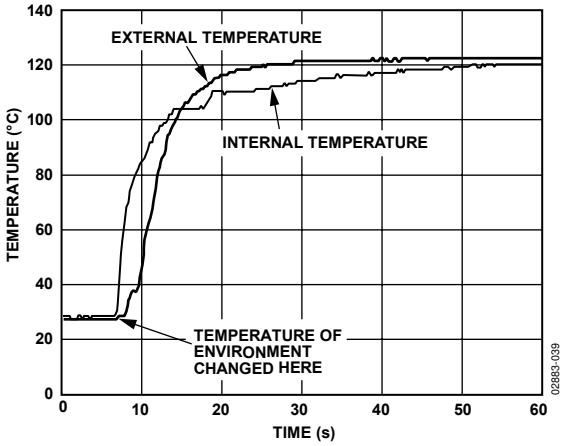

Figure 38. Temperature Sensor Response to Thermal Shock

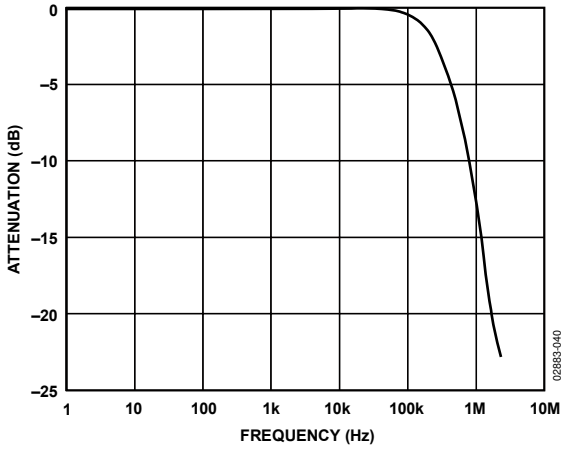

Figure 39. DAC Multiplying Bandwidth (Small Signal Frequency Response)

TERMINOLOGY

Relative Accuracy
Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the transfer function. Typical INL vs. code plots are shown in Figure 8, Figure 9, and Figure 10.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±0.9 LSB maximum ensures monotonicity. Typical DAC DNL vs. code plots can be seen in Figure 11, Figure 12, and Figure 13.

Total Unadjusted Error (TUE)
Total unadjusted error is a comprehensive specification that includes the sum of the relative accuracy error, gain error, and offset error under a specified set of conditions.

Offset Error
Offset error is a measure of the offset error of the DAC and the output amplifier (see Figure 40 and Figure 41). It can be negative or positive, and it is expressed in mV.

Offset Error Match
Offset error match is the difference in offset error between any two channels.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Gain Error Match
Gain error match is the difference in gain error between any two channels.

Offset Error Drift
Offset error drift is a measure of the change in offset error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Long-Term Temperature Drift
Long-term temperature drift is a measure of the change in temperature error with the passage of time. It is expressed in °C. The concept of long-term stability has been used for many years to describe the amount an IC parameter shifts during its lifetime. This is a concept that has typically been applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. Manufacturers perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period (typically between 500 hours and 1000 hours). As a result, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in µV.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, LDAC is high). It is expressed in dB.

Channel-to-Channel Isolation
Channel-to-channel isolation is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

Major Code Transition Glitch Energy
Major code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device. However, it is measured when the DAC is not being written to. It is specified in nV-s and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output, expressed in dB.

Round Robin
The term round robin is used to describe the ADT7516/ADT7517/ADT7519 cycling through the available measurement channels in sequence, taking a measurement on each channel.

DAC Output Settling Time
DAC output settling time is the time required, following a prescribed data change, for the output of a DAC to reach and remain within ±0.5 LSB of the final value. A typical prescribed change is from 1/4 scale to 3/4 scale.

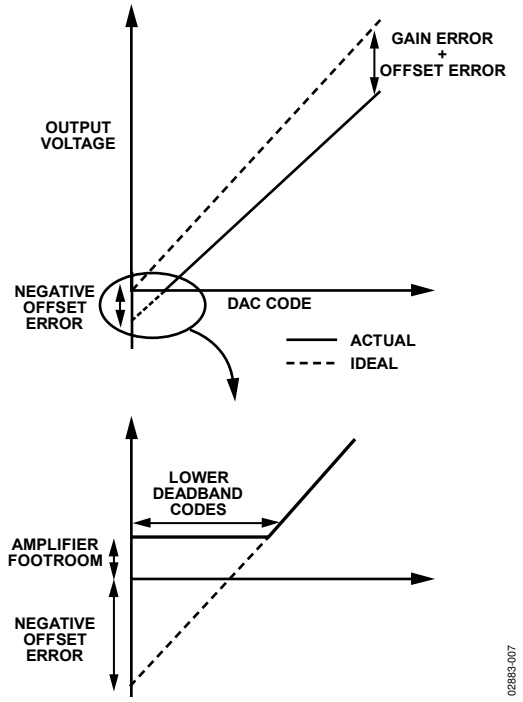

Figure 40. DAC Transfer Function with Negative Offset

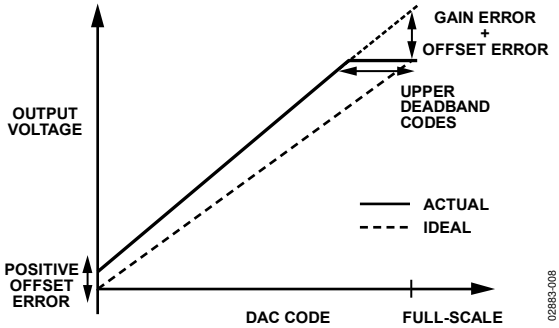

Figure 41. DAC Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)

THEORY OF OPERATION

Directly after the power-up calibration routine, the ADT7516/ADT7517/ADT7519 go into idle mode. In this mode, the devices are not performing any measurements and are fully powered up. All four DAC outputs are at 0 V.

To begin monitoring, write to the Control Configuration 1 register (Address 0x18) and set Bit C0 = 1. The ADT7516/ADT7517/ADT7519 go into the power-up default measurement mode (round robin). The devices proceed to take measurements on the V_{DD} channel, internal temperature sensor channel, external temperature sensor channel (AIN1 and AIN2), AIN3, and finally AIN4. After they finish taking measurements on the AIN4 channel, the devices immediately loop back to start taking measurements on the V_{DD} channel and repeat the same cycle as before. This loop continues until the monitoring is stopped by resetting Bit C0 of the Control Configuration 1 register to 0.

It is also possible to continue monitoring as well as switching to single-channel mode by writing to the Control Configuration 2 register (Address 0x19) and setting Bit C4 = 1. Further explanation of the single-channel and round robin measurement modes is given in later sections. All measurement channels have averaging enabled on them at power-up. Averaging forces the devices to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set Bit C5 = 1 in the Control Configuration 2 register.

There are four single-ended analog input channels on the ADT7516/ADT7517/ADT7519, AIN1 to AIN4. AIN1 and AIN2 are multiplexed with the external temperature sensor terminals (D+ and D−). Bit C1 and Bit C2 of the Control Configuration 1 register (Address 0x18) are used to select between AIN1/AIN2 and the external temperature sensor. The input range on the analog input channels is dependent on whether the ADC reference used is the internal V_{REF} or V_{DD}. To meet linearity specifications, it is recommended that the maximum V_{DD} value is 5 V. Bit C4 of the Control Configuration 3 register be used to select between the internal reference and V_{DD} as the ADC reference of the analog inputs.

Controlling the DAC outputs can be done by writing to the MSB and LSB registers of the DAC (Address 0x10 to Address 0x17). The power-up default setting is to have a low going pulse on the $\overline{\text{LDAC}}$ pin (Pin 9) controlling the updating of the DAC outputs from the DAC registers. Alternatively, one can configure the updating of the DAC outputs to be controlled by means other than the $\overline{\text{LDAC}}$ pin by setting Bit C3 = 1 of the Control Configuration 3 register (Address 0x1A). The DAC configuration register (Address 0x1B) and the LDAC configuration register (Address 0x1C) can now be used to control the DAC updating. These two registers also control the output range of the DACs and select between the internal or external reference. DAC A and DAC B outputs can be configured to give a voltage output proportional to the temperature of the internal and external temperature sensors, respectively.

The dual serial interface defaults to the I^2C protocol on power-up. To select and lock in the SPI protocol, follow the selection process as described in the Serial Interface Selection section. The I^2C protocol cannot be locked in, though the SPI protocol is automatically locked in on selection. The interface can be switched back to be I^2C on selection when the device is powered off and on. When using I^2C, the $\overline{\text{CS}}$ pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7516/ADT7517/ADT7519 devices and all of them can be controlled by the configuration registers. These features consist of enabling and disabling interrupts, polarity of the INT/$\overline{\text{INT}}$ pin, enabling and disabling the averaging on the measurement channels SMBus timeout, and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part be initiated until approximately 5 ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50 ms to power up. Power-up time is directly related to the amount of decoupling on the voltage supply line.

During the 5 ms after V_{DD} has settled, the part is performing a calibration routine. Any communication to the device during calibration interrupts this routine, and can cause erroneous temperature measurements. If it is not possible to have V_{DD} at its nominal value by the time 50 ms has elapsed or if communication to the device has started prior to V_{DD} settling, it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

CONVERSION SPEED

The internal oscillator circuit used by the ADC has the capability to output two different clock frequencies. This means that the ADC is capable of running at two different speeds when doing a conversion on a measurement channel. Thus, the time taken to perform a conversion on a channel can be reduced by setting Bit C0 of the Control Configuration 3 register (Address 0x1A). This increases the ADC clock speed from 1.4 kHz to 22 kHz. At the higher clock speed, the analog filters on the D+ and D− input pins (external temperature sensors) are switched off. This is why the power-up default setting is to have the ADC working at the slow speed. The typical times for fast and slow ADC speeds are given in the Specifications section.

The ADT7516/ADT7517/ADT7519 power up with averaging on. This means every channel is measured 16 times and internally averaged to reduce noise. The conversion time can also be sped up by turning off the averaging. This is done by setting Bit C5 of the Control Configuration 2 register (Address 0x19) to 1.

FUNCTION DESCRIPTION—VOLTAGE OUTPUT

Digital-to-Analog Converters

The ADT7516/ADT7517/ADT7519 have four resistor string DACs fabricated on a CMOS process with resolutions of 12, 10, and 8 bits, respectively. They contain four output buffer amplifiers and are written to via I²C serial interface or SPI serial interface. See the Serial Interface section for more information.

The ADT7516/ADT7517/ADT7519 operate from a single supply of 2.7 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. All four DACs share a common reference input, V_{REF}-IN. The reference input is buffered to draw virtually no current from the reference source because it offers the source a high impedance input. The devices have a power-down mode to completely turn off all DACs with a high impedance output.

Each DAC output is not updated until it receives the LDAC command. Therefore, though the DAC registers would have been written to with a new value, this value is not represented by a voltage output until the DACs receive the LDAC command. Reading back from any DAC register prior to issuing an LDAC command results in the digital value that corresponds to the DAC output voltage. Thus, the digital value written to the DAC register cannot be read back until after the LDAC command has been initiated. This LDAC command can be given by either pulling the $\overline{\text{LDAC}}$ pin low (falling edge loads DACs), setting up Bit D4 and Bit D5 of the DAC configuration register (Address 0x1B), or using the LDAC register (Address 0x1C).

When using the $\overline{\text{LDAC}}$ pin to control the DAC register loading, the low going pulse width should be 20 ns minimum. The $\overline{\text{LDAC}}$ pin has to go high and low again before the DAC registers can be reloaded.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF}-IN pin or the on-chip reference of 2.28 V provides the reference voltage for the corresponding DAC. Figure 42 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register

0 to 255 for ADT7519 (8 bits)
0 to 1023 for ADT7517 (10 bits)
0 to 4095 for ADT7516 (12 bits)

N = DAC resolution.

Resistor String

The resistor string section is shown in Figure 43. It is simply a string of resistors, each of approximately 603 Ω. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

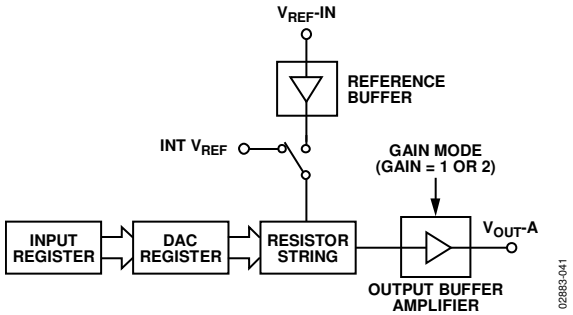

Figure 42. Single DAC Channel Architecture

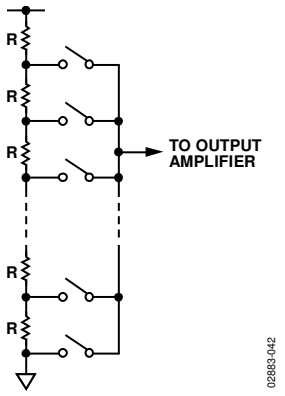

Figure 43. Resistor String

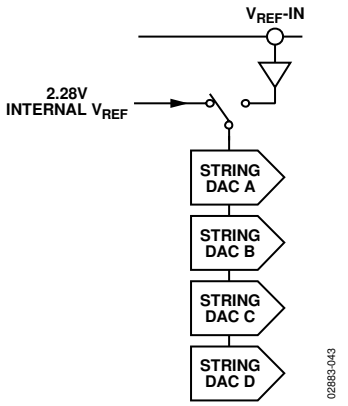

Figure 44. DAC Reference Buffer Circuit

DAC Reference Inputs

There is an input reference pin for the DACs. This reference input is buffered (see Figure 44).

The advantage of the buffered input is the high impedance it presents to the voltage source driving it. The user can have an external reference voltage as low as 1 V and as high as V_{DD}. The restriction of 1 V is due to the footroom of the reference buffer.

The $\overline{\text{LDAC}}$ configuration register controls the option to select between internal and external voltage references. The default selection is external reference.

Output Amplifier

The output buffer amplifier can generate output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, gain, and offset error.

If a gain of 1 is selected (Bit 0 to Bit 3 of the DAC configuration register = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (Bit 0 to Bit 3 of the DAC configuration register = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to V_{DD} − 0.001 V.

The output amplifier can drive a load of 4.7 kΩ to GND or V_{DD}, in parallel with 200 pF to GND or V_{DD} (see Figure 5). The source and sink capabilities of the output amplifier can be seen in the plot of Figure 18.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 µs.

Thermal Voltage Output

The ADT7516/ADT7517/ADT7519 can output voltages that are proportional to temperature. DAC A output can be configured to represent the temperature of the internal sensor and the DAC B output can be configured to represent the external temperature sensor. Bit C5 and Bit C6 of the Control Configuration 3 register select the temperature proportional output voltage. Each time a temperature measurement is taken, the DAC output is updated. The output resolution for the ADT7519 is 8 bits with 1°C change corresponding to 1 LSB change. The output resolution for the ADT7516 and ADT7517 is capable of 10 bits with 0.25°C change corresponding to 1 LSB change. The default output resolution for the ADT7516 and ADT7517 is 8 bits. To increase this to 10 bits, set C1 = 1 in the Control Configuration 3 register. The default output range is 0 V to V_{REF} and this can be increased to 0 V to 2 V_{REF}. Increasing the output voltage span to 2 V_{REF} can be done by setting D0 = 1 for DAC A (internal temperature sensor) and D1 = 1 for DAC B (external temperature sensor) in the DAC configuration register (Address 0x1B).

The output voltage is capable of tracking a maximum temperature range of −128°C to +127°C, but the default setting is −40°C to +127°C. If the output voltage range is 0 V to V_{REF}-IN (V_{REF}-IN = 2.25 V), then this corresponds to 0 V representing −40°C, and 1.48 V representing +127°C. This, of course, gives an upper deadband between 1.48 V and V_{REF}.

The internal and external analog temperature offset registers can be used to vary this upper deadband and, consequently, the temperature that 0 V corresponds to. Table 6 and Table 7 give examples of how this is done using a DAC output voltage span of V_{REF} and 2 V_{REF}, respectively. Simply write in the temperature value, in twos complement format, at which 0 V is to start. For example, if using the DAC A output and 0 V to start at −40°C, program 0xD8 into the internal analog temperature offset register (Address 0x21). This is an 8-bit register and has a temperature offset resolution of only 1°C for all device models. Use Equation 1 to Equation 4 to determine the value to program into the offset registers.

Table 6. Thermal Voltage Output (0 V to V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	−40	−128	0
0.5	+17	−71	+56
1	+73	−15	+113
1.12	+87	−1	+127
1.47	+127	+39	UDB[1]
1.5	UDB[1]	+42	UDB[1]
2	UDB[1]	+99	UDB[1]
2.25	UDB[1]	+127	UDB[1]

[1] Upper deadband has been reached. DAC output is not capable of increasing. See Figure 41.

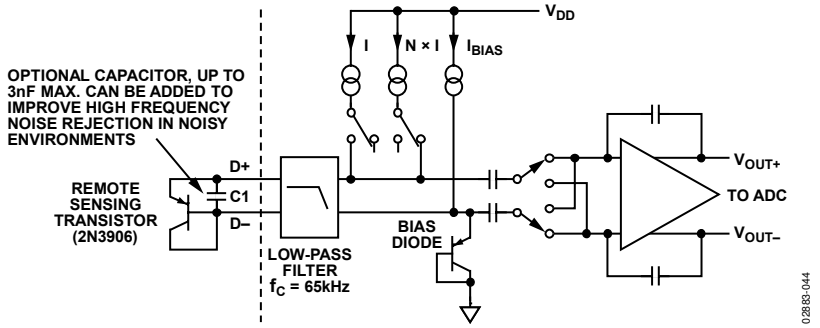

Figure 45. Signal Conditioning for External Diode Temperature Sensor

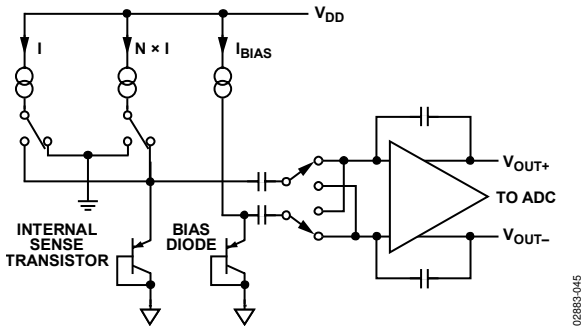

Figure 46. Top Level Structure of Internal Temperature Sensor

Table 7. Thermal Voltage Output (0 V to 2 V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	−40	−128	0
0.25	−26	−114	+14
0.5	+12	−100	+28
0.75	+3	−85	+43
1	+17	−71	+57
1.12	+23	−65	+63
1.47	+43	−45	+83
1.5	+45	−43	+85
2	+73	−15	+113
2.25	+88	0	+127
2.5	+102	+14	UDB[1]
2.75	+116	+28	UDB[1]
3	UDB[1]	+42	UDB[1]
3.25	UDB[1]	+56	UDB[1]
3.5	UDB[1]	+70	UDB[1]
3.75	UDB[1]	+85	UDB[1]
4	UDB[1]	+99	UDB[1]
4.25	UDB[1]	+113	UDB[1]
4.5	UDB[1]	+127	UDB[1]

[1] Upper deadband has been reached. DAC output is not capable of increasing. See Figure 41.

For negative temperatures,

Offset Register Code (d) = (*0 V Temp*) + 128 (1)

where D7 of *Offset Register Code* is set to 1 for negative temperatures.

For example,

Offset Register Code (d) = −40 + 128 = 88d = 0x58

Since a negative temperature has been inserted into the equation, DB7 (MSB) of the offset register code is set to 1. Therefore, 0x58 becomes 0xD8.

0x58 + DB7(1) = 0xD8

For positive temperatures,

Offset Register Code (d) = *0 V Temp* (2)

For example,

Offset Register Code (d) = 10d = 0x0A

The following equation is used to work out the various temperatures for the corresponding 8-bit DAC output:

8-Bit Temp = (*DAC O/P*)/1 LSB + (*0 V Temp*) (3)

For example, if the output is 1.5 V, V_{REF}-IN = 2.25 V, 8-bit DAC has an LSB size = 2.25 V/256 = 8.79×10^{-3}, and 0 V temp is at −128°C, then the resultant temperature is

$1.5/(8.79 \times 10^{-3}) + (-128) = +43°C$

The following equation is used to work out the various temperatures for the corresponding 10-bit DAC output:

10-Bit Temp = [(*DAC O/P*)/1 LSB] × 0.25 + (0 V *Temp*) (4)

For example, if the output is 0.4991 V, V_{REF}-IN = 2.25 V, 10-bit DAC has an LSB size = 2.25 V/1024 = 2.197×10^{-3}, and 0 V temperature is at −40°C, then the resulting temperature is

$[0.4991/(2.197 \times 10^{-3})] \times 0.25 + (-40) = +16.75°C$

Figure 47 shows a graph of the DAC output vs. temperature for a V_{REF}-IN = 2.25 V.

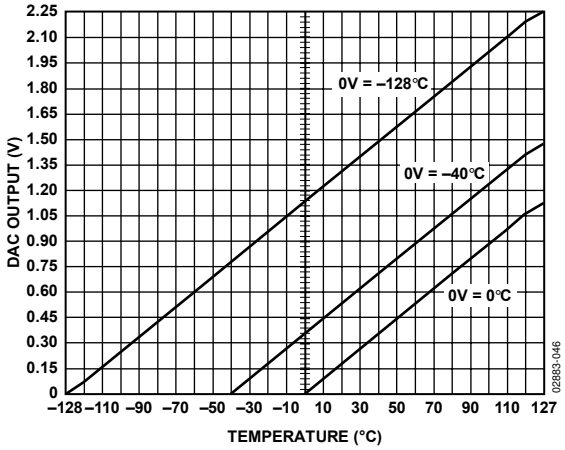

Figure 47. DAC Output vs. Temperature V_{REF}-IN = 2.25 V

FUNCTIONAL DESCRIPTION—ANALOG INPUTS

Single-Ended Inputs

The ADT7516/ADT7517/ADT7519 offer four single-ended analog input channels. The analog input range is from 0 V to 2.28 V, or 0 V to V_{DD}. To maintain the linearity specification, it is recommended that the maximum V_{DD} value be set at 5 V. Selection between the two input ranges is done by Bit C4 of the Control Configuration 3 register (Address 0x1A). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.28 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD}.

The ADC resolution is 10 bits and is mostly suitable for dc input signals. Bits[C1:C2] of the Control Configuration 1 register (Address 0x18) are used to set up Pin 7 and Pin 8 as AIN1 and AIN2. Figure 48 shows the overall view of the 4-channel analog input path.

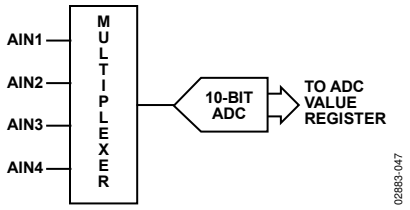

Figure 48. Quad Analog Input Path

Converter Operation

The analog input channels use a successive approximation ADC based on a capacitor DAC. Figure 49 and Figure 50 show simplified schematics of the ADC. Figure 49 shows the ADC during acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

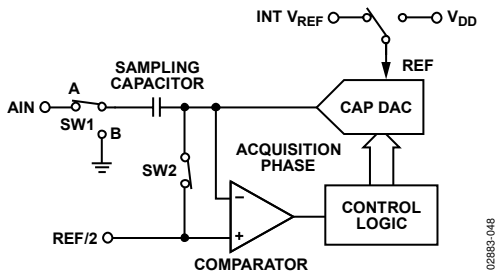

Figure 49. ADC Acquisition Phase

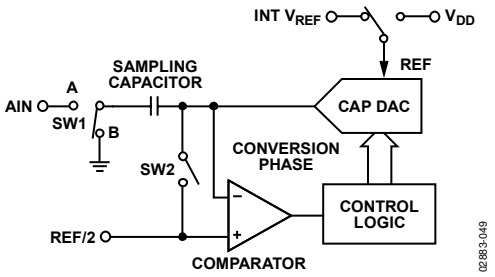

Figure 50. ADC Conversion Phase

When the ADC eventually goes into conversion phase (see Figure 50), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 51 shows the ADC transfer function for the analog inputs.

ADC TRANSFER FUNCTION

The output coding of the ADT7516/ADT7517/ADT7519 analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB). The LSB is $V_{DD}/1024$ or internal $V_{REF}/1024$, internal V_{REF} = 2.28 V. The ideal transfer characteristic is shown in Figure 51.

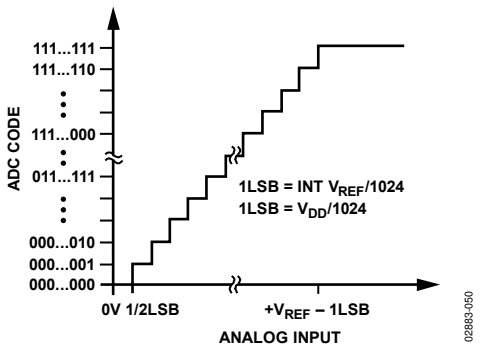

Figure 51. Single-Ended Transfer Function

To work out the voltage on any analog input channel, the following method can be used:

1 LSB = *reference* (V)/1024

Convert value read back from AIN value register into decimal.

AIN voltage = *AIN value* (d) × *LSB size*

where d = decimal.

For example, if internal reference is used, V_{REF} = 2.28 V.
AIN value = 512d

1 LSB size = 2.28 V/1024 = 2.226×10^{-3}

AIN voltage = $512 \times 2.226 \times 10^{-3}$ = 1.14 V

Analog Input ESD Protection

Figure 52 shows the input structure on any of the analog input pins that provide ESD protection. The diode provides the main ESD protection for the analog inputs. Care must be taken that the analog input signal never drops below the GND rail by more than 200 mV. If this happens, the diode becomes forward-biased and starts conducting current into the substrate. The 4 pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on resistance of the multiplexer switch.

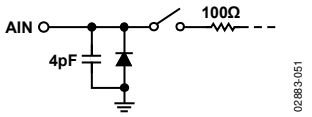

Figure 52. Equivalent Analog Input ESD Circuit

AIN Interrupts

The measured results from the AIN inputs are compared with the AIN V_{HIGH} (greater than comparison) and V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the AIN inputs exceed or equal the limit registers. These voltage limits are stored in on-chip registers. Note that the limit registers are 8 bits long and the AIN conversion result is 10 bits long. If the voltage limits are not masked out, then any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address = 0x00) and one or more out-of-limit results cause the INT/$\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application. Figure 53 shows the interrupt structure for the ADT7516/ ADT7517/ADT7519. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{\text{INT}}$ pin.

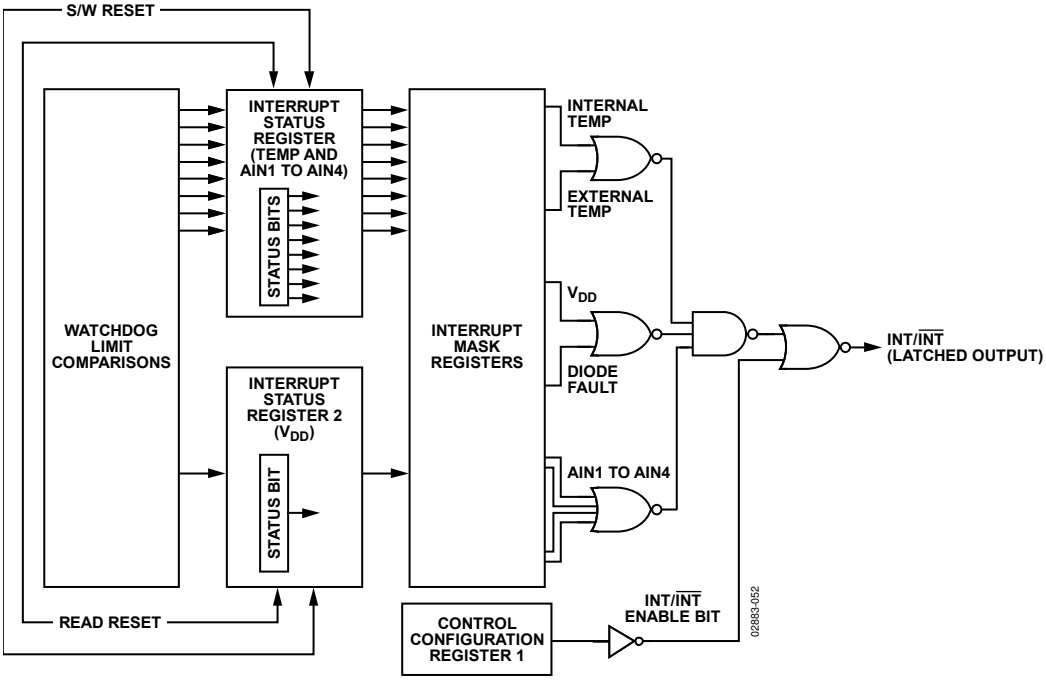

Figure 53. ADT7516/ADT7517/ADT7519 Interrupt Structure

FUNCTIONAL DESCRIPTION—MEASUREMENT

Temperature Sensor

The ADT7516/ADT7517/ADT7519 contain an ADC with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7516/ADT7517/ADT7519 operate in single-channel mode, the ADC continually processes the measurement taken on one channel only. This channel is preselected by Bits[C0:C2] in the Control Configuration 2 register (Address 0x19). When in round robin mode, the analog input multiplexer sequentially selects the V_{DD} input channel, the on-chip temperature sensor to measure its internal temperature, either the external temperature sensor or AIN1 and AIN2, AIN3, and then AIN4. These signals are digitized by the ADC and the results are stored in the various value registers.

The measured results from the temperature sensors are compared with the internal and external T_{HIGH} and T_{LOW} limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register. One or more out-of-limit results cause the INT/$\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature measuring circuit can measure temperatures from −128°C to +127°C with a resolution of 0.25°C. However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from −128°C to +127°C is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single-channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. In single-channel mode, the part is continuously monitoring the selected channel, that is, as soon as one measurement is taken another one is started on the same channel. The total time to measure a temperature channel with the ADC operating at slow speed is typically 11.4 ms (712 µs × 16) for the internal temperature sensor and 24.22 ms (1.51 ms × 16) for the external temperature sensor. The new temperature value is stored in two 8-bit registers and is ready for reading by the I^2C or SPI interface. The user has the option of disabling the averaging by setting Bit 5 in the Control Configuration 2 register (Address 0x19). The ADT7516/ADT7517/ADT7519 default on power-up is with averaging enabled.

The second method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode, the part is continuously measuring all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single-channel measurement mode or round robin measurement mode.

Once serial communication has started, any conversion in progress stops and the ADC resets. Conversion restarts immediately after the serial communication has finished. The temperature measurement proceeds normally as described above.

V_{DD} Monitoring

The ADT7516/ADT7517/ADT7519 also have the ability to monitor their own power supply. The part measures the voltage on its V_{DD} pin to a resolution of 10 bits. The resulting value is stored in two 8-bit registers; the two LSBs are stored in register Address 0x03 and the eight MSBs are stored in register Address 0x06. This allows the option of doing just a 1-byte read if 10-bit resolution is not important. The measured result is compared with the V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked, any out-of-limit comparison generates a flag in the Interrupt Status 2 register and one or more out-of-limit results cause the INT/$\overline{\text{INT}}$ output to pull either high or low, depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the internal, external, and AIN channels. The user can select the V_{DD} channel for single-channel measurement by setting Bit C4 = 1 and setting Bits[C0:C2] to all 0s in the Control Configuration 2 register.

When measuring the V_{DD} value, the reference for the ADC is sourced from the internal reference. Table 8 shows the data format. As the maximum measurable V_{DD} voltage is 7 V, internal scaling is performed on the V_{DD} voltage to match the 2.28 V internal reference value. Following is an example of how the transfer function works:

V_{DD} = 5 V

ADC Reference = 2.28 V

1 LSB = *ADC Reference*/2^{10}
= 2.28/1024
= 2.226 mV

Scale Factor = *Full-Scale* V_{CC}/*ADC Reference*
= 7/2.28
= 3.07

Conversion Result = V_{DD}/(*Scale Factor* × *LSB size*)
= 5/(3.07 × 2.226 mV)
= 0x2DC