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Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI MCU with Enhanced IRQ Handler

Data Sheet **ADuC7023**

FEATURES

- **Analog I/O**
  - **Multichannel, 12-bit, 1 MSPS ADC**
    - **Up to 12 ADC channels**
  - **Fully differential and single-ended modes**
  - **0 V to V_{REF} analog input range**
  - **12-bit voltage output DACs**
    - **4 DAC outputs available**
  - **On-chip voltage reference**
  - **On-chip temperature sensor**
  - **Voltage comparator**
- **Microcontroller**
  - **ARM7TDMI core, 16-bit/32-bit RISC architecture**
  - **JTAG port supports code download and debug**
- **Clocking options**
  - **Trimmed on-chip oscillator (±3%)**
  - **External watch crystal**
  - **External clock source up to 44 MHz**
  - **41.78 MHz PLL with programmable divider**
- **Memory**
  - **62 kB Flash/EE memory, 8 kB SRAM**
  - **In-circuit download, JTAG-based debug**
  - **Software-triggered in-circuit reprogrammability**
- **Vectored interrupt controller for FIQ and IRQ**
  - **8 priority levels for each interrupt type**
  - **Interrupt on edge or level external pin inputs**
- **On-chip peripherals**
  - **2× fully I²C-compatible channels**
  - **SPI (20 Mbps in master mode, 10 Mbps in slave mode)**
    - **With 4-byte FIFO on input and output stages**
  - **Up to 20 GPIO pins—Digital only GPIOs are 5 V tolerant**
  - **3× general-purpose timers**
    - **Watchdog timer (WDT)**
  - **Programmable logic array (PLA)**
    - **16 PLA elements**
  - **16-bit, 5-channel PWM**
- **Power**
  - **Specified for 3 V operation**
  - **Active mode: 11 mA at 5 MHz, 28 mA at 41.78 MHz**
- **Packages and temperature range**
  - **32-lead 5 mm × 5 mm LFCSP**
  - **40-lead LFCSP**
  - **36-Lead WLCSP**
- **Fully specified for −40°C to +125°C operation**
- **Tools**
  - **Low cost QuickStart development system**
  - **Full third-party support**

APPLICATIONS

Optical networking
Industrial control and automation systems
Smart sensors, precision instrumentation
Base station systems

GENERAL DESCRIPTION

The ADuC7023 is a fully integrated, 1 MSPS, 12-bit data acquisition system, incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash/EE memory on a single chip.

The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The ADC can operate in single-ended or differential input modes. The ADC input voltage is 0 V to V_{REF}. A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set.

The DAC output range is programmable to one of two voltage ranges. The DAC outputs have an enhanced feature of being able to retain their output voltage during a watchdog or software reset sequence.

The devices operate from an on-chip oscillator and a PLL, generating an internal high frequency clock of 41.78 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI®, 16-bit/32-bit RISC machine that offers up to 41 MIPS peak performance. Eight kilobytes of SRAM and 62 kilobytes of nonvolatile Flash/EE memory are provided on chip. The ARM7TDMI core views all memory and registers as a single linear array.

The ADuC7023 contains an advanced interrupt controller. The vectored interrupt controller (VIC) allows every interrupt to be assigned a priority level. It also supports nested interrupts to a maximum level of eight per IRQ and FIQ. When IRQ and FIQ interrupt sources are combined, a total of 16 nested interrupt levels are supported.

On-chip factory firmware supports in-circuit download via the I²C serial interface port, and nonintrusive emulation is supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ development system supporting this MicroConverter® family. The part contains a 16-bit PWM with five output signals.

For communication purposes, the part contains 2 × I²C channels that can be individually configured for master or slave mode. An SPI interface supporting both master and slave modes is also provided.

The parts operate from 2.7 V to 3.6 V and are specified over an industrial temperature range of −40°C to +125°C. The ADuC7023 is available in either a 32-lead or 40-lead LFCSP package. A 36-ball wafer level CSP package (WLCSP) is also available.

Rev. G Document Feedback

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COMPARABLE PARTS

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EVALUATION KITS

- ADuC7023 QuickStart Plus Development Systems

DOCUMENTATION

Application Notes

- AN-806: Flash Programming via I2C—Protocol Type 5

Data Sheet

- ADuC7023: Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI MCU with Enhanced IRQ Handler Data Sheet

User Guides

- UG-176: Evaluation Board User Guide for ADuC7023

REFERENCE DESIGNS

- CN0153

REFERENCE MATERIALS

Informational

- SFP Chipset and Reference Design Simplify 4.25 GBPS Transceivers

Technical Articles

- Integrated Route Taken to Pulse Oximetry
- Low Power, Low Cost, Wireless ECG Holter Monitor
- Part 1: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards
- Part 2: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards
- Precision Analog Microcontroller Simplifies Optical Transceiver Design

DESIGN RESOURCES

- ADuC7023 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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FUNCTIONAL BLOCK DIAGRAM

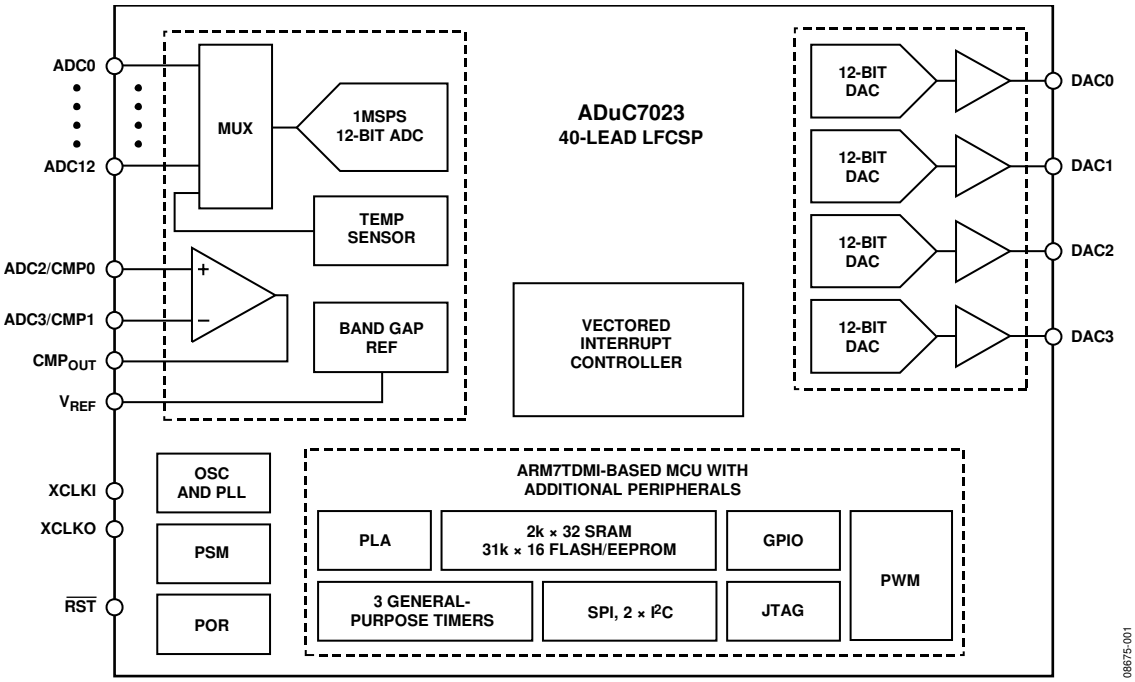

Figure 1.

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and $f_{ADC}/2$
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2		LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			$V_{CM} \pm V_{REF}/2$[6]	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±4	mV	T_A = 25°C
Reference Temperature Coefficient		±15		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		51		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					
DC Accuracy[7]					R_L = 5 kΩ, C_L = 100 pF
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
DC Accuracy[9]					R_L = 1 kΩ, C_L = 100 pF
Resolution		12		Bits	
Relative Accuracy		±2.5		LSB	
Differential Nonlinearity		±1		LSB	Guaranteed monotonic
Offset Error		±15		mV	2.5 V internal reference
Gain Error[10]		±1		%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range 1		0 to 2.5		V	V_{REF} range: AGND to AV_{DD}
Output Voltage Range 2		0 to AV_{DD}		V	
Output Impedance		2		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC IN OP AMP MODE					
DAC Output Buffer in Op Amp Mode					
Input Offset Voltage		±0.25		mV	
Input Offset Voltage Drift		8		µV/°C	
Input Offset Current		0.3		nA	
Input Bias Current		0.4		nA	
Gain		80		dB	5 kΩ load
Unity-Gain Frequency		5		MHz	R_L = 5 kΩ, C_L = 100 pF
CMRR		80		dB	
Settling Time		10		µs	R_L = 5 kΩ, C_L = 100 pF
Output Slew Rate		1.5		V/µs	R_L = 5 kΩ, C_L = 100 pF
PSRR		75		dB	
DAC AC CHARACTERISTICS					
Voltage Output Settling Time		10		µs	
Digital-to-Analog Glitch Energy		±20		nV-sec	1 LSB change at major carry (where maximum number of bits simultaneously change in the DACxDAT register)
COMPARATOR					
Input Offset Voltage		±10		mV	
Input Bias Current		1		µA	
Input Voltage Range	AGND		AV_{DD} – 1.2	V	
Input Capacitance		7		pF	
Hysteresis[4, 6]	2		15	mV	Hysteresis can be turned on or off via the CMPHYST bit in the CMPCON register
Response Time		3		µs	100 mV overdrive and configured with CMPRES = 11
TEMPERATURE SENSOR					Indicates die temperature
Voltage Output at 25°C		1.369		V	
Voltage TC		4.42		mV/°C	
Accuracy with No Calibration		±3		°C	
Accuracy with One Point Calibration Using Contents of TEMPREF Register		±1.5		°C	
θ_{JA} Thermal Impedance					
40-Lead LFCSP		26		°C/W	
32-Lead LFCSP		32.5		°C/W	
POWER SUPPLY MONITOR (PSM)					
IOV_{DD} Trip Point Selection		2.79		V	One trip point
Power Supply Trip Point Accuracy		±2		%	Of the selected nominal trip point voltage
POWER-ON RESET		2.41		V	
WATCHDOG TIMER (WDT)					
Timeout Period	0		512	sec	
FLASH/EE MEMORY					
Endurance[11]	10,000			Cycles	
Data Retention[12]	20			Years	T_J = 85°C
DIGITAL INPUTS					All digital inputs excluding XCLKI and XCLKO
Logic 1 Input Current		±0.2	±1	µA	$V_{IH} = V_{DD}$ or V_{IH} = 5 V
Logic 0 Input Current		–40	–60	µA	V_{IL} = 0 V; except TDI
		–80	–120	µA	V_{IL} = 0 V; TDI
Input Capacitance		10		pF	
LOGIC INPUTS[4]					All logic inputs excluding XCLKI
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
LOGIC OUTPUTS					All digital outputs excluding XCLKO
V_{OH}, Output High Voltage	2.4			V	I_{SOURCE} = 1.6 mA
V_{OL}, Output Low Voltage[13]			0.4	V	I_{SINK} = 1.6 mA
CRYSTAL INPUTS XCLKI AND XCLKO					
Logic Inputs, XCLKI Only					
V_{INL}, Input Low Voltage		1.1		V	
V_{INH}, Input High Voltage		1.7		V	
XCLKI Input Capacitance		20		pF	
XCLKO Output Capacitance		20		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL OSCILLATOR		32.768		kHz	
			±3	%	
MCU CLOCK RATE					
From 32 kHz Internal Oscillator		326		kHz	CD = 7
From 32 kHz External Crystal		41.78		MHz	CD = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		66		ms	
From Pause/Nap Mode		24		ns	CD = 0
		3.07		µs	CD = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[14, 15]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to DGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		200		µA	ADC in idle mode
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		8.5	10	mA	CD = 7
		11	15	mA	CD = 3
		28	35	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		14	20	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		230	650	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		1.4		mA	At 1 MSPS
		0.7		mA	At 62.5 kSPS
DAC		400		µA	Per DAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed			3	kV	
FICDM Passed			1.0	kV	

[1] All ADC channel specifications are guaranteed during normal microcontroller core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 28. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] DAC linearity is calculated using a reduced code range of 100 to 3995.
[10] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[11] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[12] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[13] Test carried out with a maximum of eight I/Os set to a low output level.
[14] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[15] IOV_{DD} power supply current decreases typically by 2 mA during a Flash/EE erase cycle.

TIMING SPECIFICATIONS

Table 2. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Slave		Master	Unit
		Min	Max	Typ	
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Slave		Unit
		Min	Max	
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

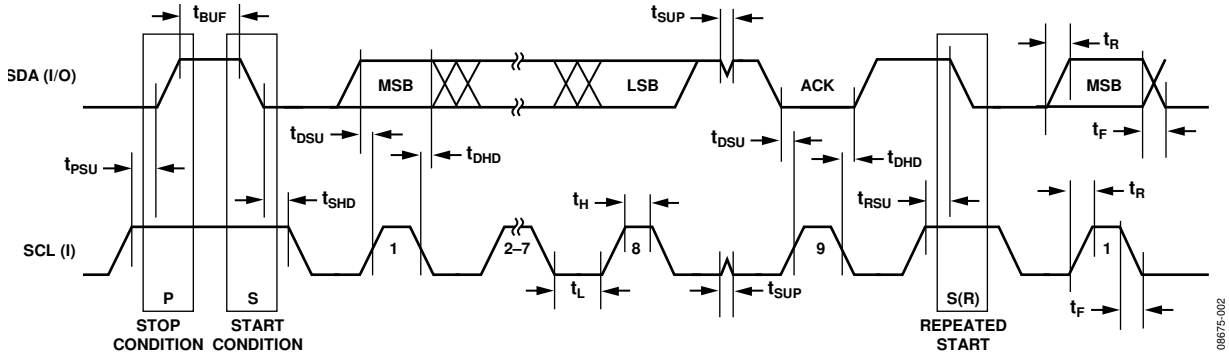

Figure 2. I²C-Compatible Interface Timing

Table 4. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

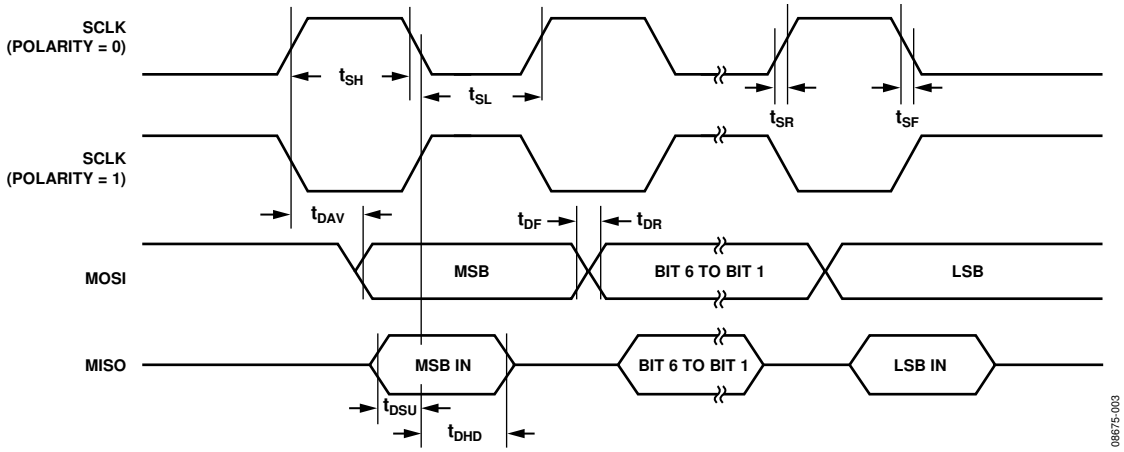

Figure 3. SPI Master Mode Timing (Phase Mode = 1)

Table 5. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

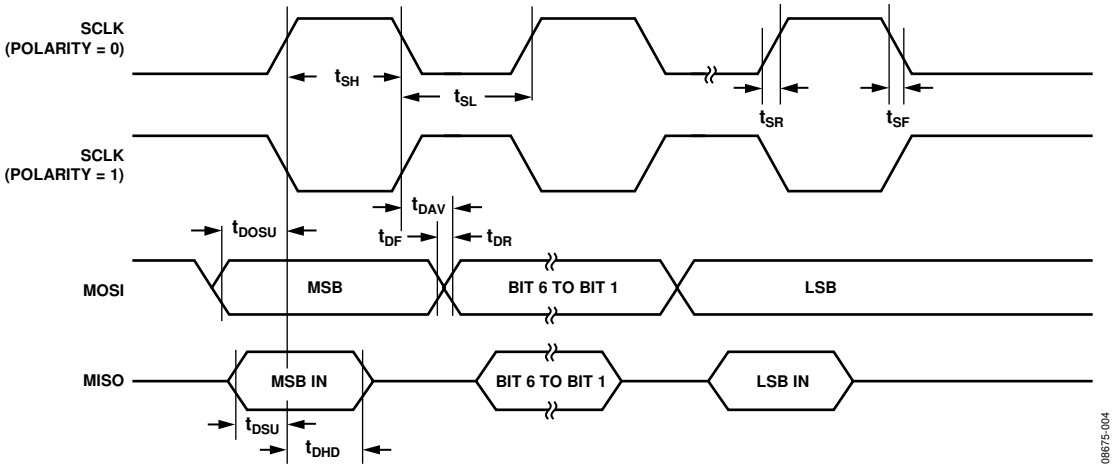

Figure 4. SPI Master Mode Timing (Phase Mode = 0)

Table 6. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

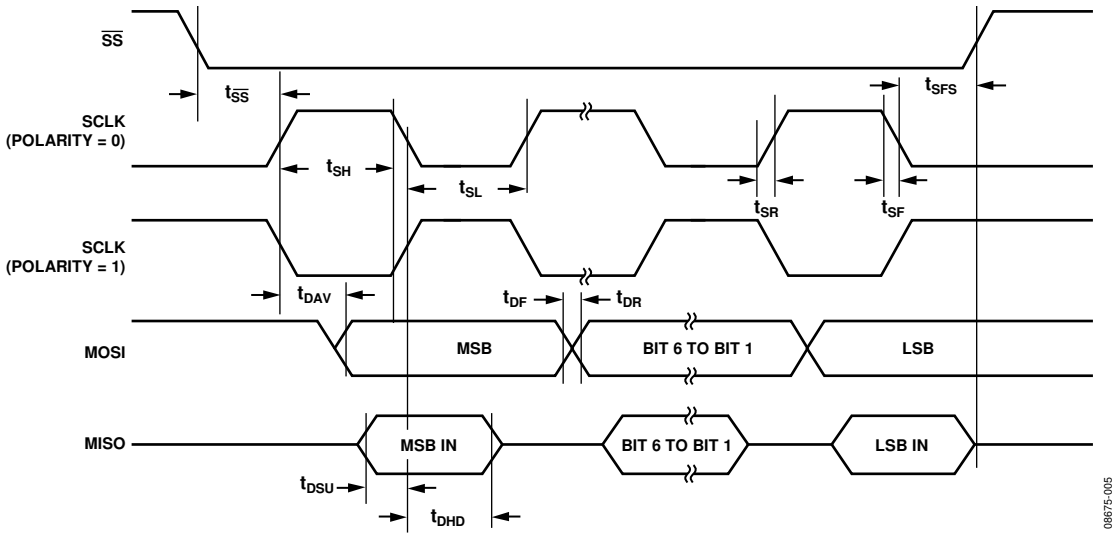

Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

Table 7. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{SS}$ edge			25	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

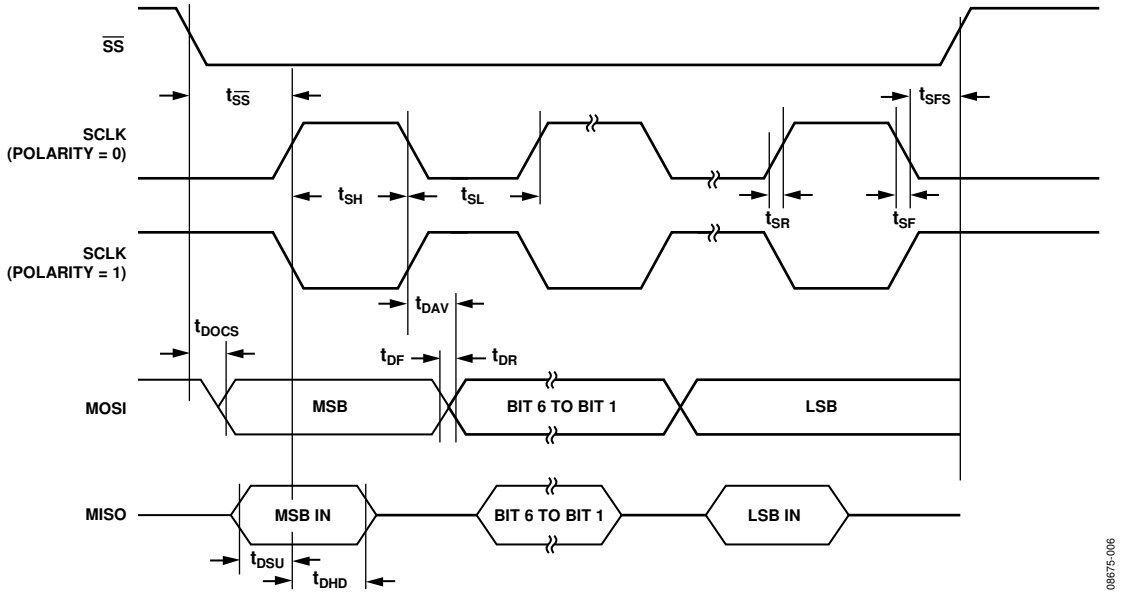

Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to DGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to DGND[1]	−0.3 V to +5.3 V
Digital Output Voltage to DGND[1]	−0.3 V to IOV_{DD} + 0.3 V
Shared Analog/Digital Inputs to AGND[2]	−0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
40-Lead LFCSP	26°C/W
32-Lead LFCSP	32.5°C/W
36-Lead WLCSP	50°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

[1] These limits apply to the P0.0, P0.1, P0.2, P0.3, P0.4, P0.5, P0.6, P0.7, P1.0, P1.1, P1.6, and P1.7 pins.
[2] These limits apply to the P1.2, P1.3, P1.4, P1.5, P2.0, P2.2, P2.3, and P2.4 pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

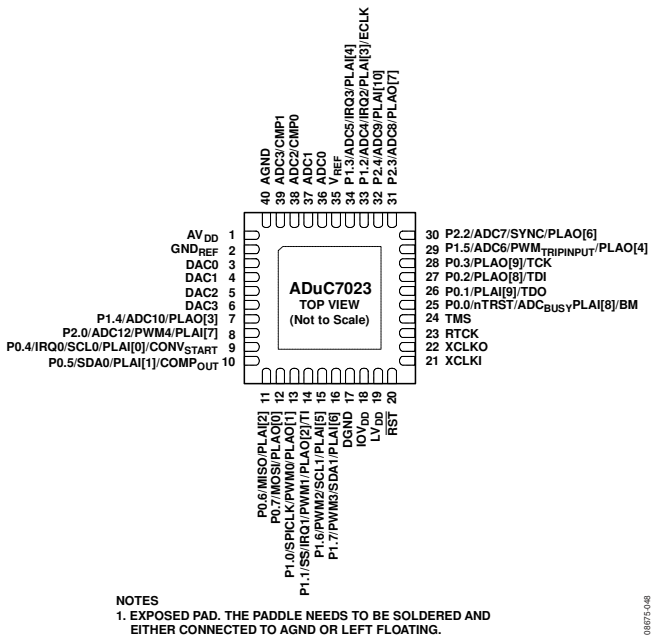

Figure 7. 40-Lead LFCSP Pin Configuration

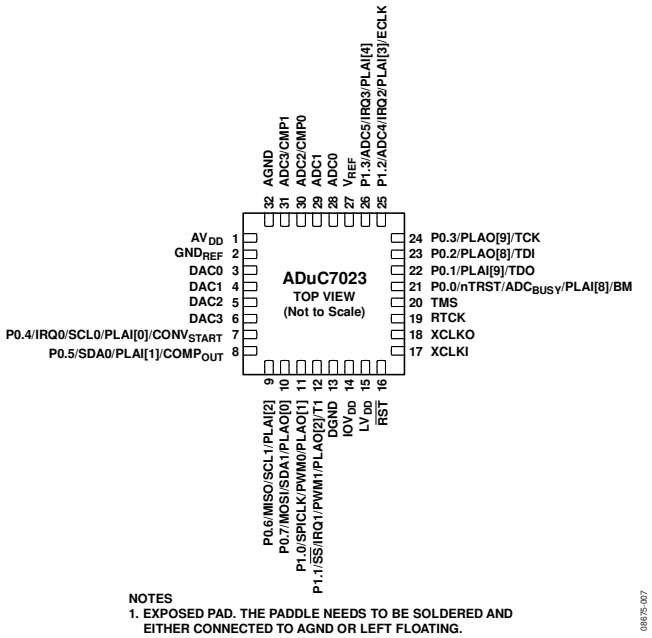

Figure 8. 32-Lead LFCSP Pin Configuration

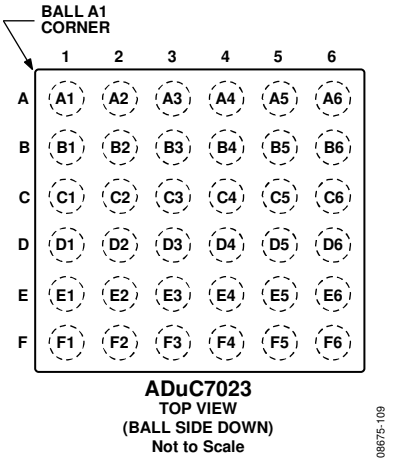

Figure 9. 36-Lead WLCSP Pin Configuration

Table 9. Pin Function Descriptions

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
0	0	N/A	Exposed Paddle	Exposed Pad. The paddle needs to be soldered and either connected to AGND or left floating.
36	28	A4	ADC0	Single-Ended or Differential Analog Input 0.
37	29	B4	ADC1	Single-Ended or Differential Analog Input 1.
38	30	A5	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
39	31	B5	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
32	N/A	B2	P2.4/ADC9/PLAI[10]	General-Purpose Input and Output Port 2.4/ADC Single-Ended or Differential Analog Input/Programmable Logic Array Input Element 10. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
31	N/A	A1	P2.3/ADC8/PLAO[7]	General-Purpose Input and Output Port 2.3/ADC Single-Ended or Differential Analog Input 8/Programmable Logic Array Output Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
30	N/A	B1	P2.2/ADC7/SYNC/PLAO[6]	General-Purpose Input and Output Port 2.2/ADC Single-Ended or Differential Analog Input 7/PWM Sync/Programmable Logic Array Output Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, pull-up resistor should be disabled manually.
8	N/A	E6	P2.0/ADC12/PWM4/PLAI[7]	General-Purpose Input and Output Port 2.0/ADC Single-Ended or Differential Analog Input 12/PWM Output 4/Programmable Logic Array Input Element 7. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as an ADC input, it is not possible to disable the internal pull-up resister. This means that this pin has a higher leakage current value than other analog input pins.
2	2	C4	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from DGND.
3	3	C5	DAC0	DAC0 Voltage Output or ADC Input.
4	4	C6	DAC1	DAC1 Voltage Output or ADC Input.
5	5	D5	DAC2	DAC2 Voltage Output
6	6	D6	DAC3	DAC3 Voltage Output
24	20	D2	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor is also required to ensure the part does not enter an erroneous state.
25	21	D1	P0.0/nTRST/ADC_{BUSY}/PLAI[8]/BM	This is a multifunction pin as follows: General-Purpose Input and Output Port 0.0. By default, this pin is configured as GPIO. JTAG Reset Input. Debug and download access. If this pin is held low, JTAG access is not possible because the JTAG interface is held in reset and P0.1/P0.2/P0.3 are configured as GPIO pins. ADC Busy Signal. Programmable Logic Array Input Element 8. Boot Mode Entry Pin. The ADuC7023 enters I^2C download mode if BM is low at reset with a flash address 0x80014 = 0xFFFFFFFF. The ADuC7023 executes code if BM is pulled high at reset or if BM is low at reset with a flash address 0x80014 not equal to 0xFFFFFFFF.
26	22	C1	P0.1/PLAI[9]/TDO	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data output pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.1. Programmable Logic Array Input Element 9. Test Data Out, JTAG Test Port Output. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
27	23	C2	P0.2/PLAO[8]/TDI	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data input pin and does not work as a GPIO. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.2. Programmable Logic Array Output Element 8. Test Data In, JTAG Test Port Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code, and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
28	24	C3	P0.3/PLAO[9]/TCK	The default value of this pin depends on the level of P0.0/BM. If P0.0/BM = 0, this pin defaults to a general purpose input. If P0.0/BM = 1, this pin defaults to a JTAG test data clock pin. This is a multifunction pin as follows: General-Purpose Input and Output Port 0.3. Programmable Logic Array Output Element 9. Test Clock, JTAG Test Port Clock Input. Debug and download access. When debugging the part via JTAG, this pin must not be toggled by user code and the GP0CON/GP0DAT register bits affecting this pin must not be changed as doing so disables JTAG access.
17	13	E3	DGND	Digital Ground.
18	14	F3	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
19	15	D3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
20	16	F2	$\overline{RST}$	Reset Input, Active Low.
23	19	E1	RTCK	Return JTAG Clock Signal. This is not the standard JTAG clock signal. It is an output signal from the JTAG controller. If using a 20-lead JTAG header, connect to Pin 11.
9	7	F6	P0.4/IRQ0/SCL0/PLAI[0]/CONV	General-Purpose Input and Output Port 0.4/External Interrupt Request 0/ I^2C0 Clock Signal/Programmable Logic Array Input Element 0/ADC External Convert Start. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
10	8	E5	P0.5/SDA0/PLAI[1]/$COMP_{OUT}$	General-Purpose Input and Output Port 0.5/I^2C0 Data Signal/ Programmable Logic Array Input Element 1/Voltage Comparator Output. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	9	F5	P0.6/MISO/SCL1/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/I^2C1 Clock On 32-Lead and 36-Ball Packages/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
	10	D4	P0.7/MOSI/SDA1/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/I^2C1 Data Signal On 32-Lead and 36-Ball Packages/Programmable Logic Array Output Element 0. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
11			P0.6/MISO/PLAI[2]	General-Purpose Input and Output Port 0.6/SPI MISO Signal/Programmable Logic Array Input Element 2. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
12			P0.7/MOSI/PLAO[0]	General-Purpose Input and Output Port 0.7/SPI MOSI Signal/Programmable Logic Array Output Element 0. By default this pin is configured as a digital input with a weak pull-up reisistor enabled.
21	17	F1	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. Connect to DGND if unused.
22	18	E2	XCLKO	Output from the Crystal Oscillator Inverter. Leave unconnected if unused.
16	N/A	N/A	P1.7/PWM3/SDA1/PLAI[6]	General-Purpose Input and Output Port 1.7/PWM Output 3/I^2C1 Data Signal/Programmable Logic Array Input Element 6. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
15	N/A	N/A	P1.6/PWM2/SCL1/PLAI[5]	General-Purpose Input and Output Port 1.6/PWM Output 2/I^2C1 Clock Signal/Programmable Logic Array Input Element 5. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
29	N/A	N/A	P1.5/ADC6/$PWM_{TRIPINPUT}$/PLAO[4]	General-Purpose Input and Output Port 1.5/ADC Single-Ended or Differential Analog Input 6/$PWM_{TRIPINPUT}$/Programmable Logic Array Output Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
7	N/A	N/A	P1.4/ADC10/PLAO[3]	General-Purpose Input and Output Port 1.4/ADC Single-Ended or Differential Analog Input 10/Programmable Logic Array Output Element 3. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.

Pin No.				
40-LFCSP	32-LFCSP	36-WLCSP	Mnemonic	Description
34	26	A3	P1.3/ADC5/IRQ3/PLAI[4]	General-Purpose Input and Output Port 1.3/ADC Single-Ended or Differential Analog Input 5/External Interrupt Request 3/ Programmable Logic Array Input Element 4. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
33	25	A2	P1.2/ADC4/IRQ2/PLAI[3]/ECLK/	General-Purpose Input and Output Port 1.2/ADC Single-Ended or Differential Analog Input 4/External Interrupt Request 2/ Programmable Logic Array Input Element 3/Input-Output for External Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled. When used as ADC input, the pull-up resistor should be disabled manually.
14	12	F4	P1.1/$\overline{SS}$/IRQ1/PWM1/PLAO[2]/T1	General-Purpose Input and Output Port 1.1/SPI Interface Slave Select (Active Low)/External Interrupt Request 1/PWM Output 1/ Programmable Logic Array Output Element 2/Timer 1 Input Clock. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
13	11	E4	P1.0/SCLK/PWM0/PLAO[1]	General-Purpose Input and Output Port 1.0/SPI Interface Clock Signal/ PWM Output 0/Programmable Logic Array Output Element 1. By default, this pin is configured as a digital input with a weak pull-up resistor enabled.
35	27	B3	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
40	32	A6	AGND	Analog Ground. Ground reference point for the analog circuitry.
1	1	B6	AV_{DD}	3.3 V Analog Power.

TYPICAL PERFORMANCE CHARACTERISTICS

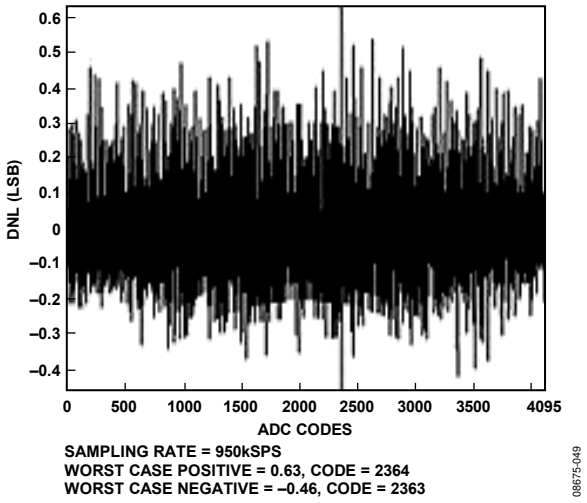

Figure 10. Typical DNL, f_{ADC} = 950 kSPS, Internal Reference Used

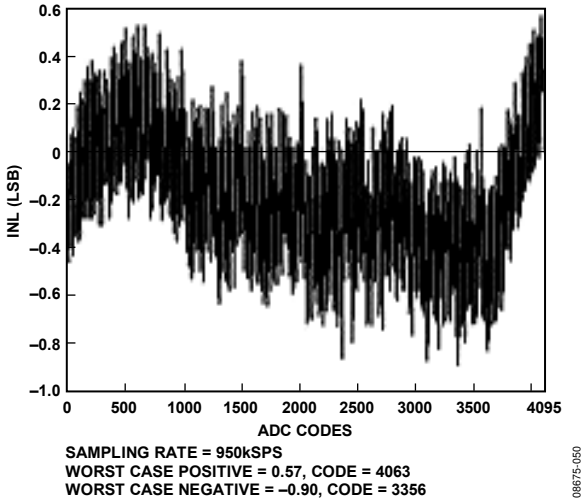

Figure 11. Typical INL, f_{ADC} = 950 kSPS, Internal Reference Used

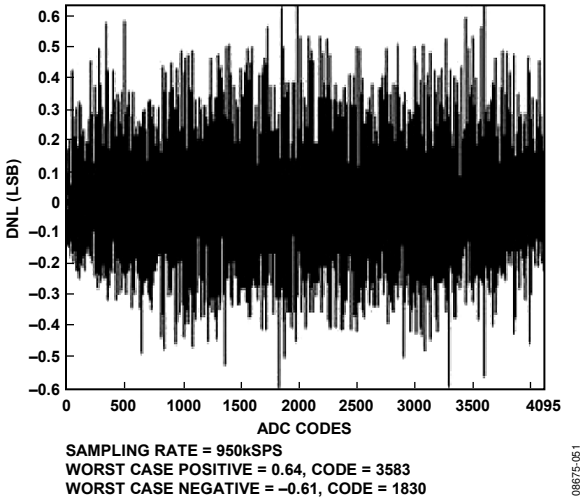

Figure 12. Typical DNL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

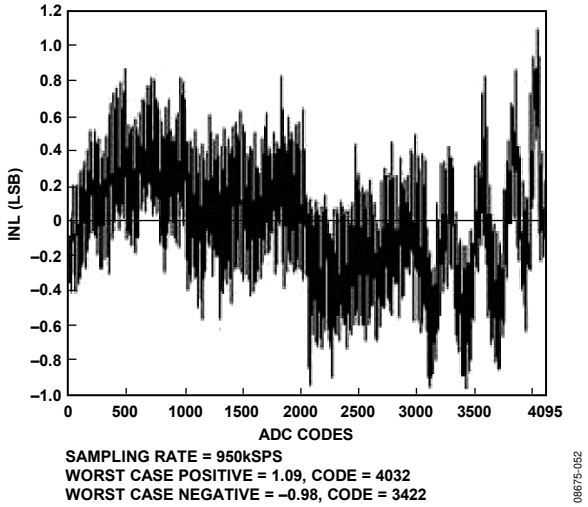

Figure 13. Typical INL, f_{ADC} = 950 kSPS, External 1.0 V Reference Used

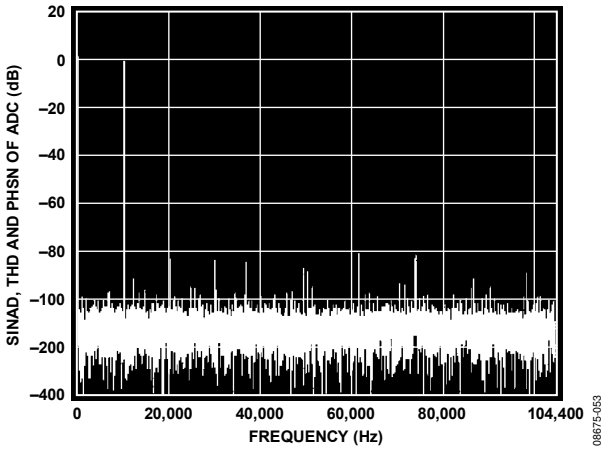

Figure 14. SINAD, THD, and PHSN of ADC , Internal 2.5 V Reference Used

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity (INL)
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes the output to settle to within a 1 LSB level for a full-scale input change.

OVERVIEW OF THE ARM7TDMI CORE

The ARM7® core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features: T support for the thumb (16-bit) instruction set, D support for debug, M support for long multiplications, and I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that has been compressed into 16 bits, called the Thumb® instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the Thumb mode has two limitations. Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time critical code. Also, the Thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM Thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are:

- Normal interrupt or IRQ. This is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ. This is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI). This can be used to make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are only used for system-level programming and exception handling.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14) as represented in Figure 15. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means the interrupt processing can begin without the need to save or restore these registers, and thus save critical time in the interrupt handling process.

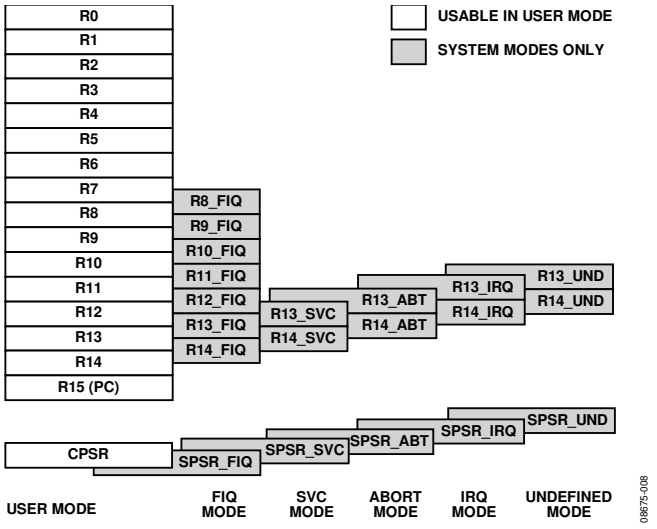

Figure 15. Register Organization

More information relative to the model of the programmer and the ARM7TDMI core architecture can be found in ARM7TDMI technical and ARM architecture manuals available directly from ARM Ltd.

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following: the longest time the request can take to pass through the synchronizer, the time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC, and the time for the data abort and FIQ entry.

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer, plus the time to enter the exception mode.

The ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

MEMORY ORGANIZATION

The ADuC7023 incorporates two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory; 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory configured boot page. These two blocks are mapped as shown in Figure 16.

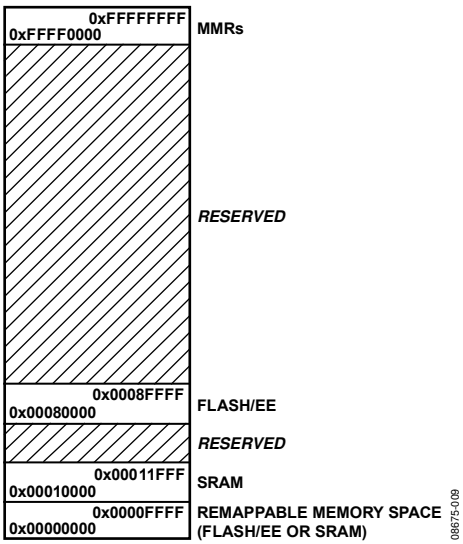

Figure 16. Physical Memory Map

By default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the Remap MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of the 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 16.

The ADuC7023 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.

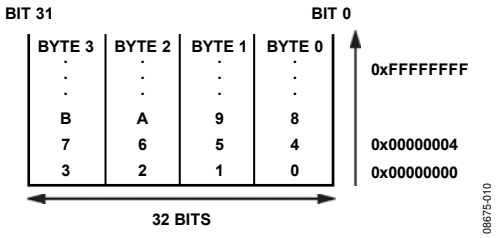

Figure 17. Little Endian Format

FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as 32k × 16 bits; 31k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

62 kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is, therefore, recommended to use Thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined later in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as 2k × 32 bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined later in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 18 are unoccupied or reserved locations and should not be accessed by user software. Table 10 to Table 23 show the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: advanced high performance bus (AHB) used for system modules and advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7023 are on the APB except the Flash/EE memory and the GPIOs.

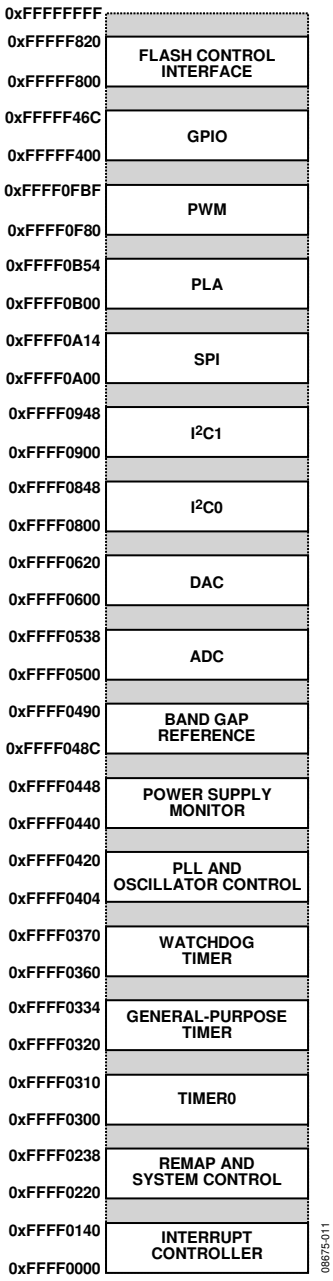

Figure 18. Memory Mapped Registers