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MicroConverter®, Small Package 12-Bit ADC with Embedded Flash MCU

ADuC814

FEATURES

ANALOG I/O
- 6-channel 247 kSPS ADC
  - 12-bit resolution
  - ADC high speed data capture mode
  - Programmable reference via on-chip DAC for low level inputs, ADC performance specified to V_{REF} = 1 V
- Dual voltage output DACs
  - 12-bit resolution, 15 µs settling time

Memory
- 8 kbytes on-chip Flash/EE program memory
- 640 bytes on-chip Flash/EE data memory
- Flash/EE, 100 year retention, 100 kcycle endurance
- 3 levels of Flash/EE program memory security
- In-circuit serial downlaod (no external hardware)
- 256 bytes on-chip data RAM

8051 based core
- 8051 compatible instruction set
- 32 kHz external crystal, on-chip programmable PLL (16.78 MHz max)
- Three 16-bit timer/counters
- 11 programmable I/O lines
- 11 interrupt sources, 2 priority levels

Power
- Specified for 3 V and 5 V operation
- Normal: 3 mA @ 3 V (core CLK = 2.1 MHz)
- Power-down: 15 µA (32 kHz oscillator running)

On-chip peripherals
- Power-on reset circuit (no need for external POR device)
- Temperature monitor (±1.5°C accuracy)
- Precision voltage reference
- Time interval counter (wake-up/RTC timer)
- UART serial I/O
- SPI®/I²C® compatible serial I/O
- Watchdog timer (WDT), power supply monitor (PSM)

Package and temperature range
- 28-lead TSSOP 4.4 mm × 9.7 mm package
- Fully specified for −40°C to +125°C operation

APPLICATIONS

Optical networking—laser power control
Base station systems—power amplifier bias control
Precision instruments, smart sensors
Battery-powered systems, precision system monitors

FUNCTIONAL BLOCK DIAGRAM

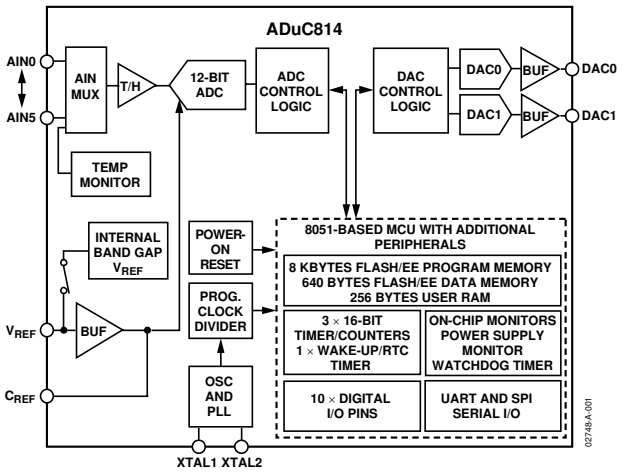

Figure 1.

GENERAL DESCRIPTION

The ADuC814 is a fully integrated 247 kSPS, 12-bit data acquisition system incorporating a high performance multichannel ADC, an 8-bit MCU, and program/data Flash/EE memory on a single chip.

This low power device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 16.78 MHz. This clock is, in turn, routed through a programmable clock divider from which the MCU core clock operating frequency is generated.

The microcontroller core is an 8052 and is compatible with an 8051 instruction. 8 kBytes of nonvolatile Flash/EE program memory are provided on-chip. 640 bytes of nonvolatile Flash/EE data memory and 256 bytes RAM are also integrated on-chip.

The ADuC814 also incorporates additional analog functionality with dual 12-bit DACs, a power supply monitor, and a band gap reference. On-chip digital peripherals include a watchdog timer, time interval counter, three timer/counters, and two serial I/O ports (SPI and UART).

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the DLOAD pin. The ADuC814 is supported by a QuickStart™ Development System.

The part operates from a single 3 V or 5 V supply over the extended temperature range −40°C to +125°C. When operating from 3 V supplies, the power dissipation for the part is below 10 mW. The ADuC814 is housed in a 28-lead TSSOP package.

Rev. A

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ADUC814* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADuC814 QuickStart Development System

DOCUMENTATION

Application Notes

- AN-1074: Understanding the Serial Download Protocol (Formerly uC004)
- AN-282: Fundamentals of Sampled Data Systems
- AN-660: XY-Matrix Keypad Interface to MicroConverter®
- AN-661: ADuC814 to ADM1032 via I²C® Interface
- AN-709: RTD Interfacing and Linearization Using an ADuC8xx MicroConverter®
- AN-759: Expanding the Number of DAC Outputs on the ADuC8xx and ADuC702x Families (uC012)
- UC-001: MicroConverter® I2C® Compatible Interface
- UC-006: A 4-wire UART-to-PC Interface
- UC-009: Addressing 16MB of External Data Memory
- UC-018: Uses of the Time Interval Counter

Data Sheet

- ADuC814: MicroConverter® , Small Package, 12-Bit ADC with Embedded Flash MCU Data Sheet
- ADuC814: Errata Sheet

User Guides

- ADuC814 Quick Reference Guide
- UG-041: ADuC8xx Evaluation Kit Getting Started User Guide

REFERENCE MATERIALS

Technical Articles

- Integrated Route Taken to Pulse Oximetry

DESIGN RESOURCES

- ADUC814 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADUC814 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

12/03 – Data Sheet Changed from REV. 0 to REV. A

Added detailed description of product .... Universal

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SPECIFICATIONS

Table 1. AV_{DD} = DV_{DD} = 2.7 V to 3.3 V or 4.5 V to 5.5 V, V_{REF} = 2.5 V internal reference, XTAL1/XTAL2 = 32.768 kHz crystal. All specifications T_{MIN} to T_{MAX}, unless otherwise specified[1]

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
ADC CHANNEL SPECIFICATIONS				
A GRADE				
DC ACCURACY[2,3]				f_{SAMPLE} = 147 kHz
Resolution	12	12	Bits	
Integral Nonlinearity	2	2	LSB max	2.5 V internal reference
	1	1	LSB typ	
	2.5	2.5	LSB typ	1.0 V external reference
Differential Nonlinearity	4	4	LSB max	2.5 V internal reference
	2	2	LSB typ	
	5	5	LSB typ	1.0 V external reference
CALIBRATED ENDPOINT ERRORS[4, 5]				
Offset Error	5	5	LSB max	
Offset Error Match	1	1	LSB typ	
Gain Error	5	5	LSB max	
Gain Error Match	1	1	LSB typ	
DYNAMIC PERFORMANCE[6]				f_{IN} = 10 kHz sine wave
				f_{SAMPLE} = 147 kHz
Signal to Noise Ratio (SNR)[7]	62.5	62.5	dB typ	
Total Harmonic Distortion (THD)	–65	–65	dB typ	
Peak Harmonic or Spurious Noise	–65	–65	dB typ	
Channel-to-Channel Crosstalk[8]	–80	–80	dB typ	
B GRADE				
DC ACCURACY[2, 3]				f_{SAMPLE} = 147 kHz
Resolution	12	12	Bits	
Integral Nonlinearity	1	1	LSB max	2.5 V internal reference
	0.3	0.3	LSB typ	
	1.5	1.5	LSB max	1.0 V external reference[11]
Differential Nonlinearity	0.9	0.9	LSB max	2.5 V internal reference
	0.25	0.25	LSB typ	
	+1.5/–0.9	1.5/–0.9	LSB max	1.0 V external reference[11]
Code Distribution	1	1	LSB typ	ADC input is a dc voltage
CALIBRATED ENDPOINT ERRORS[4, 5]				
Offset Error	2	3	LSB max	
Offset Error Match	1	1	LSB typ	
Gain Error	2	3	LSB max	
Gain Error Match	1	1	LSB typ	
DYNAMIC PERFORMANCE[6]				f_{IN} = 10 kHz sine wave
				f_{SAMPLE} = 147 kHz
Signal to Noise Ratio (SNR)[7]	71	71	dB typ	
Total Harmonic Distortion (THD)	–85	–85	dB typ	
Peak Harmonic or Spurious Noise	–85	–85	dB typ	
Channel-to-Channel Crosstalk[8]	–80	–80	dB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	
Leakage Current	1	1	µA max	
Input Capacitance	32	32	pF typ	

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
TEMPERATURE MONITOR[9]				
Voltage Output at 25°C	650	650	mV typ	
Voltage TC	–2	–2	mV/°C typ	
Accuracy	3	3	°C typ	2.5 V internal reference
Accuracy	1.5	1.5	°C typ	2.5 V external reference
DAC CHANNEL SPECIFICATIONS				DAC Load to AGND RL = 10 kΩ, CL = 100 pF
DC ACCURACY[10]				
Resolution	12	12	Bits	
Relative Accuracy	+3	+3	LSB typ	
Differential Nonlinearity[11]	–1	–1	LSB max	Guaranteed montonic
	1/2	1/2	LSB typ	
Offset Error	50	50	mV max	V_{REF} range
Gain Error	1	1	% max	V_{REF} range
	1	1	% typ	AV_{DD} range
Gain Error Mismatch	0.5	0.5	% typ	Of full scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}		Volts	DAC V_{REF} = 2.5 V
Voltage Range_1	0 to V_{DD}		Volts	DAC V_{REF} = V_{DD}
Output Impedance	0.5	0.5	Ω typ	
I_{SINK}	50	50	µA typ	
DAC AC Specifications				
Voltage Output Settling Time	15	15	µs typ	Full-scale settling time to within ½ LSB of final value
Digital-to-Analog Glitch Energy	10	10	nVs typ	1 LSB change at major carry
REFERENCE INPUT/OUTPUT				
REFERENCE OUTPUT				
Output Voltage (V_{REF})	2.5	2.5	V	
Accuracy	2.5	2.5	% max	Of V_{REF} measured at the C_{REF} pin
Power Supply Rejection	47	57	dB typ	
Reference Tempco	100	100	ppm/°C typ	
Internal V_{REF} Power-On Time[12]	80	80	ms typ	
EXTERNAL REFERENCE INPUT[13]				Internal band gap reference deselected via ADCCON2.6
Voltage Range (V_{REF})[14]	1.0	1.0	V min	
	V_{DD}	V_{DD}	V max	
Input Impedance	20	20	kΩ typ	
Input Leakage	10	10	µA max	
POWER SUPPLY MONITOR (PSM)				
V_{DD} Trip Point Selection Range	2.63	2.63	V	
	2.93	2.93	V	Four trip points selectable in this range
	3.08	3.08	V	programmed via TP1–0 in PSMCON
	4.63		V	
V_{DD} Power Supply Trip Point Accuracy	3.5	3.5	% max	
WATCH DOG TIMER (WDT)[14]				
Timeout Period	0	0	ms min	Nine time-out periods selectable in this range
	2000	2000	ms max	programmed via PRE3–0 in WDCON
LOGIC INPUTS				
INPUT VOLTAGES[14] All Inputs except SCLOCK, RESET, and XTAL1				
V_{INL}, Input Low Voltage	0.8	0.4	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
SCLOCK and RESET Only[14] (Schmitt-Triggered Inputs)				
V_{T+}	1.3	0.95	V min	
	3.0	2.5	V max	
V_{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
$V_{T+} - V_{T-}$	0.3	0.3	V min	
	0.85	0.85	V max	
INPUT CURRENTS				
P1.2–P1.7, DLOAD	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
SCLOCK[15]	–10	–3	µA min	V_{IN} = 0 V, internal pull-up
	–40	–15	µA max	V_{IN} = 0 V, internal pull-up
	±10	±10	µA max	V_{IN} = V_{DD}
RESET	±10	±10	µA max	V_{IN} = 0 V
	20	10	µA min	V_{IN} = 5 V, 3 V internal pull-down
	105	35	µA max	V_{IN} = 5 V, 3 V internal pull-down
P1.0, P1.1, Port 3[15]	±10	±10	µA max	V_{IN} = 5 V, 3 V
(includes MISO, MOSI/SDATA and $\overline{SS}$)	1	1	µA typ	
	–180	–70	µA min	V_{IN} = 2 V, V_{DD} = 5 V, 3 V
	–660	–200	µA max	
	–360	–100	µA typ	
	–20	–5	µA min	V_{IN} = 450 mV, V_{DD} = 5 V, 3 V
	–75	–25	µA max	
	–38	–12	µA typ	
INPUT CAPACITANCE	5	5	pF typ	All digital inputs
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)				
Logic Inputs, XTAL1 Only				
V_{INL}, Input Low Voltage	0.8	0.4	V typ	
V_{INH}, Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4	2.4	V min	I_{SOURCE} = 80 mA
Output Low Voltage (V_{OL})				
Port 1.0 and Port 1.1	0.4	0.4	V max	I_{SINK} = 10 mA, T_{MAX} = 85°C
Port 1.0 and Port 1.1	0.4	0.4	V max	I_{SINK} = 10 mA, T_{MAX} = 125°C
SCLOCK, MISO/MOSI	0.4	0.4	V max	I_{SINK} = 4 mA
All Other Outputs	0.4	0.4	V max	I_{SINK} = 1.6 mA
MCU CORE CLOCK				
MCU Clock Rate	131.1	131.1	kHz min	Clock rate generated via on-chip PLL, programmable via CD2-0 in PLLCON
	16.78	16.78	MHz max	
START UP TIME				
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Oscillator Running				OSC_PD = 0 in PLLCON SFR
Wake-Up with $\overline{INT0}$ Interrupt	100	100	µs typ	
Wake-Up with SPI/I^2C Interrupt	100	100	µs typ	
Wake-Up with TIC Interrupt	100	100	µs typ	
Wake-Up with External RESET	3	3	ms typ	

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
Oscillator Powered Down[16]				OSC_PD = 1 in PLLCON SFR
Wake-Up with $\overline{INT0}$ Interrupt	150	400	ms typ	
Wake-Up with SPI/I^2C Interrupt	150	400	ms typ	
Wake-Up with External RESET	150	400	ms typ	
After External RESET in Normal Mode	3	3	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[17]				
Endurance[18]	100,000	100,000	Cycles min	
Data Retention[19]	100	100	Years min	
POWER REQUIREMENTS[20, 21]				
Power Supply Voltages				
AV_{DD}/DV_{DD} – AGND		2.7	V min	AV_{DD}/DV_{DD} = 3 V nom
		3.3	V max	
	4.5		V min	AV_{DD}/DV_{DD} = 5 V nom
	5.5		V max	
Power Supply Currents, Normal Mode				
D_{VDD} Current[14]	5	2.5	mA max	Core CLK = 2.097 MHz
	4	2	mA typ	(CD bits in PLLCON = 3)
A_{VDD} Current[14]	1.7	1.7	mA max	
D_{VDD} Current	20	10	mA max	Core CLK = 16.78MHz (max)
	16	8	mA typ	(CD bits in PLLCON = 0)
A_{VDD} Current	1.7	1.7	mA max	
D_{VDD} Current[14]	3.5	1.5	mA max	Core CLK = 131.2 kHz (min)
	2.8	1.2	mA typ	(CD bits in PLLCON = 7)
A_{VDD} Current	1.7	1.7	mA max	
Power Supply Currents, Idle Mode				
D_{VDD} Current[14]	1.7	1.2	mA max	Core CLK = 2.097 MHz
	1.5	1	mA typ	(CD Bits in PLLCON = 3)
AV_{DD} Current[14]	0.15	0.15	mA max	
DV_{DD} Current[14]	6	3	mA max	Core CLK = 16.78 MHz (max)
	4	2.5	mA typ	(CD bits in PLLCON = 0)
AV_{DD} Current[14]	0.15	0.15	mA max	
DV_{DD} Current[14]	1.25	1	mA max	Core CLK = 131 kHz (min)
	1.1	0.7	mA typ	(CD bits in PLLCON = 7)
AV_{DD} Current[14]	0.15	0.15	mA max	
Power Supply Currents, Power-Down Mode				Core CLK = 2.097 MHz or 16.78 MHz (CD bits in PLLCON = 3 or 0)
DV_{DD} Current[14]		20	µA max	Oscillator on
	40	14	µA typ	
AV_{DD} Current	1	1	µA typ	
DV_{DD} Current		15	µA max	Oscillator off
	20	10	µA typ	
AV_{DD} Current	1	1	µA typ	
Typical Additional Power Supply Currents				Core CLK = 2.097 MHz, (CD bits in PLLCON = 3) $AV_{DD} = DV_{DD}$ = 5 V
PSM Peripheral	50		µA typ	
ADC	1.5		mA typ	
DAC	150		µA typ	

[1]Temperature range –40ºC to +125ºC.
[2]ADC linearity is guaranteed when operating in nonpipelined mode, i.e., ADC conversion followed sequentially by a read of the ADC result. ADC linearity is also guaranteed during normal MicroConverter core operation.
[3]ADC LSB size = V_{REF} /2^{12}, i.e., for internal V_{REF} = 2.5 V, 1 LSB = 610 µV, and for external V_{REF} = 1 V, 1 LSB = 244 µV.
[4]Offset and gain error and offset and gain error match are measured after factory calibration.
[5]Based on external ADC system components the user may need to execute a system calibration to remove additional external channel errors and achieve these specifications.
[6]Measured with coherent sampling system using external 16.77 MHz clock via P3.5 (Pin 22).
[7]SNR calculation includes distortion and noise components.
[8]Channel-to-channel crosstalk is measured on adjacent channels.
[9]The temperature monitor gives a measure of the die temperature directly; air temperature can be inferred from this result.
[10]DAC linearity is calculated using a reduced code range of 48 to 4095, 0 V to V_{REF} range; a reduced code range of 48 to 3950, 0 V to V_{DD} range. DAC output load = 10 kΩ and 100 pF.
[11]DAC differential nonlinearity specified on 0 V to V_{REF} and 0 to V_{DD} ranges.
[12]Measured with V_{REF} and C_{REF} pins decoupled with 0.1 µF capacitors to ground. Power-up time for the internal reference is determined by the value of the decoupling capacitor chosen for both the V_{REF} and C_{REF} pins.
[13]When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit. In this mode, the V_{REF} and C_{REF} pins need to be shorted together for correct operation.
[14]These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[15]Pins configured in I^2C compatible mode or SPI mode; pins configured as digital inputs during this test.
[16]These typical specifications assume no loading on the XTAL2 pin. Any additional loading on the XTAL2 pin increases the power-on times.
[17]Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.
[18]Endurance is qualified to 100 kcycles as per JEDEC Std. 22, Method A117 and measured at –40ºC, +25°C, and +125°C; typical endurance at +25°C is 700 kcycles.
[19]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature as shown in Figure 33 in the Flash/EE memory description section.
[20]Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:
Normal Mode: Reset and all digital I/O pins = open circuit, core Clk changed via CD bits in PLLCON, core executing internal software loop.
Idle Mode: Reset and all digital I/O pins = open circuit, core Clk changed via CD bits in PLLCON, PCON.0 = 1, core execution suspended in idle mode.
Power-Down Mode: Reset and all P1.2–P1.7 pins = 0.4 V; all other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[21]DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

ABSOLUTE MAXIMUM RATINGS

Table 2. Temperature = 25°C, unless otherwise noted

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
AGND to DGND[1]	–0.3 V to +0.3 V
Analog Input Voltage to AGND[2]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Analog Input Current (Indefinite)	30 mA
Reference Input Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	97.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC814.
[2] Applies to Pins P1.2 to P1.7 operating in analog or digital input mode.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

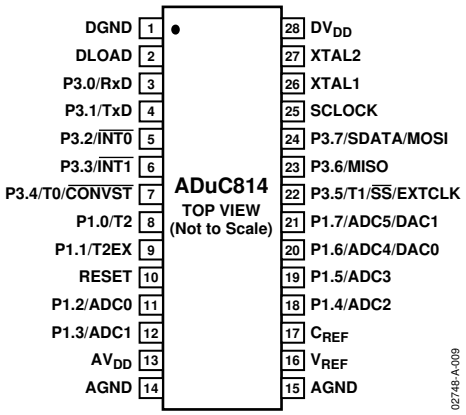

Figure 2. Pin Configuration

Table 3. Pin Descriptions

Pin No.	Mnemonic	Type	Function
1	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
2	DLOAD	I	Debug/Serial Download Mode. Enables when pulled high through a resistor on power-on or RESET. In this mode, DLOAD may also be used as an external emulation I/O pin, therefore the voltage level at this pin must not be changed during this mode of operation because it may cause an emulation interrupt that halts code execution. User code is executed when this pin is pulled low on power-on or RESET.
3–7	P3.0 – P3.4	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described next.
3	P3.0/RxD	I/O	Receiver Data Input (asynchronous) or Data Input/Output (synchronous) in Serial (UART) Mode.
4	P3.1/TxD	I/O	Transmitter Data Output (asynchronous) or Clock Output (synchronous) in Serial (UART) Mode.
5	P3.2/$\overline{\text{INT0}}$	I/O	Interrupt 0, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 0.
6	P3.3/$\overline{\text{INT1}}$	I/O	Interrupt 1, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 1.
7	P3.4/T0/ $\overline{\text{CONVST}}$	I/O	Timer/Counter 0 Input and External Trigger Input for ADC Conversion Start.
8–9	P1.0–P1.1	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 1 pins being pulled low externally, they source current because of the internal pull-up resistors When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 1 pins also have various secondary functions which are described as follows.
8	P1.0/T2	I/O	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
9	P1.1/T2EX	I/O	Digital Input. Capture/Reload trigger for Counter 2.
10	RESET	I	Reset Input. A high level on this pin while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt-trigger input stage on this pin.
11–12	P1.2–P1.3	I	Port 1.2 to P1.3. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
11	P1.2/ADC0	I	ADC Input Channel 0. Selected via ADCCON2 SFR.
12	P1.3/ADC1	I	ADC Input Channel 1. Selected via ADCCON2 SFR.
13	AV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.
14–15	AGND	G	Analog Ground. Ground reference point for the analog circuitry.
16	V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a switch and is the reference source for the analog to digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be used to connect an external reference to the analog to digital converter by setting ADCCON1.6 to 1. Connect 0.1 µF between this pin and AGND.

Pin No.	Mnemonic	Type	Function
17	C_{REF}	I	Decoupling Input for On-Chip Reference. Connect 0.1 μF between this pin and AGND.
18–21	P1.4–P1.7	I	Port 1.4 to P1.7. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
18	P1.4/ADC2	I	ADC Input Channel 2. Selected via ADCCON2 SFR.
19	P1.5/ADC3	I	ADC Input Channel 2. Selected via ADCCON2 SFR.
20	P1.6/ADC4/ DAC0	I/O	ADC Input Channel 4. Selected via ADCCON2 SFR. The voltage DAC Channel 0 can also be configured to appear on P1.6.
21	P1.7/ ADC5/DAC1	I/O	ADC Input Channel 5, selected via ADCCON2 SFR. The voltage DAC Channel 1 can also be configured to appear on P1.7.
22–24	P3.5–P3.7	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described as follows.
22	P3.5/T1		I/O Timer/Counter 1 Input. P3.5–P3.7 pins also have SPI interface functions. To enable these functions, Bit 0 of the CFG814 SFR must be set to 1.
22	P3.5/$\overline{SS}$ /EXTCLK	I/O	This pin also functions as the Slave Select input for the SPI interface when the device is operated in slave mode. P3.5 can also function as an input for an external clock. This clock effectively bypasses the PLL. This function is enabled by setting Bit 1 of the CFG814 SFR.
23	P3.6/MISO	I/O	SPI Master Input/Slave Output Data Input/Output Pin.
24	P3.7/SDATA/ MOSI	I/O	SPI Master Output/Slave Input Data Input/Output Pin.
25	SCLOCK	I/O	Serial Clock Pin for SPI Serial Interface Clock.
26	XTAL1	I	Input to the Crystal Oscillator Inverter.
27	XTAL2	O	Output from the Crystal Oscillator Inverter.
28	DV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.

I = Input, O = Output, S = Supply, G - Ground.

The following notes apply to the entire data sheet:

- In bit designation tables, *set* implies a Logic 1 state, and *cleared* implies a Logic 0 state, unless otherwise stated.
- *Set* and *cleared* also imply that the bit is set or cleared by the ADuC814 hardware, unless otherwise stated.
- User software should not write to reserved or unimplemented bits as they may be used in future products.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 … 000) to (0000 … 001) from the ideal, i.e., +1/2 LSB.

Full-Scale Error

This is the deviation of the last code transition from the ideal AIN voltage (full-scale error has been adjusted out).

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to =- (Noise + Distortion)} = (6.02N + 1.76)$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the harmonics to the fundamental.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and including dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is the noise peak.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-sec.

TYPICAL PERFORMANCE CURVES

The typical performance plots presented in this section illustrate typical performance of the ADuC814 under various operating conditions. Note that all typical plots in this section were generated using the ADuC814BRU, i.e., the B-grade part.

Figure 3 and Figure 4 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.3 LSBs.

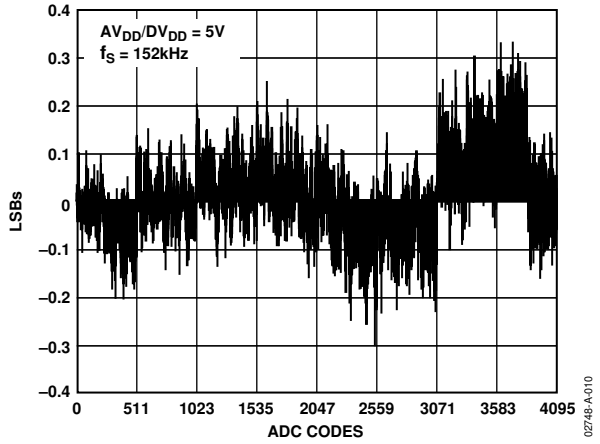

Figure 3. Typical INL Error, V_{DD} = 5 V

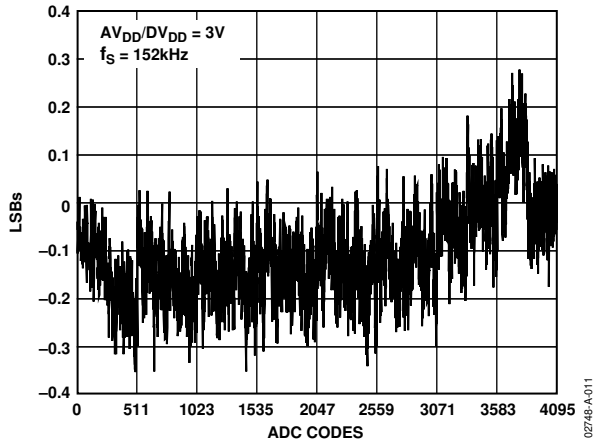

Figure 4. Typical INL Error, V_{DD} = 3 V

Figure 5 and Figure 6 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

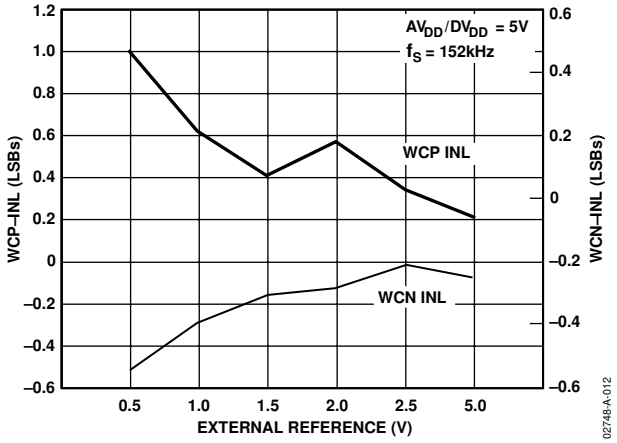

Figure 5. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 5 V

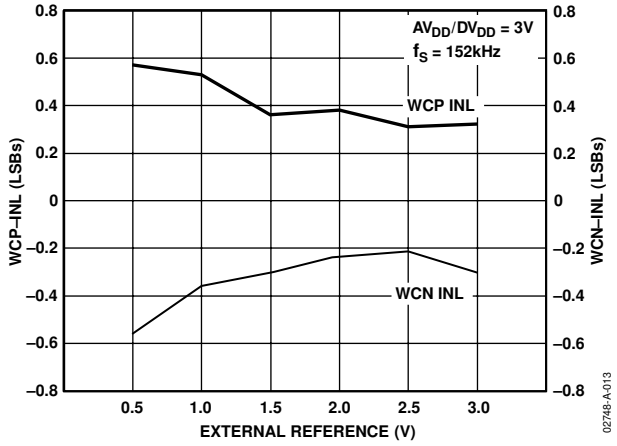

Figure 6. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 3 V

Figure 7 and Figure 8 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.2 LSBs.

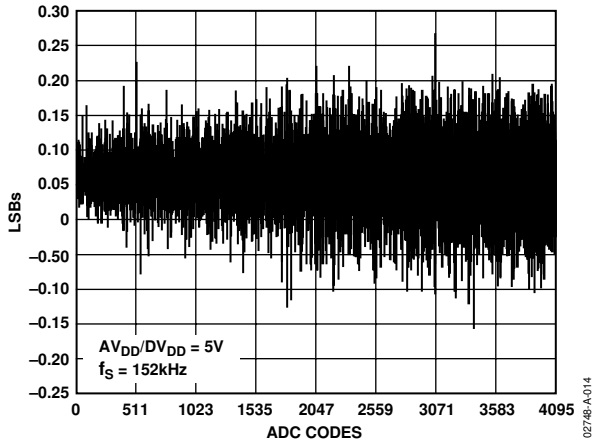

Figure 7. Typical DNL Error, V_{DD} = 5 V

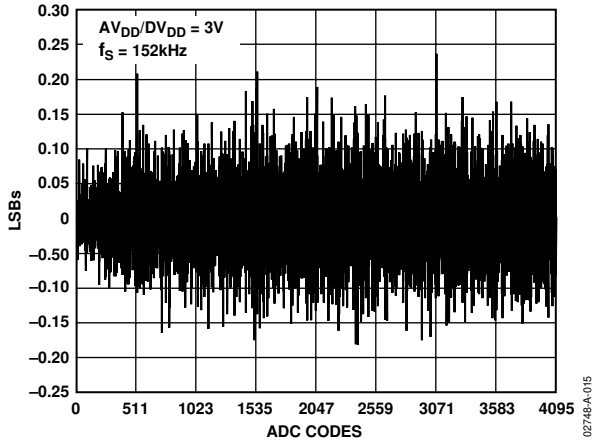

Figure 8. Typical DNL Error, V_{DD} = 3 V

Figure 9 and Figure 10 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

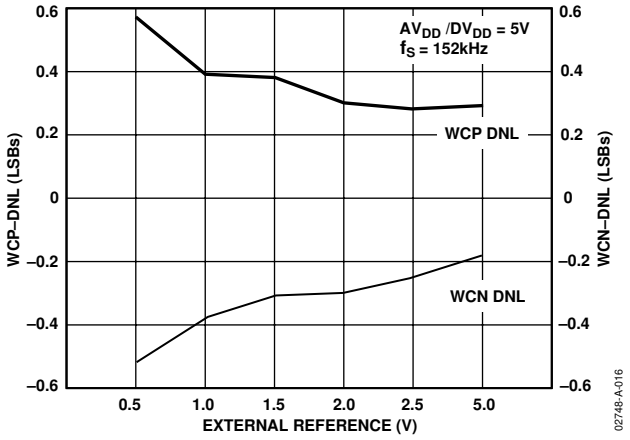

Figure 9. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 5 V

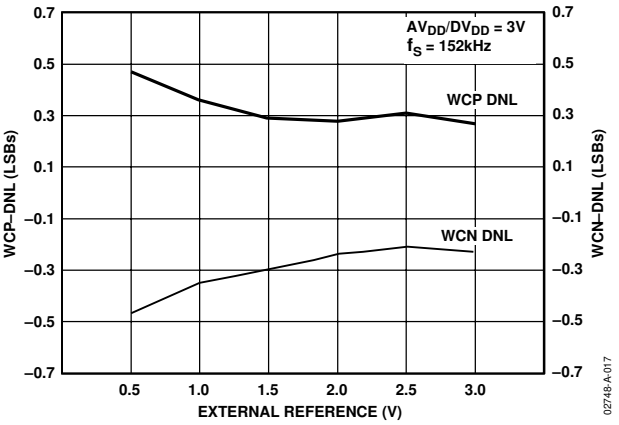

Figure 10. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 3 V

Figure 11 shows a histogram plot of 10,000 ADC conversion results on a dc input with V_{DD} = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

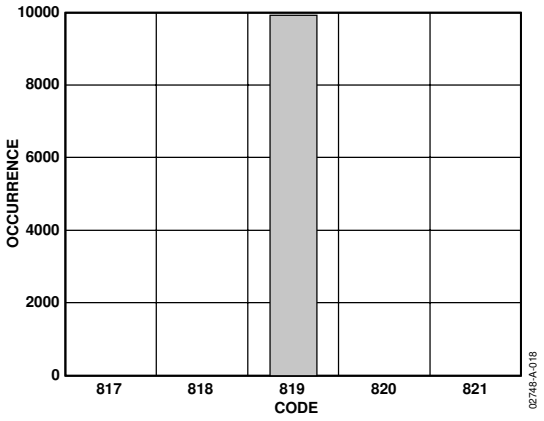

Figure 11. Code Histogram plot, V_{DD} = 5 V

Figure 12 shows a histogram plot of 10,000 ADC conversion results on a dc input for V_{DD} = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output bin.

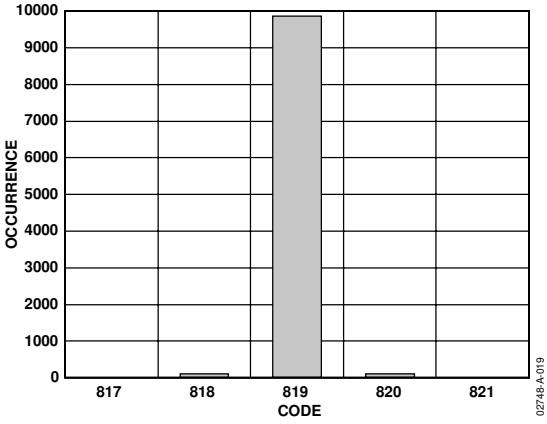

Figure 12. Code Histogram Plot, V_{DD} = 3 V

Figure 13 and Figure 14 show typical FFT plots for the ADuC814. These plots were generated using an external clock input via P3.5 to achieve coherent sampling. The ADC is using its internal reference (2.5 V) sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resultant FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, a 71 dB signal-to-noise ratio (SNR), and a THD greater than −80 dB.

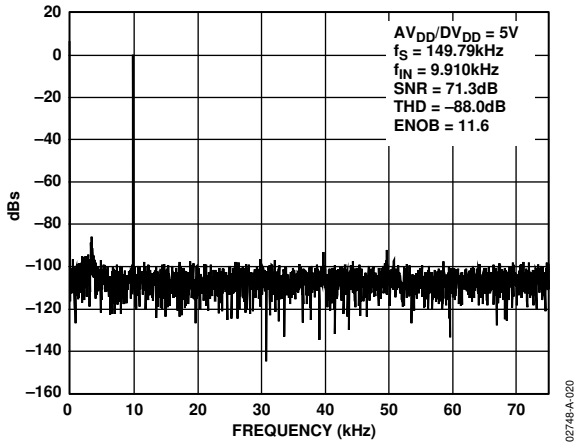

Figure 13. ADuC814 Dynamic Performance at V_{DD} = 5 V

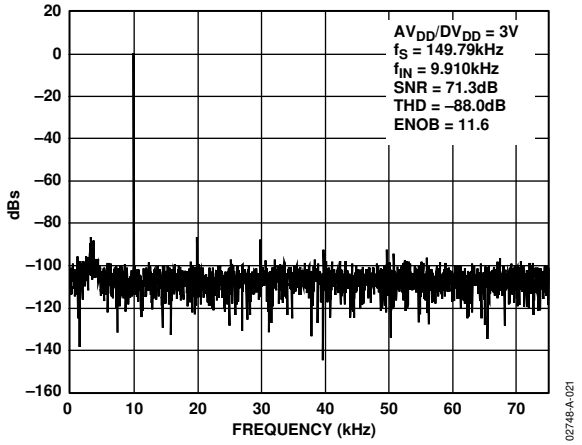

Figure 14. ADuC814 Dynamic Performance at V_{DD} = 3 V

Figure 15 and Figure 16 show typical dynamic performance versus external reference voltages. Again excellent ac performance can be observed in both plots with some roll-off being observed as V_{REF} falls below 1 V.

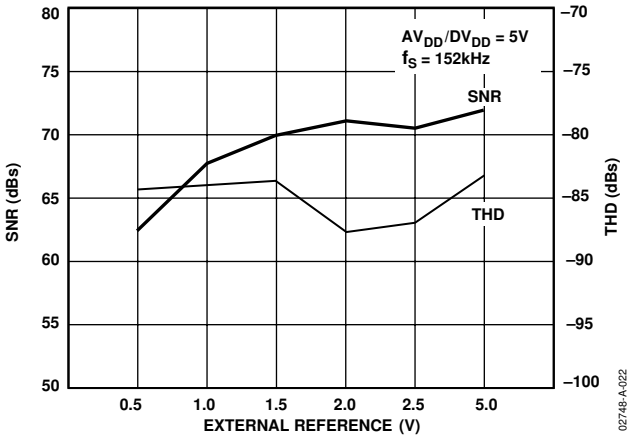

Figure 15. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 5 V

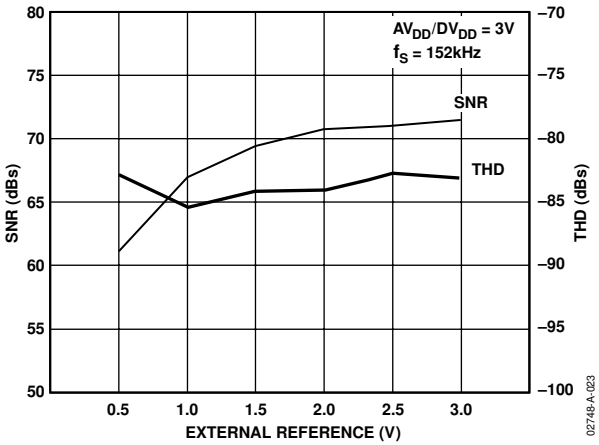

Figure 16. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 3 V

ADuC814 ARCHITECTURE, MAIN FEATURES

The ADuC814 is a fully integrated 247 kSPS 12-bit data acquisition system incorporating a high performance multi-channel ADC, an 8-bit MCU, and program/data Flash/EE memory on a single chip.

This low power device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 16.78 MHz. This clock is, in turn, routed through a programmable clock divider from which the MCU core clock operating frequency is generated.

The microcontroller core is an 8052, and therefore 8051, instruction set compatible. The microcontroller core machine cycle consists of 12 core clock periods of the selected core operating frequency. Eight kbytes of nonvolatile Flash/EE program memory are provided on-chip. 640 bytes of nonvolatile Flash/EE data memory and 256 bytes RAM are also integrated on-chip.

The ADuC814 also incorporates additional analog functionality with dual 12-bit DACs, a power supply monitor, and a band gap reference. On-chip digital peripherals include a watchdog timer, time interval counter, three timer/counters, and three serial I/O ports (SPI, UART, I^2C).

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the DLOAD pin. A detailed functional block diagram of the ADuC814 is shown in Figure 17.

The ADuC814 is supported by a QuickStart Development System. This is a full-featured, low cost system, consisting of PC-based (Windows compatible) hardware and software development tools.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is below 10 mW. The ADuC814 is housed in a 28-lead TSSOP package and is specified for operation over an extended temperature range −40°C to +125°C.

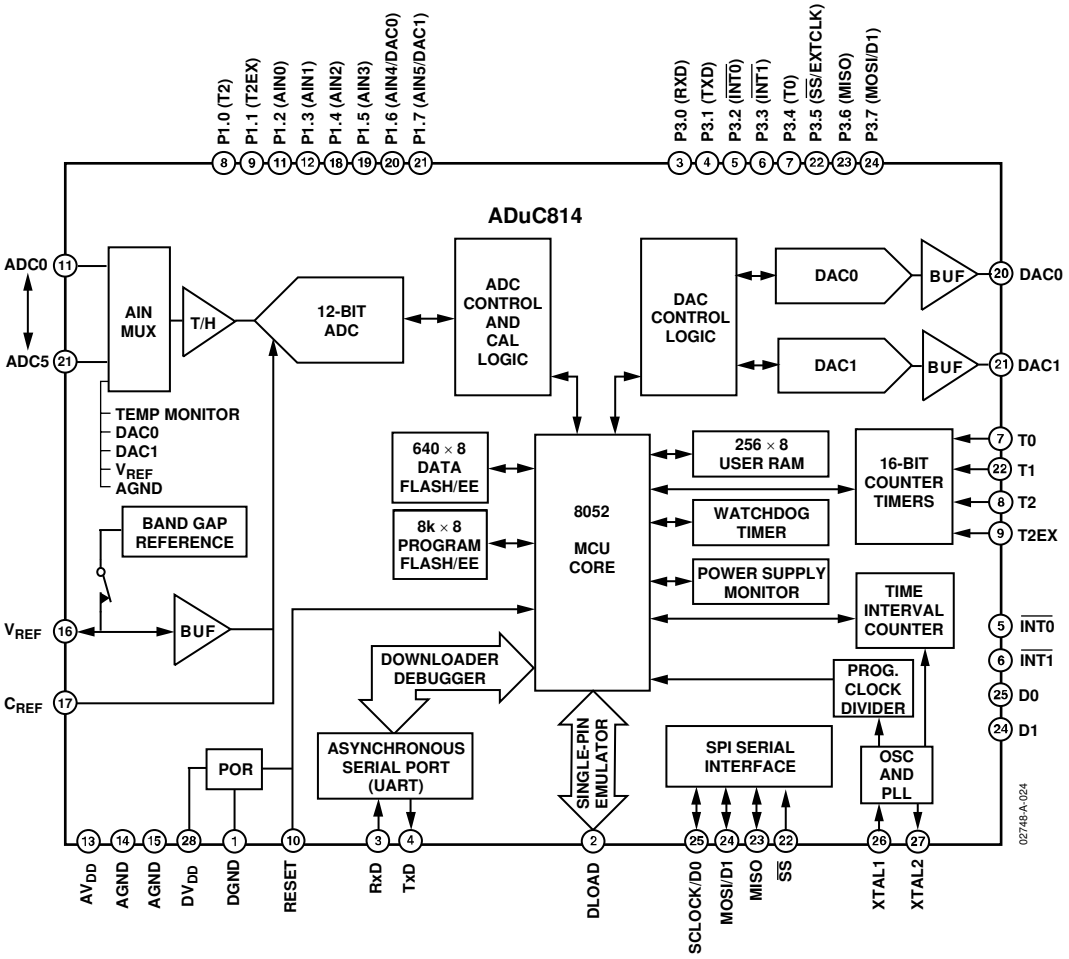

Figure 17. ADuC814 Block Diagram

MEMORY ORGANIZATION

The ADuC814 does not have Port 0 and Port 2 pins and therefore does not support external program or data memory interfaces. The device executes code from the internal 8-kByte Flash/EE program memory. This internal code space can be programmed via the UART serial port interface while the device is in-circuit. The program memory space of the ADuC814 is shown in Figure 18.

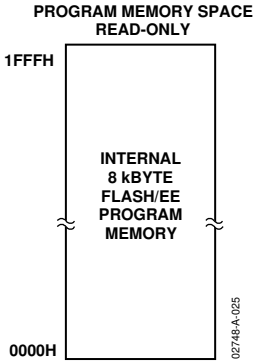

Figure 18. Program Memory Map

The data memory address space consists of internal memory only. The internal memory space is divided into four physically separate and distinct blocks, namely the lower 128 bytes of RAM, the upper 128 bytes of RAM, the 128 bytes of special function register (SFR) area, and a 640-byte Flash/EE data memory. While the upper 128 bytes of RAM and the SFR area share the same address locations, they are accessed through different addressing modes.

The lower 128 bytes of data memory can be accessed through direct or indirect addressing, the upper 128 bytes of RAM can be accessed through indirect addressing, and the SFR area is accessed through direct addressing.

Also, as shown in Figure 19, an additional 640 bytes of Flash/EE data memory are available to the user and can be accessed indirectly via a group of control registers mapped into the SFR area. Access to the Flash/EE data memory is discussed in detail later as part of the Flash/EE Memory section.

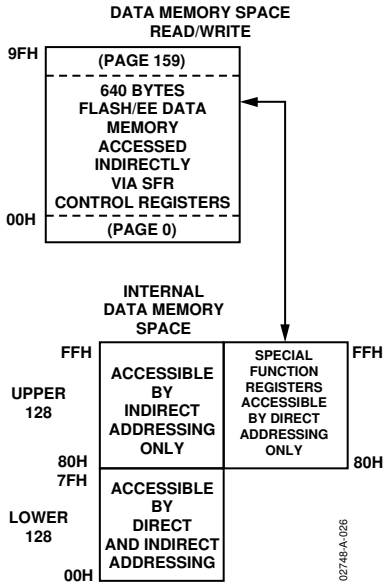

Figure 19. Data Memory Map

The lower 128 bytes of internal data memory are mapped as shown in Figure 20. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 to R7. The next 16 bytes (128 bits), locations 20H to 2FH above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 256 bytes.

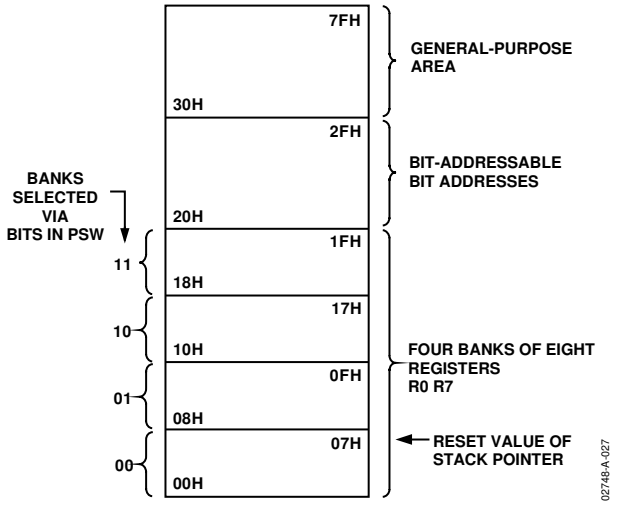

Figure 20. Lower 128 Bytes of Internal Data Memory

RESET initializes the stack pointer to location 07H and increments it once to start from location 08H, which is also the first register (R0) of Register Bank 1. If more than one register bank is being used, the stack pointer should be initialized to an area of RAM not used for data storage.

The SFR space is mapped to the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC814 via the SFR area is shown in Figure 21. A complete SFR map is shown in Figure 22.

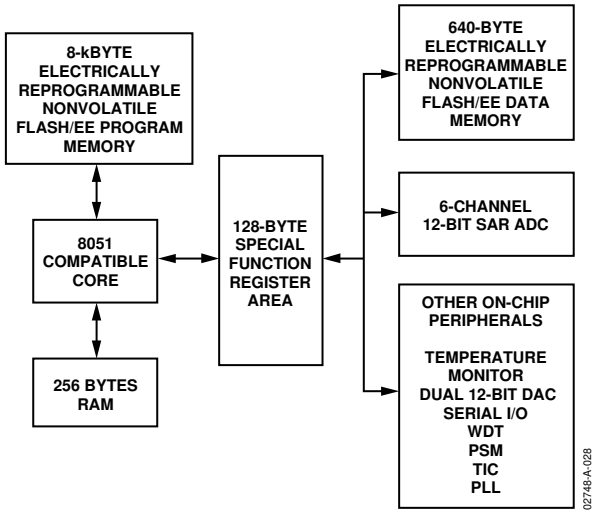

Figure 21. Programming Model

OVERVIEW OF MCU-RELATED SFRS

Accumulator SFR

ACC is the accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the accumulator as A.

B SFR

The B register is used with the ACC for multiplication and division operations. For other instructions it can be treated as a general-purpose scratchpad register.

Stack Pointer SFR

The SP register is the stack pointer and is used to hold an internal RAM address called the *top of the stack*. The SP register is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Data Pointer

The data pointer is made up of two 8-bit registers, named DPH (high byte) and DPL (low byte). These registers provide memory addresses for internal code access. The pointer may be manipulated as a 16-bit register (DPTR = DPH, DPL), or as two independent 8-bit registers (DPH, DPL).

Program Status Word SFR

The program status word (PSW) register is the program status word that contains several bits reflecting the current status of the CPU as detailed in Table 4.

SFR Address	D0H
Power-On Default	00H
Bit Addressable	Yes

CY	AC	F0	RS1	RS0	OV	F1	P

Table 4. PSW SFR Bit Designations

Bit No.	Name	Description		
7	CY	Carry Flag.		
6	AC	Auxiliary Carry Flag.		
5	F0	General-Purpose Flag.		
4	RS1	Register Bank Select Bits.		
3	RS0	RS1	RS0	Selected Bank
		0	0	0
		0	1	1
		1	0	2
		1	1	3
2	OV	Overflow Flag.		
1	F1	General-Purpose Flag.		
0	P	Parity Bit.		

Power Control SFR

The power control (PCON) register contains bits for power-saving options and general-purpose status flags as shown in Table 5.

SFR Address 87H
Power-On Default 00H
Bit Addressable No

SMOD	SERIPD	INT0PD	---	GF1	GF0	PD	IDL

Table 5. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate.
6	SERIPD	SPI Power-Down Interrupt Enable.
5	INT0PD	$\overline{\text{INT0}}$ Power-Down Interrupt Enable.
4	RSVD	Reserved.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable.
0	IDL	Idle Mode Enable.

SPECIAL FUNCTION REGISTERS

All registers, except the program counter and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

Figure 22 shows a full SFR memory map and SFR contents on RESET; NOT USED indicates unoccupied SFR locations.

Unoccupied locations in the SFR address space are not implemented, i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for future use are shaded (RESERVED) and should not be accessed by the user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0[5] F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
D1 EFH 0	D1EN EEH 0	D0 EDH 0	ECH 0	D0EN EBH 0	EAH 0	E9H 0	E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
ADCI DFH 0	ADCSPI DEH 0	CCONV DDH 0	SCONV DCH 0	CS3 DBH 0	CS2 DAH 0	CS1 D9H 0	CS0 D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RS1 D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WD C1H 0	WDWR C0H 0	BITS
PSI BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH 0	PT0 B9H 0	PX0 B8H 0	BITS
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	TI 99H 0	RI 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS

SPICON[1] F8H 04H	DAC0L F9H 00H	DAC0H FAH 00H	DAC1L FBH 00H	DAC1H FCH 00H	DACCON FDH 04H	RESERVED	RESERVED
B[1] F0H 00H	ADCOFSL F1H 00H	ADCOFSH F2H 20H	ADCGAINL F3H 00H	ADCGAINH F4H 00H	ADCCON3 F5H 00H	RESERVED	SPIDAT F7H 00H
DCON[1] E8H 00H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADCCON1 EFH 00H
ACC[1] E0H 00H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
ADCCON2[1] D8H 00H	ADCDATAL D9H 00H	ADCDATAH DAH 00H	RESERVED	RESERVED	RESERVED	RESERVED	PSMCON DFH DEH
PSW[1] D0H 00H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLLCON D7H 53H
T2CON[1] C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON[1] C0H 10H	RESERVED	CHIPID C2H 0XH	RESERVED	NOT USED	RESERVED	EDARL C6H 00H	RESERVED
IP[1] B8H 00H	ECON B9H 00H	ETIM1 BAH 00H	ETIM2 BBH 00H	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3[1] B0H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NOT USED
IE[1] A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
NOT USED	TIMECON A1H 00H	HTHSEC A2H 00H	SEC A3H 00H	MIN A4H 00H	HOUR A5H 00H	INTVAL A6H 00H	NOT USED
SCON[1] 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	CFG814 9CH 04H	NOT USED	NOT USED	NOT USED
P1[1,2] 90H FFH	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
TCON[1] 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
NOT USED	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	RESERVED	RESERVED	RESERVED	PCON 87H 00H

SFR MAP KEY:

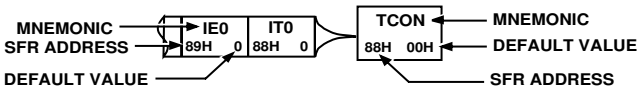

Figure 22. Special Function Register Locations and Reset Values

Note the following about SFRs:

- SFRs whose address ends in 0H or 8H are bit addressable.
- Only P1.0 and P1.1 can operate as digital I/O pins. P1.2–P1.7 can be configured as analog inputs (ADC inputs) or as digital inputs.
- The CHIPID SFR contains the silicon revision ID byte and may change for future silicon revisions.
- These registers are reconfigured at power-on with factory calculated calibration coefficients that can be overwritten by user code. See the calibration options in ADCCON3 SFR.
- When the SPIM bit in the SPICON SFR is cleared, the SPR0 bit reflects the level on the $\overline{SS}$ pin (Pin 22).

ADC CIRCUIT INFORMATION

GENERAL OVERVIEW

The ADC block incorporates a 4.05 msec, 6-channel, 12-bit resolution, single-supply ADC. This block provides the user with a multichannel multiplexer, track-and-hold amplifier, on-chip reference, offset calibration features and ADC. All components in this block are easily configured via a 3-register SFR interface.

The ADC consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 V to V_{REF}. A precision, factory calibrated 2.5 V reference is provided on-chip. An external reference may also be used via the external V_{REF} pin. This external reference can be in the range 1.0 V to AV_{DD}.

Single or continuous conversion modes can be initiated in software. In hardware, a convert signal can be applied to an external pin (CONVST), or alternatively Timer 2 can be configured to generate a repetitive trigger for ADC conversions.

The ADuC814 has a high speed ADC to SPI interface data capture logic implemented on-chip. Once configured, this logic transfers the ADC data to the SPI interface without the need for CPU intervention.

The ADC has six external input channels. Two of the ADC channels are multiplexed with the DAC outputs, ADC4 with DAC0, and ADC5 with DAC1. When the DAC outputs are in use, any ADC conversion on these channels represents the DAC output voltage. Due care must be taken to ensure that no external signal is trying to drive these ADC/DAC channels while the DAC outputs are enabled.

In addition to the six external channels of the ADC, five internal signals are also routed through the front end multiplexer. These signals include a temperature monitor, DAC0, DAC1, V_{REF}, and AGND. The temperature monitor is a voltage output from an on-chip band gap reference, which is proportional to absolute temperature. These internal channels can be selected similarly to the external channels via CS3–CS0 bits in the ADCCON2 SFR.

The ADuC814 is shipped with factory programmed offset and gain calibration coefficients that are automatically downloaded to the ADC on a power-on or RESET event, ensuring optimum ADC performance. The ADC core contains automatic endpoint self-calibration and system calibration options that allow the user to overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used.

ADC TRANSFER FUNCTION

The analog input range for the ADC is 0 V to V_{REF}. For this range, the designed code transitions occur midway between successive integer LSB values, i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs. The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when V_{REF} = 2.5 V. The ideal input/output transfer characteristic for the 0 V to V_{REF} range is shown in Figure 23.

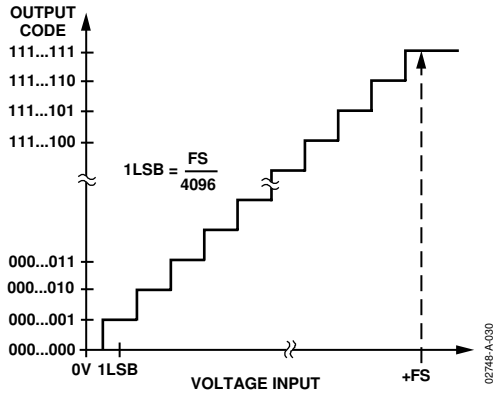

Figure 23. ADuC814 ADC Transfer Function

ADC Data Output Format

Once configured via the ADCCON1–3 SFRs, the ADC converts the analog input and provides an ADC 12-bit result word in the ADCDATAH/L SFRs. The ADCDATAL SFR contains the bottom 8 bits of the 12-bit result. The bottom nibble of the ADCDATAH SFR contains the top 4 bits of the result, while the top nibble contains the channel ID of the ADC channel which has been converted on. This ID corresponds to the channel selection bits CD3–CD0 in the ADCCON2 SFR. The format of the ADC 12-bit result word is shown in Figure 24.

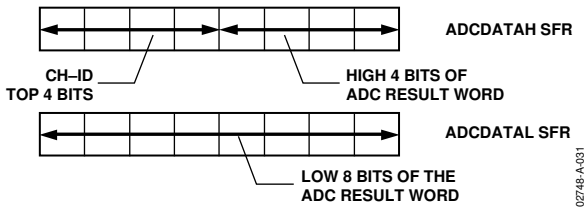

Figure 24. ADC Result Format

SFR INTERFACE TO ADC BLOCK

The ADC operation is fully controlled via three SFRs: ADCCON1, ADCCON2, and ADCCON3. These three registers control the mode of operation.

ADCCON1 (ADC CONTROL SFR 1)

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes, and power-down modes as detailed below.

SFR Address EFH
SFR Power-on Default 00H
Bit Addressable No

MODE	EXT_REF	CK1	CK0	AQ1	AQ0	T2C	EXC

Table 6. ADCCON1 SFR Bit Designations

Bit No.	Name	Description
7	MODE	Mode Bit. This bit selects the operating mode of the ADC. Set to 1 by the user to power on the ADC. Set to 0 by the user to power down the ADC.
6	EXT_REF	External Reference Select Bit. This bit selects which reference the ADC uses when performing a conversion. Set to 1 by the user to switch in an external reference. Set to 0 by the user to switch in the on-chip band gap reference.
5	CK1	ADC Clock Divide Bits.
4	CK0	CK1 and CK0 combine to select the divide ratio for the PLL master clock used to generate the ADC clock. To ensure correct ADC operation, the divider ratio must be chosen to reduce the ADC clock to 4.5 MHz and below. The divider ratio is selected as follows: CK1 CK0 PLL Divider 0 0 8 0 1 4 1 0 16 1 1 32
3	AQ1	The ADC Acquisition Time Select Bits.
2	AQ0	AQ1 and AQ0 combine to select the number of ADC clocks required for the input track-and-hold amplifier to acquire the input signal. The acquisition time is selected as follows: AQ1 AQ0 No. ADC Clks 0 0 1 0 1 2 1 0 3 1 1 4
1	T2C	The Timer2 Conversion Bit. T2C is set to enable the Timer2 overflow bit to be used as the ADC convert start trigger input.
0	EXC	The External Trigger Enable Bit. EXC is set to allow the external CONVST pin be used as the active low convert start trigger input. When enabled, a rising edge on this input pin trigger a conversion. This pin should remain low for a minimum pulse width of 100 nsec at the required sample rate.

ADCCON2 (ADC CONTROL SFR 2)

The ADCCON2 (byte addressable) register controls ADC channel selection and conversion modes as detailed below.

SFR Address D8H
SFR Power-On Default 00H
Bit Addressable Yes

ADCI	ADCSPI	CCONV	SCOVC	CS3	CS2	CS1	CS0

Table 7. ADCCON2 SFR Bit Designations

Bit No.	Name	Description
7	ADCI	ADC Interrupt Bit. ADCI is set at the end of a single ADC conversion cycle. If the ADC interrupt is enabled, the ADCI bit is cleared when user code vectors to the ADC interrupt routine. Otherwise the ADCI bit should be cleared by the user code.
6	ADCSPI	ADCSPI Mode Enable Bit. ADCSPI is set to enable the ADC conversion results to be transferred directly to the SPI data buffer (SPIDAT) without intervention from the CPU.
5	CCONV	Continuous Conversion Bit. CCONV is set to initiate the ADC into a continuous mode of conversion. In this mode the ADC starts converting based on the timing and channel configuration already set up in the ADCCON SFRs. The ADC automatically starts another conversion once a previous conversion cycle has completed. When operating in this mode from 3 V supplies, the ADC should be configured for ADC clock divide of 16 using CK1 and CK0 bits in ADCCON1, and ADC acquisition time should be set to four ADC clocks using AQ1, AQ0 bits in ADCCON1 SFR.
4	SCONV	Single Conversion Bit. SCONV is set to initiate a single conversion cycle. The SCONV bit is automatically reset to 0 on completion of the single conversion cycle. When operating in this mode from 3 V supplies, the maximum ADC sampling rate should not exceed 147 kSPS.
3	CS3	Channel Selection Bits. CS3–CS0 allow the user to program the ADC channel selection under software control. Once a conversion is initiated, the channel converted is pointed to by these channel selection bits. The Channel Select bits operate as follows:
2	CS2	
1	CS1	
0	CS0	

CS3	CS2	CS1	CS0	CHANNEL	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	X	Not a vaild selection. No ADC channel selected.
0	1	1	1	X	Not a valid selection. No ADC channel selected.
1	0	0	0	Temperature Sensor	
1	0	0	1	DAC0	
1	0	1	0	DAC1	
1	0	1	1	AGND	
1	1	0	0	V_{REF}	

ADCCON3 (ADC CONTROL SFR 3)

The ADCCON3 register controls the operation of various calibration modes as well as giving an indication of ADC busy status.

SFR Address F5H
SFR Power-On Default 00H

BUSY	GNCLD	AVGS1	AVGS0	OFCLD	MODCAL	TYPECAL	SCAL

Table 8. ADCCON3 SFR Bit Designations

Bit No.	Name	Description
7	BUSY	ADC Busy Status Bit. BUSY is a read-only status bit that is set during a valid ADC conversion or calibration cycle. Busy is automatically cleared by the core at the end of a conversion or calibration cycle.
6	GNCLD	Gain Calibration Disable Bit. This bit enables/disables the gain calibration coefficients from affecting the ADC results. Set to 0 to enable gain calibration coefficient Set to 1 to disable gain calibration coefficient.
5	AVGS1	Number of Averages Selection Bits.
4	AVGS0	This bit selects the number of ADC readings averaged for each bit decision during a calibration cycle. AVGS1 AVGS0 Number of Averages 0 0 15 0 1 1 1 0 31 1 1 63
3	OFCLD	Offset Calibration Disable Bit. This bit enables/disables the offset calibration coefficients from affecting the ADC results. Set to 0 to enable offset calibration coefficient. Set to 1 to disable the offset calibration coefficient
2	MODCAL	Calibration Mode Select Bit. This bit should be set to 1 for all calibration cycles.
1	TYPECAL	Calibration Type Select Bit. This bit selects between offset (zero-scale) and gain (full-scale) calibration. Set to 0 for offset calibration. Set to 1 for gain calibration.
0	SCAL	Start Calibration Cycle Bit. When set, this bit starts the selected calibration cycle. It is automatically cleared when the calibration cycle is completed.