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MicroConverter®, Dual 16-Bit/24-Bit Σ-Δ ADCs with Embedded 62 kB Flash MCU

ADuC834

FEATURES

High Resolution Σ-Δ ADCs
- 2 Independent ADCs (16-Bit and 24-Bit Resolution)
- 24-Bit No Missing Codes, Primary ADC
- 21-Bit rms (18.5-Bit p-p) Effective Resolution @ 20 Hz
- Offset Drift 10 nV/°C, Gain Drift 0.5 ppm/°C

Memory
- 62 Kbytes On-Chip Flash/EE Program Memory
- 4 Kbytes On-Chip Flash/EE Data Memory
- Flash/EE, 100 Year Retention, 100 Kcycles Endurance
- 3 Levels of Flash/EE Program Memory Security
- In-Circuit Serial Download (No External Hardware)
- High Speed User Download (5 Seconds)
- 2304 Bytes On-Chip Data RAM

8051-Based Core
- 8051 Compatible Instruction Set
- 32 kHz External Crystal
- On-Chip Programmable PLL (12.58 MHz Max)
- 3 × 16-Bit Timer/Counter
- 26 Programmable I/O Lines
- 11 Interrupt Sources, Two Priority Levels
- Dual Data Pointer, Extended 11-Bit Stack Pointer

On-Chip Peripherals
- Internal Power on Reset Circuit
- 12-Bit Voltage Output DAC
- Dual 16-Bit Σ-Δ DACs/PWMs
- On-Chip Temperature Sensor
- Dual Excitation Current Sources
- Time Interval Counter (Wake-Up/RTC Timer)
- UART, SPI®, and I²C® Serial I/O
- High Speed Baud Rate Generator (Including 115,200)
- Watchdog Timer (WDT)
- Power Supply Monitor (PSM)

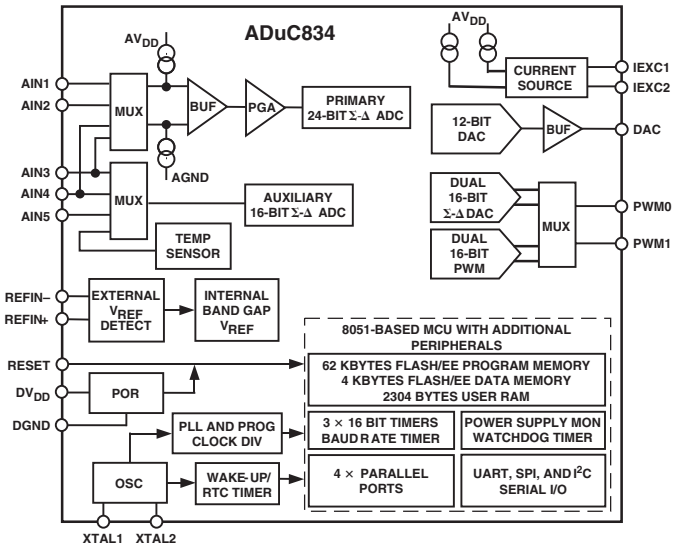
Power
- Normal: 2.3 mA Max @ 3.6 V (Core CLK = 1.57 MHz)
- Power-Down: 20 μA Max with Wake-Up Timer Running
- Specified for 3 V and 5 V Operation

Package and Temperature Range
- 52-Lead MQFP (14 mm × 14 mm), –40°C to +125°C
- 56-Lead LFCSP (8 mm × 8 mm), –40°C to +85°C

APPLICATIONS

Intelligent Sensors
Weigh Scales
Portable Instrumentation, Battery-Powered Systems
4–20 mA Transmitters
Data Logging
Precision System Monitoring

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADuC834 is a complete smart transducer front end, integrating two high resolution Σ-Δ ADCs, an 8-bit MCU, and program/data Flash/EE memory on a single chip.

The two independent ADCs (primary and auxiliary) include a temperature sensor and a PGA (allowing direct measurement of low level signals). The ADCs with on-chip digital filtering and programmable output data rates are intended for the measurement of wide dynamic range, low frequency signals, such as those in weigh scale, strain-gage, pressure transducer, or temperature measurement applications.

The device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an 8052 and therefore 8051 instruction set compatible with 12 core clock periods per machine cycle.

62 Kbytes of nonvolatile Flash/EE program memory, 4 Kbytes of nonvolatile Flash/EE data memory, and 2304 bytes of data RAM are provided on-chip. The program memory can be configured as data memory to give up to 60 Kbytes of NV data memory in data logging applications.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the $\overline{EA}$ pin. The ADuC834 is supported by a QuickStart™ development system featuring low cost software and hardware development tools.

REV. B

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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ADUC834* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADuC834 QuickStart Development System

DOCUMENTATION

Application Notes

- AN-1074: Understanding the Serial Download Protocol (Formerly uC004)
- AN-1139: Understanding the Parallel Programming Protocol
- AN-282: Fundamentals of Sampled Data Systems
- AN-644: Frequency Measurement Using Timer 2 on a MicroConverter ® (uC013)
- AN-645: Interfacing an HD44780 Character LCD to a MicroConverter ® (uC014)
- AN-660: XY-Matrix Keypad Interface to MicroConverter®
- AN-709: RTD Interfacing and Linearization Using an ADuC8xx MicroConverter®
- AN-759: Expanding the Number of DAC Outputs on the ADuC8xx and ADuC702x Families (uC012)
- UC-001: MicroConverter® I2C® Compatible Interface
- UC-002: Developing in C with the Keil uVision2 IDE
- UC-006: A 4-wire UART-to-PC Interface
- UC-007: User Download (ULOAD) Mode
- UC-008: Using the ADuC834 C-library
- UC-009: Addressing 16MB of External Data Memory
- UC-018: Uses of the Time Interval Counter

Data Sheet

- ADuC834: MicroConverter® Dual 16-/24- Bit SIgma-Delta ADCs with Embedded 62KB Flash MCU Data Sheet
- ADuC834: Silicon Errata Sheet

User Guides

- ADuC834 Quick Reference Guide
- UG-041: ADuC8xx Evaluation Kit Getting Started User Guide

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Integrated Route Taken to Pulse Oximetry

DESIGN RESOURCES

- ADUC834 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADUC834 EngineerZone Discussions.

SAMPLE AND BUY

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SPECIFICATIONS[1]

(AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V, REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	ADuC834	Test Conditions/Comments	Unit
ADC SPECIFICATIONS			
Conversion Rate	5.4	On Both Channels	Hz min
	105	Programmable in 0.732 ms Increments	Hz max
Primary ADC			
No Missing Codes[2]	24	20 Hz Update Rate	Bits min
Resolution	13.5	Range = ±20 mV, 20 Hz Update Rate	Bits p-p typ
	18.5	Range = ±2.56 V, 20 Hz Update Rate	Bits p-p typ
Output Noise	See Tables X and XI in ADuC834 ADC Description	Output Noise Varies with Selected Update Rate and Gain Range	
Integral Nonlinearity	±15	1 LSB_{16}	ppm of FSR max
Offset Error[3]	±3		μV typ
Offset Error Drift	±10		nV/°C typ
Full-Scale Error[4]	±10		μV typ
Gain Error Drift[5]	±0.5		ppm/°C typ
ADC Range Matching	±2	AIN = 18 mV	μV typ
Power Supply Rejection (PSR)	113	AIN = 7.8 mV, Range = ±20 mV	dBs typ
	80	AIN = 1 V, Range = ±2.56 V	dBs min
Common-Mode DC Rejection			
On AIN	95	At DC, AIN = 7.8 mV, Range = ±20 mV	dBs min
	113	At DC, AIN = 1 V, Range = ±2.56 V	dBs typ
On REFIN	125	At DC, AIN = 1 V, Range = ±2.56 V	dBs typ
Common-Mode 50 Hz/60 Hz Rejection[2]		20 Hz Update Rate	
On AIN	95	50 Hz/60 Hz ±1 Hz, AIN = 7.8 mV, Range = ±20 mV	dBs min
	90	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V	dBs min
On REFIN	90	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V	dBs min
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate	dBs min
On REFIN	60	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate	dBs min
Auxiliary ADC			
No Missing Codes[2]	16		Bits min
Resolution	16	Range = ±2.5 V, 20 Hz Update Rate	Bits p-p typ
Output Noise	See Table XII in ADuC834 ADC Description	Output Noise Varies with Selected Update Rate	
Integral Nonlinearity	±15		ppm of FSR max
Offset Error[3]	–2		LSB typ
Offset Error Drift	1		μV/°C typ
Full-Scale Error[6]	–2.5		LSB typ
Gain Error Drift[5]	±0.5		ppm/°C typ
Power Supply Rejection (PSR)	80	AIN = 1 V, 20 Hz Update Rate	dBs min
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	50 Hz/60 Hz ±1 Hz	dBs min
On REFIN	60	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate	dBs min
DAC PERFORMANCE			
DC Specifications[7]			
Resolution	12		Bits
Relative Accuracy	±3		LSB typ
Differential Nonlinearity	–1	Guaranteed 12-Bit Monotonic	LSB max
Offset Error	±50		mV max
Gain Error[8]	±1	AV_{DD} Range	% max
	±1	V_{REF} Range	% typ
AC Specifications[2, 7]			
Voltage Output Settling Time	15	Settling Time to 1 LSB of Final Value	μs typ
Digital-to-Analog Glitch Energy	10	1 LSB Change at Major Carry	nVs typ

SPECIFICATIONS (continued)

Parameter	ADuC834	Test Conditions/Comments	Unit
INTERNAL REFERENCE			
ADC Reference			
Reference Voltage	1.25 ± 1%	Initial Tolerance @ 25°C, V_{DD} = 5 V	V min/max
Power Supply Rejection	45		dBs typ
Reference Tempco	100		ppm/°C typ
DAC Reference			
Reference Voltage	2.5 ± 1%	Initial Tolerance @ 25°C, V_{DD} = 5 V	V min/max
Power Supply Rejection	50		dBs typ
Reference Tempco	±100		ppm/°C typ
ANALOG INPUTS/REFERENCE INPUTS			
Primary ADC			
Differential Input Voltage Ranges[9, 10]		External Reference Voltage = 2.5 V	
		RN2, RN1, RN0 of ADC0CON Set to	
Bipolar Mode (ADC0CON3 = 0)	±20	0 0 0 (Unipolar Mode 0 mV to 20 mV)	mV
	±40	0 0 1 (Unipolar Mode 0 mV to 40 mV)	mV
	±80	0 1 0 (Unipolar Mode 0 mV to 80 mV)	mV
	±160	0 1 1 (Unipolar Mode 0 mV to 160 mV)	mV
	±320	1 0 0 (Unipolar Mode 0 mV to 320 mV)	mV
	±640	1 0 1 (Unipolar Mode 0 mV to 640 mV)	mV
	±1.28	1 1 0 (Unipolar Mode 0 V to 1.28 V)	V
	±2.56	1 1 1 (Unipolar Mode 0 V to 2.56 V)	V
Analog Input Current[2]	±1	T_{MAX} = 85°C	nA max
	±5	T_{MAX} = 125°C	nA max
Analog Input Current Drift	±5	T_{MAX} = 85°C	pA/°C typ
	±15	T_{MAX} = 125°C	pA/°C typ
Absolute AIN Voltage Limits[2]	AGND + 100 mV		V min
	AV_{DD} – 100 mV		V max
Auxiliary ADC			
Input Voltage Range[9, 10]	0 to V_{REF}	Unipolar Mode, for Bipolar Mode See Note 11	V
Average Analog Input Current	125	Input Current Will Vary with Input	nA/V typ
Average Analog Input Current Drift[2]	±2	Voltage on the Unbuffered Auxiliary ADC	pA/V/°C typ
Absolute AIN Voltage Limits[2, 11]	AGND – 30 mV		V min
	AV_{DD} + 30 mV		V max
External Reference Inputs			
REFIN(+) to REFIN(–) Range[2]	1		V min
	AV_{DD}		V max
Average Reference Input Current	1	Both ADCs Enabled	μA/V typ
Average Reference Input Current Drift	±0.1		nA/V/°C typ
'NO Ext. REF' Trigger Voltage	0.3	NOXREF Bit Active if V_{REF} < 0.3 V	V min
	0.65	NOXREF Bit Inactive if V_{REF} > 0.65 V	V max
ADC SYSTEM CALIBRATION			
Full-Scale Calibration Limit	+1.05 × FS		V max
Zero-Scale Calibration Limit	–1.05 × FS		V min
Input Span	0.8 × FS		V min
	2.1 × FS		V max
ANALOG (DAC) OUTPUT			
Voltage Range	0 to V_{REF}	DACRN = 0 in DACCON SFR	V typ
	0 to AV_{DD}	DACRN = 1 in DACCON SFR	V typ
Resistive Load	10	From DAC Output to AGND	kΩ typ
Capacitive Load	100	From DAC Output to AGND	pF typ
Output Impedance	0.5		Ω typ
I_{SINK}	50		μA typ
TEMPERATURE SENSOR			
Accuracy	±2		°C typ
Thermal Impedance (θ_{JA})	90	MQFP Package	°C/W typ
	52	CSP Package (Base Floating)[12]	°C/W typ

Parameter	ADuC834	Test Conditions/Comments	Unit
TRANSDUCER BURNOUT CURRENT SOURCES			
AIN+ Current	–100	AIN+ Is the Selected Positive Input to the Primary ADC	nA typ
AIN– Current	+100	AIN– Is the Selected Negative Input to the Auxiliary ADC	nA typ
Initial Tolerance @ 25°C	±10		% typ
Drift	0.03		%/°C typ
EXCITATION CURRENT SOURCES			
Output Current	–200	Available from Each Current Source	μA typ
Initial Tolerance @ 25°C	±10		% typ
Drift	200		ppm/°C typ
Initial Current Matching @ 25°C	±1	Matching between Both Current Sources	% typ
Drift Matching	20		ppm/°C typ
Line Regulation (AV_{DD})	1	AV_{DD} = 5 V + 5%	μA/V typ
Load Regulation	0.1		μA/V typ
Output Compliance[2]	AV_{DD} – 0.6		V max
	AGND		min
LOGIC INPUTS			
All Inputs Except SCLOCK, RESET, and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	DV_{DD} = 5 V	V max
	0.4	DV_{DD} = 3 V	V max
V_{INH}, Input High Voltage	2.0		V min
SCLOCK and RESET Only (Schmitt-Triggered Inputs)[2]			
V_{T+}	1.3/3	DV_{DD} = 5 V	V min/V max
	0.95/2.5	DV_{DD} = 3 V	V min/V max
V_{T-}	0.8/1.4	DV_{DD} = 5 V	V min/V max
	0.4/1.1	DV_{DD} = 3 V	V min/V max
$V_{T+} - V_{T-}$	0.3/0.85	DV_{DD} = 5 V	V min/V max
	0.3/0.85	DV_{DD} = 3 V	V min/V max
Input Currents			
Port 0, P1.2–P1.7, $\overline{EA}$	±10	V_{IN} = 0 V or V_{DD}	μA max
SCLOCK, MOSI, MISO, $\overline{SS}$[13]	–10 min, –40 max	V_{IN} = 0 V, DV_{DD} = 5 V, Internal Pull-Up	μA min/μA max
	±10	V_{IN} = V_{DD}, DV_{DD} = 5 V	μA max
RESET	±10	V_{IN} = 0 V, DV_{DD} = 5 V	μA max
	35 min, 105 max	V_{IN} = V_{DD}, DV_{DD} = 5 V, Internal Pull-Down	μA min/μA max
P1.0, P1.1, Ports 2 and 3	±10	V_{IN} = V_{DD}, DV_{DD} = 5 V	μA max
	–180	V_{IN} = 2 V, DV_{DD} = 5 V	μA min
	–660		μA max
	–20	V_{IN} = 450 mV, DV_{DD} = 5 V	μA min
	–75		μA max
Input Capacitance	5	All Digital Inputs	pF typ
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)			
Logic Inputs, XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	DV_{DD} = 5 V	V max
	0.4	DV_{DD} = 3 V	V max
V_{INH}, Input High Voltage	3.5	DV_{DD} = 5 V	V min
	2.5	DV_{DD} = 3 V	V min
XTAL1 Input Capacitance	18		pF typ
XTAL2 Output Capacitance	18		pF typ

SPECIFICATIONS (continued)

Parameter	ADuC834	Test Conditions/Comments	Unit
LOGIC OUTPUTS (Not Including XTAL2)[2]			
V_{OH}, Output High Voltage	2.4	V_{DD} = 5 V, I_{SOURCE} = 80 μA	V min
	2.4	V_{DD} = 3 V, I_{SOURCE} = 20 μA	V min
V_{OL}, Output Low Voltage[14]	0.4	I_{SINK} = 8 mA, SCLOCK, MOSI/SDATA	V max
	0.4	I_{SINK} = 10 mA, P1.0 and P1.1	V max
	0.4	I_{SINK} = 1.6 mA, All Other Outputs	V max
Floating State Leakage Current[2]	±10		μA max
Floating State Output Capacitance	5		pF typ
POWER SUPPLY MONITOR (PSM)			
AV_{DD} Trip Point Selection Range	2.63	Four Trip Points Selectable in This Range	V min
	4.63	Programmed via TPA1–0 in PSMCON	V max
AV_{DD} Power Supply Trip Point Accuracy	±3.0	T_{MAX} = 85°C	% max
	±4.0	T_{MAX} = 125°C	% max
DV_{DD} Trip Point Selection Range	2.63	Four Trip Points Selectable in This Range	V min
	4.63	Programmed via TPD1–0 in PSMCON	V max
DV_{DD} Power Supply Trip Point Accuracy	±3.0	T_{MAX} = 85°C	% max
	±4.0	T_{MAX} = 125°C	% max
WATCHDOG TIMER (WDT)			
Timeout Period	0	Nine Timeout Periods in This Range	ms min
	2000	Programmed via PRE3–0 in WDCON	ms max
MCU CORE CLOCK RATE		Clock Rate Generated via On-Chip PLL	
MCU Clock Rate[2]	98.3	Programmable via CD2–0 Bits in PLLCON SFR	kHz min
	12.58		MHz max
START-UP TIME			
At Power-On	300		ms typ
After External RESET in Normal Mode	3		ms typ
After WDT Reset in Normal Mode	3	Controlled via WDCON SFR	ms typ
From Idle Mode	10		μs typ
From Power-Down Mode			
Oscillator Running		OSC_PD Bit = 0 in PLLCON SFR	
Wake-Up with $\overline{INT0}$ Interrupt	20		μs typ
Wake-Up with SPI Interrupt	20		μs typ
Wake-Up with TIC Interrupt	20		μs typ
Wake-Up with External RESET	3		ms typ
Oscillator Powered Down		OSC_PD Bit = 1 in PLLCON SFR	
Wake-Up with $\overline{INT0}$ Interrupt	20		μs typ
Wake-Up with SPI Interrupt	20		μs typ
Wake-Up with External RESET	5		ms typ
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[15]			
Endurance[16]	100,000		Cycles min
Data Retention[17]	100		Years min

Parameter	ADuC834	Test Conditions/Comments	Unit
POWER REQUIREMENTS		DV_{DD} and AV_{DD} Can Be Set Independently	
Power Supply Voltages			
AV_{DD}, 3 V Nominal Operation	2.7		V min
	3.6		V max
AV_{DD}, 5 V Nominal Operation	4.75		V min
	5.25		V max
DV_{DD}, 3 V Nominal Operation	2.7		V min
	3.6		V max
DV_{DD}, 5 V Nominal Operation	4.75		V min
	5.25		V max
5 V POWER CONSUMPTION		DV_{DD} = 4.75 V to 5.25 V, AV_{DD} = 5.25 V	
Power Supply Currents Normal Mode[18, 19]			
DV_{DD} Current	4	Core CLK = 1.57 MHz	mA max
DV_{DD} Current	13	Core CLK = 12.58 MHz	mA typ
	16	Core CLK = 12.58 MHz	mA max
AV_{DD} Current	180	Core CLK = 1.57 MHz or 12.58 MHz	μA max
Typical Additional Power Supply Currents (AI_{DD} and DI_{DD})		Core CLK = 1.57 MHz	
PSM Peripheral	50		μA typ
Primary ADC	1		mA typ
Auxiliary ADC	500		μA typ
DAC	150		μA typ
Dual Current Sources	400		μA typ
3 V POWER CONSUMPTION		DV_{DD} = 2.7 V to 3.6 V	
Power Supply Currents Normal Mode[18, 19]			
DV_{DD} Current	2.3	Core CLK = 1.57 MHz	mA max
DV_{DD} Current	8	Core CLK = 12.58 MHz	mA typ
	10	Core CLK = 12.58 MHz	mA max
AV_{DD} Current	180	AV_{DD} = 5.25 V, Core CLK = 1.57 MHz or 12.58 MHz	μA max
Power Supply Currents Power-Down Mode[18, 19]		Core CLK = 1.57 MHz or 12.58 MHz	
DV_{DD} Current	20	T_{MAX} = 85°C; Osc. On, TIC On	μA max
	40	T_{MAX} = 125°C; Osc. On, TIC On	μA max
DV_{DD} Current	10	Osc. Off	μA typ
AV_{DD} Current	1	AV_{DD} = 5.25 V; T_{MAX} = 85°C; Osc. On or Osc. Off	μA max
	3	AV_{DD} = 5.25 V; T_{MAX} = 125°C; Osc. On or Osc. Off	μA max

NOTES

[1] Temperature Range for ADuC834BS (MQFP package) is –40°C to +125°C.
Temperature Range for ADuC834BCP (CSP package) is –40°C to +85°C.

[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.

[3] System Zero-Scale Calibration can remove this error.

[4] The primary ADC is factory calibrated at 25°C with $AV_{DD} = DV_{DD} = 5$ V yielding this full-scale error of 10 μV. If user power supply or temperature conditions are significantly different from these, an Internal Full-Scale Calibration will restore this error to 10 μV. A system zero-scale and full-scale calibration will remove this error altogether.

[5] Gain Error Drift is a span drift. To calculate Full-Scale Error Drift, add the Offset Error Drift to the Gain Error Drift times the full-scale input.

[6] The auxiliary ADC is factory calibrated at 25°C with $AV_{DD} = DV_{DD} = 5$ V yielding this full-scale error of –2.5 LSB. A system zero-scale and full-scale calibration will remove this error altogether.

[7] DAC linearity and ac specifications are calculated using: reduced code range of 48 to 4095, 0 to V_{REF}; reduced code range of 100 to 3950, 0 to V_{DD}.

[8] Gain Error is a measure of the span error of the DAC.

[9] In general terms, the bipolar input voltage range to the primary ADC is given by $RangeADC = \pm(V_{REF}\ 2^{RN})/125$, where:
V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0, e.g., V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0 the $Range_{ADC} = \pm 1.28$ V. In unipolar mode, the effective range is 0 V to 1.28 V in our example.

[10] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0 and XREF1 bits in ADC0CON and ADC1CON, respectively.

[11] In bipolar mode, the Auxiliary ADC can only be driven to a minimum of AGND – 30 mV as indicated by the Auxiliary ADC absolute AIN voltage limits. The bipolar range is still $–V_{REF}$ to $+V_{REF}$; however, the negative voltage is limited to –30 mV.

[12] The ADuC834BCP (CSP Package) has been qualified and tested with the base of the CSP Package floating.

[13] Pins configured in SPI Mode, pins configured as digital inputs during this test.

[14] Pins configured in I^2C Mode only.

[15] Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

[16] Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 Kcycles.

[17] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure 16 in the Flash/EE Memory section of this data sheet.

[18] Power Supply current consumption is measured in Normal, Idle, and Power-Down modes under the following conditions:
Normal mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.
Idle mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0 = 1, Core Execution suspended in idle mode.
Power-Down mode: Reset = 0.4 V, All P0 pins and P1.2–P1.7 Pins = 0.4 V, All other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core Execution suspended in power-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR.

[19] DV_{DD} power supply current will increase typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

AV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
AGND to DGND[2]	–0.3 V to +0.3 V
AV_{DD} to DV_{DD}	–2 V to +5 V
Analog Input Voltage to AGND[3]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MQFP)	90°C/W
θ_{JA} Thermal Impedance (LFCSP Base Floating)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

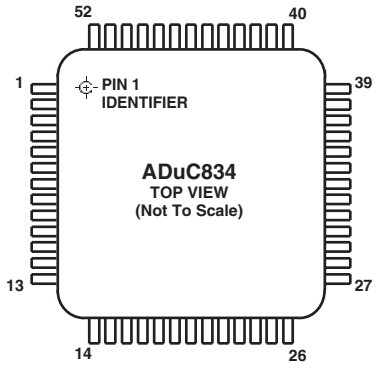
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]AGND and DGND are shorted internally on the ADuC834.

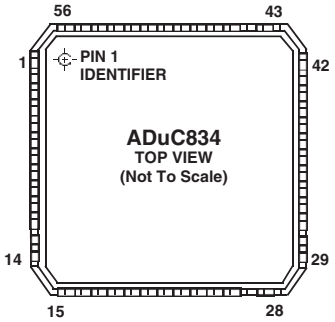
[3]Applies to P1.2 to P1.7 pins operating in analog or digital input modes.

PIN CONFIGURATION

52-Lead MQFP



56-Lead LFCSP



NOTES

1. EXPOSED PAD. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO THE METAL PLATE ON THE PCB AND TO DGND.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuC834 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

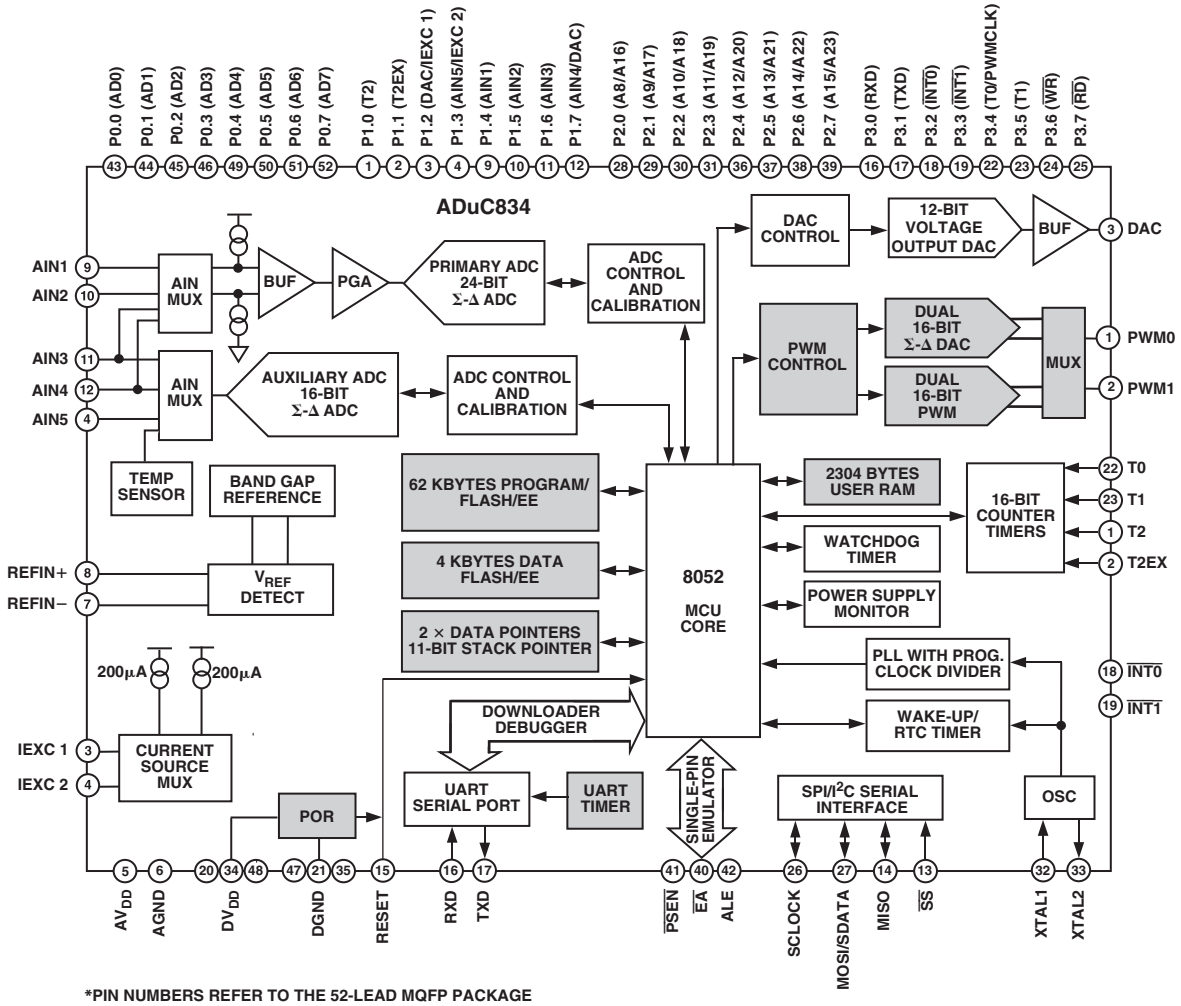


Figure 1. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin No. 52-Lead MQFP	Pin No. 56-Lead CSP	Mnemonic	Type*	Description
1, 2	56, 1	P1.0/P1.1	I/O	P1.0 and P1.1 can function as a digital inputs or digital outputs and have a pull-up configuration as described below for Port 3. P1.0 and P1.1 have an increased current drive sink capability of 10 mA.
		P1.0/T2/PWM0	I/O	P1.0 and P1.1 also have various secondary functions as described below. P1.0 can also be used to provide a clock input to Timer 2. When enabled, counter 2 is incremented in response to a negative transition on the T2 input pin. If the PWM is enabled, the PWM0 output will appear at this pin.
		P1.1/T2EX/PWM1	I/O	P1.1 can also be used to provide a control input to Timer 2. When enabled, a negative transition on the T2EX input pin will cause a Timer 2 capture or reload event. If the PWM is enabled, the PWM1 output will appear at this pin.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No. 52-Lead MQFP	Pin No. 56-Lead CSP	Mnemonic	Type*	Description
3–4, 9–12	2–3, 11–14	P1.2–P1.7	I	Port 1.2 to Port 1.7 have no digital output driver; they can function as a digital input for which '0' must be written to the port bit. As a digital input, these pins must be driven high or low externally. These pins also have the following analog functionality:
		P1.2/DAC/IEXC1	I/O	The voltage output from the DAC or one or both current sources (200 μA or 2 × 200 μA) can be configured to appear at this pin.
		P1.3/AIN5/IEXC2	I/O	Auxiliary ADC Input or one or both current sources can be configured at this pin.
		P1.4/AIN1	I	Primary ADC, Positive Analog Input
		P1.5/AIN2	I	Primary ADC, Negative Analog Input
		P1.6/AIN3	I	Auxiliary ADC Input or Muxed Primary ADC, Positive Analog Input
		P1.7/AIN4/DAC	I/O	Auxiliary ADC Input or Muxed Primary ADC, Negative Analog Input. The voltage output from the DAC can also be configured to appear at this pin.
5	4, 5	AV_{DD}	S	Analog Supply Voltage, 3 V or 5 V
6	6, 7, 8	AGND	S	Analog Ground. Ground reference pin for the analog circuitry.
7	9	REFIN(–)	I	Reference Input, Negative Terminal
8	10	REFIN(+)	I	Reference Input, Positive Terminal
13	15	$\overline{SS}$	I	Slave Select Input for the SPI Interface. A weak pull-up is present on this pin.
14	16	MISO	I/O	Master Input/Slave Output for the SPI Interface. There is a weak pull-up on this input pin.
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt trigger input stage on this pin.
16–19, 22–25	18–21, 24–27	P3.0–P3.7	I/O	Bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for two core clock periods of the instruction cycle. Port 3 pins also have various secondary functions including:
		P3.0/RXD	I/O	Receiver Data for UART Serial Port
		P3.1/TXD	I/O	Transmitter Data for UART Serial Port
		P3.2/$\overline{INT0}$	I/O	External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
		P3.3/$\overline{INT1}$	I/O	External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
		P3.4/T0/ PWMCLK	I/O	Timer/Counter 0 External Input. If the PWM is enabled, an external clock may be input at this pin.
		P3.5/T1	I/O	Timer/Counter 1 External Input
		P3.6/$\overline{WR}$	I/O	External Data Memory Write Strobe. Latches the data byte from Port 0 into an external data memory.
		P3.7/$\overline{RD}$	I/O	External Data Memory Read Strobe. Enables the data from an external data memory to Port 0.
20, 34, 48	22, 36, 51	DV_{DD}	S	Digital Supply, 3 V or 5 V.
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
26		SCLOCK	I/O	Serial Interface Clock for Either the I^2C or SPI Interface. As an input, this pin is a Schmitt-triggered input and a weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be directly controlled in software as a digital output pin.
27		MOSI/SDATA	I/O	Serial Data I/O for the I^2C Interface or Master Output/Slave Input for the SPI Interface. A weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be directly controlled in software as a digital output pin.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No. 52-Lead MQFP	Pin No. 56-Lead CSP	Mnemonic	Type*	Description
28–31 36–39	30–33 39–42	P2.0–P2.7 (A8–A15) (A16–A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the 24-bit external data memory space.
32	34	XTAL1	I	Input to the Crystal Oscillator Inverter
33	35	XTAL2	O	Output from the Crystal Oscillator Inverter. (See "Hardware Design Considerations" for description.)
40	43	$\overline{EA}$	I/O	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000h to F7FFh. When held low, this input enables the device to fetch all instructions from external program memory. To determine the mode of code execution, i.e., internal or external, the $\overline{EA}$ pin is sampled at the end of an external RESET assertion or as part of a device power cycle. $\overline{EA}$ may also be used as an external emulation I/O pin, and therefore the voltage level at this pin must not be changed during normal mode operation as it may cause an emulation interrupt that will halt code execution.
41	44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. $\overline{PSEN}$ can also be used to enable serial download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external code or data memory access cycles. It is activated every six oscillator periods except during an external data memory access. It can be disabled by setting the PCON.4 bit in the PCON SFR.
43–46 49–52	46–49 52–55	P0.0–P0.7 (AD0–AD3) (AD4–AD7)	I/O	P0.0–P0.7, these pins are part of Port0, which is an 8-bit, open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. An external pull-up resistor will be required on P0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and databus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.
		EPAD		Exposed Pad. The LFCSP has an exposed pad that must be soldered to the metal plate on the PCB and to DGND.

*I = Input, O = Output, S = Supply.

MEMORY ORGANIZATION

The ADuC834 contains four different memory blocks, namely:

- 62 Kbytes of On-Chip Flash/EE Program Memory
- 4 Kbytes of On-Chip Flash/EE Data Memory
- 256 bytes of General-Purpose RAM
- 2 Kbytes of Internal XRAM

(1) Flash/EE Program Memory

The ADuC834 provides 62 Kbytes of Flash/EE program memory to run user code. The user can choose to run code from this internal memory or run code from an external program memory.

If the user applies power or resets the device while the $\overline{EA}$ pin is pulled low externally, the part will execute code from the external program space; otherwise, if $\overline{EA}$ is pulled high externally, the part defaults to code execution from its internal 62 Kbytes of Flash/EE program memory.

Unlike the ADuC824, where code execution can overflow from the internal code space to external code space once the PC becomes greater than 1FFFH, the ADuC834 does not support the rollover from F7FFH in internal code space to F800H in external code space. Instead, the 2048 bytes between F800H and FFFFH will appear as NOP instructions to user code.

Permanently embedded firmware allows code to be serially downloaded to the 62 Kbytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

56 Kbytes of the program memory can be reprogrammed during runtime; thus the code space can be upgraded in the field using a user defined protocol or it can be used as a data memory. This will be discussed in more detail in the Flash/EE Memory section of the data sheet.

(2) Flash/EE Data Memory

4 Kbytes of Flash/EE Data Memory are available to the user and can be accessed indirectly via a group of registers mapped into the Special Function Register (SFR) area. Access to the Flash/EE Data memory is discussed in detail later as part of the Flash/EE Memory section in this data sheet.

(3) General-Purpose RAM

The general-purpose RAM is divided into two separate memories, namely the upper and the lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing; the upper 128 bytes of RAM can only be accessed through indirect addressing as it shares the same address space as the SFR space, which can only be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 2. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits), locations 20H through 2FH above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

Reset initializes the stack pointer to location 07H. Any CALL or PUSH pre-increments the SP before loading the stack. Therefore, loading the stack starts from locations 08H, which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

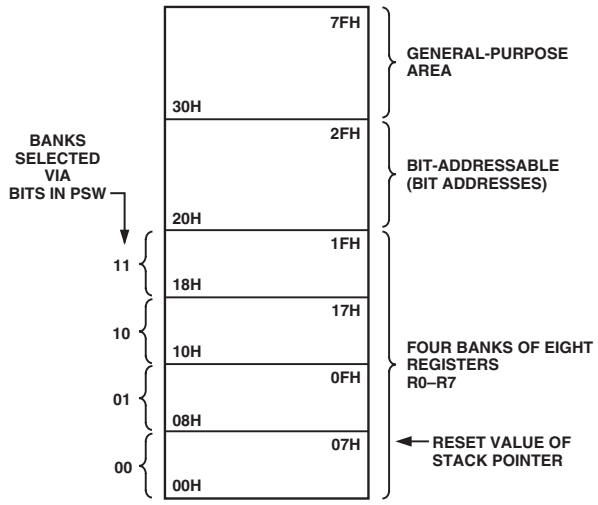


Figure 2. Lower 128 Bytes of Internal Data Memory

(4) Internal XRAM

The ADuC834 contains 2 Kbytes of on-chip extended data memory. This memory, although on-chip, is accessed via the MOVX instruction. The 2 Kbytes of internal XRAM are mapped into the bottom 2 Kbytes of the external address space if the CFG834.0 bit is set. Otherwise, access to the external data memory will occur just like a standard 8051.

Even with the CFG834.0 bit set, access to the external XRAM will occur once the 24-bit DPTR is greater than 0007FFH.

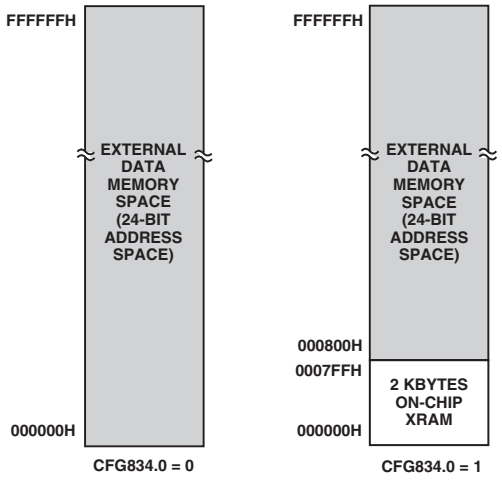


Figure 3. Internal and External XRAM

GENERAL NOTES PERTAINING TO THIS DATA SHEET

1. SET implies a Logic 1 state and CLEARED implies a Logic 0 state unless otherwise stated.
2. SET and CLEARED also imply that the bit is set or automatically cleared by the ADuC834 hardware unless otherwise stated.
3. User software should not write 1s to reserved or unimplemented bits as they may be used in future products.
4. Any pin numbers used throughout this data sheet refer to the 52-lead MQFP package, unless otherwise stated.

When accessing the internal XRAM, the P0 and P2 port pins, as well as the $\overline{RD}$ and $\overline{WR}$ strobes, will not be output as per a standard 8051 MOVX instruction. This allows the user to use these port pins as standard I/O.

The upper 1792 bytes of the internal XRAM can be configured to be used as an extended 11-bit stack pointer. By default, the stack will operate exactly like an 8052 in that it will roll over from FFH to 00H in the general-purpose RAM. On the ADuC834 however, it is possible (by setting CFG834.7) to enable the 11-bit extended stack pointer. In this case, the stack will roll over from FFH in RAM to 0100H in XRAM. The 11-bit stack pointer is visible in the SP and SPH SFRs. The SP SFR is located at 81H as with a standard 8052. The SPH SFR is located at B7H. The 3 LSBs of this SFR contain the three extra bits necessary to extend the 8-bit stack pointer into an 11-bit stack pointer.

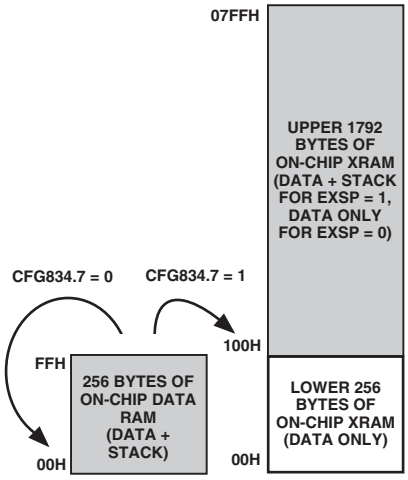


Figure 4. Extended Stack Pointer Operation

External Data Memory (External XRAM)
Just like a standard 8051 compatible core, the ADuC834 can access external data memory using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory.

The ADuC834 however, can access up to 16 Mbytes of external data memory. This is an enhancement of the 64 Kbytes external data memory space available on a standard 8051 compatible core.

The external data memory is discussed in more detail in the ADuC834 Hardware Design Considerations section.

SPECIAL FUNCTION REGISTERS (SFRS)
The SFR space is mapped into the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC834 via the SFR area is shown in Figure 5.

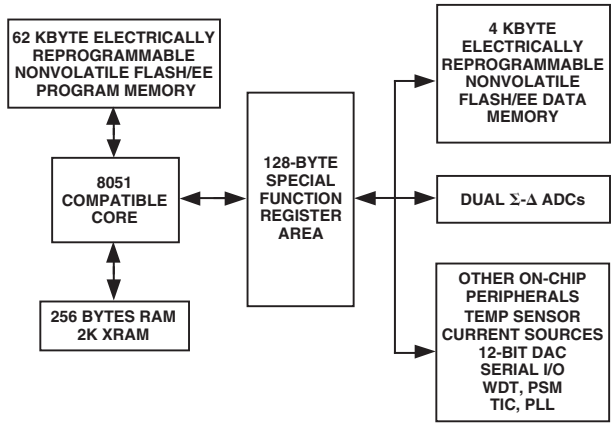


Figure 5. Programming Model

All registers, except the Program Counter (PC) and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

Accumulator SFR (ACC)
ACC is the Accumulator Register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR (B)
The B Register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratchpad register.

Data Pointer (DPTR)
The Data Pointer is made up of three 8-bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).

The ADuC834 supports dual data pointers. Refer to the Dual Data Pointer section in this data sheet.

Stack Pointer (SP and SPH)
The SP SFR is the stack pointer and is used to hold an internal RAM address that is called the 'top of the stack.' The SP Register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP Register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

As mentioned earlier, the ADuC834 offers an extended 11-bit stack pointer. The three extra bits to make up the 11-bit stack pointer are the 3 LSBs of the SPH byte located at B7H.

Program Status Word (PSW)
The PSW SFR contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power-On Default Value	00H
Bit Addressable	Yes

Table I. PSW SFR Bit Designations

Bit	Name	Description		
7	CY	Carry Flag		
6	AC	Auxiliary Carry Flag		
5	F0	General-Purpose Flag		
4	RS1	Register Bank Select Bits		
3	RS0	RS1	RS0	Selected Bank
		0	0	0
		0	1	1
		1	0	2
		1	1	3
2	OV	Overflow Flag		
1	F1	General-Purpose Flag		
0	P	Parity Bit		

Power Control SFR (PCON)
The PCON SFR contains bits for power-saving options and general-purpose status flags as shown in Table II.

The TIC (wake-up/RTC timer) can be used to accurately wake up the ADuC834 from power-down at regular intervals. To use the TIC to wake up the ADuC834 from power-down, the OSC_PD bit in the PLLCON SFR must be clear and the TIC must be enabled.

SFR Address	87H
Power-On Default Value	00H
Bit Addressable	No

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	SERIPD	SPI Power-Down Interrupt Enable
5	INT0PD	$\overline{\text{INT0}}$ Power-Down Interrupt Enable
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

ADuC834 CONFIGURATION SFR (CFG834)
The CFG834 SFR contains the necessary bits to configure the internal XRAM and the extended SP. By default it configures the user into 8051 mode, i.e., extended SP is disabled, internal XRAM is disabled.

SFR Address	AFH
Power-On Default Value	00H
Bit Addressable	No

Table III. CFG834 SFR Bit Designations

Bit	Name	Description
7	EXSP	Extended SP Enable. If this bit is set, the stack will roll over from SPH/SP = 00FFH to 0100H. If this bit is clear, the SPH SFR will be disabled and the stack will roll over from SP = FFH to SP = 00H
6	—	Reserved for Future Use
5	—	Reserved for Future Use
4	—	Reserved for Future Use
3	—	Reserved for Future Use
2	—	Reserved for Future Use
1	—	Reserved for Future Use
0	XRAMEN	XRAM Enable Bit. If this bit is set, the internal XRAM will be mapped into the lower 2 Kbytes of the external address space. If this bit is clear, the internal XRAM will not be accessible and the external data memory will be mapped into the lower 2 Kbytes of external data memory. (See Figure 3.)

COMPLETE SFR MAP

Figure 6 shows a full SFR memory map and the SFR contents after RESET. NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations that are reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS
$\overline{RD}$ B7H 1	$\overline{WR}$ B6H 1	T1 B5H 1	T0 B4H 1	$\overline{INT1}$ B3H 1	$\overline{INT0}$ B2H 1	TXD B1H 1	RXD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

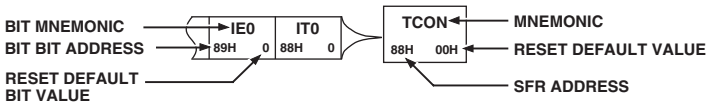
SPICON F8H 04H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	RESERVED	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	GN0L[1] E9H 55H	GN0M[1] EAH 55H	GN0H[1] EBH 53H	GN1L[1] ECH 9AH	GN1H[1] EDH 59H	RESERVED	RESERVED
ACC E0H 00H	OF0L E1H 00H	OF0M E2H 00H	OF0H E3H 80H	OF1L E4H 00H	OF1H E5H 80H	RESERVED	RESERVED
ADCSTAT D8H 00H	ADC0L D9H 00H	ADC0M DAH 00H	ADC0H DBH 00H	ADC1L DCH 00H	ADC1H DDH 00H	RESERVED	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 00H	ADC0CON D2H 07H	ADC1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H 2×H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	EADRH C7H 00H
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	RESERVED	RESERVED	SPH B7H 00H
IE A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG834 AFH 00H
P2 A0H FFH	TIMECON A1H 00H	HTHSEC[2] A2H 00H	SEC[2] A3H 00H	MIN[2] A4H 00H	HOUR[2] A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SCON 98H 00H	SBUF 99H 00H	RESERVED	RESERVED	NOT USED	T3FD 9DH 00H	T3CON 9EH 00H	RESERVED
P1 90H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

NOTES

[1]CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY CALIBRATED VALUES.

[2]THESE SFRS MAINTAIN THEIR PRERESET VALUES AFTER A RESET IF TIMECON.0 = 1.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT-ADDRESSABLE.

Figure 6. Special Function Register Locations and Their Reset Default Values

ADC SFR INTERFACE

Both ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following pages.

ADCSTAT	ADC Status Register. Holds general status of the primary and auxiliary ADCs.
ADCMODE	ADC Mode Register. Controls general modes of operation for primary and auxiliary ADCs.
ADC0CON	Primary ADC Control Register. Controls specific configuration of primary ADC.
ADC1CON	Auxiliary ADC Control Register. Controls specific configuration of auxiliary ADC.
SF	Sinc Filter Register. Configures the decimation factor for the $Sinc^3$ filter and thus the primary and auxiliary ADC update rates.
ICON	Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H	Primary ADC 24-bit conversion result is held in these three 8-bit registers.
ADC1L/H	Auxiliary ADC 16-bit conversion result is held in these two 8-bit registers.
OF0L/M/H	Primary ADC 24-bit Offset Calibration Coefficient is held in these three 8-bit registers.
OF1L/H	Auxiliary ADC 16-bit Offset Calibration Coefficient is held in these two 8-bit registers.
GN0L/M/H	Primary ADC 24-bit Gain Calibration Coefficient is held in these three 8-bit registers.
GN1L/H	Auxiliary ADC 16-bit Gain Calibration Coefficient is held in these two 8-bit registers.

ADCSTAT—(ADC Status Register)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including reference detect and conversion overflow/underflow flags.

SFR Address	D8H
Power-On Default Value	00H
Bit Addressable	Yes

Table IV. ADCSTAT SFR Bit Designations

Bit	Name	Description
7	RDY0	Ready Bit for primary ADC. Set by hardware on completion of ADC conversion or calibration cycle. Cleared directly by the user or indirectly by write to the mode bits to start another primary ADC conversion or calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for auxiliary ADC. Same definition as RDY0 referred to the auxiliary ADC.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration.
4	NOXREF	No External Reference Bit *(only active if primary or auxiliary ADC is active)*. Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When Set, conversion results are clamped to all ones, if using external reference. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all zeros or all ones. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC.
1	—	Reserved for Future Use
0	—	Reserved for Future Use

ADCMODE (ADC Mode Register)
Used to control the operational mode of both ADCs.

SFR Address	D1H
Power-On Default Value	00H
Bit Addressable	No

Table V. ADCMODE SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	—	Reserved for Future Use
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0 below. Cleared by the user to place the primary ADC in power-down mode.
4	ADC1EN	Auxiliary ADC Enable. Set by the user to enable the auxiliary ADC and place it in the mode selected in MD2–MD0 below. Cleared by the user to place the auxiliary ADC in power-down mode.
3	—	Reserved for Future Use
2	MD2	Primary and auxiliary ADC Mode bits.
1	MD1	These bits select the operational mode of the enabled ADC as follows:
0	MD0	MD2 MD1 MD0
		0 0 0 ADC Power-Down Mode (Power-On Default)
		0 0 1 Idle Mode. In Idle Mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.
		0 1 0 Single Conversion Mode. In Single Conversion Mode, a single conversion is performed on the enabled ADC. On completion of the conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/L) are updated, the relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000.
		0 1 1 Continuous Conversion. In Continuous Conversion Mode, the ADC data registers are regularly updated at the selected update rate (see SF Register).
		1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s).
		1 0 1 Internal Full-Scale Calibration Internal or External V_{REF} (as determined by XREF0 and XREF1 bits in ADC0/1CON) is automatically connected to the enabled ADC input(s) for this calibration.
		1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON Register.
		1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON Register.

NOTES
1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2–0 Bits with no change is also treated as a reset. (See exception to this in Note 3 below.)
2. If ADC0CON is written when ADC0EN = 1, or if ADC0EN is changed from 0 to 1, then both ADCs are also immediately reset. In other words, the primary ADC is given priority over the auxiliary ADC and any change requested on the primary ADC is immediately responded to.
3. On the other hand, if ADC1CON is written or if ADC1EN is changed from 0 to 1, only the auxiliary ADC is reset. For example, if the primary ADC is continuously converting when the auxiliary ADC change or enable occurs, the primary ADC continues undisturbed. Rather than allow the auxiliary ADC to operate with a phase difference from the primary ADC, the auxiliary ADC will fall into step with the outputs of the primary ADC. The result is that the first conversion time for the auxiliary ADC will be delayed up to three outputs while the auxiliary ADC update rate is synchronized to the primary ADC.
4. Once ADCMODE has been written with a calibration mode, the RDY0/1 bits (ADCSTAT) are immediately reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in ADCSTAT are written, and the MD2–0 bits are reset to 000 to indicate the ADC is back in power-down mode.
5. Any calibration request of the auxiliary ADC while the temperature sensor is selected will fail to complete. Although the RDY1 bit will be set at the end of the calibration cycle, no update of the calibration SFRs will take place and the ERR1 bit will be set.
6. Calibrations are performed at maximum SF (see SF SFR) value guaranteeing optimum calibration operation.

ADC0CON (Primary ADC Control Register) and ADC1CON (Auxiliary ADC Control Register)
The ADC0CON and ADC1CON SFRs are used to configure the primary and auxiliary ADC for reference and channel selection, unipolar or bipolar coding and, in the case of the primary ADC, for range (the auxiliary ADC operates on a fixed input range of $\pm V_{REF}$).

ADC0CON	**Primary ADC Control SFR**	**ADC1CON**	**Auxiliary ADC Control SFR**
SFR Address	D2H	SFR Address	D3H
Power-On Default Value	07H	Power-On Default Value	00H
Bit Addressable	No	Bit Addressable	No

Table VI. ADC0CON SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	XREF0	Primary ADC External Reference Select Bit. Set by user to enable the primary ADC to use the external reference via REFIN(+)/REFIN(–). Cleared by user to enable the primary ADC to use the internal band gap reference (V_{REF} = 1.25 V).
5	CH1	Primary ADC Channel Selection Bits
4	CH0	Written by the user to select the differential input pairs used by the primary ADC as follows: CH1 CH0 Positive Input Negative Input 0 0 AIN1 AIN2 0 1 AIN3 AIN4 1 0 AIN2 AIN2 (Internal Short) 1 1 AIN3 AIN2
3	UNI0	Primary ADC Unipolar Bit. Set by user to enable unipolar coding, i.e., zero differential input will result in 000000H output. Cleared by user to enable bipolar coding, i.e., zero differential input will result in 800000H output.
2	RN2	Primary ADC Range Bits.
1	RN1	Written by the user to select the primary ADC input range as follows:
0	RN0	RN2 RN1 RN0 Selected Primary ADC Input Range (V_{REF} = 2.5 V) 0 0 0 ±20 mV (0 mV–20 mV in Unipolar Mode) 0 0 1 ±40 mV (0 mV–40 mV in Unipolar Mode) 0 1 0 ±80 mV (0 mV–80 mV in Unipolar Mode) 0 1 1 ±160 mV (0 mV–160 mV in Unipolar Mode) 1 0 0 ±320 mV (0 mV–320 mV in Unipolar Mode) 1 0 1 ±640 mV (0 mV–640 mV in Unipolar Mode) 1 1 0 ±1.28 V (0 V–1.28 V in Unipolar Mode) 1 1 1 ±2.56 V (0 V–2.56 V in Unipolar Mode)

Table VII. ADC1CON SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	XREF1	Auxiliary ADC External Reference Bit. Set by user to enable the auxiliary ADC to use the external reference via REFIN(+)/REFIN(–). Cleared by user to enable the auxiliary ADC to use the internal band gap reference.
5	ACH1	Auxiliary ADC Channel Selection Bits.
4	ACH0	Written by the user to select the single-ended input pins used to drive the auxiliary ADC as follows: ACH1 ACH0 Positive Input Negative Input 0 0 AIN3 AGND 0 1 AIN4 AGND 1 0 Temp Sensor AGND (Temp Sensor routed to the ADC input) 1 1 AIN5 AGND
3	UNI1	Auxiliary ADC Unipolar Bit. Set by user to enable unipolar coding, i.e., zero input will result in 0000H output. Cleared by user to enable bipolar coding, i.e., zero input will result in 8000H output.
2	—	Reserved for Future Use
1	—	Reserved for Future Use
0	—	Reserved for Future Use

NOTES
1. When the temperature sensor is selected, user code must select internal reference via XREF1 bit above and clear the UNI1 bit (ADC1CON.3) to select bipolar coding.
2. The temperature sensor is factory calibrated to yield conversion results 8000H at 0°C.
3. A +1°C change in temperature will result in a +1 LSB change in the ADC1H Register ADC conversion result.

ADC0H/ADC0M/ADC0L (Primary ADC Conversion Result Registers)
These three 8-bit registers hold the 24-bit conversion result from the primary ADC.

SFR Address	ADC0H	High Data Byte	DBH
	ADC0M	Middle Data Byte	DAH
	ADC0L	Low Data Byte	D9H
Power-On Default Value	00H	ADC0H, ADC0M, ADC0L	
Bit Addressable	No	ADC0H, ADC0M, ADC0L	

ADC1H/ADC1L (Auxiliary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the auxiliary ADC.

SFR Address	ADC1H	High Data Byte	DDH
	ADC1L	Low Data Byte	DCH
Power-On Default Value	00H	ADC1H, ADC1L	
Bit Addressable	No	ADC1H, ADC1L	

OF0H/OF0M/OF0L (Primary ADC Offset Calibration Registers*)
These three 8-bit registers hold the 24-bit offset calibration coefficient for the primary ADC. These registers are configured at power-on with a factory default value of 800000H. However, these bytes will be automatically overwritten if an internal or system zero-scale calibration of the primary ADC is initiated by the user via MD2–0 bits in the ADCMODE Register.

SFR Address	OF0H	Primary ADC Offset Coefficient High Byte	E3H
	OF0M	Primary ADC Offset Coefficient Middle Byte	E2H
	OF0L	Primary ADC Offset Coefficient Low Byte	E1H
Power-On Default Value	800000H	OF0H, OF0M, OF0L, respectively	
Bit Addressable	No	OF0H, OF0M, OF0L	

OF1H/OF1L (Auxiliary ADC Offset Calibration Registers*)
These two 8-bit registers hold the 16-bit offset calibration coefficient for the auxiliary ADC. These registers are configured at power-on with a factory default value of 8000H. However, these bytes will be automatically overwritten if an internal or system zero-scale calibration of the auxiliary ADC is initiated by the user via the MD2–0 bits in the ADCMODE Register.

SFR Address	OF1H	Auxiliary ADC Offset Coefficient High Byte	E5H
	OF1L	Auxiliary ADC Offset Coefficient Low Byte	E4H
Power-On Default Value	8000H	OF1H and OF1L, respectively	
Bit Addressable	No	OF1H, OF1L	

GN0H/GN0M/GN0L (Primary ADC Gain Calibration Registers*)
These three 8-bit registers hold the 24-bit gain calibration coefficient for the primary ADC. These registers are configured at power-on with a factory-calculated internal full-scale calibration coefficient. Every device will have an individual coefficient. However, these bytes will be automatically overwritten if an internal or system full-scale calibration of the primary ADC is initiated by the user via MD2–0 bits in the ADCMODE Register.

SFR Address	GN0H	Primary ADC Gain Coefficient High Byte	EBH
	GN0M	Primary ADC Gain Coefficient Middle Byte	EAH
	GN0L	Primary ADC Gain Coefficient Low Byte	E9H
Power-On Default Value		Configured at Factory Final Test; see Notes above.	
Bit Addressable	No	GN0H, GN0M, GN0L	

GN1H/GN1L (Auxiliary ADC Gain Calibration Registers*)
These two 8-bit registers hold the 16-bit gain calibration coefficient for the auxiliary ADC. These registers are configured at power-on with a factory-calculated internal full-scale calibration coefficient. Every device will have an individual coefficient. However, these bytes will be automatically overwritten if an internal or system full-scale calibration of the auxiliary ADC is initiated by the user via MD2–0 bits in the ADCMODE Register.

SFR Address	GN1H	Auxiliary ADC Gain Coefficient High Byte	EDH
	GN1L	Auxiliary ADC Gain Coefficient Low Byte	ECH
Power-On Default Value		Configured at Factory Final Test; see Notes above.	
Bit Addressable	No	GN1H, GN1L	

*These registers can be overwritten by user software only if Mode bits MD0–2 (ADCMODE SFR) are zero.

SF (Sinc Filter Register)
The number in this register sets the decimation factor and thus the output update rate for the primary and auxiliary ADCs. This SFR cannot be written by user software while either ADC is active. The update rate applies to both primary and auxiliary ADCs and is calculated as follows:

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

Where: f_{ADC} = ADC Output Update Rate

f_{MOD} = Modulator Clock Frequency = 32.768 kHz

SF = Decimal Value of SF Register

The allowable range for SF is 0DH to FFH. Examples of *SF* values and corresponding conversion update rates (f_{ADC}) and conversion times (t_{ADC}) are shown in Table VIII. The power-on default value for the SF Register is 45H, resulting in a default ADC update rate of just under 20 Hz. Both ADC inputs are chopped to minimize offset errors, which means that the settling time for a single conversion, or the time to a first conversion result in Continuous Conversion mode, is 2 × t_{ADC}. As mentioned earlier, all calibration cycles will be carried out automatically with a maximum, i.e., FFH, SF value to ensure optimum calibration performance. Once a calibration cycle has completed, the value in the SF Register will be that programmed by user software.

Table VIII. SF SFR Bit Designations

SF(dec)	SF(hex)	f_{ADC}(Hz)	t_{ADC}(ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

ICON (Current Sources Control Register)
Used to control and configure the various excitation and burnout current source options available on-chip.

SFR Address D5H
Power-On Default Value 00H
Bit Addressable No

Table IX. ICON SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	BO	Burnout Current Enable Bit. Set by user to enable both transducer burnout current sources in the primary ADC signal paths. Cleared by user to disable both transducer burnout current sources.
5	ADC1IC	Auxiliary ADC Current Correction Bit. Set by user to allow scaling of the auxiliary ADC by an internal current source calibration word.
4	ADC0IC	Primary ADC Current Correction Bit. Set by user to allow scaling of the primary ADC by an internal current source calibration word.
3	I2PIN*	Current Source-2 Pin Select Bit. Set by user to enable current source-2 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1). Cleared by user to enable current source-2 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2).
2	I1PIN*	Current Source-1 Pin Select Bit. Set by user to enable current source-1 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2). Cleared by user to enable current source-1 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1).
1	I2EN	Current Source-2 Enable Bit. Set by user to turn on excitation current source-2 (200 μA). Cleared by user to turn off excitation current source-2 (200 μA).
0	I1EN	Current Source-1 Enable Bit. Set by user to turn on excitation current source-1 (200 μA). Cleared by user to turn off excitation current source-1 (200 μA).

*Both current sources can be enabled to the same external pin, yielding a 400 μA current source.

PRIMARY AND AUXILIARY ADC NOISE PERFORMANCE

Tables X, XI, and XII show the output rms noise in μV and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates on both the primary and auxiliary ADCs. The numbers are typical and are generated at a differential input voltage of 0 V. The output update rate is selected via the Sinc Filter (SF) SFR. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit.

The QuickStart Development system PC software comes complete with an ADC noise evaluation tool. This tool can be easily used with the evaluation board to see these figures from silicon.

Table X. Primary ADC, Typical Output RMS Noise (μV)
Typical Output RMS Noise vs. Input Range and Update Rate; Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table XI. Primary ADC, Peak-to-Peak Resolution (Bits)
Peak-to-Peak Resolution vs. Input Range and Update Rate; Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13.5	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	19	19.5

Typical RMS Resolution vs. Input Range and Update Rate: RMS Resolution in Bits*

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	14.7	15.7	16.7	17.7	17.7	18.2	18.7	18.7
69	19.79	16.2	16.7	17.7	18.7	19.7	20.2	20.7	21.2
255	5.35	16.7	17.7	18.7	19.7	20.7	21.2	21.7	22.2

*Based on a six-sigma limit, the rms resolution is 2.7 bits greater than the peak-to-peak resolution.

Table XII. Auxiliary ADC

Typical Output RMS Noise vs. Update Rate*
Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	10.75
69	19.79	2.00
255	5.35	1.15

*ADC converting in Bipolar mode

Peak-to-Peak Resolution vs. Update Rate[1]
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	16[2]
69	19.79	16
255	5.35	16

NOTES
[1]ADC converting in Bipolar mode
[2]In Unipolar mode, peak-to-peak resolution at 105 Hz is 15 bits.

PRIMARY AND AUXILIARY ADC CIRCUIT DESCRIPTION

Overview

The ADuC834 incorporates two independent Σ-Δ ADCs (primary and auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain gage, pressure transducer, or temperature measurement applications.

Primary ADC

This ADC is intended to convert the primary sensor input. The input is buffered and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V being driven from one of three differential input channel options AIN1/2, AIN3/4, or AIN3/2. The input channel is internally buffered, allowing the part to handle significant source impedances on the analog input and allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. On-chip burnout currents can also be turned on. These currents can be used to check that a transducer on the selected channel is still operational before attempting to take measurements.

The ADC employs a Σ-Δ conversion technique to realize up to 24 bits of no missing codes performance. The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A chopping scheme is also employed to minimize ADC offset errors. A block diagram of the primary ADC is shown in Figure 7.

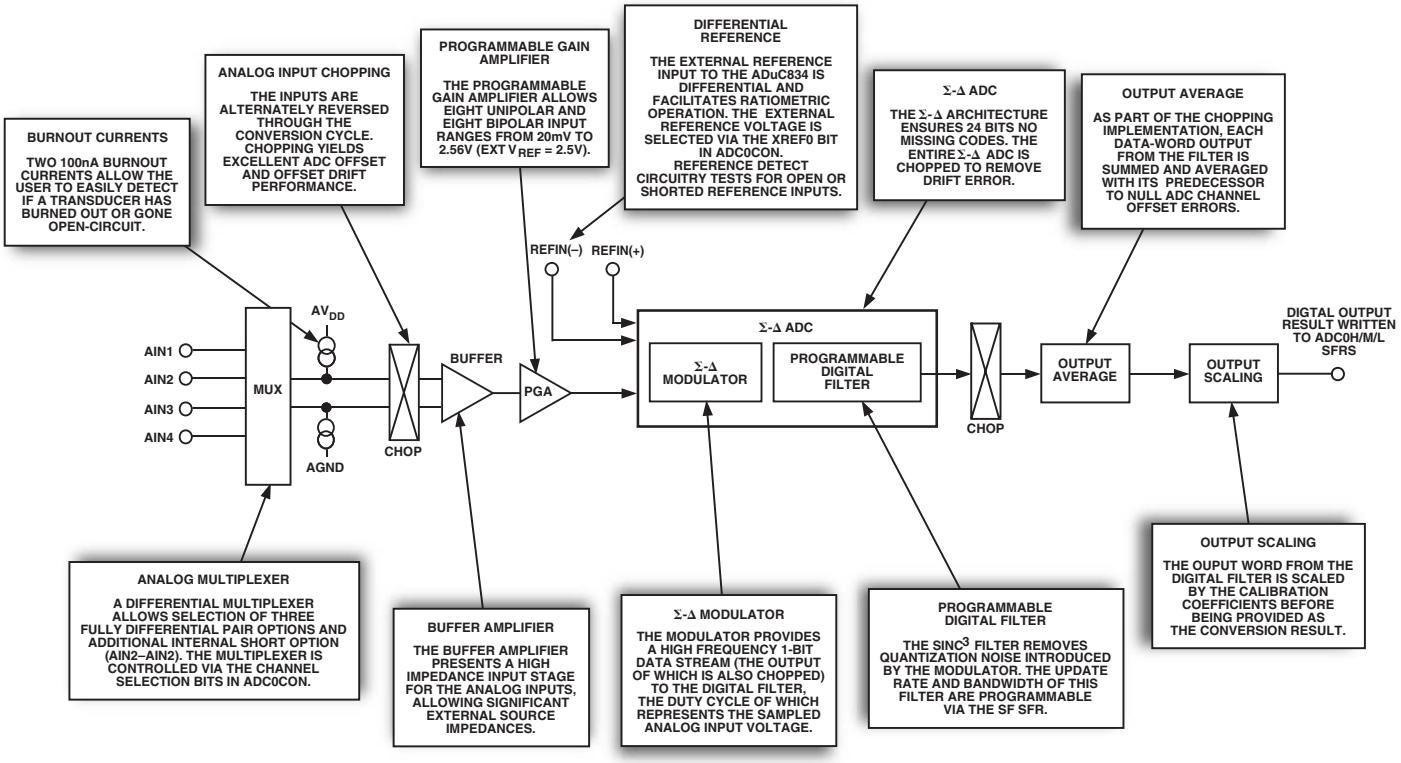


Figure 7. Primary ADC Block Diagram

Auxiliary ADC

The auxiliary ADC is intended to convert supplementary inputs such as those from a cold junction diode or thermistor. This ADC is not buffered and has a fixed input range of 0 V to 2.5 V (assuming an external 2.5 V reference). The single-ended inputs can be driven from AIN3, AIN4, or AIN5 Pins, or directly from the on-chip temperature sensor voltage. A block diagram of the auxiliary ADC is shown in Figure 8.

Analog Input Channels

The primary ADC has four associated analog input pins (labelled AIN1 to AIN4) that can be configured as two fully differential input channels. Channel selection bits in the ADC0CON SFR detailed in Table VI allow three combinations of differential pair selection as well as an additional shorted input option (AIN2–AIN2).

The auxiliary ADC has three external input pins (labelled AIN3 to AIN5) as well as an internal connection to the on-chip temperature sensor. All inputs to the auxiliary ADC are single-ended inputs referenced to the AGND on the part. Channel selection bits in the ADC1CON SFR previously detailed in Table VII allow selection of one of four inputs.

Two input multiplexers switch the selected input channel to the on-chip buffer amplifier in the case of the primary ADC and directly to the Σ-Δ modulator input in the case of the auxiliary ADC. When the analog input channel is switched, the settling time of the part must elapse before a new valid word is available from the ADC.

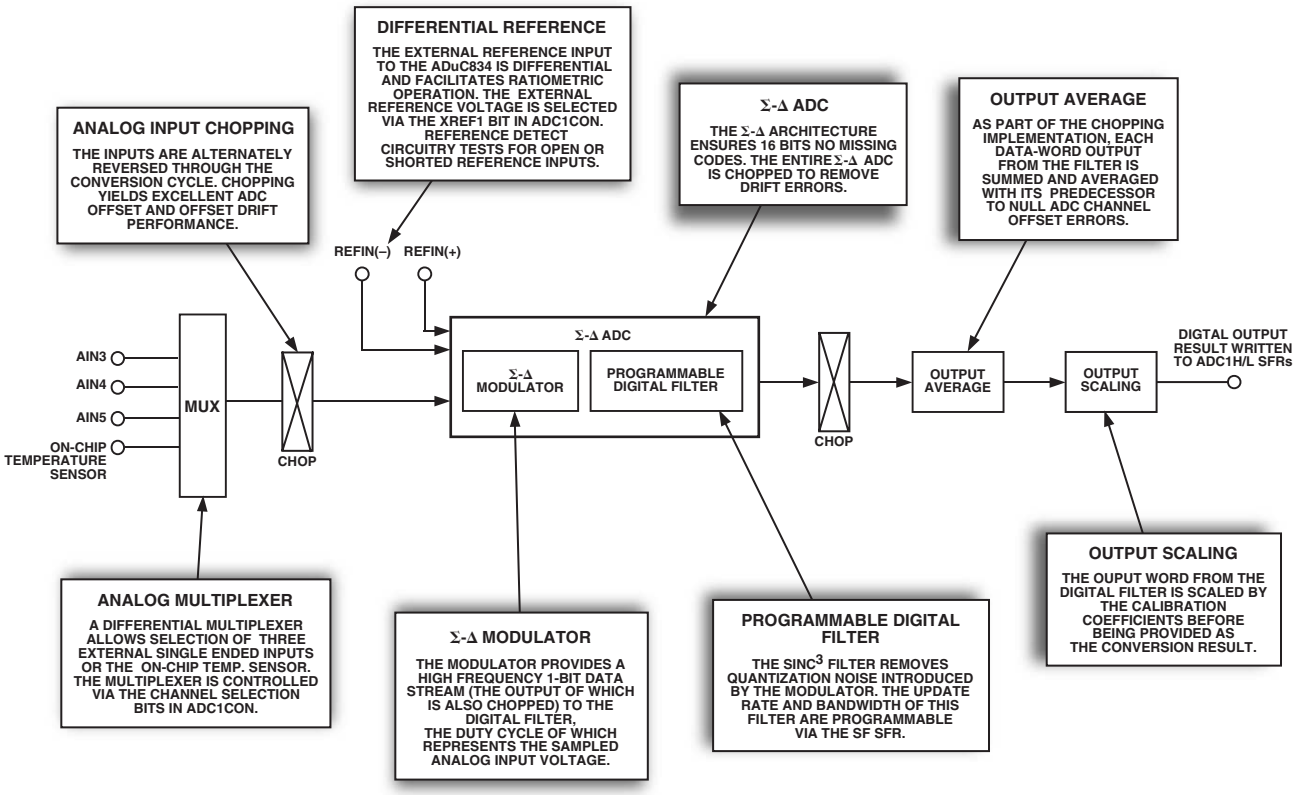


Figure 8. Auxiliary ADC Block Diagram