Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management

Data Sheet

ADuCM4050

FEATURES

- EEMBC ULPMark™-CP score (3 V): 189
- Ultra low power active and hibernate modes
- Active mode dynamic current: 41 µA/MHz (typical)
- Flexi mode: 400 µA (typical)
- Hibernate mode: 0.65 µA (typical)
- Shutdown mode: 50 nA (typical)
- Shutdown mode (fast wake-up): 0.20 µA (typical)
- ARM Cortex-M4F processor at 52 MHz with FPU, MPU, ITM with SWD interface
- Power management
- Single-supply operation (connected to VBAT pins): 1.74 V to 3.6 V
- Optional buck converter for improved efficiency
- Memory options
- 512 kB of embedded flash memory with ECC
- 4 kB of cache memory to reduce active power
- 128 kB of configurable system SRAM with parity
- Safety
  - Watchdog with dedicated on-chip oscillator
  - Hardware CRC with programmable polynomial
  - Multiparity bit protected SRAM
  - ECC protected embedded flash
- Security
  - Hardware cryptographic accelerator supporting AES-128, AES-256, and SHA-256
  - Protected key storage in flash, SHA-256-based keyed HMAC and key wrap and unwrap
  - User code protection
  - TRNG
- Digital peripherals
  - 3 SPI interfaces to enable glueless interface to sensors, radios, and converters
  - 1 I^2C and 2 UART peripheral interfaces
  - SPORT for natively interfacing with converters and radios
  - Programmable GPIOs (44 in LFCSP and 51 in WLCSP)
  - 3 general-purpose timers with PWM support
  - RGB timer for driving RGB LED
  - RTC0 for time keeping
  - RTC1 with SensorStrobe and time stamping
  - Programmable beeper
  - 27-channel DMA controller
- Clocking features
  - 26 MHz clock: on-chip oscillator, external crystal oscillator, SYS_CLKIN for external clock, and integrated PLL
  - 32 kHz clock: on-chip oscillator and low power crystal oscillator
  - Clock fail detection for external crystals
- Analog peripherals
  - 12-bit SAR ADC, 1.8 MSPS, 8 channels, and digital comparator

APPLICATIONS

- Internet of Things (IoT)
- Smart agriculture, smart building, smart metering, smart city, smart machine, and sensor network
- Wearables
- Fitness and clinical
- Machine learning and neural networks

FUNCTIONAL BLOCK DIAGRAM

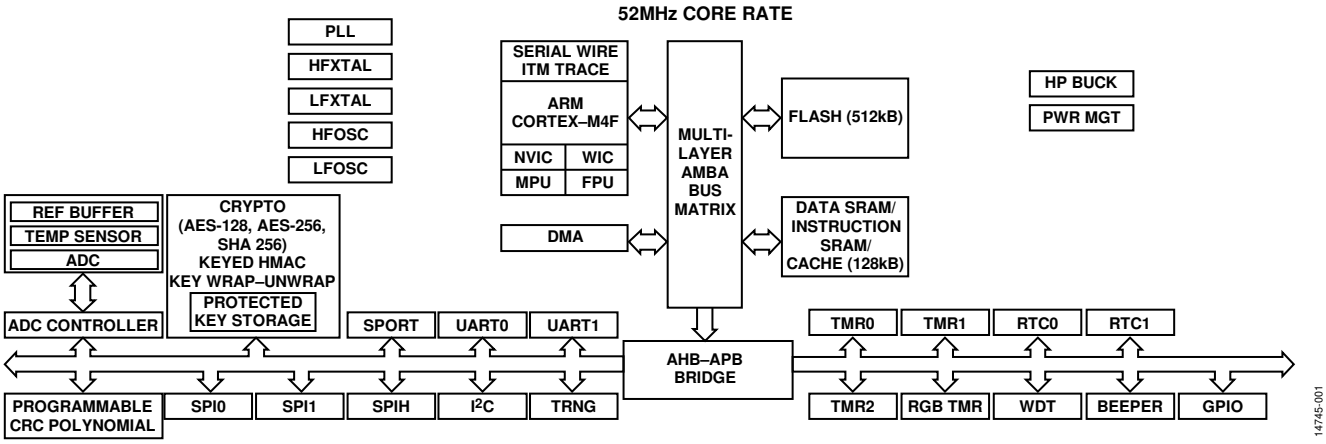

Figure 1.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM4050 microcontroller unit (MCU) is an ultra low power integrated microcontroller system with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM® Cortex®-M4F processor. The MCU also has a collection of digital peripherals, embedded static random access memory (SRAM) and embedded flash memory, and an analog subsystem that provides clocking, reset, and power management capabilities in addition to an analog-to-digital converter (ADC) subsystem.

This data sheet describes the ARM Cortex-M4F core and memory architecture used on the ADuCM4050 MCU. It does not provide detailed programming information about the ARM processor.

The system features include an up to 52 MHz ARM Cortex-M4F processor, 512 kB of embedded flash memory with error correction code (ECC), an optional 4 kB cache for lower active power, and 128 kB system SRAM with parity. The ADuCM4050 features a power management unit (PMU), multilayer advanced microcontroller bus architecture (AMBA) bus matrix, central direct memory access (DMA) controller, and beeper interface.

The ADuCM4050 features cryptographic hardware supporting advanced encryption standard (AES)-128 and AES-256 with secure hash algorithm (SHA)-256 and the following modes: electronic code book (ECB), cipher block chaining (CBC), counter (CTR), and cipher block chaining-message authentication code (CCM/CCM*) modes.

The ADuCM4050 has protected key storage with key wrap/unwrap, and keyed hashed message authentication code (HMAC) with key unwrap.

The ADuCM4050 supports serial port (SPORT), serial peripheral interface (SPI), I^2C, and universal asynchronous receiver/transmitter (UART) peripheral interfaces.

The ADuCM4050 features a real-time clock (RTC), general-purpose and watchdog timers, and programmable general-purpose input/output (GPIO) pins. There is a hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial. The device also features a power on reset (POR) and power supply monitor (PSM), a 12-bit successive approximation register (SAR) ADC, a red/green/blue (RGB) timer for driving RGB LED, and a true random number generator (TRNG).

To support low dynamic and hibernate power management, the ADuCM4050 MCU provides a collection of power modes and features such as dynamic- and software-controlled clock gating and power gating.

For full details on the ADuCM4050 MCU, refer to the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.

PRODUCT HIGHLIGHTS

1. Ultra low power consumption.
2. Robust operation.
3. Full voltage monitoring in deep sleep modes.
4. ECC support on flash.
5. Parity error detection on SRAM memory.
6. Leading edge security.
7. Fast encryption provides read protection to user algorithms.
8. Write protection prevents device reprogramming by unauthorized code.
9. Failure detection of 32 kHz low frequency external crystal oscillator (LFXTAL) via interrupt.
10. SensorStrobe™ for precise time synchronized sampling of external sensors. Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer. Software intervention is not required after setup. No pulse drift due to software execution.

SPECIFICATIONS

OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL BATTERY SUPPLY VOLTAGE[1, 2]	V_{BAT}	1.74	3.0	3.6	V	
INPUT VOLTAGE						
High Level	V_{IH}	2.5			V	V_{BAT} = 3.6 V
Low Level	V_{IL}			0.45	V	V_{BAT} = 1.74 V
ADC SUPPLY VOLTAGE	V_{BAT_ADC}	1.74	3.0	3.6	V	
OUTPUT VOLTAGE[3]						
High Level	V_{OH}	1.4			V	V_{BAT} = 1.74 V, I_{OH} = −1.0 mA
Low Level	V_{OL}			0.4	V	V_{BAT} = 1.74 V, I_{OL} = 1.0 mA
INPUT CURRENT PULL-UP[4]						
High Level	I_{IHPU}		0.01	0.2	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level	I_{ILPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
THREE-STATE LEAKAGE CURRENT						
High Level[5]	I_{OZH}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Up[6]	I_{OZHPU}			0.30	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Down[7]	I_{OZHPD}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level[5]	I_{OZL}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Up[6]	I_{OZLPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Down[7]	I_{OZLPD}			0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
INPUT CAPACITANCE	C_{IN}		10		pF	T_J = 25°C
V_{BAT} POWER-ON RESET	V_{VBAT_POR}	1.49	1.59	1.64	V	Power-on reset level on V_{BAT}; trip point is detected when battery is decaying[8]
Junction Temperature	T_J	−40		+85	°C	$T_{AMBIENT}$ = −40°C to +85°C

[1] Value applies to VBAT_ANA1, VBAT_ANA2, VBAT_DIG1, and VBAT_DIG2 pins.
[2] Must remain powered (even if the associated function is not used).
[3] Applies to the output and bidirectional pins: P0_00 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[4] Applies to the $\overline{\text{SYS\_HWRST}}$ input pin with pull-up.
[5] Applies to the three-state pins: P0_00 to P0_05, P0_08 to P0_15, P1_00 to P1_15, P2_00 to P2_15, P3_00 to P3_03.
[6] Applies to the three-state pins with pull-ups: P0_00 to P0_05, P0_07 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[7] Applies to the P0_06 three-state pin with pull-down.
[8] This specification is valid when the device is powered up; if the battery decays and falls below 1.71 V, power-on reset is detected. For safer operation of the device, adhere to the V_{BAT} specification.

EMBEDDED FLASH SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH						
Endurance		10,000			Cycles	
Data Retention			10		Years	

POWER SUPPLY CURRENT SPECIFICATIONS

Active Mode

Table 3.

Parameter	Min	Typ[1]	Max[2]	Unit	Test Conditions/Comments
ACTIVE MODE[3]					Current consumption when V_{BAT} = 3.0 V
Buck Enabled		1.27	2.71	mA	Code executing from flash, cache enabled, system peripheral clock (PCLK) disabled, advanced high performance clock (HCLK) = 26 MHz[4]
		1.83	3.28	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz[4]
		1.40	2.84	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		1.97	3.41	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		2.33	3.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz[5]
		2.94	4.39	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz[5]
		2.59	4.04	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		3.21	4.65	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		1.43	2.87	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz[4]
		1.56	3.00	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz[4]
		2.64	4.09	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz[5]
		2.90	4.35	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz[5]
Dynamic Current		41		µA/MHz	Code executing from flash, cache enabled
Buck Disabled		2.34	4.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 26 MHz[4]
		3.38	5.82	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz[4]
		2.60	5.04	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		3.65	6.09	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		4.46	6.90	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz[5]
		5.61	8.05	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz[5]
		4.98	7.42	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		6.14	8.58	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		2.66	5.10	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz[4]
		2.92	5.36	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz[4]
		5.08	7.52	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz[5]
		5.60	8.04	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz[5]
Dynamic Current		82		µA/MHz	Code executing from flash, cache enabled

[1] T_J = 25°C
[2] T_J = 85°C
[3] The code being executed is a prime number generation in a continuous loop, with high frequency RC oscillator (HFOSC) as the system clock source.
[4] Zero wait states and low buck load.
[5] One wait state and high buck load.

Flexi Mode

Table 4.

Parameter	Min	Typ[1]	Max[2]	Unit	Test Conditions/Comments
FLEXI™ MODE					Current consumption when V_{BAT} = 3.0 V
Buck Enabled		0.40	1.85	mA	PCLK disabled, HCLK = 26 MHz
		0.54	1.98	mA	PCLK = 26 MHz, HCLK = 26 MHz
		0.62	2.06	mA	PCLK disabled, HCLK = 52 MHz
		0.88	2.33	mA	PCLK = 52 MHz, HCLK = 52 MHz
Buck Disabled		0.62	3.06	mA	PCLK disabled, HCLK = 26 MHz
		0.88	3.32	mA	PCLK = 26 MHz, HCLK = 26 MHz
		1.04	3.48	mA	PCLK disabled, HCLK = 52 MHz
		1.57	4.01	mA	PCLK = 52 MHz, HCLK = 52 MHz

[1] T_J = 25°C.
[2] T_J = 85°C.

Deep Sleep Modes—V_{BAT} = 1.8 V

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIBERNATE MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.78		µA	Real-Time Clock 1 (RTC1) and Real-Time Clock 0 (RTC0) disabled, 16 kB SRAM retained, LFXTAL off
		0.89		µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		0.96		µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		1.06		µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		1.35		µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		1.44		µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		1.51		µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		1.60		µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		0.85		µA	RTC1 enabled, 16 kB SRAM retained, low frequency RC oscillator (LFOSC) as RTC1 source
		1.66		µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		1.08		µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		1.11		µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		1.14		µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		1.82		µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		1.84		µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		1.87		µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
T_J = 85°C		2.79	6.90	µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		3.46	9.00	µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		4.73	12.50	µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		5.38	14.80	µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		6.26	16.70	µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		6.85	18.70	µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		8.12	22.30	µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		8.74	24.50	µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		2.95	7.30	µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		8.92	25.50	µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		3.16	7.77	µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		3.16	7.78	µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		3.22	7.92	µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		9.07	25.70	µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		9.10	25.76	µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		9.15	25.91	µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
SHUTDOWN MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.03		µA	RTC0 disabled
		0.37		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.31	1.30	µA	RTC0 disabled
		0.78	2.93	µA	RTC0 enabled, LFXTAL as RTC0 source
FAST SHUTDOWN MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.17		µA	RTC0 disabled
		0.51		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.47	1.50	µA	RTC0 disabled
		0.94	3.53	µA	RTC0 enabled, LFXTAL as RTC0 source

[1] Buck enable/disable does not affect power consumption.

Deep Sleep Modes—V_{BAT} = 3.0 V

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIBERNATE MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.65		µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		0.72		µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		0.77		µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		0.83		µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		1.09		µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		1.13		µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		1.17		µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		1.22		µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		0.68		µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		1.26		µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		0.87		µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		0.95		µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		0.97		µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		1.38		µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		1.46		µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		1.48		µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
T_J = 85°C		2.00	4.60	µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		2.38	5.70	µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		2.98	7.80	µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		3.29	9.00	µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		4.04	10.06	µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		4.41	11.80	µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		4.94	13.70	µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		5.20	15.50	µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		2.11	5.00	µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		5.32	16.00	µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		2.53	5.75	µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		2.61	5.92	µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		2.64	5.98	µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		6.03	16.12	µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		6.10	16.30	µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		6.12	16.37	µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
SHUTDOWN MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.05		µA	RTC0 disabled
		0.68		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.45	1.60	µA	RTC0 disabled
		1.26	4.18	µA	RTC0 enabled, LFXTAL as RTC0 source
FAST SHUTDOWN MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.20		µA	RTC0 disabled
		0.83		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.62	1.80	µA	RTC0 disabled
		1.43	4.74	µA	RTC0 enabled, LFXTAL as RTC0 source

[1] Buck enable/disable does not affect power consumption.

Deep Sleep Modes—V_{BAT} = 3.6 V

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIBERNATE MODE[1]					V_{BAT} = 3.6 V
T_J = 25°C		0.66		µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		0.73		µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		0.77		µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		0.82		µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		1.04		µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		1.08		µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		1.12		µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		1.16		µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		0.69		µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		1.19		µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		0.85		µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		0.96		µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		0.98		µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		1.32		µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		1.43		µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		1.45		µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
T_J = 85°C		1.95	5.00	µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		2.29	6.00	µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		2.82	7.20	µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		3.14	8.20	µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		3.78	10.00	µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		4.10	11.00	µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		4.63	12.30	µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		4.95	14.90	µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		2.07	5.30	µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		5.06	15.20	µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		2.52	6.19	µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		2.63	6.48	µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		2.65	6.53	µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		5.51	15.34	µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		5.62	15.64	µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		5.64	15.71	µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
SHUTDOWN MODE[1]					V_{BAT} = 3.6 V
T_J = 25°C		0.07		µA	RTC0 disabled
		1.05		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.58	1.90	µA	RTC0 disabled
		1.79	5.57	µA	RTC0 enabled, LFXTAL as RTC0 source
FAST SHUTDOWN MODE[1]					V_{BAT} = 3.6 V
T_J = 25°C		0.22		µA	RTC0 disabled
		1.21		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.75	2.10	µA	RTC0 disabled
		1.97	6.32	µA	RTC0 enabled, LFXTAL as RTC0 source

[1] Buck enable/disable does not affect power consumption.

ADC SPECIFICATIONS

Table 8.

Parameter[1, 2]	Min	Typ[3]	Max	Unit	Test Conditions/Comments
INTEGRAL NONLINEARITY ERROR					
64-Lead LFCSP		±1.6		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF}) [4]
64-Lead LFCSP		−1.7 to +1.3		LSB	3.0 V (V_{BAT})/2.5 V (internal/external V_{REF})[4]
72-Ball WLCSP		±1.4		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
DIFFERENTIAL NONLINEARITY ERROR					
64-Lead LFCSP		−0.7 to +1.15		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
64-Lead LFCSP		−0.7 to +1.1		LSB	3.0 V (V_{BAT})/2.5 V (internal/external V_{REF})[4]
72-Ball WLCSP		−0.75 to +1.0		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
OFFSET ERROR					
64-Lead LFCSP		±0.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
64-Lead LFCSP		±0.5		LSB	3.0 V (V_{BAT})/2.5 V (external V_{REF})[4]
72-Ball WLCSP		±0.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
GAIN ERROR					
64-Lead LFCSP		±2.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
64-Lead LFCSP		±0.5		LSB	3.0 V (V_{BAT})/2.5 V (external V_{REF})[4]
72-Ball WLCSP		±3.0		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
I V_{BAT_ADC}[5]					
64-Lead LFCSP		129		µA	1.8 V (V_{BAT})/1.25 V (internal V_{REF})[6]
64-Lead LFCSP		157		µA	3.0 V (V_{BAT})/2.5 V (internal V_{REF})[6]
72-Ball WLCSP		124		µA	1.8 V (V_{BAT})/1.25 V (internal V_{REF}) [6]
64-Lead LFCSP		47		µA	1.8 V (V_{BAT})/1.25 V (external V_{REF})[7]
64-Lead LFCSP		51		µA	3.0 V (V_{BAT})/2.5 V (external V_{REF})[7]
72-Ball WLCSP		46		µA	1.8 V (V_{BAT})/1.25 V (external V_{REF}) [7]
INTERNAL REFERENCE VOLTAGE		1.25		V	Internal reference, 1.25 V selected
		2.50		V	Internal reference, 2.5 V selected
ADC SAMPLING FREQUENCY (f_S)[8]	0.01		1.8	MSPS	

[1] The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.
[2] The specifications are characterized after performing internal ADC offset calibration.
[3] T_J = 25°C.
[4] f_{IN} = 1068 Hz, f_S = 100 kSPS, internal reference in low power mode, 400,000 samples end point method used.
[5] Current consumption from VBAT_ADC supply when ADC is performing the conversion.
[6] f_{IN} = 1068 Hz, f_S = 100 kSPS, internal reference in low power mode.
[7] f_{IN} = 1068 Hz, f_S = 100 kSPS, sine wave with 1.25 V p-p applied at ADC0_VIN1 channel input.
[8] Effects of analog source impedance must be considered when selecting ADC sampling frequency.

TEMPERATURE SENSOR SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					Internal reference = 1.25 V with C_{LOAD} = 0.1 µF and 4.7 µF on the VREFP_ADC pin
Accuracy		±2		°C	$T_{AMBIENT}$ = 25°C to +5°C
		±3		°C	$T_{AMBIENT}$ = −40°C to +85°C

SYSTEM CLOCKS

External Crystal Oscillator Specifications

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)						
Frequency	f_{LFXTAL}		32,768		Hz	
External Capacitance from SYS_LFXTAL_IN Pin to Ground and from SYS_LFXTAL_OUT Pin to Ground	C_{LFXTAL}	6		10	pF	External capacitors on SYS_LFXTAL_IN and SYS_LFXTAL_OUT pins must be selected considering the printed circuit board (PCB) trace capacitance due to routing
Crystal Equivalent Series Resistance	ESR_{LFXTAL}	30		50	kΩ	
Crystal Drive Level[1]				50	nW	
Oscillator Transconductance[1]	gm_{LFXTAL}	8			µS	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)						
Frequency	f_{HFXTAL}		26		MHz	
External Capacitance from SYS_HFXTAL_IN Pin to Ground and from SYS_HFXTAL_OUT Pin to Ground	C_{HFXTAL}			20	pF	External capacitors on SYS_HFXTAL_IN and SYS_HFXTAL_OUT pins must be selected considering the PCB trace capacitance due to routing
Crystal Equivalent Series Resistance	ESR_{HFXTAL}			50	kΩ	

[1] Guaranteed by design.

On-Chip Resistor-Capacitor (RC) Oscillator Specifications

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	f_{LFOSC}	30,800	32,768	35,062	Hz
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	f_{HFOSC}	25.03	26	27.07	MHz

System Clocks and Phase-Locked Loop (PLL) Specifications

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit
PLL SPECIFICATIONS					
PLL Input Clock Frequency[1]	f_{PLLIN}	16		26	MHz
PLL Output Clock Frequency[2, 3]	f_{PLLOUT}	16		60	MHz
System Peripheral Clock (PCLK) Frequency	f_{PCLK}	0.8125		52	MHz
Advanced High Performance Bus Clock (HCLK) Frequency	f_{HCLK}	0.8125		52	MHz

[1] The input to the PLL can come from either the high frequency external crystal (HFXTAL), SYS_CLKIN pin or from the high frequency internal RC oscillator (HFOSC).
[2] For the maximum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 16, PLL DIV2 = 1 for PLL input clock = 26 MHz; and PLL MSEL = 13, PLL NSEL = 26, PLL DIV2 = 1 for PLL input clock = 16 MHz; see the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference for more information on these configuration options.
[3] For the minimum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 30, PLL DIV2 = 0 for PLL input clock = 26 MHz; and PLL MSEL = 8, PLL NSEL = 30, PLL DIV2 = 0 for 16 MHz.

TIMING SPECIFICATIONS

Reset Timing

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit
RESET TIMING REQUIREMENTS					
$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low[1]	t_{WRST}	4			µs

[1] Applies after power-up sequence is complete.

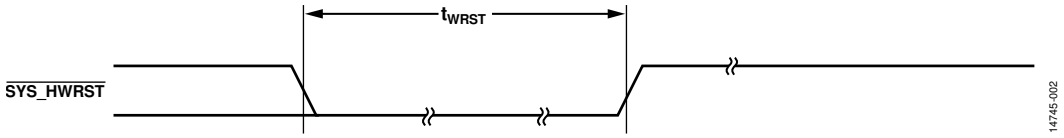

Figure 2. Reset Timing

Serial Ports Timing

Table 14.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL CLOCK SERIAL PORTS						
Timing Requirements						
Frame Sync Setup Before-SPORT Clock[1]	t_{SFSE}	5			ns	Externally generated frame sync in transmit or receive mode
Frame Sync Hold After SPORT Clock[1]	t_{HFSE}	5			ns	Externally generated frame sync in transmit or receive mode
Receive Data Setup Before Receive SPORT Clock[1]	t_{SDRE}	5			ns	
Receive Data Hold After SPORT Clock[1]	t_{HDRE}	8			ns	
SPORT Clock Width[2]	t_{SCLKW}	38.5			ns	
SPORT Clock Period[2]	t_{SPTCLK}	77			ns	
Switching Characteristics[3]						
Frame Sync Delay After SPORT Clock	t_{DFSE}			20	ns	Internally generated frame sync in transmit or receive mode
Frame Sync Hold After SPORT Clock	t_{HOFSE}	2			ns	Internally generated frame sync in transmit or receive mode
Transmit Data Delay After Transmit SPORT Clock	t_{DDTE}			20	ns	
Transmit Data Hold After Transmit SPORT Clock	t_{HDTE}	1			ns	
INTERNAL CLOCK SERIAL PORTS						
Timing Requirements[1]						
Receive Data Setup Before SPORT Clock	t_{SDRI}	25			ns	
Receive Data Hold After SPORT Clock	t_{HDRI}	0			ns	
Switching Characteristics						
Frame Sync Delay After SPORT Clock[3]	t_{DFSI}			20	ns	Internally generated frame sync in transmit or receive mode
Frame Sync Hold After SPORT Clock[3]	t_{HOFSI}	−8			ns	Internally generated frame sync in transmit or receive mode
Transmit Data Delay After SPORT Clock[3]	t_{DDTI}			20	ns	
Transmit Data Hold After SPORT Clock[3]	t_{HDTI}	−7			ns	
SPORT Clock Width	t_{SCLKIW}	$t_{PCLK} - 1.5$			ns	
SPORT Clock Period	t_{SPTCLK}	$(2 \times t_{PLCK}) - 1$			ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ENABLE AND THREE-STATE SERIAL PORTS						
Switching Characteristics						
Data Enable from Internal Transmit SPORT Clock[3]	t_{DDTIN}	5			ns	
Data Disable from Internal Transmit SPORT Clock[3]	t_{DDTTI}			160	ns	

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPORT Clock.
[3] These specifications are referenced to the drive edge.

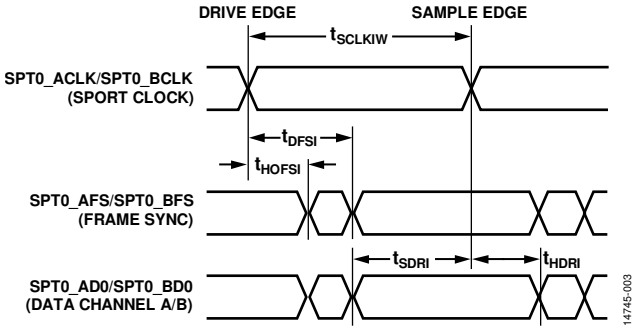

Figure 3. Serial Ports (Data Receive Mode through Internal Clock)

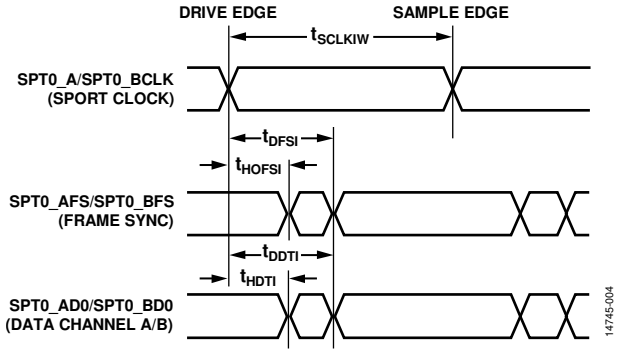

Figure 4. Serial Ports (Data Transmit Mode through Internal Clock)

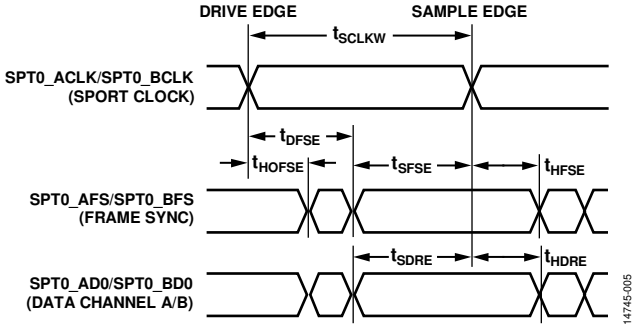

Figure 5. Serial Ports (Data Receive Mode through External Clock)

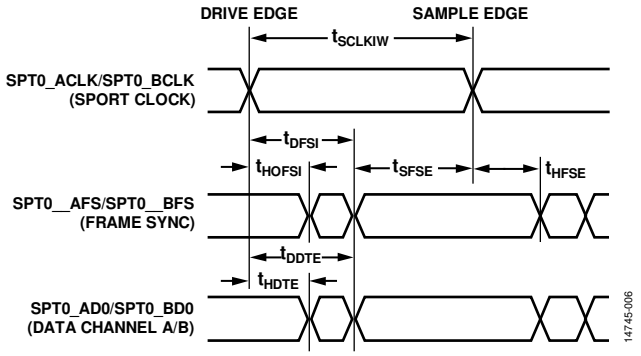

Figure 6. Serial Ports (Data Transmit Mode through External Clock)

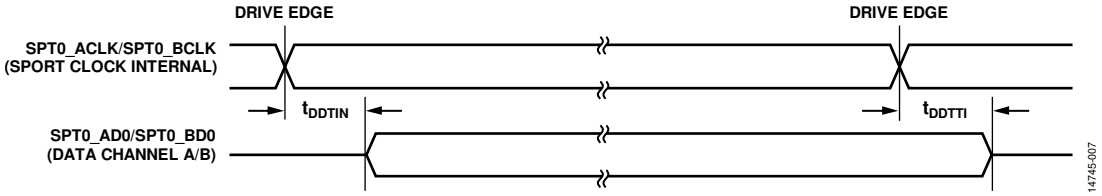

Figure 7. Enable and Three-State Serial Ports

SPI Timing

Table 15.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SPI MASTER MODE TIMING					
Timing Requirements					
Chip Select (CS) to Serial Clock (SCLK) Edge	t_{CS}	$(2 \times t_{PCLK}) - 6.5$			ns
SCLK Low Pulse Width	t_{SL}	$t_{PCLK} - 3.5$			ns
SCLK High Pulse Width	t_{SH}	$t_{PCLK} - 3.5$			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	5			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	20			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			25	ns
Data Output Setup Before SCLK Edge	t_{DOSU}	$t_{PCLK} - 2.2$			ns
CS High After SCLK Edge	t_{SFS}	$t_{PCLK} + 2$			ns
High Speed SPI (SPIH) MASTER MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	$(2 \times t_{PCLK}) - 6.5$			ns
SCLK Low Pulse Width	t_{SL}	$t_{PCLK} - 2$			ns
SCLK High Pulse Width	t_{SH}	$t_{PCLK} - 2$			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	3.5			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	12			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			12.5	ns
Data Output Setup Before SCLK Edge	t_{DOSU}	$t_{PCLK} - 2.2$			ns
CS High After SCLK Edge	t_{SFS}	$t_{PCLK} + 2$			ns
SPI SLAVE MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	38.5			ns
SCLK Low Pulse Width	t_{SL}	38.5			ns
SCLK High Pulse Width	t_{SH}	38.5			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	6			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	8			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			20	ns
Data Output Valid After CS Edge	t_{DOCS}			20	ns
CS High After SCLK Edge	t_{SFS}	38.5			ns
SPIH SLAVE MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	19.23			ns
SCLK Low Pulse Width	t_{SL}	19.23			ns
SCLK High Pulse Width	t_{SH}	19.23			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	1			
Data Input Hold Time After SCLK Edge	t_{DHD}	1			
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			15	ns
Data Output Valid After CS Edge	t_{DOCS}			15	ns
CS High After SCLK Edge	t_{SFS}	19.23			ns

[1] These specifications are characterized with respect to double drive strength.

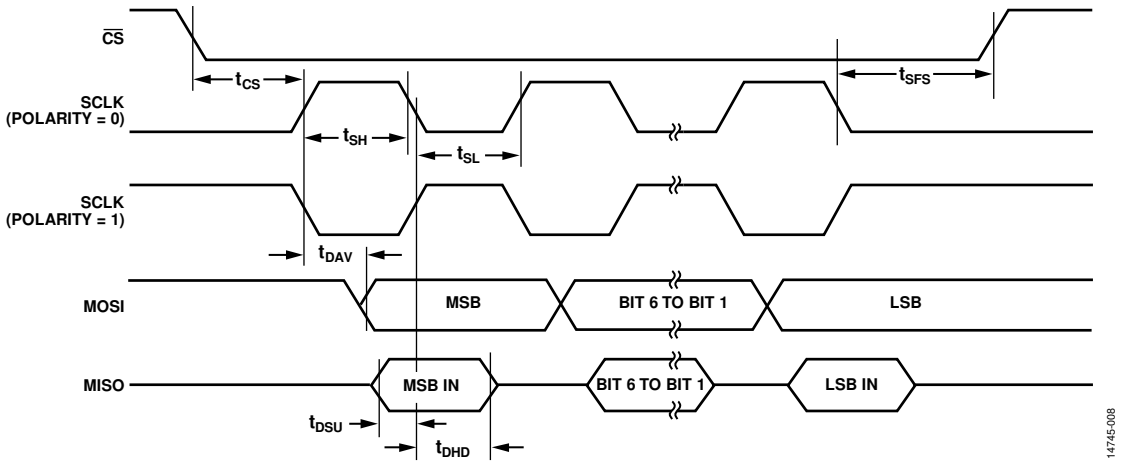

Figure 8. SPI Master Mode Timing (Phase Mode = 1)

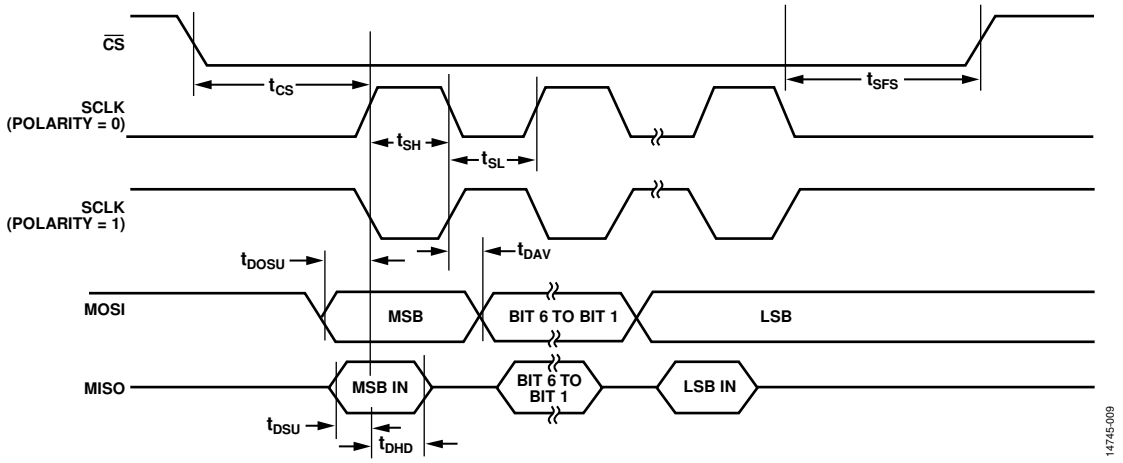

Figure 9. SPI Master Mode Timing (Phase Mode = 0)

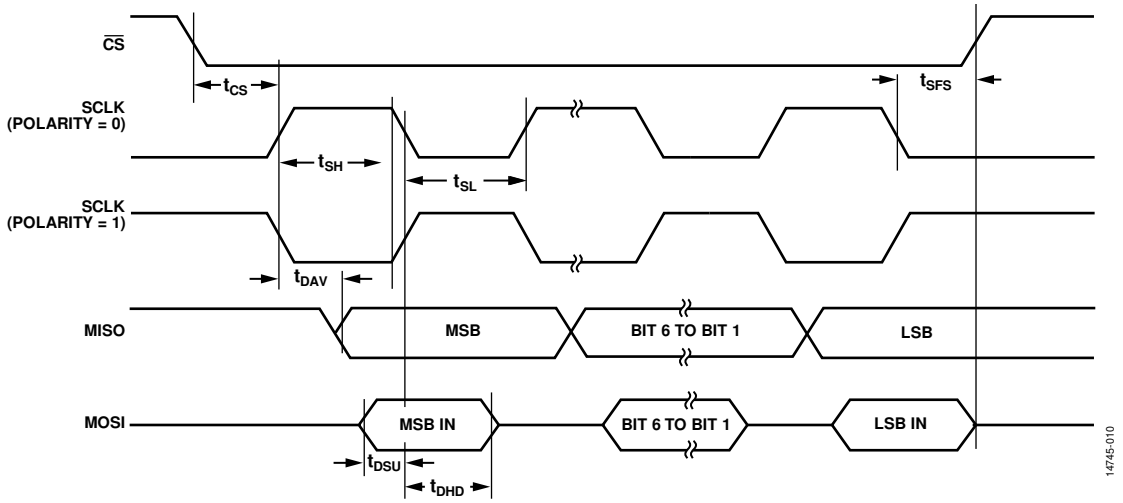

Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

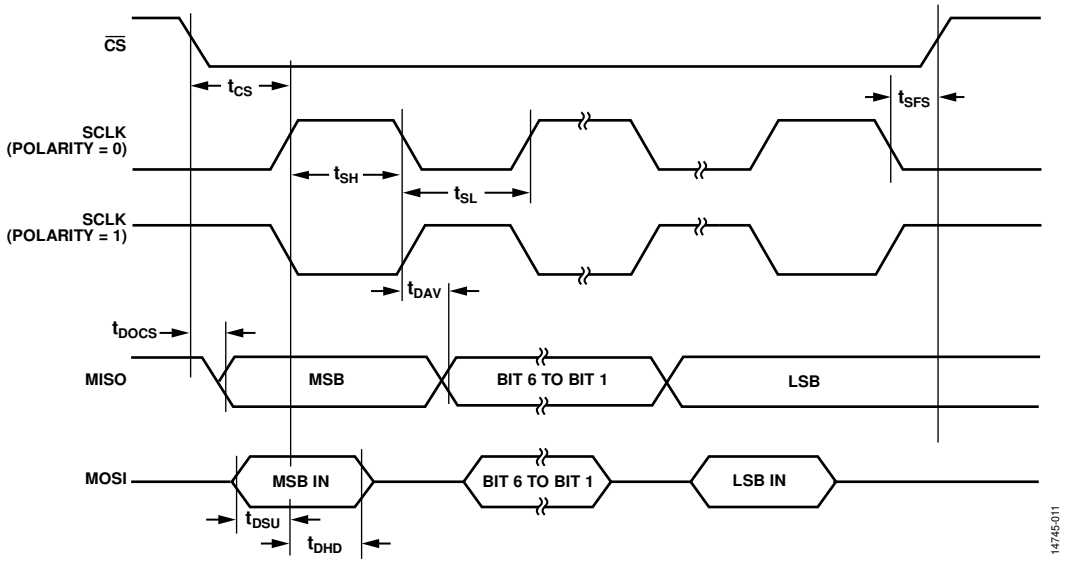

Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

I²C Specifications

Table 16.

Parameter	Symbol	Min	Typ	Max	Unit
I²C SCLK FREQUENCY					
Standard Mode			100		kHz
Fast Mode			400		kHz

General-Purpose Port Timing

Table 17.

Parameter	Symbol	Min	Typ	Max	Unit
TIMING REQUIREMENTS					
General-Purpose Port Pin Input Pulse Width	t_{WFI}	$4 \times t_{PCLK}$			ns

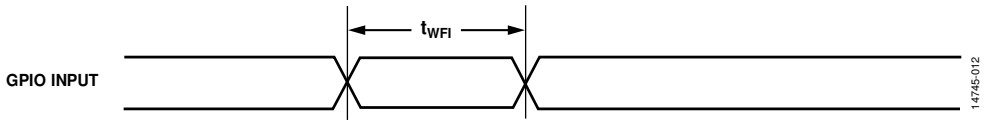

Figure 12. General-Purpose Timing

RTC1 (FLEX_RTC) Specifications

Table 18.

Parameter	Symbol	Min	Typ	Max	Unit
SensorStrobe					
Minimum Output Frequency			0.5		Hz
Maximum Output Frequency			16.384		kHz
RTC1 ALARM					
Minimum Time Resolution			30.52		µs

Timer Pulse-Width Modulation (PWM) Output Cycle Timing

Table 19.

Parameter	Symbol	Min	Typ	Max	Unit
SWITCHING REQUIREMENTS					
Timer Pulse Width Modulation Output	t_{PWMO}	$(4 \times t_{PCLK}) - 6$		$256 \times (216 - 1)$	ns

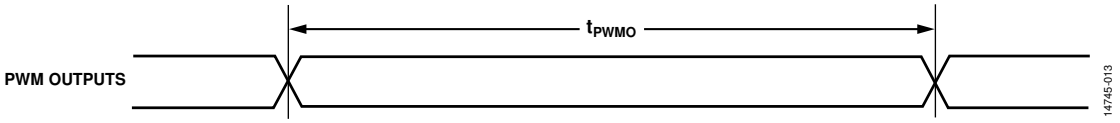

Figure 13. Timer PWM Output Cycle Timing

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
Supply	
VBAT_ANA1, VBAT_ANA2, VBAT_ADC, VBAT_DIG1, VBAT_DIG2, and VREFP_ADC	−0.3 V to +3.6 V
Analog	
VDCDC_CAP1N, VDCDC_CAP1P, VDCDC_OUT, VDCDC_CAP2N, and VDCDC_CAP2P	−0.3 V to +3.6 V
VLDO_OUT, SYS_HFXTAL_IN, SYS_HFXTAL_OUT, SYS_LFXTAL_IN, and SYS_LFXTAL_OUT	−0.3 V to +1.32 V
Digital Input/Output	
P0_xx, P1_xx, P2_xx, P3_xx, and $\overline{\text{SYS\_HWRST}}$	−0.3 V to +3.6 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (to calculate power dissipation.

Table 21. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-64-17	26.3	1.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

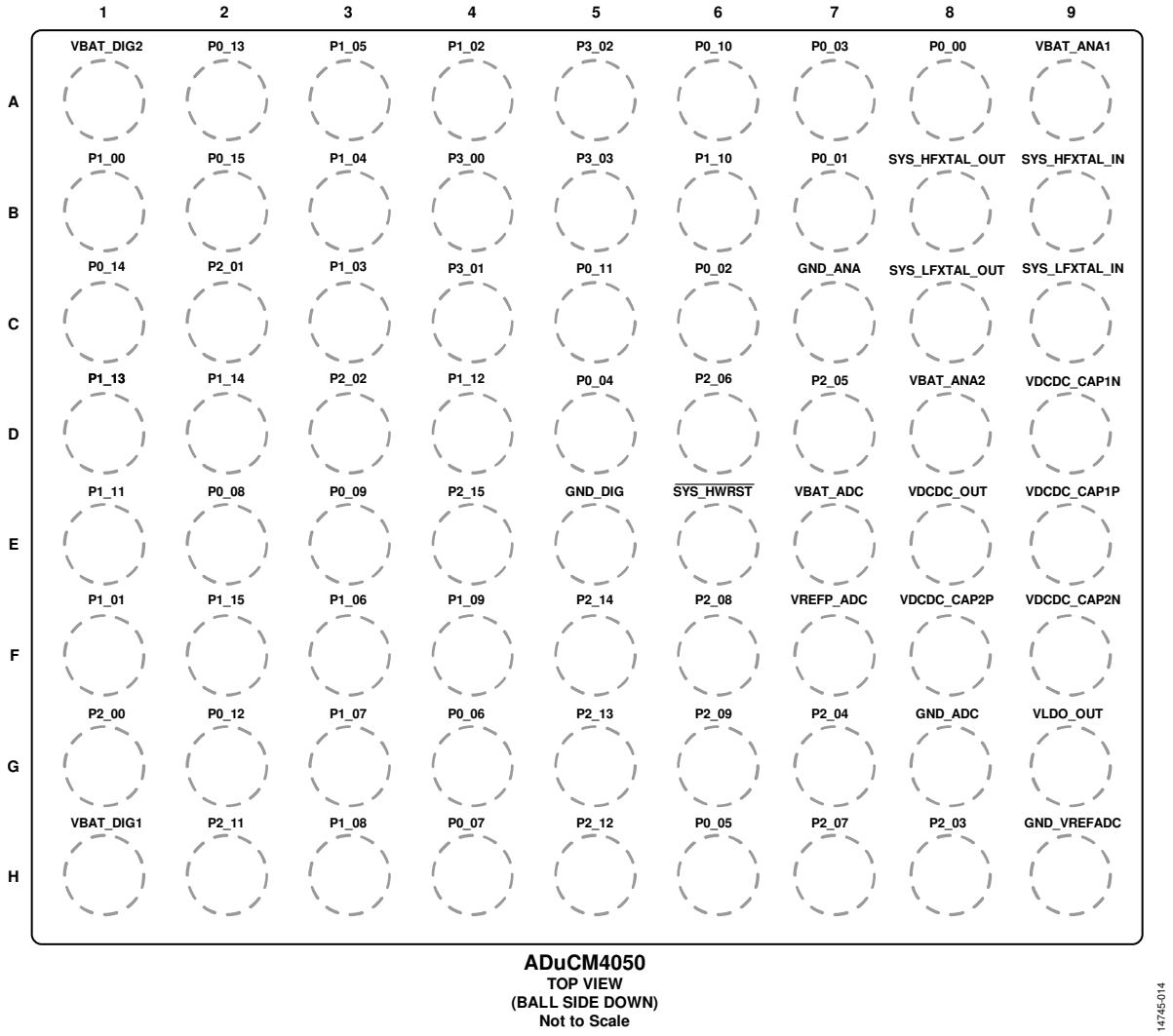

Figure 14. 72-Ball WLCSP Pin Configuration

Table 22. 72-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
A1	VBAT_DIG2	Not applicable	External Supply for Digital Circuits in the MCU.
A2	P0_13	GPIO13/SYS_WAKE2	GPIO. See the GPIO Multiplexing section for more information.
A3	P1_05	GPIO21, SPI2_CS0	GPIO. See the GPIO Multiplexing section for more information.
A4	P1_02	GPIO18, SPI2_CLK	GPIO. See the GPIO Multiplexing section for more information.
A5	P3_02	GPIO50, RGB_TMR0_3, SPT0_AD0	GPIO. See the GPIO Multiplexing section for more information.
A6	P0_10	GPIO10, UART0_TX	GPIO. See the GPIO Multiplexing section for more information.
A7	P0_03	GPIO03, SPI0_CS0, SPT0_BCNV, SPI2_RDY	GPIO. See the GPIO Multiplexing section for more information.
A8	P0_00	GPIO00, SPI0_CLK, SPT0_BCLK	GPIO. See the GPIO Multiplexing section for more information.
A9	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
B1	P1_00	GPIO16/SYS_WAKE1	GPIO. See the GPIO Multiplexing section for more information.
B2	P0_15	GPIO15/SYS_WAKE0	GPIO. See the GPIO Multiplexing section for more information.
B3	P1_04	GPIO20, SPI2_MISO	GPIO. See the GPIO Multiplexing section for more information.
B4	P3_00	GPIO48, RGB_TMR0_1, SPT0_ACLK	GPIO. See the GPIO Multiplexing section for more information.
B5	P3_03	GPIO51, SPT0_ACNV	GPIO. See the GPIO Multiplexing section for more information.

Pin No.	Mnemonic	Signal Names	Description
B6	P1_10	GPIO26, SPI0_CS1, SYS_CLKIN, SPI1_CS3	GPIO. See the GPIO Multiplexing section for more information.
B7	P0_01	GPIO01, SPI0_MOSI, SPT0_BFS	GPIO. See the GPIO Multiplexing section for more information.
B8	SYS_HFXTAL_OUT	Not applicable	High Frequency Crystal Output.
B9	SYS_HFXTAL_IN	Not applicable	High Frequency Crystal Input.
C1	P0_14	GPIO14, TMR0_OUT, SPI1_RDY	GPIO. See the GPIO Multiplexing section for more information.
C2	P2_01	GPIO33/SYS_WAKE3, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
C3	P1_03	GPIO19, SPI2_MOSI	GPIO. See the GPIO Multiplexing section for more information.
C4	P3_01	GPIO49, RGB_TMR0_2, SPT0_AFS	GPIO. See the GPIO Multiplexing section for more information.
C5	P0_11	GPIO11, UART0_RX	GPIO. See the GPIO Multiplexing section for more information.
C6	P0_02	GPIO02, SPI0_MISO, SPT0_BD0	GPIO. See the GPIO Multiplexing section for more information.
C7	GND_ANA	Not applicable	Ground Reference for Analog Circuits in the MCU.
C8	SYS_LFXTAL_OUT	Not applicable	Low Frequency Crystal Output.
C9	SYS_LFXTAL_IN	Not applicable	Low Frequency Crystal Input.
D1	P1_13	GPIO29, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
D2	P1_14	GPIO30, SPI0_RDY	GPIO. See the GPIO Multiplexing section for more information.
D3	P2_02	GPIO34, SPT0_ACNV, SPI1_CS2	GPIO. See the GPIO Multiplexing section for more information.
D4	P1_12	GPIO28, RTC1_SS2	GPIO. See the GPIO Multiplexing section for more information.
D5	P0_04	GPIO04, I2C0_SCL	GPIO. See the GPIO Multiplexing section for more information.
D6	P2_06	GPIO38, ADC0_VIN3	GPIO. See the GPIO Multiplexing section for more information.
D7	P2_05	GPIO37, ADC0_VIN2	GPIO. See the GPIO Multiplexing section for more information.
D8	VBAT_ANA2	Not applicable	External Supply for Analog Circuits in the MCU.
D9	VDCDC_CAP1N	Not applicable	Buck Converter Capacitor 1 Negative Terminal.
E1	P1_11	GPIO27, TMR1_OUT	GPIO. See the GPIO Multiplexing section for more information.
E2	P0_08	GPIO08, BPR0_TONE_N	GPIO. See the GPIO Multiplexing section for more information.
E3	P0_09	GPIO09, BPR0_TONE_P, SPI2_CS1	GPIO. See the GPIO Multiplexing section for more information.
E4	P2_15	GPIO47, SPI2_CS2, SPI1_CS3, SPI0_CS1	GPIO. See the GPIO Multiplexing section for more information.
E5	GND_DIG	Not applicable	Ground Reference for Digital Circuits in the MCU.
E6	$\overline{\text{SYS\_HWRST}}$	Not applicable	Hardware Reset Pin.
E7	VBAT_ADC	Not applicable	External Supply for Internal ADC.
E8	VDCDC_OUT	Not applicable	Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
E9	VDCDC_CAP1P	Not applicable	Buck Converter Capacitor 1 Positive Terminal.
F1	P1_01	SYS_BMODE0, GPIO17	GPIO. See the GPIO Multiplexing section for more information.
F2	P1_15	GPIO31, SPT0_ACLK, UART1_TX	GPIO. See the GPIO Multiplexing section for more information.
F3	P1_06	GPIO22, SPI1_CLK, RGB_TMR0_1	GPIO. See the GPIO Multiplexing section for more information.
F4	P1_09	GPIO25, SPI1_CS0, SWV	GPIO. See the GPIO Multiplexing section for more information.
F5	P2_14	GPIO46, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.
F6	P2_08	GPIO40, ADC0_VIN5, SPI0_CS2, RTC1_SS3	GPIO. See the GPIO Multiplexing section for more information.
F7	VREFP_ADC	Not applicable	External Reference Voltage for Internal ADC.
F8	VDCDC_CAP2P	Not applicable	Buck Converter Capacitor 2 Positive Terminal.
F9	VDCDC_CAP2N	Not applicable	Buck Converter Capacitor 2 Negative Terminal.
G1	P2_00	GPIO32, SPT0_AFS, UART1_RX	GPIO. See the GPIO Multiplexing section for more information.
G2	P0_12	GPIO12, SPT0_AD0, UART0_SOUT_EN	GPIO. See the GPIO Multiplexing section for more information.
G3	P1_07	GPIO23, SPI1_MOSI, RGB_TMR0_2	GPIO. See the GPIO Multiplexing section for more information.
G4	P0_06	SWD0_CLK, GPIO06	GPIO. See the GPIO Multiplexing section for more information.
G5	P2_13	GPIO45, UART1_RX, SPI0_CS2	GPIO. See the GPIO Multiplexing section for more information.
G6	P2_09	GPIO41, ADC0_VIN6, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.

Pin No.	Mnemonic	Signal Names	Description
G7	P2_04	GPIO36, ADC0_VIN1	GPIO. See the GPIO Multiplexing section for more information.
G8	GND_ADC	Not applicable	Ground Pin for Internal ADC.
G9	VLDO_OUT	Not applicable	Low Drop Out Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
H1	VBAT_DIG1	Not applicable	External Supply for Digital Circuits in the MCU.
H2	P2_11	GPIO43, SPI1_CS1, SYS_CLKOUT, RTC1_SS1	GPIO. See the GPIO Multiplexing section for more information.
H3	P1_08	GPIO24, SPI1_MISO, RGB_TMR0_3	GPIO. See the GPIO Multiplexing section for more information.
H4	P0_07	SWD0_DATA, GPIO07	GPIO. See the GPIO Multiplexing section for more information.
H5	P2_12	GPIO44, UART1_TX, SPI2_CS3	GPIO. See the GPIO Multiplexing section for more information.
H6	P0_05	GPIO05, I2C0_SDA	GPIO. See the GPIO Multiplexing section for more information.
H7	P2_07	GPIO39, ADC0_VIN4, SPI2_CS3	GPIO. See the GPIO Multiplexing section for more information.
H8	P2_03	GPIO35, ADC0_VIN0	GPIO. See the GPIO Multiplexing section for more information.
H9	GND_VREFADC	Not applicable	Ground for ADC Reference Supply.

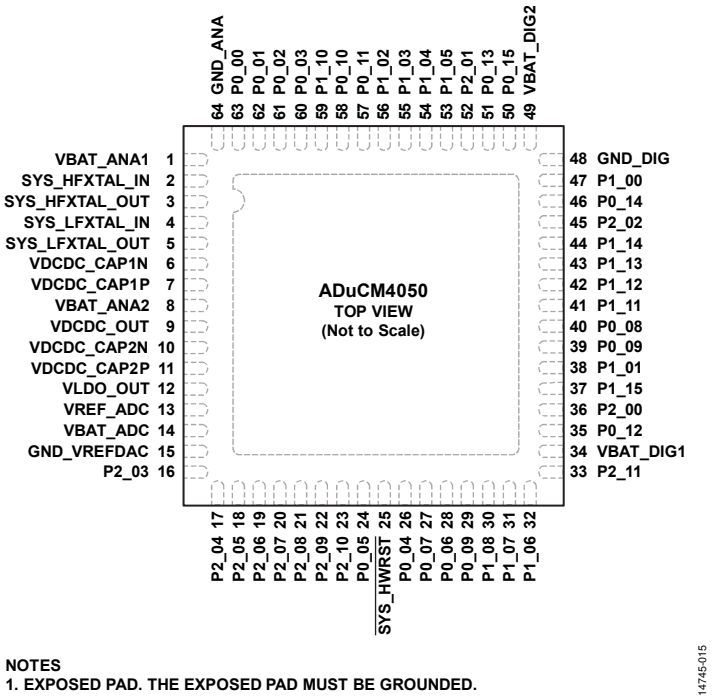

Figure 15. 64-Lead LFCSP Pin Configuration

Table 23. 64-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
1	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
2	SYS_HFXTAL_IN	Not applicable	High Frequency Crystal Input.
3	SYS_HFXTAL_OUT	Not applicable	High Frequency Crystal Output.
4	SYS_LFXTAL_IN	Not applicable	Low Frequency Crystal Input.
5	SYS_LFXTAL_OUT	Not applicable	Low Frequency Crystal Output.
6	VDCDC_CAP1N	Not applicable	Buck Converter Capacitor 1 Negative Terminal.
7	VDCDC_CAP1P	Not applicable	Buck Converter Capacitor 1 Positive Terminal.
8	VBAT_ANA2	Not applicable	External Supply for Analog Circuits in the MCU.
9	VDCDC_OUT	Not applicable	Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
10	VDCDC_CAP2N	Not applicable	Buck Converter Capacitor 2 Negative Terminal.
11	VDCDC_CAP2P	Not applicable	Buck Converter Capacitor 2 Positive Terminal.
12	VLDO_OUT	Not applicable	Low Dropout Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
13	VREF_ADC	Not applicable	External Reference Voltage for Internal ADC.
14	VBAT_ADC	Not applicable	External Supply for Internal ADC.
15	GND_VREFADC	Not applicable	Ground for Internal ADC.
16	P2_03	GPIO35, ADC0_VIN0	GPIO. See the GPIO Multiplexing section for more information.
17	P2_04	GPIO36, ADC0_VIN1	GPIO. See the GPIO Multiplexing section for more information.
18	P2_05	GPIO37, ADC0_VIN2	GPIO. See the GPIO Multiplexing section for more information.
19	P2_06	GPIO38, ADC0_VIN3	GPIO. See the GPIO Multiplexing section for more information.
20	P2_07	GPIO39, ADC0_VIN4, SPI2_CS3	GPIO. See the GPIO Multiplexing section for more information.
21	P2_08	GPIO40, ADC0_VIN5, SPI0_CS2, RTC1_SS3	GPIO. See the GPIO Multiplexing section for more information.
22	P2_09	GPIO41, ADC0_VIN6, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.
23	P2_10	GPIO42, ADC0_VIN7, SPI2_CS2	GPIO.
24	P0_05	GPIO05, I2C0_SDA	GPIO. See the GPIO Multiplexing section for more information.
25	$\overline{\text{SYS\_HWRST}}$	Not applicable	Hardware Reset Pin.
26	P0_04	GPIO04, I2C0_SCL	GPIO. See the GPIO Multiplexing section for more information.
27	P0_07	SWD0_DATA, GPIO07	GPIO. See the GPIO Multiplexing section for more information.

Pin No.	Mnemonic	Signal Names	Description
28	P0_06	SWD0_CLK, GPIO06	GPIO. See the GPIO Multiplexing section for more information.
29	P1_09	GPIO25, SPI1_CS0, SWV	GPIO. See the GPIO Multiplexing section for more information.
30	P1_08	GPIO24, SPI1_MISO, RGB_TMR0_3	GPIO. See the GPIO Multiplexing section for more information.
31	P1_07	GPIO23, SPI1_MOSI, RGB_TMR0_2	GPIO. See the GPIO Multiplexing section for more information.
32	P1_06	GPIO22, SPI1_CLK, RGB_TMR0_1	GPIO. See the GPIO Multiplexing section for more information.
33	P2_11	GPIO43, SPI1_CS1, SYS_CLKOUT, RTC1_SS1	GPIO. See the GPIO Multiplexing section for more information.
34	VBAT_DIG1	Not applicable	External Supply for Digital Circuits in the MCU.
35	P0_12	GPIO12, SPT0_AD0, UART0_SOUT_EN	GPIO. See the GPIO Multiplexing section for more information.
36	P2_00	GPIO32, SPT0_AFS, UART1_RX	GPIO. See the GPIO Multiplexing section for more information.
37	P1_15	GPIO31, SPT0_ACLK, UART1_TX	GPIO. See the GPIO Multiplexing section for more information.
38	P1_01	SYS_BMODE0, GPIO17	GPIO. See the GPIO Multiplexing section for more information.
39	P0_09	GPIO09, BPR0_TONE_P, SPI2_CS1	GPIO. See the GPIO Multiplexing section for more information.
40	P0_08	GPIO08, BPR0_TONE_N	GPIO. See the GPIO Multiplexing section for more information.
41	P1_11	GPIO27, TMR1_OUT	GPIO. See the GPIO Multiplexing section for more information.
42	P1_12	GPIO28, RTC1_SS2	GPIO. See the GPIO Multiplexing section for more information.
43	P1_13	GPIO29, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
44	P1_14	GPIO30, SPI0_RDY	GPIO. See the GPIO Multiplexing section for more information.
45	P2_02	GPIO34, SPT0_ACNV, SPI1_CS2	GPIO. See the GPIO Multiplexing section for more information.
46	P0_14	GPIO14, TMR0_OUT, SPI1_RDY	GPIO. See the GPIO Multiplexing section for more information.
47	P1_00	GPIO16/SYS_WAKE1	GPIO. See the GPIO Multiplexing section for more information.
48	GND_DIG	Not applicable	Ground Reference for Digital Circuits in the MCU.
49	VBAT_DIG2	Not applicable	External Supply for Digital Circuits in the MCU.
50	P0_15	GPIO15/SYS_WAKE0	GPIO. See the GPIO Multiplexing section for more information.
51	P0_13	GPIO13/SYS_WAKE2	GPIO. See the GPIO Multiplexing section for more information.
52	P2_01	GPIO33/SYS_WAKE3, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
53	P1_05	GPIO21, SPI2_CS0	GPIO. See the GPIO Multiplexing section for more information.
54	P1_04	GPIO20, SPI2_MISO	GPIO. See the GPIO Multiplexing section for more information.
55	P1_03	GPIO19, SPI2_MOSI	GPIO. See the GPIO Multiplexing section for more information.
56	P1_02	GPIO18, SPI2_CLK	GPIO. See the GPIO Multiplexing section for more information.
57	P0_11	GPIO11, UART0_RX	GPIO. See the GPIO Multiplexing section for more information.
58	P0_10	GPIO10, UART0_TX	GPIO. See the GPIO Multiplexing section for more information.
59	P1_10	GPIO26, SPI0_CS1, SYS_CLKIN, SPI1_CS3	GPIO. See the GPIO Multiplexing section for more information.
60	P0_03	GPIO03, SPI0_CS0, SPT0_BCNV, SPI2_RDY	GPIO. See the GPIO Multiplexing section for more information.
61	P0_02	GPIO02, SPI0_MISO, SPT0_BD0	GPIO. See the GPIO Multiplexing section for more information.
62	P0_01	GPIO01, SPI0_MOSI, SPT0_BFS	GPIO. See the GPIO Multiplexing section for more information.
63	P0_00	GPIO00, SPI0_CLK, SPT0_BCLK	GPIO. See the GPIO Multiplexing section for more information.
64	GND_ANA	Not applicable	Ground Reference for Analog Circuits in the MCU.
	EPAD	Not applicable	Exposed Pad. The exposed pad must be grounded.