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PWM Controller and Transformer Driver with Quad-Channel Isolators

Data Sheet **ADuM3470/ADuM3471/ADuM3472/ADuM3473/ADuM3474**

FEATURES

- Isolated PWM controller
- Integrated transformer driver
- Regulated adjustable output: 3.3 V to 24 V
- 2 W output power
- 70% efficiency at guaranteed load of 400 mA at 5.0 V output
- Quad dc-to-25 Mbps (NRZ) signal isolation channels
- 20-lead SSOP package
- High temperature operation: 105°C maximum
- High common-mode transient immunity: >25 kV/µs
- 200 kHz to 1 MHz adjustable oscillator frequency
- Soft start function at power-up
- Pulse-by-pulse overcurrent protection
- Thermal shutdown
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak
- Qualified for automotive applications

APPLICATIONS

- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation
- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Process controls
- Automotive

GENERAL DESCRIPTION

The ADuM3470/ADuM3471/ADuM3472/ADuM3473/ADuM3474 devices[1] are quad-channel digital isolators with an integrated PWM controller and transformer driver for an isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides up to 2 W of regulated, isolated power at 3.3 V to 24 V from a 5.0 V input supply or from a 3.3 V supply. This eliminates the need for a separate, isolated dc-to-dc converter in 2 W isolated designs. The *i*Coupler chip scale transformer technology is used to isolate the logic signals, and the integrated transformer driver with isolated secondary side control provides higher efficiency for the isolated dc-to-dc converter. The result is a small form factor, total isolation solution. The ADuM347x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide).

FUNCTIONAL BLOCK DIAGRAMS

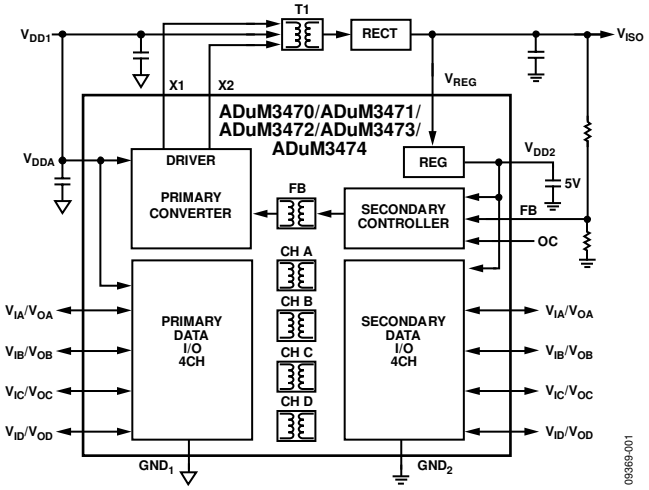

Figure 1. Functional Block Diagram

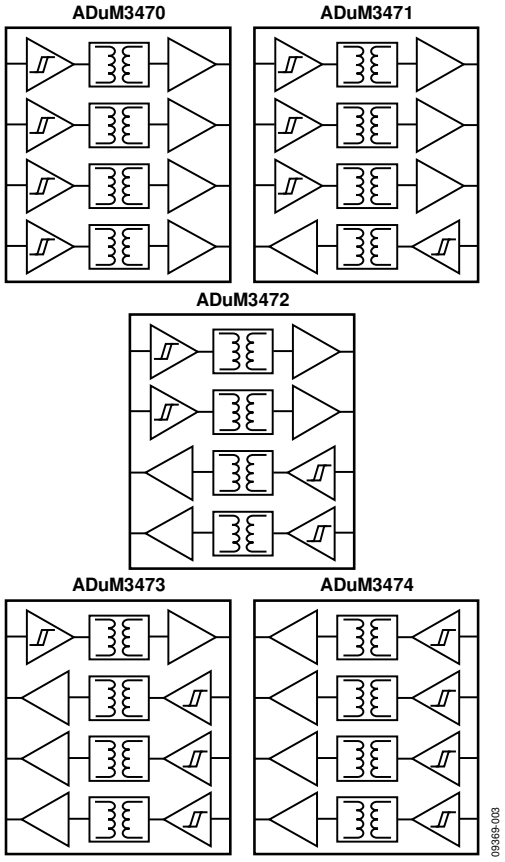

Figure 2. Block Diagrams of I/O Channels

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

Rev. B Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds (see the application schematic in Figure 38). All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 5.0 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Isolated Output Voltage	V_{ISO}	4.5	5.0	5.5	V	I_{ISO} = 0 mA, V_{ISO} = V_{FB} × (R1 + R2)/R2
Feedback Voltage Setpoint	V_{FB}	1.125	1.25	1.375	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (N)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open loop)
Switch On Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DD1}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[1]						f ≤ 1 MHz
Maximum Output Supply Current[2]	$I_{ISO (MAX)}$	400			mA	V_{ISO} = 5.0 V
Efficiency at Maximum Output Supply Current[3]			70		%	I_{ISO} = $I_{ISO (MAX)}$
*i*COUPLER DATA CHANNELS						
DC to 2 Mbps Data Rate[1]						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM3470			14	30	mA	
ADuM3471			15	30	mA	
ADuM3472			16	30	mA	
ADuM3473			17	30	mA	
ADuM3474			18	30	mA	
25 Mbps Data Rate (C Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM3470			44		mA	
ADuM3471			46		mA	
ADuM3472			48		mA	
ADuM3473			50		mA	
ADuM3474			52		mA	
Available V_{ISO} Supply Current[4]	$I_{ISO (LOAD)}$					C_L = 15 pF, f = 12.5 MHz
ADuM3470			390		mA	
ADuM3471			388		mA	
ADuM3472			386		mA	
ADuM3473			384		mA	
ADuM3474			382		mA	
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1 (MAX)}$		550		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = 5 V, I_{ISO} = 400 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	μA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
A Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			1000	ns	
Maximum Data Rate		1			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}		55	100	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	
Propagation Delay Skew	t_{PSK}			50	ns	
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	
C Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			40	ns	
Maximum Data Rate		25			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}	30	45	60	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels	t_{PSKCD}			8	ns	
Opposing Directional Channels	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity						V_{CM} = 1000 V, transient magnitude = 800 V
At Logic High Output	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}
At Logic Low Output	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels is not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of the available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

3.0 V ≤ V_{DD1} = V_{DDA} ≤ 3.6 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds (see the application schematic in Figure 38). All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 3.3 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, V_{ISO} = V_{FB} × (R1 + R2)/R2
Feedback Voltage Setpoint	V_{FB}	1.125	1.25	1.375	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 20 mA to 100 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (N)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open loop)
Switch On Resistance	R_{ON}		0.6		Ω	
Undervoltage Lockout, V_{DD1}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[1]						f ≤ 1 MHz,
Maximum Output Supply Current[2]	$I_{ISO (MAX)}$	250			mA	V_{ISO} = 3.3 V
Efficiency at Maximum Output Supply Current[3]			70		%	I_{ISO} = $I_{ISO (MAX)}$
*i*COUPLER DATA CHANNELS						
DC to 2 Mbps Data Rate[1]						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM3470			9	20	mA	
ADuM3471			10	20	mA	
ADuM3472			11	20	mA	
ADuM3473			11	20	mA	
ADuM3474			12	20	mA	
25 Mbps Data Rate (C Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM3470			28		mA	
ADuM3471			29		mA	
ADuM3472			31		mA	
ADuM3473			32		mA	
ADuM3474			34		mA	
Available V_{ISO} Supply Current[4]	$I_{ISO (LOAD)}$					C_L = 15 pF, f = 12.5 MHz
ADuM3470			244		mA	
ADuM3471			243		mA	
ADuM3472			241		mA	
ADuM3473			240		mA	
ADuM3474			238		mA	
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1 (MAX)}$		350		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = 3.3 V, I_{ISO} = 250 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−10	+0.01	+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Input Threshold	V_{IH}	1.6			V	
Logic Low Input Threshold	V_{IL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
A Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			1000	ns	
Maximum Data Rate		1			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}		60	100	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			40	ns	
Propagation Delay Skew	t_{PSK}			50	ns	
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	
C Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			40	ns	
Maximum Data Rate		25			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}	30	60	75	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			8	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew	t_{PSK}			45	ns	
Channel-to-Channel Matching						
Codirectional Channels	t_{PSKCD}			8	ns	
Opposing Directional Channels	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity						V_{CM} = 1000 V, transient magnitude = 800 V
At Logic High Output	$\lvert CM_H \rvert$	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}
At Logic Low Output	$\lvert CM_L \rvert$	25	35		kV/μs	V_{Ix} = 0 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels is not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of the available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds (see the application schematic in Figure 38). All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, V_{ISO} = V_{FB} × (R1 + R2)/R2
Feedback Voltage Setpoint	V_{FB}	1.125	1.25	1.375	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (N)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open loop)
Switch On Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DD1}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[1]						f ≤ 1 MHz
Maximum Output Supply Current[2]	$I_{ISO (MAX)}$	400			mA	V_{ISO} = 3.3 V
Efficiency at Maximum Output Supply Current[3]			70		%	I_{ISO} = $I_{ISO (MAX)}$
*i*COUPLER DATA CHANNELS						
DC to 2 Mbps Data Rate[1]						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM3470			9	30	mA	
ADuM3471			9	30	mA	
ADuM3472			10	30	mA	
ADuM3473			10	30	mA	
ADuM3474			10	30	mA	
25 Mbps Data Rate (C Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM3470			33		mA	
ADuM3471			33		mA	
ADuM3472			33		mA	
ADuM3473			33		mA	
ADuM3474			33		mA	
Available V_{ISO} Supply Current[4]	$I_{ISO (LOAD)}$					C_L = 15 pF, f = 12.5 MHz
ADuM3470			393		mA	
ADuM3471			392		mA	
ADuM3472			390		mA	
ADuM3473			389		mA	
ADuM3474			388		mA	
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1 (MAX)}$		375		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
A Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			1000	ns	
Maximum Data Rate		1			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}		55	100	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	
Propagation Delay Skew	t_{PSK}			50	ns	
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	
C Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			40	ns	
Maximum Data Rate		25			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}	30	50	70	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels	t_{PSKCD}			8	ns	
Opposing Directional Channels	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity						V_{CM} = 1000 V, transient magnitude = 800 V
At Logic High Output	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}
At Logic Low Output	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels is not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of the available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/15 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{REG} = V_{ISO} = 15 V; V_{DD2} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds (see the application schematic in Figure 39). All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{REG} = V_{ISO} = 15 V, V_{DD2} = 5.0 V.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Isolated Output Voltage	V_{ISO}	13.5	15	16.5	V	I_{ISO} = 0 mA, V_{ISO} = V_{FB} × (R1 + R2)/R2
Feedback Voltage Setpoint	V_{FB}	1.125	1.25	1.375	V	I_{ISO} = 0 mA
V_{DD2} Linear Regulator						
Regulator Voltage	V_{DD2}	4.6	5.0	5.7	V	V_{REG} = 7 V to 15 V, I_{DD2} = 0 mA to 50 mA
Dropout Voltage	$V_{DD2 (DO)}$		0.5	1.5	V	I_{DD2} = 50 mA
Line Regulation	$V_{ISO (LINE)}$		1	20	mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	3	%	I_{ISO} = 20 mA to 100 mA
Output Ripple	$V_{ISO (RIP)}$		200		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (N)}$		500		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open loop)
Switch On Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DD1}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[1]						f ≤ 1 MHz
Maximum Output Supply Current[2]	$I_{ISO (MAX)}$	100			mA	V_{ISO} = 5.0 V
Efficiency at Maximum Output Supply Current[3]			70		%	I_{ISO} = $I_{ISO (MAX)}$
*i*COUPLER DATA CHANNELS						
DC to 2 Mbps Data Rate[1]						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM3470			25	45	mA	
ADuM3471			27	45	mA	
ADuM3472			29	45	mA	
ADuM3473			31	45	mA	
ADuM3474			33	45	mA	
25 Mbps Data Rate (C Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM3470			73		mA	
ADuM3471			83		mA	
ADuM3472			93		mA	
ADuM3473			102		mA	
ADuM3474			112		mA	
Available V_{ISO} Supply Current[4]	$I_{ISO (LOAD)}$					C_L = 15 pF, f = 12.5 MHz
ADuM3470			91		mA	
ADuM3471			89		mA	
ADuM3472			86		mA	
ADuM3473			83		mA	
ADuM3474			80		mA	
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1 (MAX)}$		425		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = 5 V, I_{ISO} = 100 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	μA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
A Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			1000	ns	
Maximum Data Rate		1			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}		55	100	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	
Propagation Delay Skew	t_{PSK}			50	ns	
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	
C Grade						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width	PW			40	ns	
Maximum Data Rate		25			Mbps	
Propagation Delay	t_{PHL}, t_{PLH}	30	45	60	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels	t_{PSKCD}			8	ns	
Opposing Directional Channels	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity						V_{CM} = 1000 V, transient magnitude = 800 V
At Logic High Output	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}
At Logic Low Output	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels is not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of the available current at less than the maximum data rate.

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE AND CAPACITANCE						
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		50.5		°C/W	Thermocouple is located at the center of the package underside; test conducted on a 4-layer board with thin traces[3]
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}		150		°C	T_J rising
Thermal Shutdown Hysteresis	TS_{SD-HYS}		20		°C	

[1] The device is considered a 2-terminal device: Pin 1 to Pin 10 are shorted together, and Pin 11 to Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

The ADuM3470/ADuM3471/ADuM3472/ADuM3473/ADuM3474 are approved by the organizations listed in Table 6. Refer to Table 11 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-insulation waveforms and insulation levels.

Table 6.

UL	CSA	VDE
Recognized under the UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3470/ADuM3471/ADuM3472/ADuM3473/ADuM3474 is proof tested by applying an insulation test voltage of ≥3000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM3470/ADuM3471/ADuM3472/ADuM3473/ADuM3474 is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 7.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>5.1	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>5.1	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Distance (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component denotes DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

Table 8.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	1.25	A
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

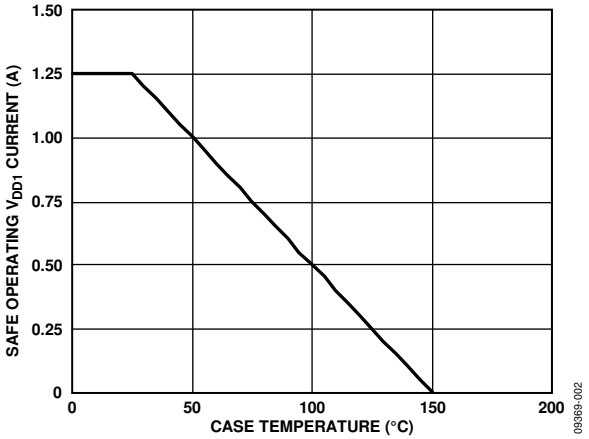


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 9.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]				
V_{DD1} at V_{ISO} = 3.3 V	V_{DD1}	3.0	3.6	V
V_{DD1} at V_{ISO} = 5.0 V	V_{DD1}	3.0	3.6	V
V_{DD1} at V_{ISO} = 5.0 V	V_{DD1}	4.5	5.5	V
Minimum Load	$I_{ISO (MIN)}$	10		mA

[1] All voltages are relative to their respective grounds.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages[1]	
V_{DD1},[2] V_{DDA}, V_{DD2}	−0.5 V to +7.0 V
V_{REG}, X1, X2	−0.5 V to +20.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID})[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective grounds.
[2] V_{DD1} is the power supply for the push-pull transformer.
[3] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the Printed Circuit Board (PCB) Layout section.
[4] See Figure 3 for maximum rated current values for various temperatures.
[5] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

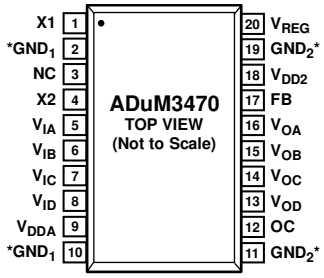
Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	565	V peak	All certifications
AC Voltage, Unipolar Waveform			
Basic Insulation	848	V peak	Working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	848	V peak	Working voltage per IEC 60950-1

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



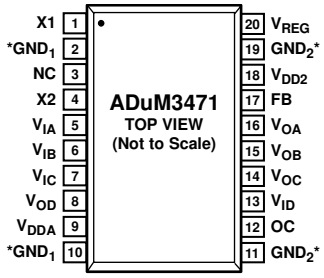
NOTES
1. NC = NO INTERNAL CONNECTION.
2. PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

09369-004

Figure 4. ADuM3470 Pin Configuration

Table 12. ADuM3470 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for the Primary Side of the Isolator. Pin 2 and Pin 10 are internally connected to each other; it is recommended that both pins be connected to a common ground.
3	NC	No Internal Connection.
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{ID}	Logic Input D.
9	V_{DDA}	Supply Voltage for the Primary Side, 3.0 V to 5.5 V. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for the Secondary Side of the Isolator. Pin 11 and Pin 19 are internally connected to each other; it is recommended that both pins be connected to a common ground.
12	OC	Oscillator Control Pin. When the OC pin is connected high to the V_{DD2} pin, the secondary controller runs in open-loop (unregulated) mode. To regulate the output voltage, connect a resistor between the OC pin and GND_2; the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{OD}	Logic Output D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from the V_{ISO} output to the FB pin to set the V_{FB} voltage equal to the 1.25 V internal reference level using the formula $V_{ISO} = V_{FB} \times (R1 + R2)/R2$. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage for the Secondary Side Controller and the Side 2 Data Channels. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller and the Side 2 Data Channels. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.



NOTES
1. NC = NO INTERNAL CONNECTION.
2. PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

09369-005

Figure 5. ADuM3471 Pin Configuration

Table 13. ADuM3471 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for the Primary Side of the Isolator. Pin 2 and Pin 10 are internally connected to each other; it is recommended that both pins be connected to a common ground.
3	NC	No Internal Connection.
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Supply Voltage for the Primary Side, 3.0 V to 5.5 V. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for the Secondary Side of the Isolator. Pin 11 and Pin 19 are internally connected to each other; it is recommended that both pins be connected to a common ground.
12	OC	Oscillator Control Pin. When the OC pin is connected high to the V_{DD2} pin, the secondary controller runs in open-loop (unregulated) mode. To regulate the output voltage, connect a resistor between the OC pin and GND_2; the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from the V_{ISO} output to the FB pin to set the V_{FB} voltage equal to the 1.25 V internal reference level using the formula $V_{ISO} = V_{FB} \times (R1 + R2)/R2$. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage for the Secondary Side Controller and the Side 2 Data Channels. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller and the Side 2 Data Channels. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

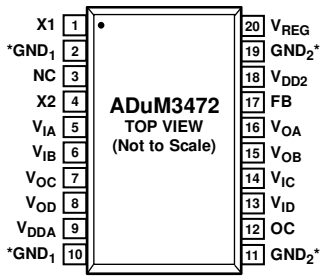


Figure 6. ADuM3472 Pin Configuration

Table 14. ADuM3472 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for the Primary Side of the Isolator. Pin 2 and Pin 10 are internally connected to each other; it is recommended that both pins be connected to a common ground.
3	NC	No Internal Connection.
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Supply Voltage for the Primary Side, 3.0 V to 5.5 V. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for the Secondary Side of the Isolator. Pin 11 and Pin 19 are internally connected to each other; it is recommended that both pins be connected to a common ground.
12	OC	Oscillator Control Pin. When the OC pin is connected high to the V_{DD2} pin, the secondary controller runs in open-loop (unregulated) mode. To regulate the output voltage, connect a resistor between the OC pin and GND_2; the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from the V_{ISO} output to the FB pin to set the V_{FB} voltage equal to the 1.25 V internal reference level using the formula $V_{ISO} = V_{FB} \times (R1 + R2)/R2$. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage for the Secondary Side Controller and the Side 2 Data Channels. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller and the Side 2 Data Channels. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

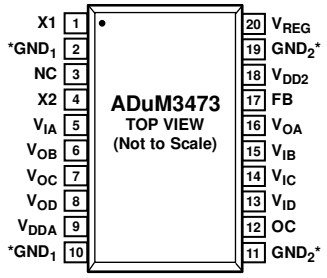
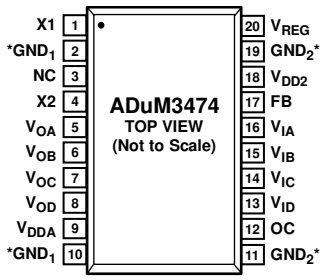


Figure 7. ADuM3473 Pin Configuration

Table 15. ADuM3473 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for the Primary Side of the Isolator. Pin 2 and Pin 10 are internally connected to each other; it is recommended that both pins be connected to a common ground.
3	NC	No Internal Connection.
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Supply Voltage for the Primary Side, 3.0 V to 5.5 V. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for the Secondary Side of the Isolator. Pin 11 and Pin 19 are internally connected to each other; it is recommended that both pins be connected to a common ground.
12	OC	Oscillator Control Pin. When the OC pin is connected high to the V_{DD2} pin, the secondary controller runs in open-loop (unregulated) mode. To regulate the output voltage, connect a resistor between the OC pin and GND_2; the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from the V_{ISO} output to the FB pin to set the V_{FB} voltage equal to the 1.25 V internal reference level using the formula $V_{ISO} = V_{FB} \times (R1 + R2)/R2$. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage for the Secondary Side Controller and the Side 2 Data Channels. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller and the Side 2 Data Channels. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.



NOTES
1. NC = NO INTERNAL CONNECTION.
2. PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED TO EACH OTHER; IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

09369-008

Figure 8. ADuM3474 Pin Configuration

Table 16. ADuM3474 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for the Primary Side of the Isolator. Pin 2 and Pin 10 are internally connected to each other; it is recommended that both pins be connected to a common ground.
3	NC	No Internal Connection.
4	X2	Transformer Driver Output 2.
5	V_{OA}	Logic Output A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Supply Voltage for the Primary Side, 3.0 V to 5.5 V. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for the Secondary Side of the Isolator. Pin 11 and Pin 19 are internally connected to each other; it is recommended that both pins be connected to a common ground.
12	OC	Oscillator Control Pin. When the OC pin is connected high to the V_{DD2} pin, the secondary controller runs in open-loop (unregulated) mode. To regulate the output voltage, connect a resistor between the OC pin and GND_2; the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{IA}	Logic Input A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from the V_{ISO} output to the FB pin to set the V_{FB} voltage equal to the 1.25 V internal reference level using the formula $V_{ISO} = V_{FB} \times (R1 + R2)/R2$. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage for the Secondary Side Controller and the Side 2 Data Channels. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller and the Side 2 Data Channels. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

Table 17. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DD1} State	V_{DD2} State	V_{Ox} Output[1]	Notes
High	Powered	Powered	High	Normal operation, data is high
Low	Powered	Powered	Low	Normal operation, data is low

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).

TYPICAL PERFORMANCE CHARACTERISTICS

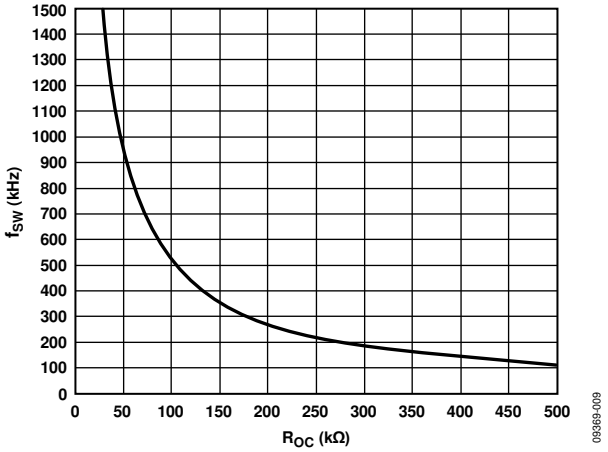


Figure 9. Switching Frequency (f_{SW}) vs. R_{OC} Resistance

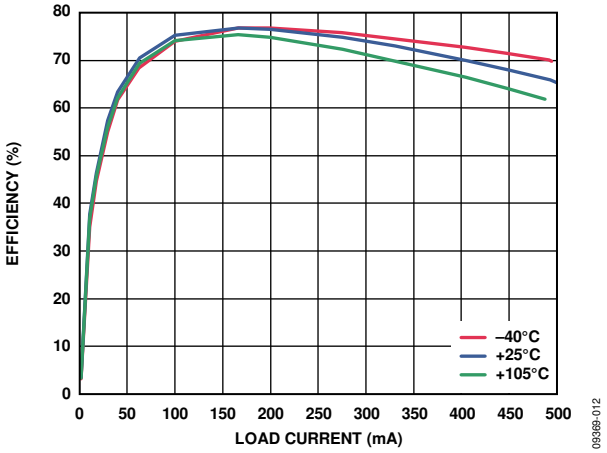


Figure 12. Typical Efficiency over Temperature with Coilcraft Transformer, f_{SW} = 500 kHz, 5 V Input to 5 V Output

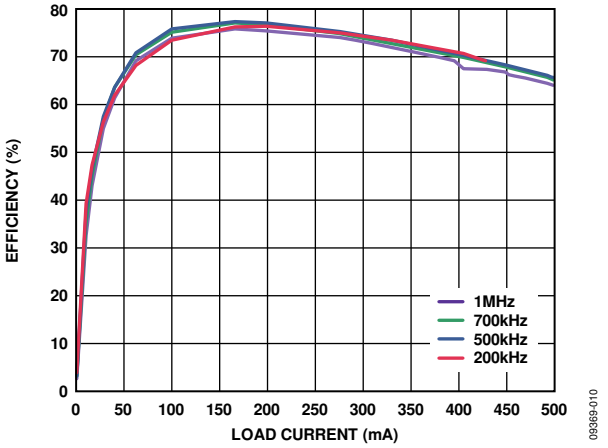


Figure 10. Typical Efficiency at Various Switching Frequencies with Coilcraft Transformer, 5 V Input to 5 V Output

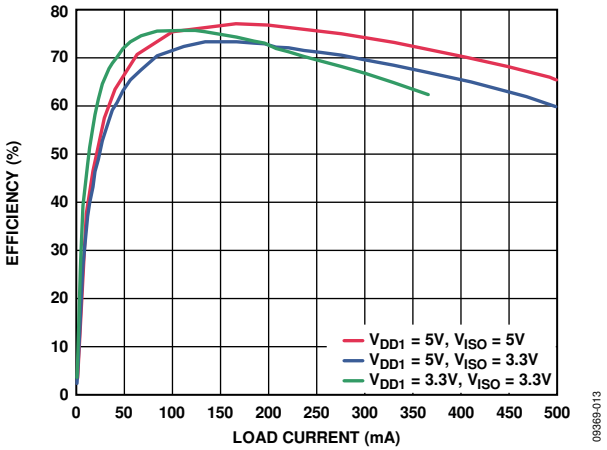


Figure 13. Single-Supply Efficiency with Coilcraft Transformer, f_{SW} = 500 kHz

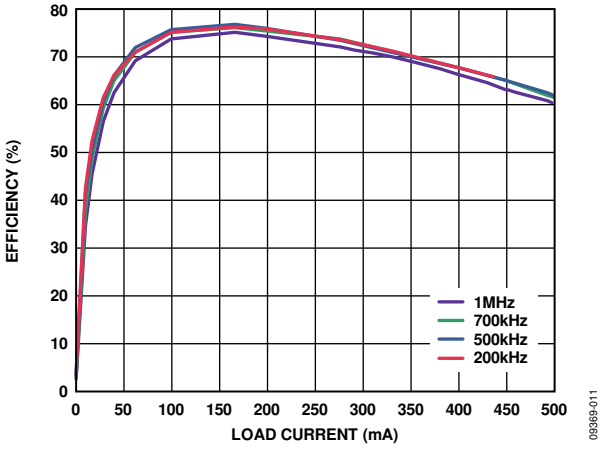


Figure 11. Typical Efficiency at Various Switching Frequencies with Halo Transformer, 5 V Input to 5 V Output

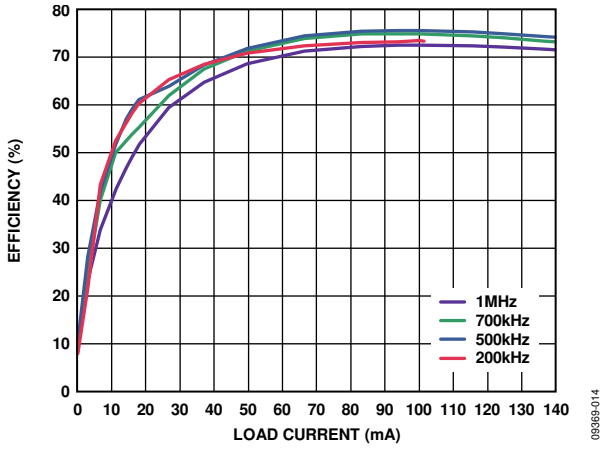


Figure 14. Typical Efficiency at Various Switching Frequencies with Coilcraft Transformer, 5 V Input to 15 V Output

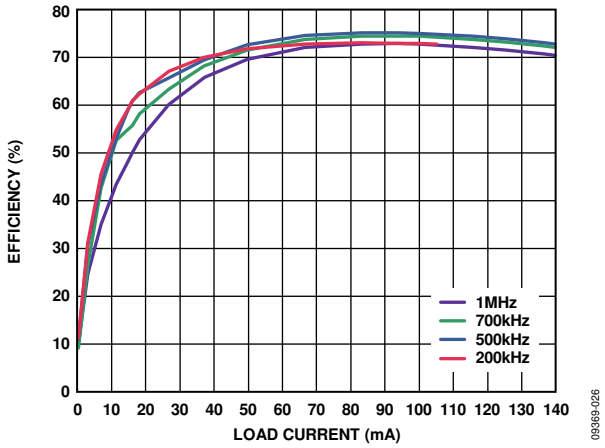


Figure 15. Typical Efficiency at Various Switching Frequencies with Halo Transformer, 5 V Input to 15 V Output

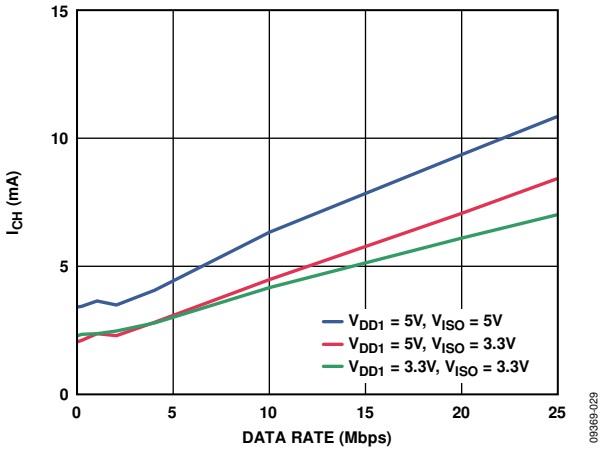


Figure 18. Typical Single-Supply I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

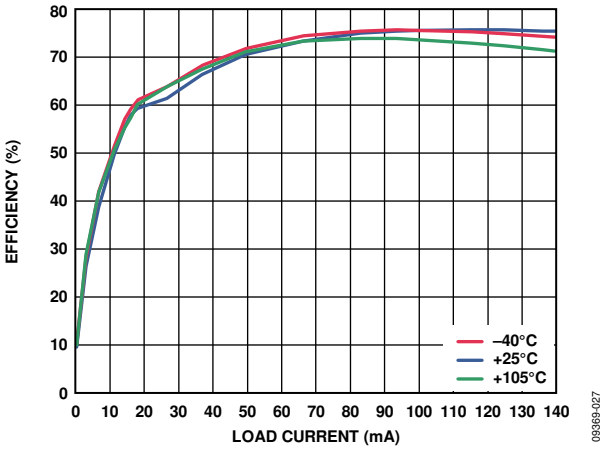


Figure 16. Typical Efficiency over Temperature with Coilcraft Transformer, f_{SW} = 500 kHz, 5 V Input to 15 V Output

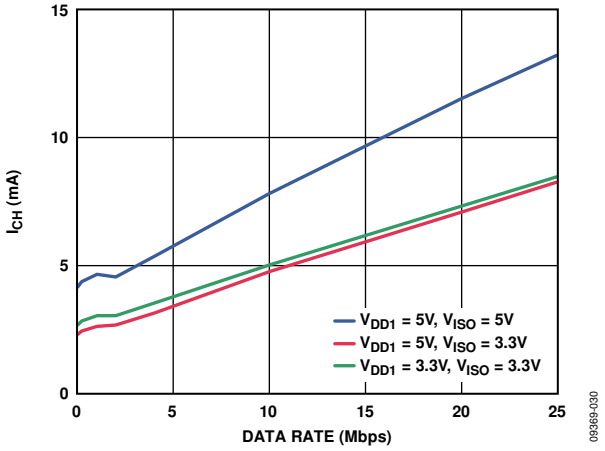


Figure 19. Typical Single-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load)

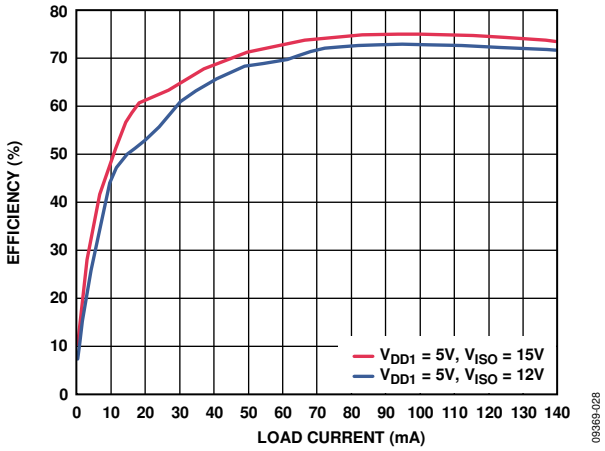


Figure 17. Double-Supply Efficiency with Coilcraft Transformer, f_{SW} = 500 kHz

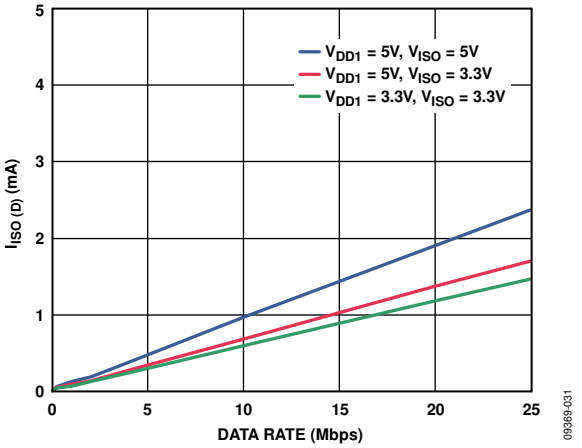


Figure 20. Typical Single-Supply $I_{ISO (D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

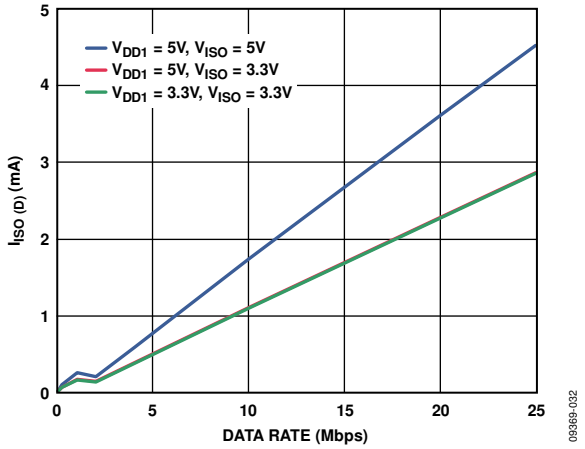


Figure 21. Typical Single-Supply $I_{ISO\ (D)}$ Dynamic Supply Current per Input Channel

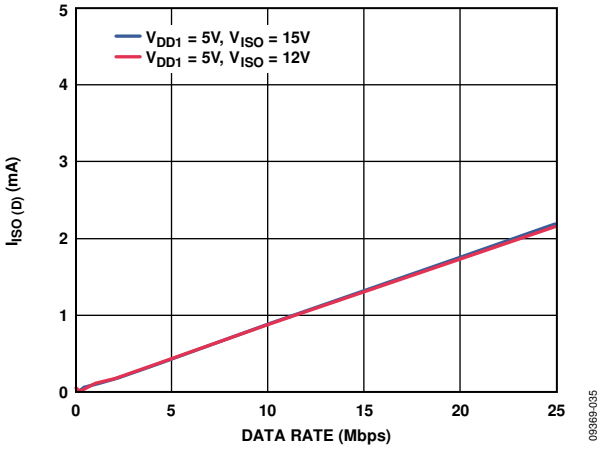


Figure 24. Typical Double-Supply $I_{ISO\ (D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

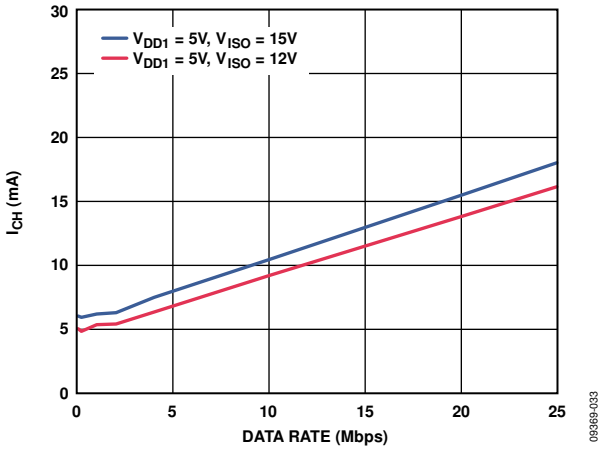


Figure 22. Typical Double-Supply I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

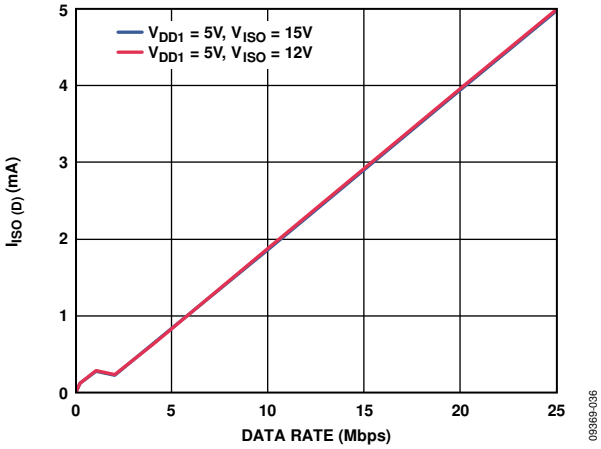


Figure 25. Typical Double-Supply $I_{ISO\ (D)}$ Dynamic Supply Current per Input Channel

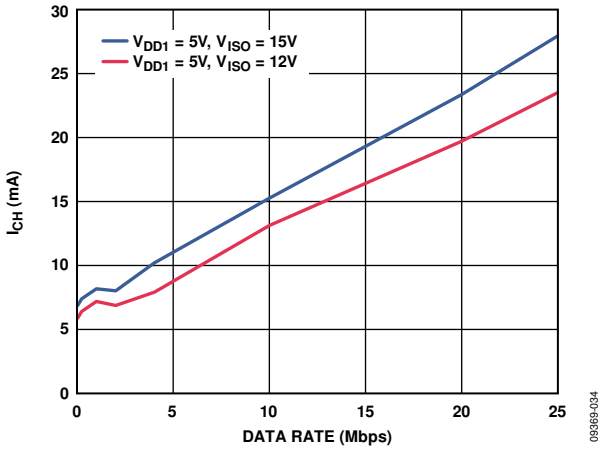


Figure 23. Typical Double-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load)

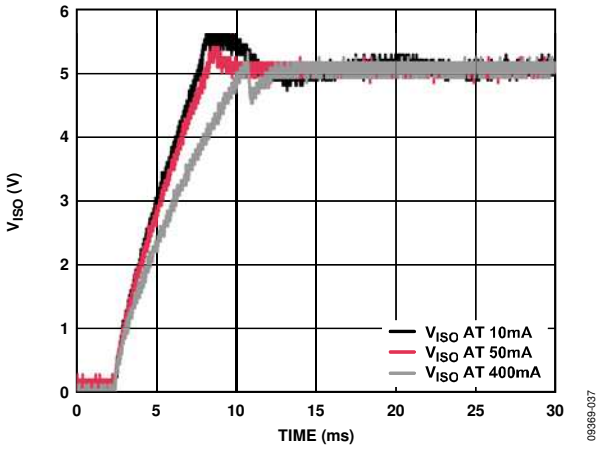


Figure 26. Typical V_{ISO} Startup with 10 mA, 50 mA, and 400 mA Output Load, 5 V Input to 5 V Output

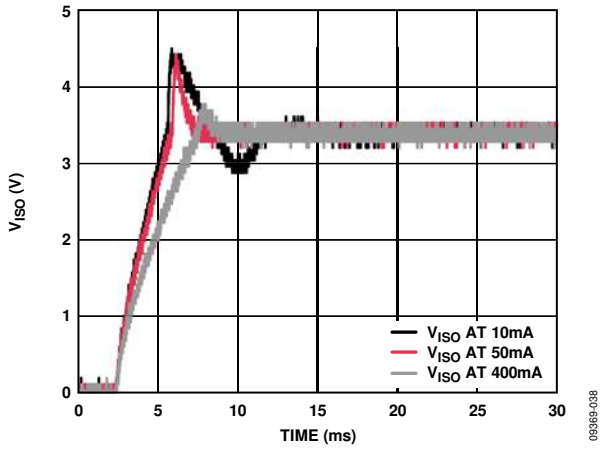


Figure 27. Typical V_{ISO} Startup with 10 mA, 50 mA, and 400 mA Output Load, 5 V Input to 3.3 V Output

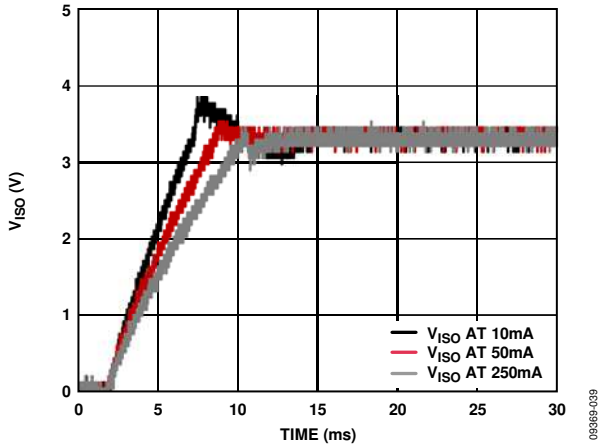


Figure 28. Typical V_{ISO} Startup with 10 mA, 50 mA, and 250 mA Output Load, 3.3 V Input to 3.3 V Output

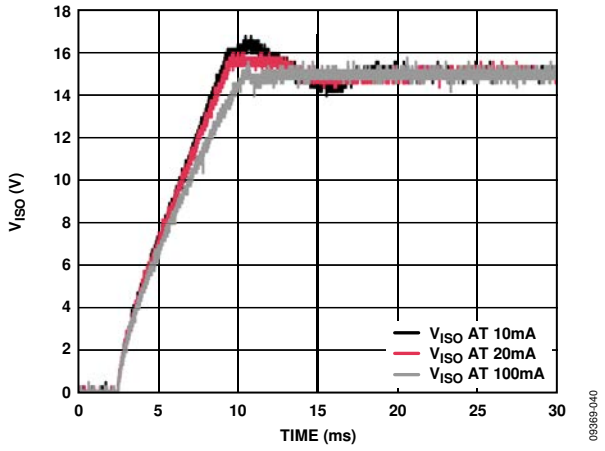


Figure 29. Typical V_{ISO} Startup with 10 mA, 20 mA, and 100 mA Output Load, 5 V Input to 15 V Output

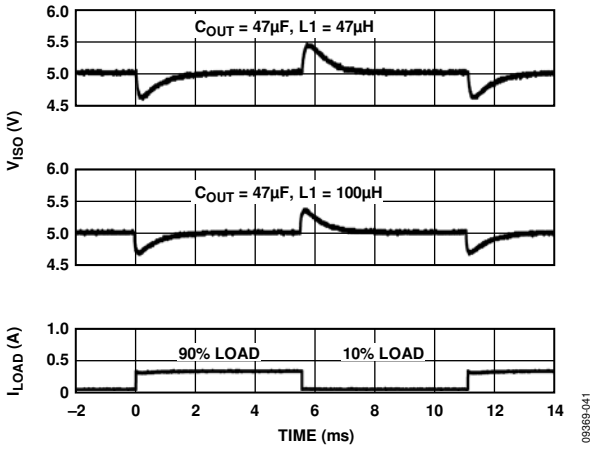


Figure 30. Typical V_{ISO} Load Transient Response at 10% to 90% of 400 mA Load, f_{SW} = 500 kHz, 5 V Input to 5 V Output

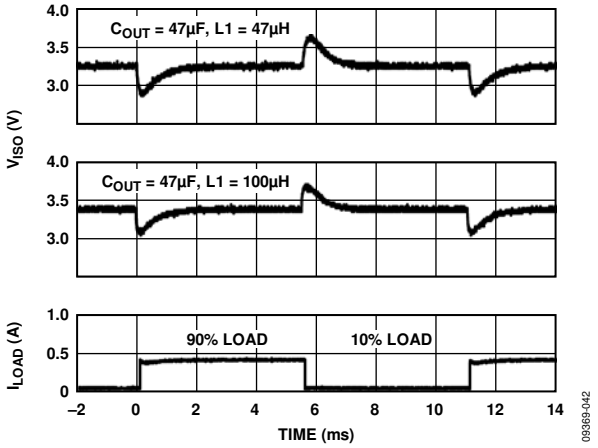


Figure 31. Typical V_{ISO} Load Transient Response at 10% to 90% of 400 mA Load, f_{SW} = 500 kHz, 5 V Input to 3.3 V Output

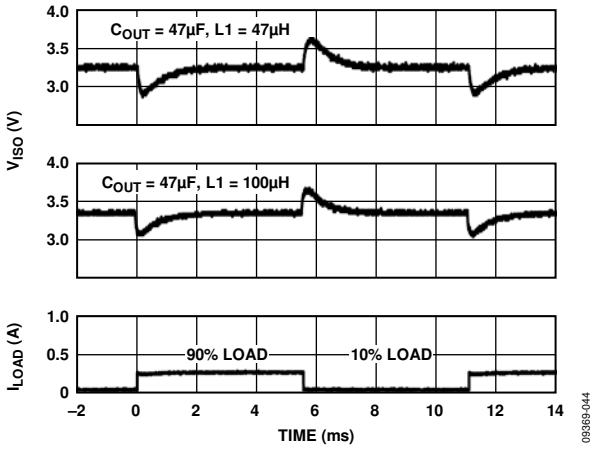


Figure 32. Typical V_{ISO} Load Transient Response at 10% to 90% of 250 mA Load, f_{SW} = 500 kHz, 3.3 V Input to 3.3 V Output

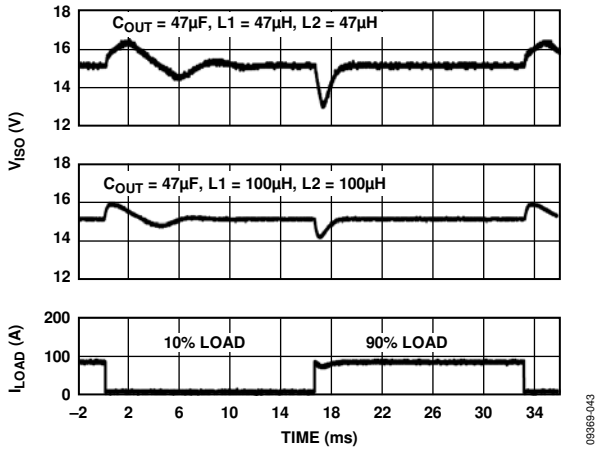


Figure 33. Typical V_{ISO} Load Transient Response at 10% to 90% of 100 mA Load, f_{SW} = 500 kHz, 5 V Input to 15 V Output

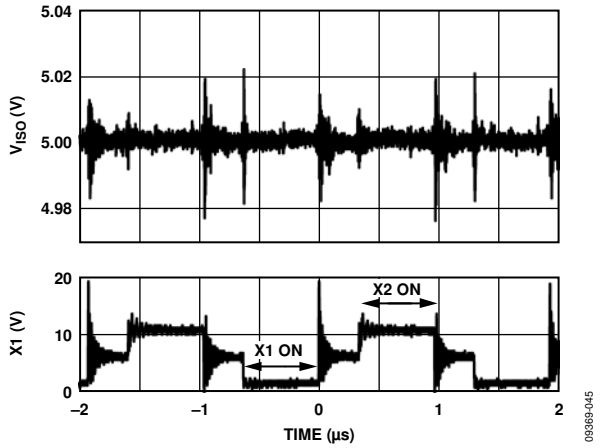


Figure 34. Typical V_{ISO} Output Voltage Ripple at 400 mA Load, f_{SW} = 500 kHz, 5 V Input to 5 V Output

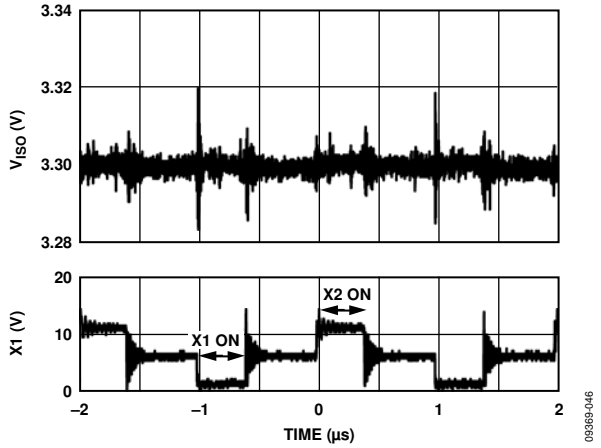


Figure 35. Typical V_{ISO} Output Voltage Ripple at 400 mA Load, f_{SW} = 500 kHz, 5 V Input to 3.3 V Output

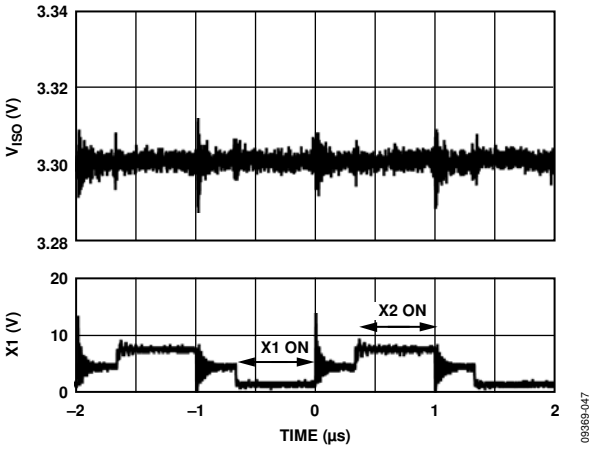


Figure 36. Typical V_{ISO} Output Voltage Ripple at 250 mA Load, f_{SW} = 500 kHz, 3.3 V Input to 3.3 V Output

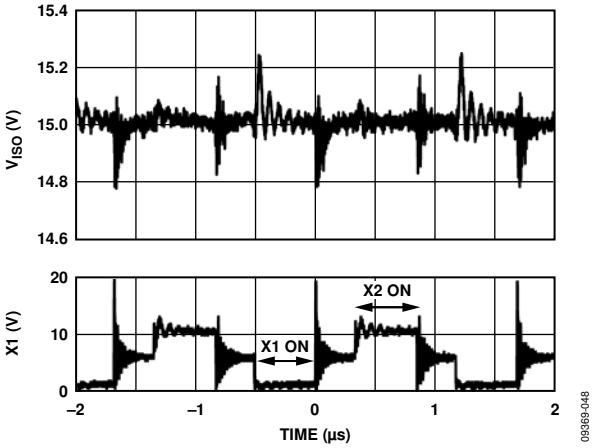


Figure 37. Typical V_{ISO} Output Voltage Ripple at 100 mA Load, f_{SW} = 500 kHz, 5 V Input to 15 V Output

TERMINOLOGY

$I_{DD1 (Q)}$
$I_{DD1 (Q)}$ is the minimum operating current drawn at the V_{DD1} power input when there is no external load at V_{ISO} and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current.

$I_{DD1 (D)}$
$I_{DD1 (D)}$ is the typical input supply current with all channels simultaneously driven at a maximum data rate of 25 Mbps with the full capacitive load representing the maximum dynamic load conditions. Treat resistive loads on the outputs separately from the dynamic load.

$I_{DD1 (MAX)}$
$I_{DD1 (MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

t_{PHL} Propagation Delay
The t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

t_{PLH} Propagation Delay
The t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew (t_{PSK})
t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel-to-Channel Matching
Channel-to-channel matching is the absolute value of the difference in propagation delays between two channels when operated with identical loads.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate
The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM347x uses a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DD1} power is supplied to an oscillating circuit that switches current to the primary side of an external power transformer using internal push-pull switches at the X1 and X2 pins. Power transferred to the secondary side of the transformer is full wave rectified with external Schottky diodes (D1 and D2), filtered with the L1 inductor and C_{OUT} capacitor, and regulated to the isolated power supply voltage from 3.3 V to 15 V.

The secondary (V_{ISO}) side controller regulates the output using a feedback voltage, V_{FB}, from a resistor divider on the output to create a PWM control signal that is sent to the primary (V_{DD1}) side by a dedicated *i*Coupler data channel labeled V_{FB}. The primary side PWM converter varies the duty cycle of the X1 and X2 switches to modulate the oscillator circuit and control the power being sent to the secondary side. This feedback allows for significantly higher power and efficiency.

The ADuM347x devices implement undervoltage lockout (UVLO) with hysteresis on the V_{DDA} power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

A minimum load current of 10 mA is recommended to ensure optimum load regulation. Smaller loads can generate excess noise on the output due to short or erratic PWM pulses. Excess noise generated in this way can cause regulation problems in some circumstances.

APPLICATION SCHEMATICS

The ADuM347x devices have three main application schematics, as shown in Figure 38 to Figure 40. Figure 38 has a center-tapped secondary and two Schottky diodes that provide full wave rectification for a single output, typically for power supplies of 3.3 V, 5 V, 12 V, and 15 V. For single supplies when V_{ISO} = 3.3 V or 5 V, V_{REG}, V_{DD2}, and V_{ISO} can be connected together.

Figure 39 shows a voltage doubling circuit that can be used for a single supply with an output that exceeds 15 V; 15 V is the largest supply that can be connected to the regulator input, V_{REG} (Pin 20). In the circuit shown in Figure 39, the output voltage can be as high as 24 V, and the voltage at the V_{REG} pin can be as high as 12 V. When using the circuit shown in Figure 39 to obtain an output voltage lower than 10 V (for example, V_{DD1} = 3.3 V, V_{ISO} = 5 V), connect V_{REG} to V_{ISO} directly.

Figure 40, which also uses a voltage doubling secondary circuit, is an example of a coarsely regulated, positive power supply and an unregulated, negative power supply for outputs of approximately ±5 V, ±12 V, and ±15 V.

For all the circuits shown in Figure 38 to Figure 40, the isolated output voltage (V_{ISO}) can be set with the voltage dividers, R1 and R2 (values 1 kΩ to 100 kΩ) using the following equation:

$$V_{ISO} = V_{FB} \times (R1 + R2)/R2$$

where V_{FB} is the internal feedback voltage (approximately 1.25 V).

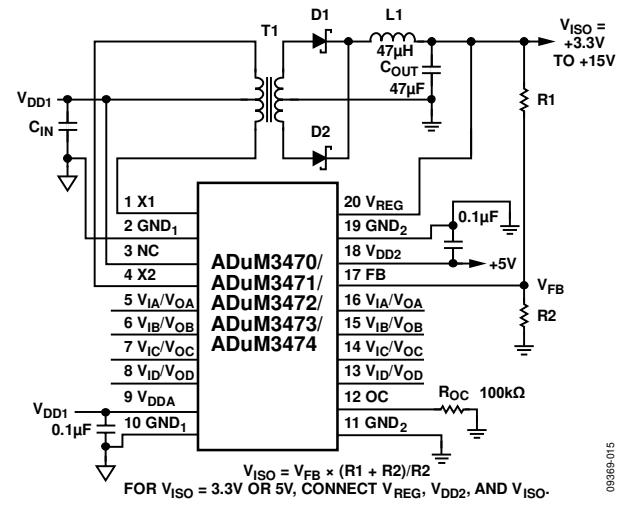


Figure 38. Single Power Supply

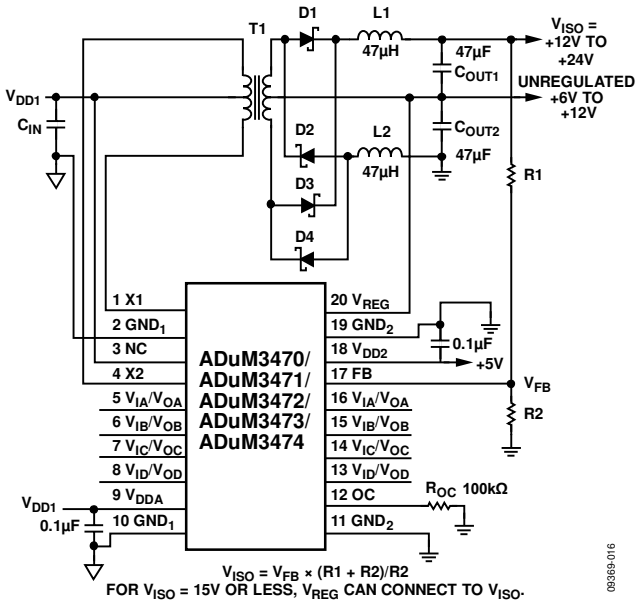


Figure 39. Doubling Power Supply

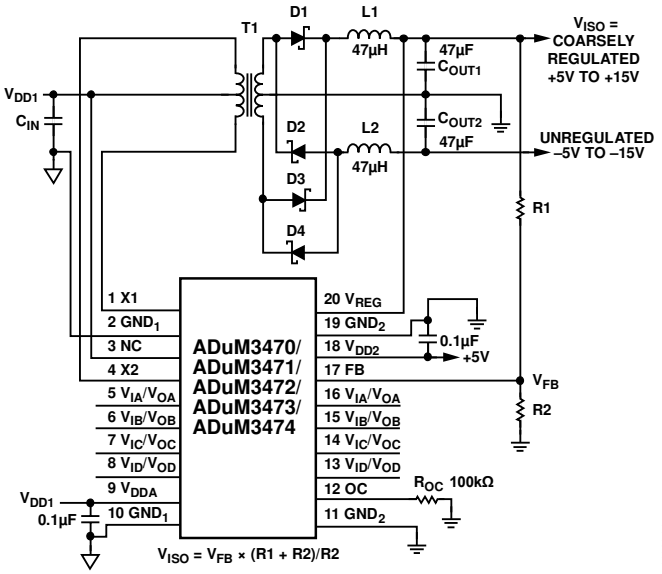


Figure 40. Positive Supply and Unregulated Negative Supply