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Isolated Switching Regulator with Quad-Channel Isolators

Data Sheet **ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474**

FEATURES

- Isolated PWM feedback with built in compensation
- Primary side transformer driver for up to 2.5 W output power with 5 V input voltage
- Regulated adjustable output: 3.3 V to 24 V
- Up to 80% efficiency
- Quad dc-to-25 Mbps (NRZ) signal isolation channels
- 200 kHz to 1 MHz adjustable oscillator
- Soft start function at power-up
- Pulse-by-pulse overcurrent protection
- Thermal shutdown
- 5000 V rms isolation
- High common-mode transient immunity: >25 kV/µs
- 20-lead SOIC package with 8.3 mm creepage
- High temperature operation: 105°C

APPLICATIONS

- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Process controls
- RS-232/RS-422/RS-485 transceivers

FUNCTIONAL BLOCK DIAGRAM

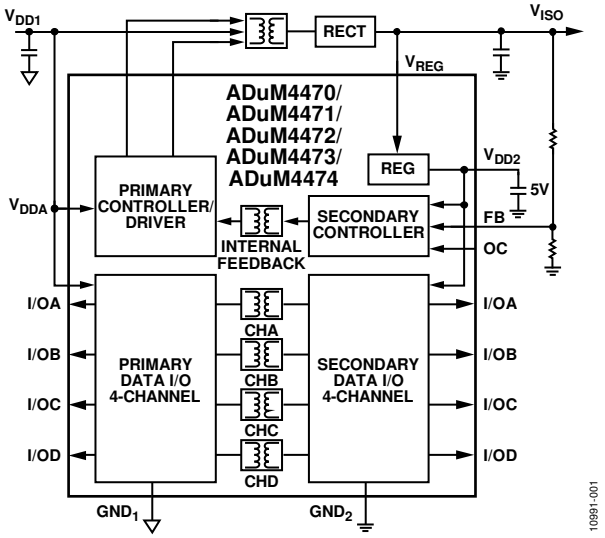

Figure 1.

GENERAL DESCRIPTION

The ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474[1] are quad-channel, digital isolators with a regulated dc-to-dc isolated power supply controller and an internal MOSFET driver. The dc-to-dc controller has an internal isolated PWM feedback from the secondary side, based on the *i*Coupler® chip scale transformer technology and complete loop compensation. This eliminates the need to use an optocoupler for feedback and compensates the loop for stability.

The ADuM447x isolators provide a more stable output voltage and higher efficiency compared to unregulated isolated dc-to-dc power supplies. The fully integrated feedback and loop compensation in a wide-body SOIC package provide a smaller form factor and 8.3 mm creepage distance solution.

The regulated feedback provides a relatively flat efficiency curve over the full output power range. The ADuM447x enable a dc-to-dc converter with a 3.3 V to 24 V isolated output voltage range from either a 5.0 V or a 3.3 V input voltage, with an output power of up to 2.5 W.

The ADuM447x isolators provide four independent isolation channels in a variety of channel configurations and data rates. (The x in ADuM447x throughout this data sheet stands for the ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474.)

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7075 329 B2. Other patents pending.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/12—Revision 0: Initial Version

BLOCK DIAGRAMS OF I/O CHANNELS

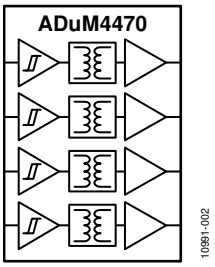

Figure 2. ADuM4470

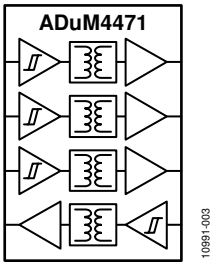

Figure 3. ADuM4471

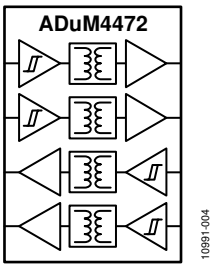

Figure 4. ADuM4472

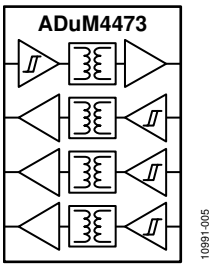

Figure 5. ADuM4473

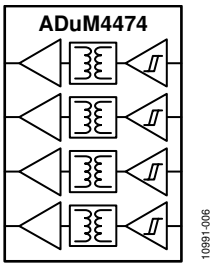

Figure 6. ADuM4474

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ (V_{DD1} = V_{DDA}) ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 5.0 V.

Table 1. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	4.5	5.0	5.5	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF||47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	400	500		mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			72		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			14	30	mA	
ADuM4471			15	30	mA	
ADuM4472			16	30	mA	
ADuM4473			17	30	mA	
ADuM4474			18	30	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			44		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			46		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			48		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			50		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			52		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			390		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			388		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			386		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			384		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			382		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			550		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

3.0 V ≤ V_{DD1} = V_{DDA} ≤ 3.6 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 3.3 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 2. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.6		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	250			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			68		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1MHz
ADuM4470			9	20	mA	
ADuM4471			10	20	mA	
ADuM4472			11	20	mA	
ADuM4473			11	20	mA	
ADuM4474			12	20	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			28		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			29		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			31		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			32		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			34		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			244		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			243		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			241		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			240		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			238		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			350		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}	1.6			V	
Logic Low Input Threshold	V_{IL}			0.4	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		60	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	60	70	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			8	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 3. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	400			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			70		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			9	30	mA	
ADuM4471			10	30	mA	
ADuM4472			11	30	mA	
ADuM4473			11	30	mA	
ADuM4474			12	30	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			393		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			392		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			390		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			389		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			375		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			350		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	50	70	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			8	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/15 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{REG} = V_{ISO} = 15 V; V_{DD2} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 49. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{REG} = V_{ISO} = 15 V, V_{DD2} = 5.0 V.

Table 4. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	13.8	15	16.2	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
V_{DD2} Linear Regulator						
Regulator Voltage		4.5	5.0	5.5	V	V_{REG} = 7 V to 15 V, I_{DD2} = 0 mA to 50 mA
Dropout Voltage			0.5	1.5		I_{DD2} = 50 mA
Line Regulation	$V_{ISO (LINE)}$		1	20	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	3	%	I_{ISO} = 20 mA to 80 mA
Output Ripple	$V_{ISO (RIP)}$		200		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		500		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	100			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			78		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			25	45	mA	
ADuM4471			27	45	mA	
ADuM4472			29	45	mA	
ADuM4473			31	45	mA	
ADuM4474			33	45	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			73		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			83		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			93		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			102		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			112		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			91		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			89		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			86		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			83		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			80		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			425		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[2]
Thermal Shutdown						
Thermal Shutdown Threshold	TS_{SD}		150		°C	T_J rising
Thermal Shutdown Hysteresis	TS_{SD-HYS}		20		°C	

[1] The device is considered a 2-terminal device: Pin 1 to Pin 10 are shorted together; and Pin 11 to Pin 20 are shorted together.
[2] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS (PENDING)

Table 6.

UL	CSA	VDE
Recognized under the UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 5000 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage Reinforced insulation per CSA60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Reinforced insulation per IEC 60601-1 250 V rms (353 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM447x is proof tested by applying an insulation test voltage of ≥6000 V rms for 1 sec (current leakage detection limit = 10 μA).
[2] In accordance with DIN V VDE V 0884-10, each of the ADuM447x is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 7.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 8.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 7)			
Case Temperature		T_S	150	°C
Side 1, Side 2 P_{VDDA}, P_{VREG} Power Dissipation		P_{VDDA}, P_{VREG}	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

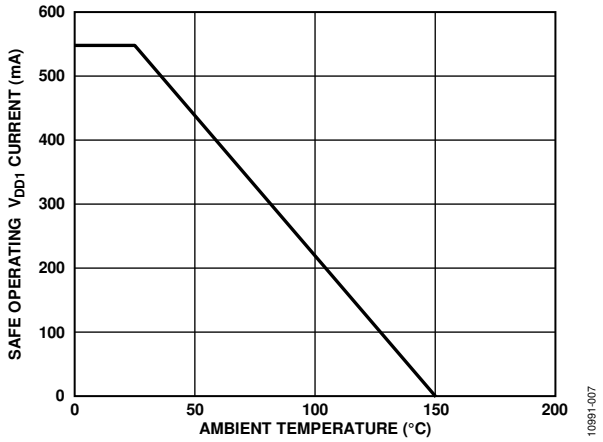

Figure 7. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 9.

Parameter	Symbol	Min	Max	Unit
Temperature				
Operating Temperature	T_A	−40	+105	°C
Supply Voltage				
V_{DD1} at $V_{ISO} = 3.3$ V	V_{DD1}	3.0	3.6	V
V_{DD1} at $V_{ISO} = 3.3$ V	V_{DD1}	4.5	5.5	V
V_{DD1} at $V_{ISO} = 5.0$ V	V_{DD1}	4.5	5.5	V
Load				
Minimum Load	$I_{ISO(MIN)}$	10		mA

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages	
V_{DDA}, V_{DD2} [1, 2]	−0.5 V to +7.0 V
V_{REG}, X1, X2[1]	−0.5 V to +20.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID})	−0.5 V to +V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO} +0.5 V
Average Output Current per Pin	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DD1} is the power supply for the push-pull transformer, and V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	848	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	848	V peak	50-year minimum lifetime
DC Voltage	848	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

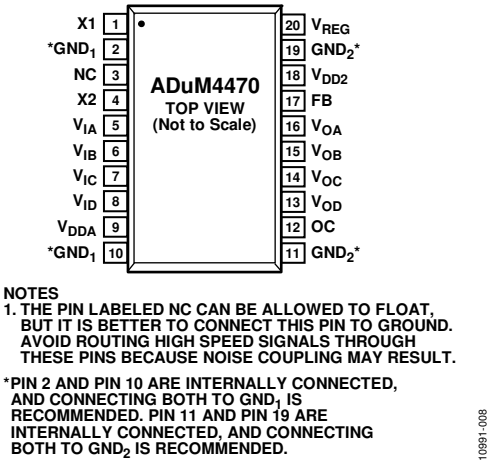

Figure 8. ADuM4470 Pin Configuration

Table 12. ADuM4470 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 8).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{ID}	Logic Input D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{OD}	Logic Output D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

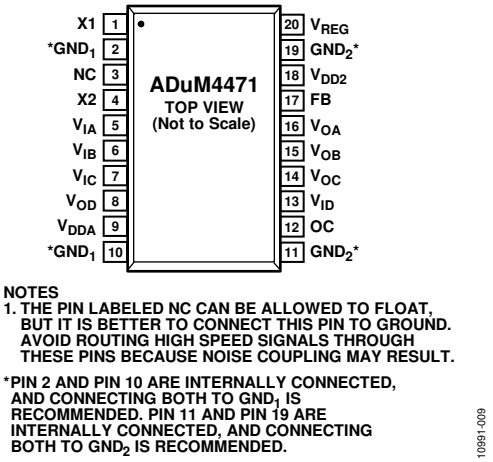

Figure 9. ADuM4471 Pin Configuration

Table 13. ADuM4471 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 9).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

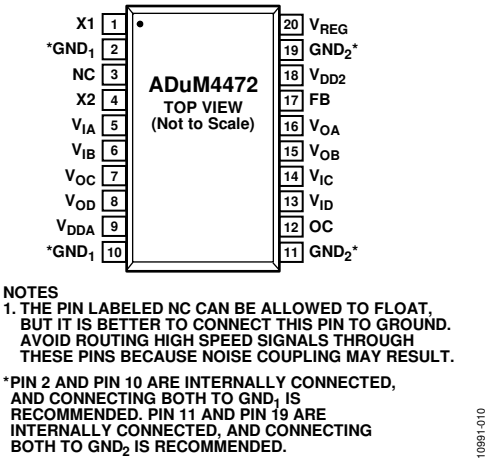

Figure 10. ADuM4472 Pin Configuration

Table 14. ADuM4472 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 10).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

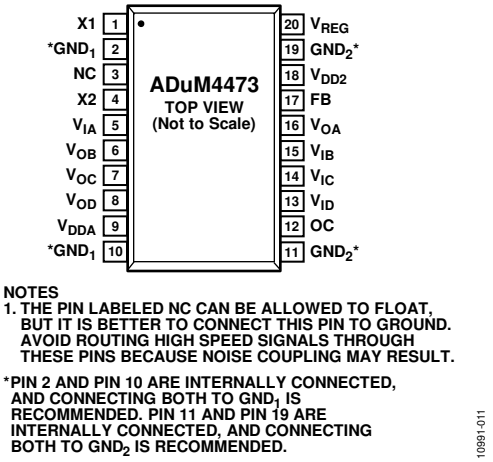

Figure 11. ADuM4473 Pin Configuration

Table 15. ADuM4473 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 11).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

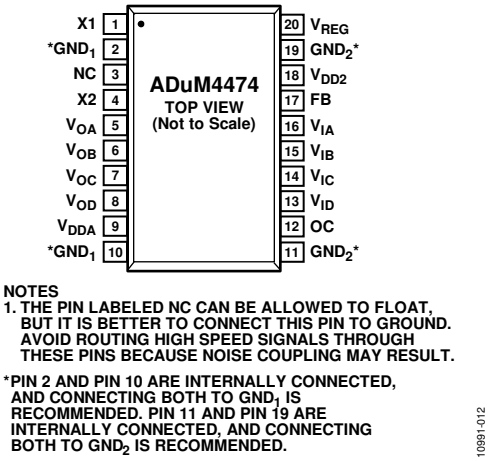

Figure 12. ADuM4474 Pin Configuration

Table 16. ADuM4474 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 12).
4	X2	Transformer Driver Output 2.
5	V_{OA}	Logic Output A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{IA}	Logic Input A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

TYPICAL PERFORMANCE CHARACTERISTICS

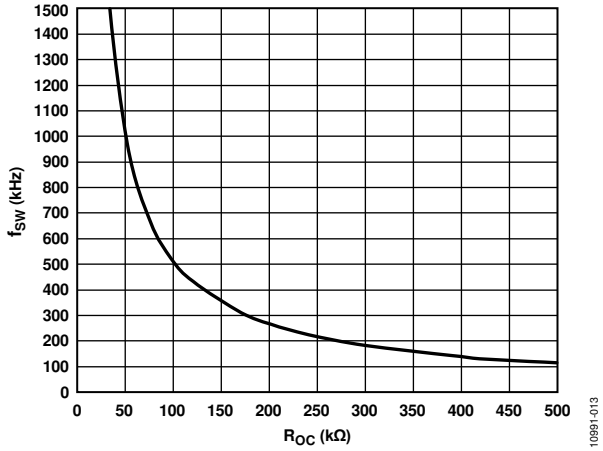

Figure 13. Switching Frequency (f_{SW}) vs. R_{OC} Resistance

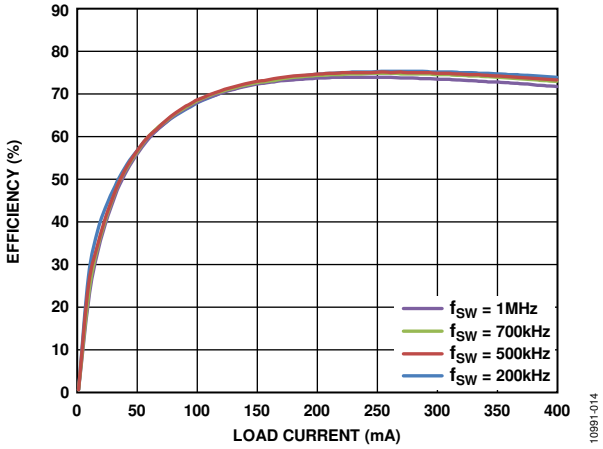

Figure 14. Typical Efficiency at 5 V Input to 5 V Output at Various Switching Frequencies with 1:2 Coilcraft Transformer (CR7983-CL)

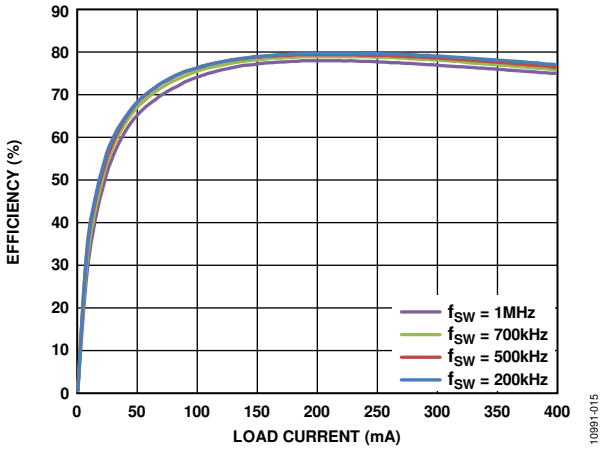

Figure 15. Typical Efficiency at 5 V Input to 5 V Output at Various Switching Frequencies with1:2 Halo Transformer (TGSAD-260V8LF)

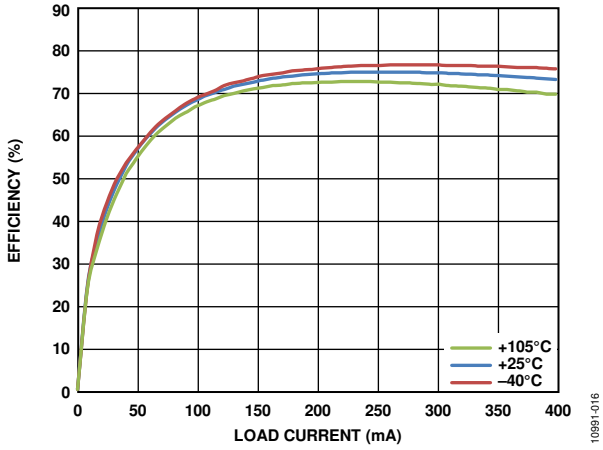

Figure 16. 5 V Input to 5 V Output Efficiency over Temperature with Coilcraft Transformer (CR7983-CL) at 500 kHz f_{SW}

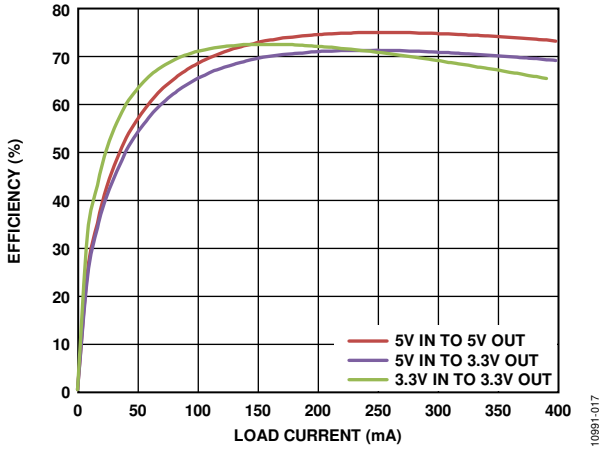

Figure 17. Single-Supply Efficiency with Coilcraft Transformer (CR7983-CL) at 500 kHz f_{SW}

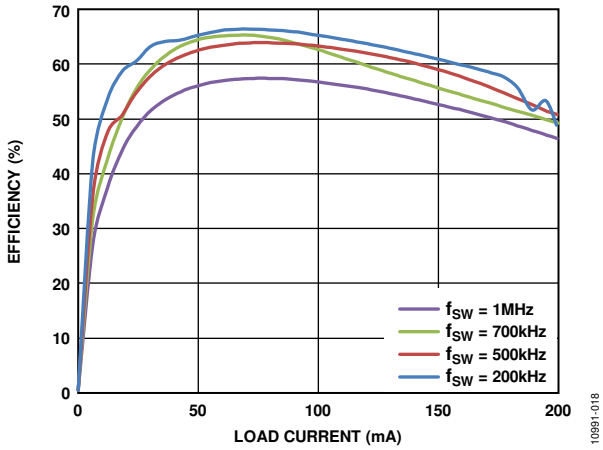

Figure 18. Typical Efficiency at 3.3 V Input to 5 V Output at Various Switching Frequencies with 1:3 Coilcraft Transformer (CR7984-CL)

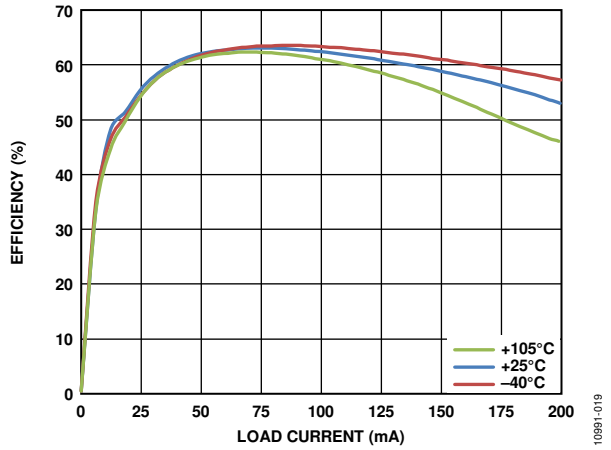

Figure 19. Typical Efficiency at 3.3 V In to 5 V Out over Temperature with 1:3 Coilcraft Transformer (CR7984-CL) at 500 kHz f_{sw}

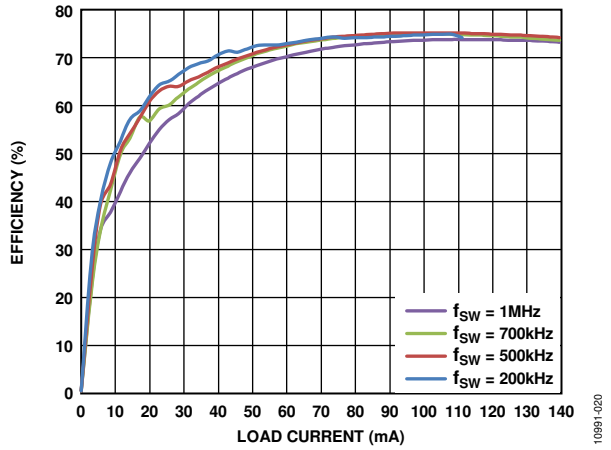

Figure 20. 5 V Input to 15 V Output Efficiency at Various Switching Frequencies with 1: 3 Coilcraft Transformer (CR7984-CL)

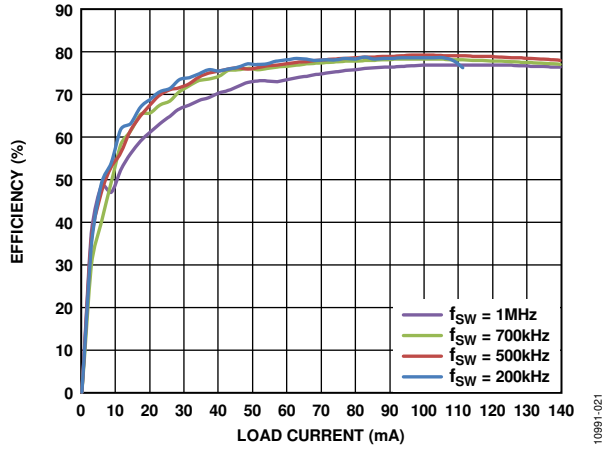

Figure 21. 5 V Input to 15 V Output Efficiency at Various Switching Frequencies with 1:3 Halo Transformer (TGSAD-290V8LF)

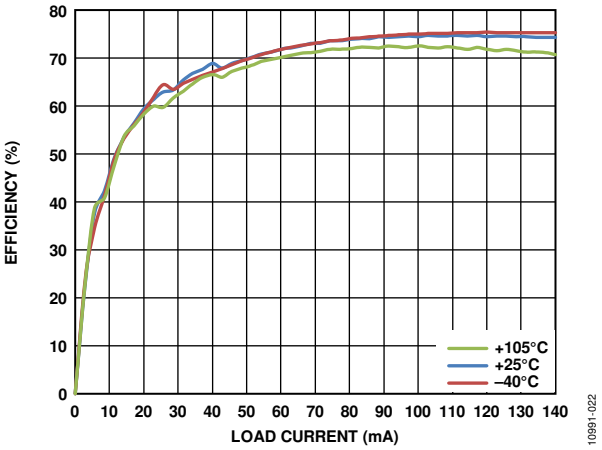

Figure 22. 5 V Input to 15 V Output Efficiency over Temperature with Coilcraft Transformer (CR7984-CL) at 500 kHz f_{SW}

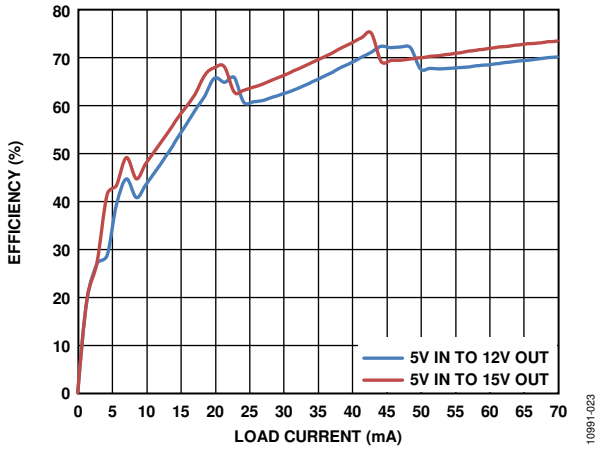

Figure 23. Double-Supply Efficiency with Coilcraft Transformer (CR7985-CL) at 500 kHz f_{SW}

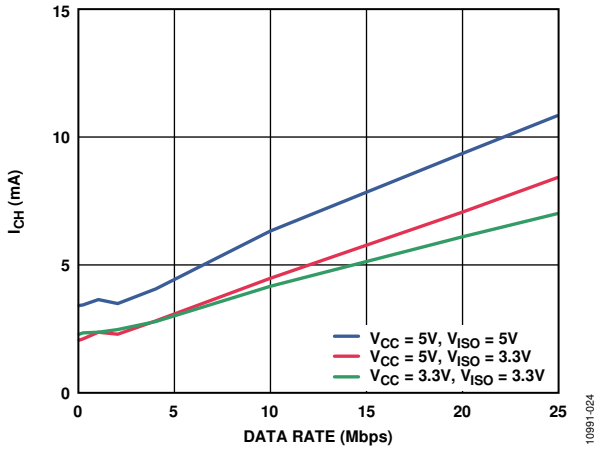

Figure 24. Typical Single-Supply I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

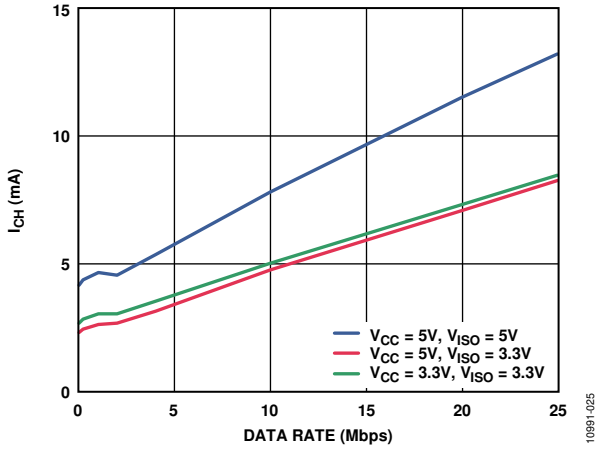

Figure 25. Typical Single-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load)

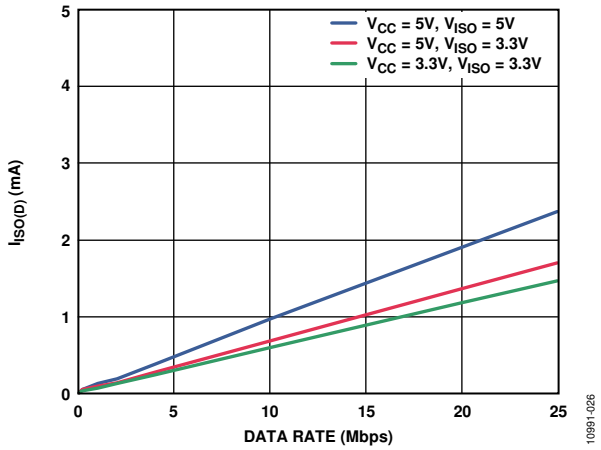

Figure 26. Typical Single-Supply $I_{ISO(D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

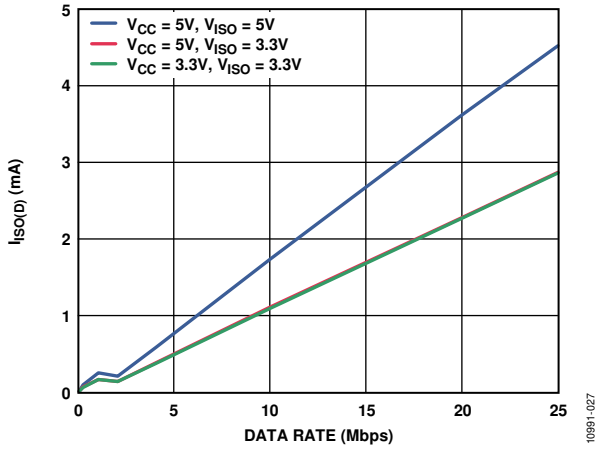

Figure 27. Typical Single-Supply $I_{ISO(D)}$ Dynamic Supply Current per Input Channel (15 pF Output Load)

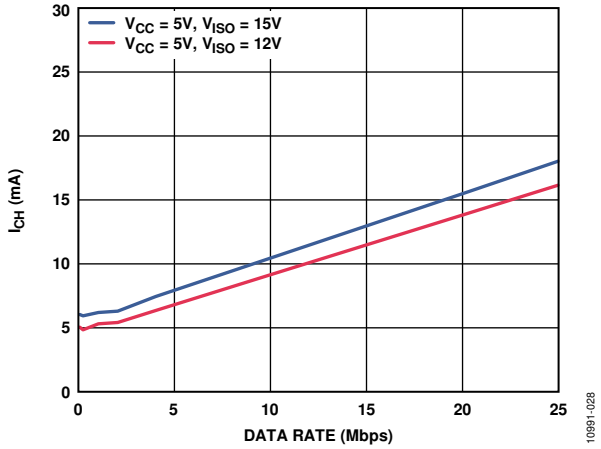

Figure 28. Typical Double-Supply Current I_{CH} Per Forward Data Channel (15 pF Output Load)

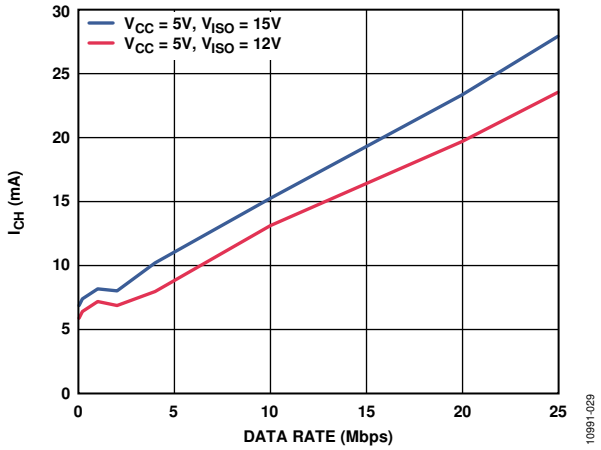

Figure 29. Typical Double-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Data)

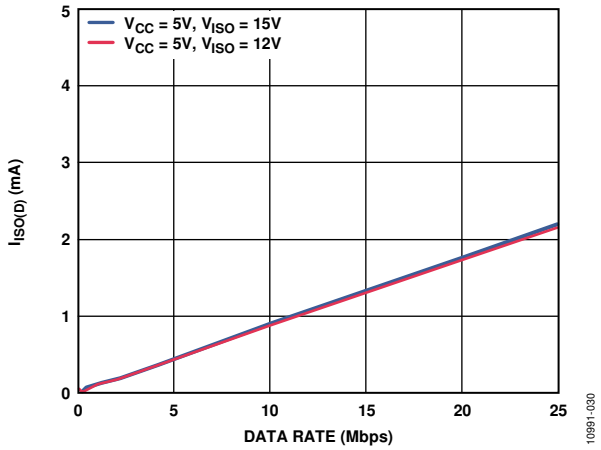

Figure 30. Typical Double-Supply $I_{ISO(D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

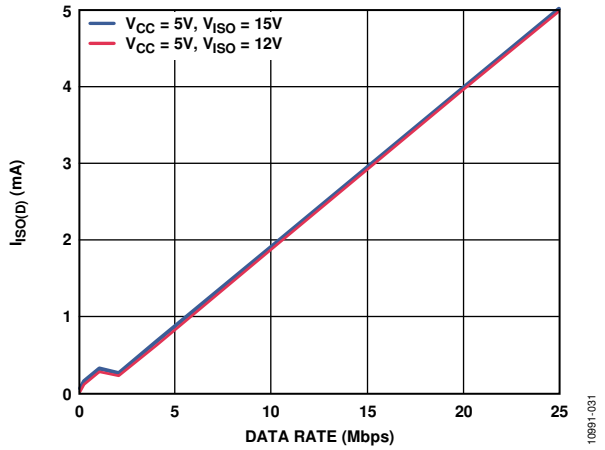

Figure 31. Typical Double-Supply $I_{ISO(D)}$ Dynamic Supply Current per Input Channel

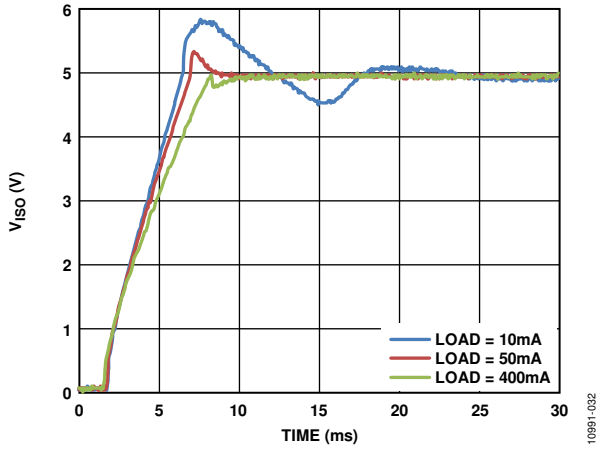

Figure 32. Typical V_{ISO} Startup 5 V Input to 5 V Output with 10 mA, 50 mA, and 400 mA Output Load

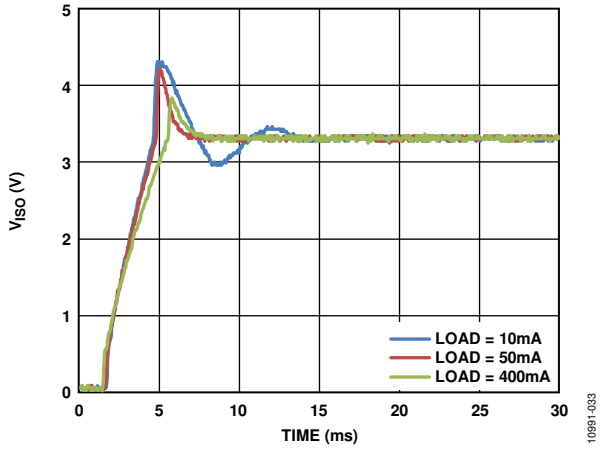

Figure 33. Typical V_{ISO} Startup 5 V Input to 3.3 V Output with 10 mA, 50 mA, and 400 mA Output Load

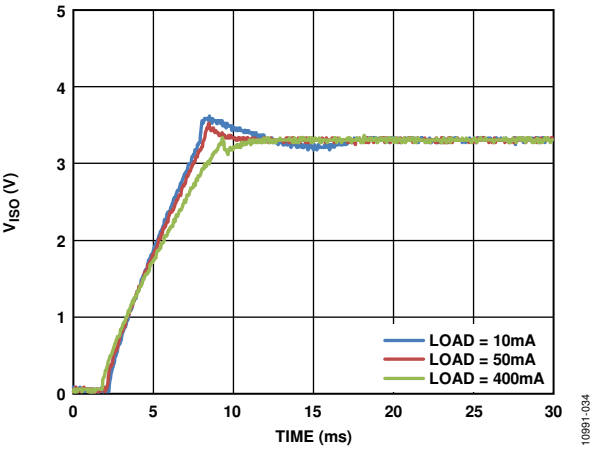

Figure 34. Typical V_{ISO} Startup 3.3 V Input to 3.3 V Output with 10 mA, 50 mA, and 250 mA Output Load

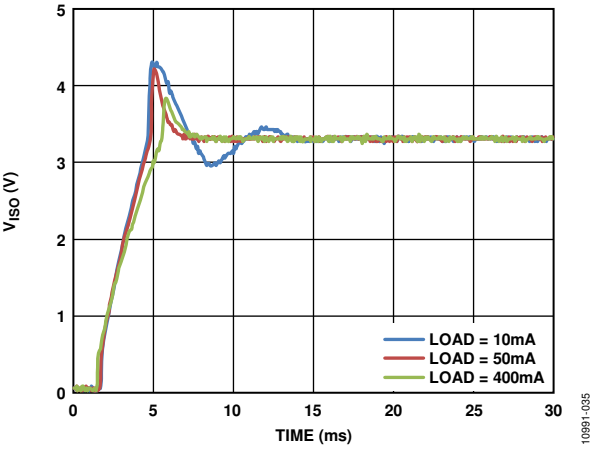

Figure 35. Typical V_{ISO} Startup 5 V Input to 15 V Output with 10 mA, 20 mA, and 100 mA Output Load

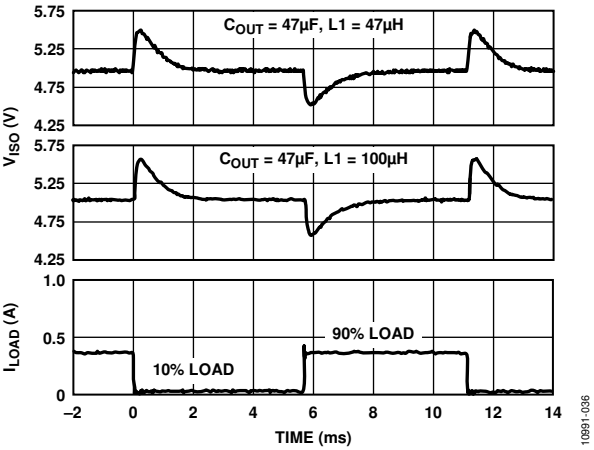

Figure 36. Typical V_{ISO} Load Transient Response 5 V Input to 5 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW}

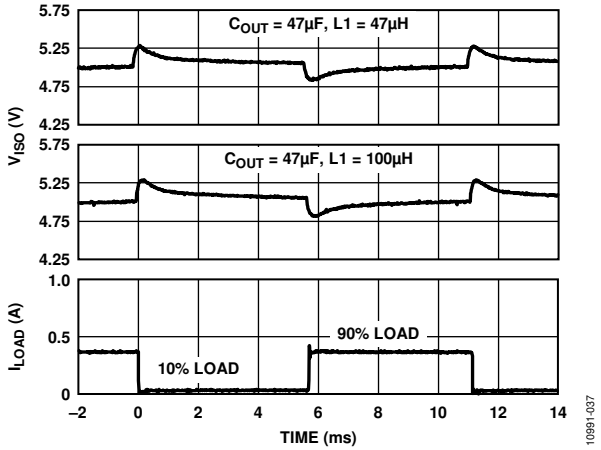

Figure 37. Typical V_{ISO} Load Transient Response 5 V Input to 5 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

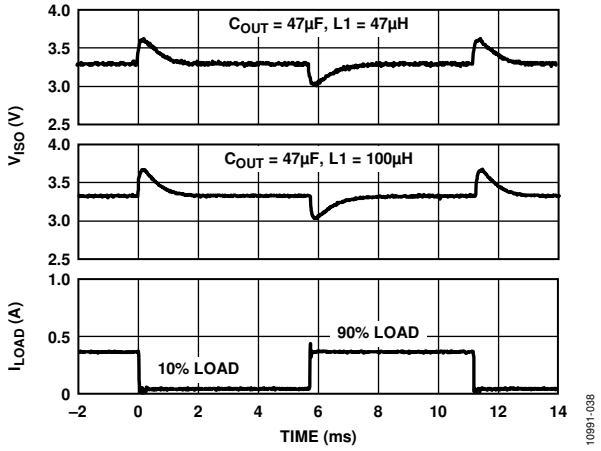

Figure 38. Typical V_{ISO} Load Transient Response 5 V Input to 3.3 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW}

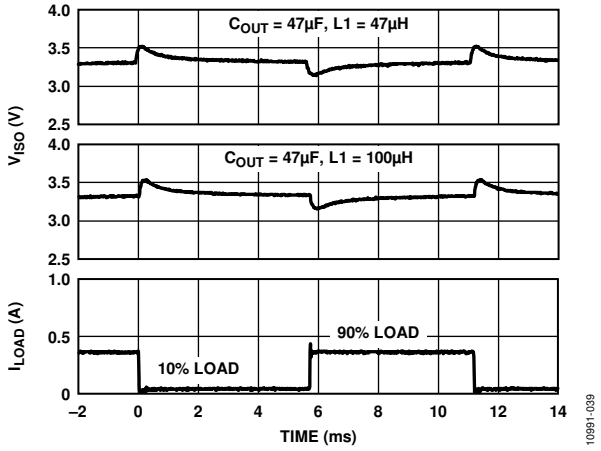

Figure 39. Typical V_{ISO} Load Transient Response 5 V Input to 3.3 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

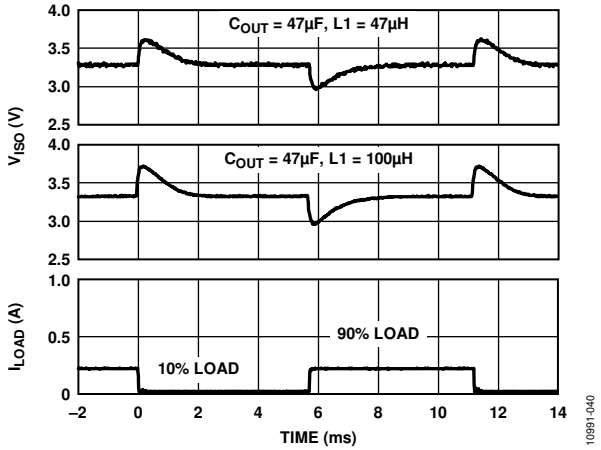

Figure 40. Typical V_{ISO} Load Transient Response 3.3 V Input to 3.3 V Output at 10% to 90% of 250 mA Load at 500 kHz f_{SW}

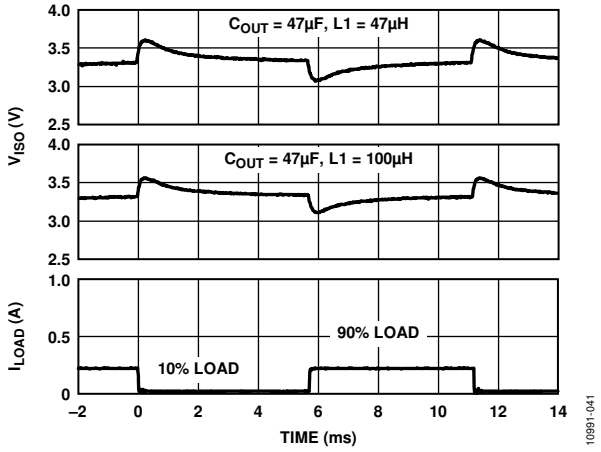

Figure 41. Typical V_{ISO} Load Transient Response 3.3 V Input to 3.3 V Output at 10% to 90% of 250 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

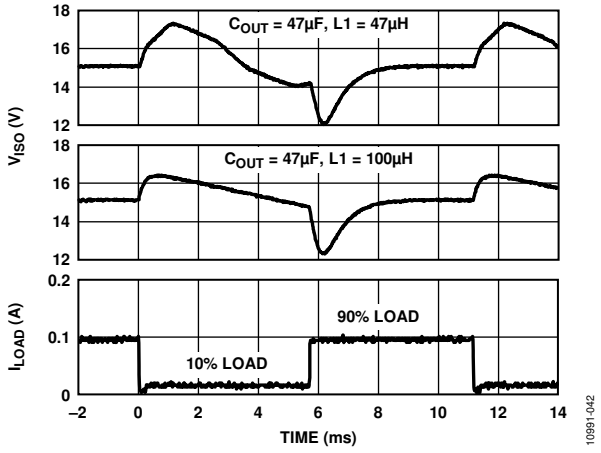

Figure 42. Typical V_{ISO} Load Transient Response 5 V Input to 15 V Output at 10% to 90% of 100 mA Load at 500 kHz f_{SW}

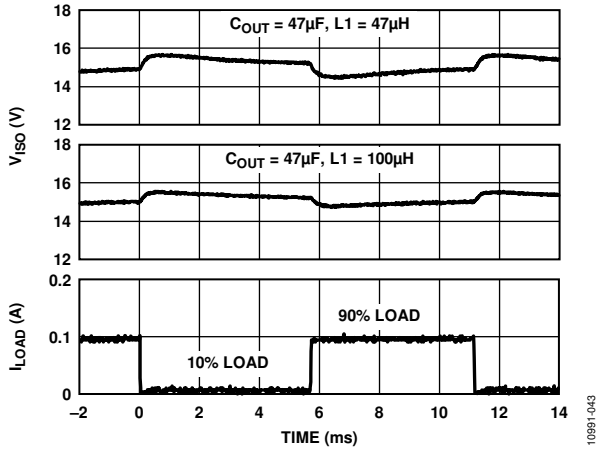

Figure 43. Typical V_{ISO} Load Transient Response 5 V Input to 15 V Output at 10% to 90% of 100 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

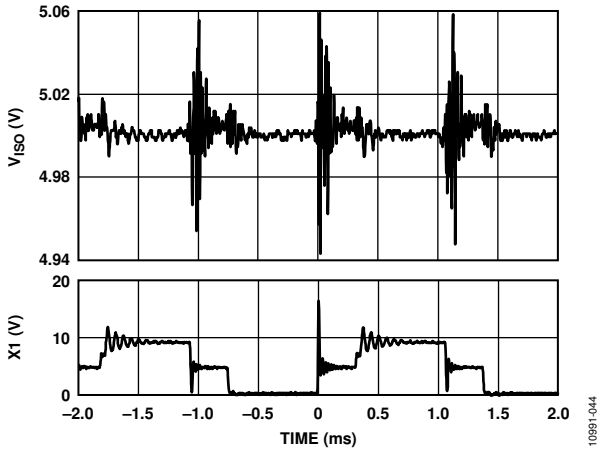

Figure 44. Typical V_{ISO} Output Ripple, 5 V Input to 5 V Output at 400 mA Load at 500 kHz f_{SW}

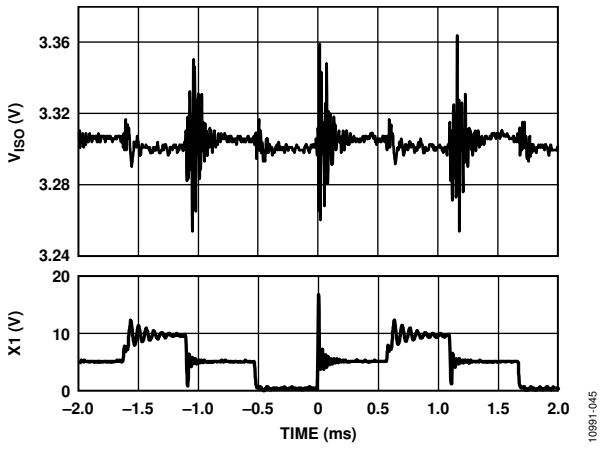

Figure 45. Typical V_{ISO} Output Ripple, 5 V Input to 3.3 V Output at 400 mA Load at 500 kHz f_{SW}

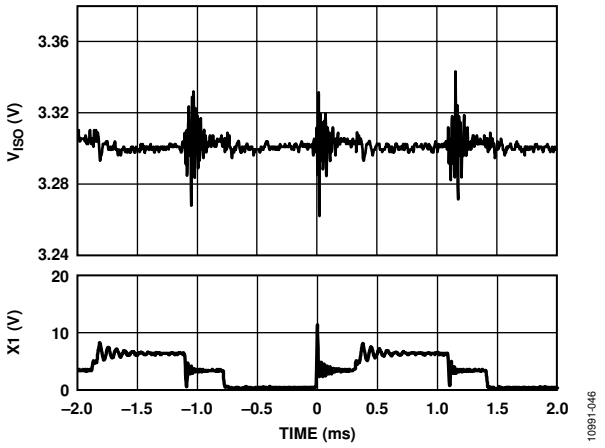

Figure 46. Typical V_{ISO} Output Ripple, 3.3 V Input to 3.3 V Output at 250 mA Load at 500 kHz f_{SW}

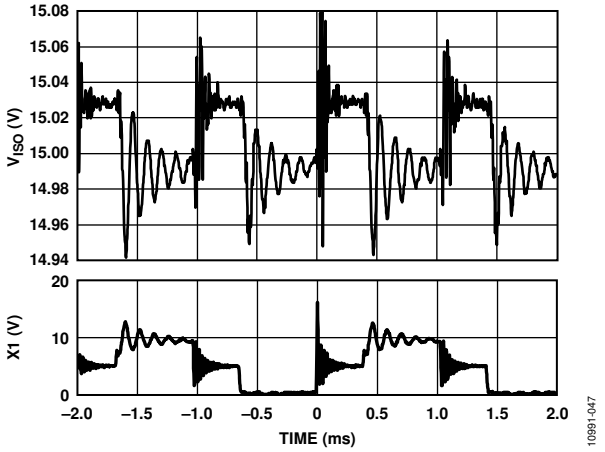

Figure 47. Typical V_{ISO} Output Ripple, 5 V Input to 15 V Output at 100 mA Load at 500 kHz f_{SW}