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Quad-Channel Isolators with Integrated DC-to-DC Converters

Data Sheet

ADuM5410/ADuM5411/ADuM5412

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- Up to 150 mW output power
- Quad dc to 150 Mbps signal isolation channels
- 24-lead SSOP package with 5.3 mm minimum creepage
- High temperature operation: 105°C
- High common-mode transient immunity: 100 kV/µs
- Safety and regulatory approvals
  - UL recognition (pending)
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 565 V peak

APPLICATIONS

- RS-232 transceivers
- Power supply startup bias and gate drives
- Isolated sensor interfaces
- Industrial PLCs

GENERAL DESCRIPTION

The ADuM5410/ADuM5411/ADuM5412[1] are quad-channel digital isolators with *iso*Power®, integrated, isolated dc-to-dc converters. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converters provide regulated, isolated power that is adjustable between 3.15 V and 5.25 V. Popular voltage combinations and the associated power levels are shown in Table 1.

The ADuM5410/ADuM5411/ADuM5412 eliminate the need for a separate, isolated dc-to-dc converter in low power, isolated designs. The *i*Coupler chip scale transformer technology is used for isolated logic signals and for the magnetic components of the dc-to-dc converters. The result is a small form factor, total isolation solution.

The ADuM5410/ADuM5411/ADuM5412 isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide for more information).

FUNCTIONAL BLOCK DIAGRAM

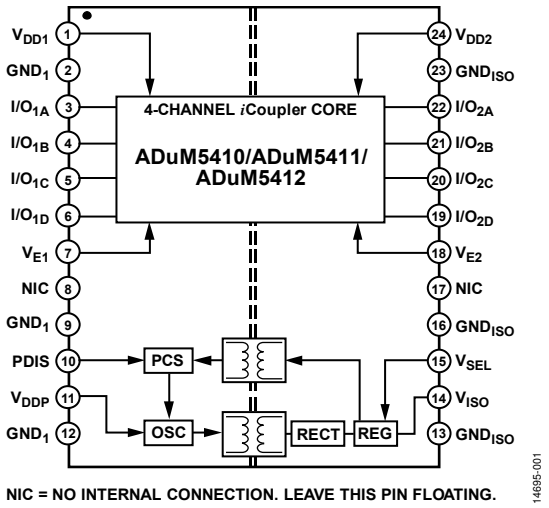

Figure 1.

Table 1. Power Levels

Input Voltage (V)	Output Voltage (V)	Output Power (mW)
5	5	150
5	3.3	100
3.3	3.3	66

Table 2. Data Input/Output Port Assignments

Ch.	Pin No.	ADuM5410	ADuM5411	ADuM5412
I/O_{1A}	3	V_{IA}	V_{IA}	V_{IA}
I/O_{1B}	4	V_{IB}	V_{IB}	V_{IB}
I/O_{1C}	5	V_{IC}	V_{IC}	V_{OC}
I/O_{1D}	6	V_{ID}	V_{OD}	V_{OD}
I/O_{2A}	22	V_{OA}	V_{OA}	V_{OA}
I/O_{2B}	21	V_{OB}	V_{OB}	V_{OB}
I/O_{2C}	20	V_{OC}	V_{OC}	V_{IC}
I/O_{2D}	19	V_{OD}	V_{ID}	V_{ID}

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

7/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDP} = V_{ISO} = 5 V, V_{SEL} resistor network: R1 = 10 kΩ ±1%, R2 = 30.9 kΩ ± 1% between V_{ISO} and GND_{ISO} (see Figure 31). Minimum/maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DD1}, V_{DDP}, V_{ISO} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 3. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Setpoint	V_{ISO}	4.7	5.0	5.4	V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 30.9 kΩ
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	30			mA	V_{ISO} > 4.5 V
Efficiency at $I_{ISO (MAX)}$			29		%	I_{ISO} = 27 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		104	140	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 4. Data Channel Supply Current Specifications

		1 Mbps			25 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM5410	I_{DD1}		6.8	10		7.8	12		11.8	17.4	mA	
	I_{DD2}		2.1	3.7		3.9	5.7		9.2	13	mA	
ADuM5411	I_{DD1}		5.8	10.3		7.0	10.9		11.4	15.9	mA	
	I_{DD2}		4.0	6.85		5.5	8.5		10.3	14.0	mA	
ADuM5412	I_{DD1}		4.3	7.7		6.0	9.3		10.3	14.2	mA	
	I_{DD2}		5.3	8.7		6.7	10.1		11.0	14.9	mA	

Table 5. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate				150	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter			490		ps p-p	
			70		ps rms	

Table 6. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{ISO} or 0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{ISO} or 0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD1} − 0.2 or V_{DD2} − 0.2	V_{DD1} or V_{DD2}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DD1} − 0.5 or V_{DD2} − 0.5	V_{DD1} − 0.2 or V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM5410						
	$I_{DD1 (Q)}$		1.2	2.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		2.0	2.72	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		12.0	20.0	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		2.0	2.92	mA	V_{Ix} = Logic 1
ADuM5411						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.9	2.62	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		10.0	17.0	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		6.0	10.0	mA	V_{Ix} = Logic 1
ADuM5412						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.6	2.46	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.2	11.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		8.4	11.5	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] I_{Ox} is the Channel x output current, where x means A, B, C, or D.
[2] V_{IxH} is the input side logic high.
[3] V_{IxL} is the input side logic low.
[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDP} = V_{ISO} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ, ±1%, R2 = 16.9 kΩ ± 1% between V_{ISO} and GND_{ISO} (see Figure 31). Minimum/maximum specifications apply over the entire recommended operation range, which is 3.0 V ≤ V_{DD1}, V_{DDP}, V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 10 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 10 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 2 mA to 18 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	20			mA	3.6 V > V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			27		%	I_{ISO} = 18 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		77	115	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 8. Data Channel Supply Current Specifications

		1 Mbps			25 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM5410	I_{DD1}		6.6	9.8		7.4	11.2		10.7	15.9	mA	
	I_{DD2}		2.0	3.7		3.5	5.5		8.2	11.6	mA	
ADuM5411	I_{DD1}		5.65	10.1		6.65	10.5		10.4	14.9	mA	
	I_{DD2}		3.9	6.65		5.2	8.0		9.4	12.8	mA	
ADuM5412	I_{DD1}		4.3	7.7		5.6	9.0		9.1	13	mA	
	I_{DD2}		5.0	8.4		6.2	9.6		9.8	13.7	mA	

Table 9. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.7			ns	Within PWD limit
Data Rate				150	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3.0	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			640		ps p-p	
			75		ns rms	

Table 10. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{ISO} or 0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{ISO} or 0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD1} − 0.2 or V_{DD2} − 0.2	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{DD2} − 0.5	V_{DD1} − 0.2 or V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM5410						
	$I_{DD1 (Q)}$		1.2	2.12	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		2.0	2.68	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		12.0	19.6	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		2.0	2.8	mA	V_{Ix} = Logic 1
ADuM5411						
	$I_{DD1 (Q)}$		1.5	2.36	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.8	2.52	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.8	16.7	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.7	9.7	mA	V_{Ix} = Logic 1
ADuM5412						
	$I_{DD1 (Q)}$		1.6	2.4	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.6	2.4	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		8.4	11.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\|CM_H\|$	75	100		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDP} = 5.0 V, V_{ISO} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ ± 1%, R2 = 16.9 kΩ ±1% between V_{ISO} and GND_{ISO} (see Figure 31). Minimum/maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DD1} = V_{DDP} ≤ 5.5 V, 3.0 V ≤ V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 11. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	30			mA	3.6 V > V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			24		%	I_{ISO} = 27 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		85	115	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 12. Data Channel Supply Current Specifications

		1 Mbps			25 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM5410	I_{DD1}		6.8	10		7.8	12		11.8	17.4	mA	
	I_{DD2}		2.0	3.7		3.5	5.5		8.2	11.6	mA	
ADuM5411	I_{DD1}		5.8	10.3		7.0	10.9		11.4	15.9	mA	
	I_{DD2}		3.9	6.65		5.2	8.0		9.4	12.8	mA	
ADuM5412	I_{DD1}		4.3	7.7		6.0	9.3		10.3	14.2	mA	
	I_{DD2}		5.0	8.4		6.2	9.6		9.8	13.7	mA	

Table 13. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.7			ns	Within PWD limit
Data Rate				150	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3.0	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			640		ps p-p	
			75		ns rms	

Table 14. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{ISO} or 0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{ISO} or 0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD1} − 0.2 or V_{DD2} − 0.2	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{DD2} − 0.5	V_{DD1} − 0.2 or V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM5410						
	$I_{DD1 (Q)}$		1.2	2.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		2.0	2.68	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		12.0	20.0	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		2.0	2.8	mA	V_{Ix} = Logic 1
ADuM5411						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.8	2.52	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		10.0	17.0	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.7	9.7	mA	V_{Ix} = Logic 1
ADuM5412						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.6	2.4	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.2	11.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		8.4	11.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\|CM_H\|$	75	100		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 15. Data Channel Supply Current Specifications

		1 Mbps			25 Mbps			100 Mbps				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												C_L = 0 pF
ADuM5410	I_{DD1}		6.5	9.8		7.3	11.1		10.4	15.5	mA	
	I_{DD2}		2.0	3.6		3.3	5.2		7.3	10.2	mA	
ADuM5411	I_{DD1}		5.6	10.0		6.4	10.4		9.7	14.5	mA	
	I_{DD2}		3.8	6.55		4.8	7.7		8.3	11.5	mA	
ADuM5412	I_{DD1}		4.3	7.7		5.4	8.8		8.8	12.7	mA	
	I_{DD2}		5.0	8.4		6.1	9.5		9.5	13.4	mA	

Table 16. Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate				150	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			800		ps p-p	
			190		ps rms	

Table 17. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{ISO} or 0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{ISO} or 0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD1} − 0.2 or V_{DD2} − 0.2	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{DD2} − 0.5	V_{DD1} − 0.2 or V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM5410						
	$I_{DD1 (Q)}$		1.2	2.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		2.0	2.64	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.2	19.6	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		2.0	2.76	mA	V_{Ix} = Logic 1
ADuM5411						
	$I_{DD1 (Q)}$		1.46	2.32	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.75	2.47	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.7	16.6	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.67	9.67	mA	V_{Ix} = Logic 1
ADuM5412						
	$I_{DD1 (Q)}$		1.6	2.32	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.6	2.32	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		8.4	11.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\|CM_H\|$	75	100		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 1.8 V. Minimum/maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 18. Data Channel Supply Current Specifications

		1 Mbps			25 Mbps			100 Mbps				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												C_L = 0 pF
ADuM5410	I_{DD1}		6.4	9.8		7.2	11		10.2	15.2	mA	
	I_{DD2}		1.9	3.5		3.1	5.0		6.8	10	mA	
ADuM5411	I_{DD1}		5.5	9.1		6.3	10.0		9.6	14.0	mA	
	I_{DD2}		3.72	6.45		4.8	7.5		8.4	11.2	mA	
ADuM5412	I_{DD1}		4.3	7.7		5.3	8.7		8.6	12.6	mA	
	I_{DD2}		4.9	8.3		6.0	9.4		9.3	13.3	mA	

Table 19. Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate				150	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			470		ps p-p	
			70		ps rms	

Table 20. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDx}$	V	
Output Voltages						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low	V_{OL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	µA	$0 \text{ V} \le V_{Ix} \le V_{DDx}$
Quiescent Supply Current						
ADuM5410						
	$I_{DD1 (Q)}$		1.2	1.92	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		2.0	2.64	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		12.0	19.6	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		2.0	2.76	mA	V_{Ix} = Logic 1
ADuM5411						
	$I_{DD1 (Q)}$		1.4	2.28	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.73	2.45	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.6	16.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.6	9.6	mA	V_{Ix} = Logic 1
ADuM5412						
	$I_{DD1 (Q)}$		1.6	2.28	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.6	2.28	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		8.4	11.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\lvert CM_H \rvert$	75	100		kV/µs	$V_{Ix} = V_{DD1}$ or V_{ISO}, $V_{CM} = 1000$ V, transient magnitude = 800 V
	$\lvert CM_L \rvert$	75	100		kV/µs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 21. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		50		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

[1] The device is considered a 2-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

Table 22.

UL(Pending)[1]	CSA(Pending)	VDE (Pending)[2]	CQC (Pending)
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 2500 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced Insulation 565 V peak, V_{IOSM} = 4 kV peak	GB4943.1-2011:
	Basic insulation at 400 V rms (565 V peak)		
	Basic insulation (1MOPP), 250 V rms (354 V peak)		Basic insulation at 400 V rms (565 V peak)
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at 300 V rms mains, 530 V rms (750 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADuM5410/ADuM5411/ADuM5412 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM5410/ADuM5411/ADuM5412 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 23. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	5.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	5.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	5.6	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		17	µm min	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 24. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1059	V peak
Input to Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	3535	V peak
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	2500	V rms
Surge Isolation Voltage Basic	$V_{IOSM(TEST)}$ = 10 kV; 1.2 µs rise time; 50 µs, 50% fall time	V_{ISOM}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		I_{S1}	2.5	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

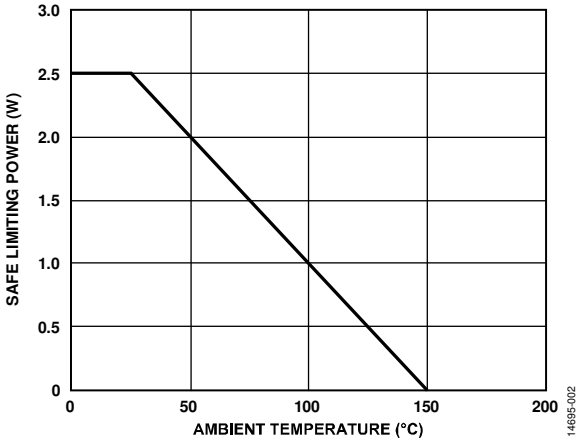

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 25.

Parameter	Symbol	Min	Max	Unit
Operating Temperature[1]	T_A	−40	+105	°C
Supply Voltages[2]				
V_{DDP} at V_{ISO} = 3.0 V to 3.6 V	V_{DDP}	3.0	5.5	V
V_{DDP} at V_{ISO} = 4.5 V to 5.5 V		4.5	5.5	V
V_{DD1}, V_{DD2}	V_{DD1}, V_{DD2}	1.7	5.5	V

[1] Operation at 105°C requires reduction of the maximum load current as specified in Table 26.
[2] Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 26.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DDP}, V_{DD2}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	
T_A = −40°C to +105°C	30 mA
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}, V_{SEL}, PDIS)[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1,3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−150 kV/µs to +150 kV/µs

[1] All voltages are relative to their respective ground.
[2] The V_{ISO} pin provides current for dc and dynamic loads on the V_{ISO} input/output channels. This current must be included when determining the total V_{ISO} supply current. For ambient temperatures between 85°C and 105°C, the maximum allowed current is reduced.
[3] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.
[4] See Figure 2 for the maximum rated current values for various temperatures.
[5] Common-mode transients refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 27. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	560	V peak	All certifications, 50-year operation
Unipolar Waveform			
Basic Insulation	560	V peak	
DC Voltage			
Basic Insulation	560	V peak	

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

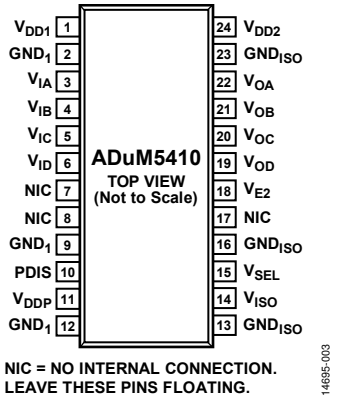

Figure 3. ADuM5410 Pin Configuration

Table 28. ADuM5410 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.
2, 9, 12	GND_1	Ground 1. Ground reference for the primary isolator. Pin 2, Pin 9, and Pin 12 are internally connected, and it is recommended that these pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7, 8, 17	NIC	No Internal Connection. Leave these pins floating.
10	PDIS	Power Disable. When tied to any GND_1 pin, the power converter is active; when a logic high voltage is applied, the power supply enters a low power standby mode.
11	V_{DDP}	Primary Supply Voltage, 3.0 V to 5.5 V.
13, 16, 23	GND_{ISO}	Ground Reference for V_{DD2} and V_{ISO} on Side 2. Pin 13, Pin 16, and Pin 23 are internally connected, and it is recommended that these pins be connected to a common ground.
14	V_{ISO}	Secondary Supply Voltage Output for External Loads. Connect to V_{DD2} to power the isolator channels.
15	V_{SEL}	Output Voltage Selection.
18	V_{E2}	Output Enable 2. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled. In noisy environments, connecting V_{E2} to either an external logic high or logic low is recommended.
19	V_{OD}	Logic Output D.
20	V_{OC}	Logic Output C.
21	V_{OB}	Logic Output B.
22	V_{OA}	Logic Output A.
24	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.

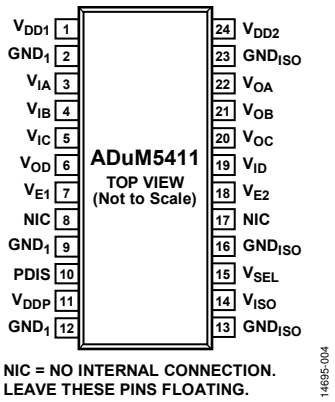

Figure 4. ADuM5411 Pin Configuration

Table 29. ADuM5411 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.
2, 9, 12	GND_1	Ground 1. Ground reference for the primary isolator. Pin 2, Pin 9, and Pin 12 are internally connected, and it is recommended that these pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. When V_{E1} is high or disconnected, the V_{OD} output is enabled. When V_{E1} is low, the V_{OD} output is disabled. In noisy environments, connecting V_{E1} to either an external logic high or logic low is recommended.
8, 17	NIC	No Internal Connection. Leave these pins floating.
10	PDIS	Power Disable. When tied to any GND_1 pin, the power converter is active; when a logic high voltage is applied, the power supply enters a low power standby mode.
11	V_{DDP}	Primary Supply Voltage, 3.0 V to 5.5 V.
13, 16, 23	GND_{ISO}	Ground Reference for V_{DD2} and V_{ISO} on Side 2. Pin 13, Pin 16, and Pin 23 are internally connected, and it is recommended that these pins be connected to a common ground.
14	V_{ISO}	Secondary Supply Voltage Output for External Loads. Connect to V_{DD2} to power the isolator channels.
15	V_{SEL}	Output Voltage Selection.
18	V_{E2}	Output Enable 2. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, and V_{OC} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, and V_{OC} outputs are disabled. In noisy environments, connecting V_{E2} to either an external logic high or logic low is recommended.
19	V_{ID}	Logic Input D.
20	V_{OC}	Logic Output C.
21	V_{OB}	Logic Output B.
22	V_{OA}	Logic Output A.
24	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.

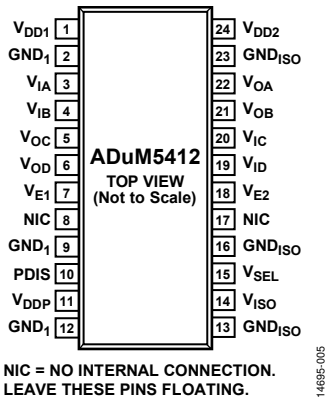

Figure 5. ADuM5412 Pin Configuration

Table 30. ADuM5412 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.
2, 9, 12	GND_1	Ground 1. Ground reference for the primary isolator. Pin 2, Pin 9, and Pin 12 are internally connected, and it is recommended that these pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. When V_{E1} is high or disconnected, the V_{OC} and V_{OD} outputs are enabled. When V_{E1} is low, the V_{OC} and V_{OD} outputs are disabled. In noisy environments, connecting V_{E1} to either an external logic high or logic low is recommended.
8, 17	NIC	No Internal Connection. Leave these pins floating.
10	PDIS	Power Disable. When tied to any GND_1 pin, the power converter is active; when a logic high voltage is applied, the power supply enters a low power standby mode.
11	V_{DDP}	Primary Supply Voltage, 3.0 V to 5.5 V.
13, 16, 23	GND_{ISO}	Ground Reference for V_{DD2} and V_{ISO} on Side 2. Pin 13, Pin 16, and Pin 23 are internally connected, and it is recommended that these pins be connected to a common ground.
14	V_{ISO}	Secondary Supply Voltage Output for External Loads. Connect to V_{DD2} to power the isolator channels.
15	V_{SEL}	Output Voltage Selection.
18	V_{E2}	Output Enable 2. When V_{E2} is high or disconnected, the V_{OA} and V_{OB} outputs are enabled. When V_{E2} is low, the V_{OA} and V_{OB} outputs are disabled. In noisy environments, connecting V_{E2} to either an external logic high or logic low is recommended.
19	V_{ID}	Logic Input D.
20	V_{IC}	Logic Input C.
21	V_{OB}	Logic Output B.
22	V_{OA}	Logic Output A.
24	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. This pin is independent of V_{DDP} and operates between 3.0 V and 5.5 V.

TRUTH TABLES

Table 31. Truth Table (Positive Logic)

V_{DDP} (V)	V_{SEL} Input	PDIS Input Logic	V_{ISO} Output (V)	Notes
5	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	5	
5	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	3.3	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	
5	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	3.3	
5	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	5	This configuration is not recommended
3.3	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	

Table 32. Data Section Truth Table (Positive Logic)

V_{DDI} State[1]	V_{Ix} Input[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
Powered	High	Powered	High	Normal operation, data is high
Powered	Low	Powered	Low	Normal operation, data is low
Don't care	Don't care	Unpowered	High-Z	Output is off
Unpowered	Low	Powered	Low	Output default low
Unpowered	High	Powered	Indeterminate	If a high level is applied to an input when no supply is present, the input can parasitically power the input side, causing unpredictable operation

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively. V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (Channel A, Channel B, Channel C, or Channel D).

TYPICAL PERFORMANCE CHARACTERISTICS

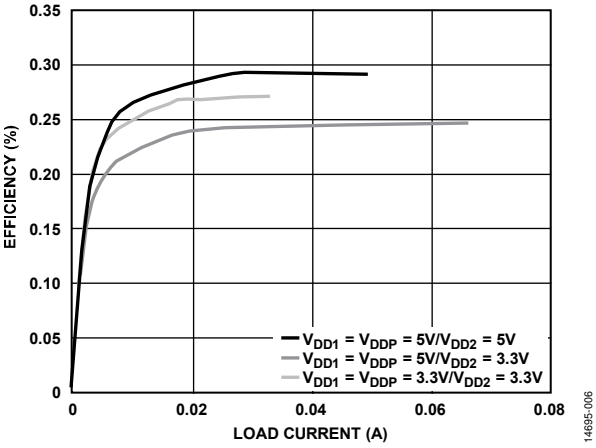

Figure 6. Power Supply Efficiency at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

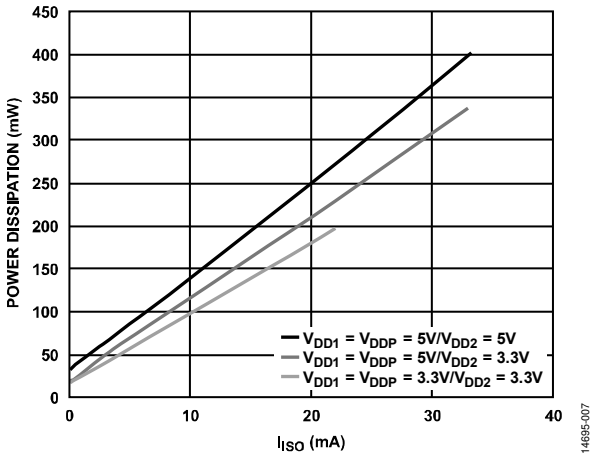

Figure 7. Total Power Dissipation vs. Output Supply Current, I_{ISO}, with Data Channels Idle

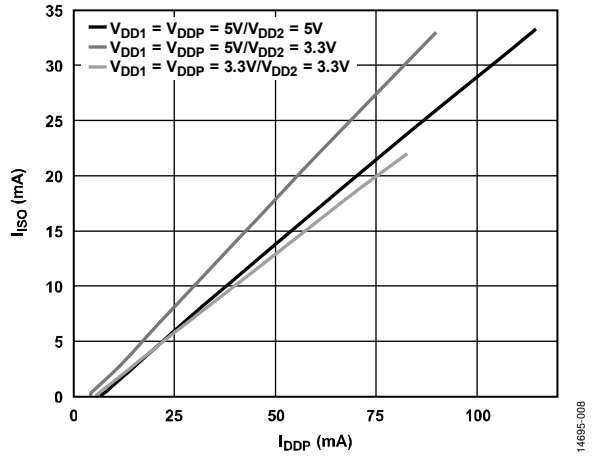

Figure 8. Isolated I_{ISO} as a Function of External Load, No Dynamic Current Draw at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

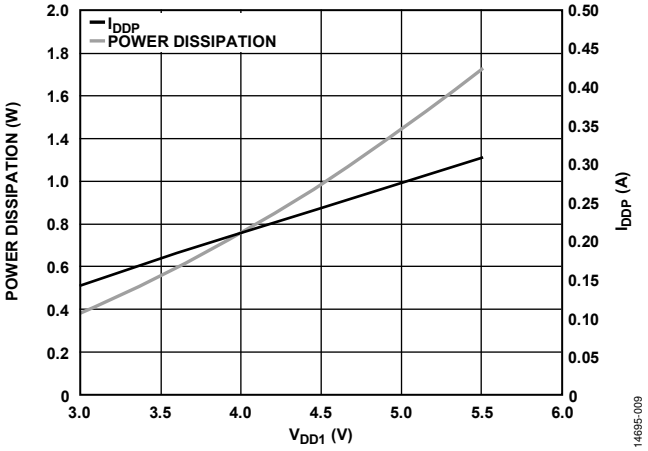

Figure 9. Short-Circuit Input Current (I_{DDP}) and Power Dissipation vs. V_{DD1} Supply Voltage

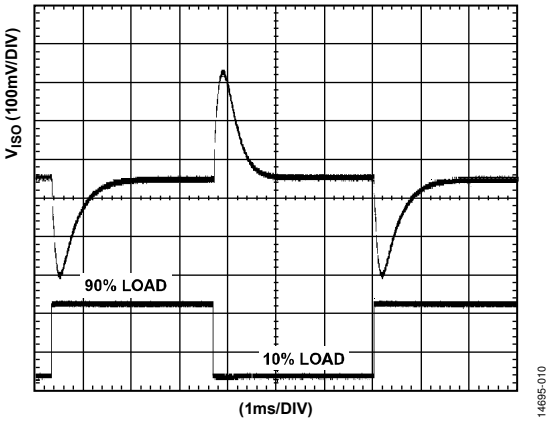

Figure 10. V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

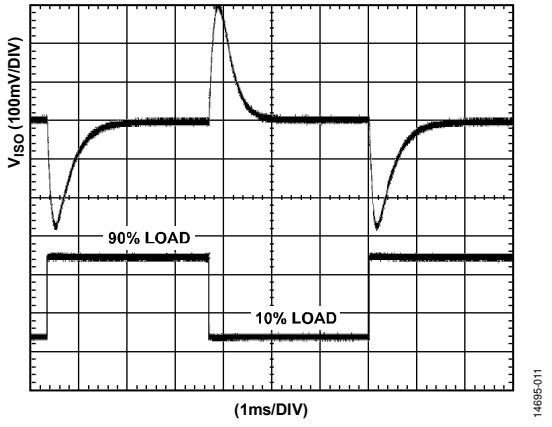

Figure 11. Transient Load Response, 3 V Output, 10% to 90% Load Step

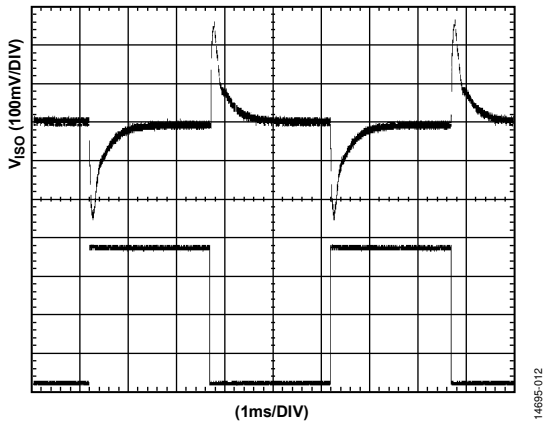

Figure 12. Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

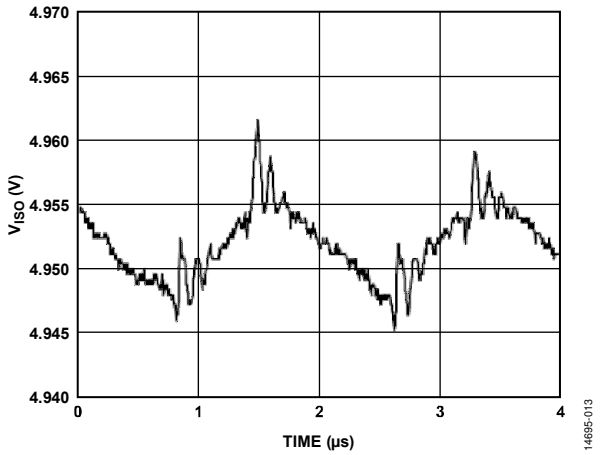

Figure 13. Output Voltage Ripple at 90% Load, V_{ISO} = 5 V

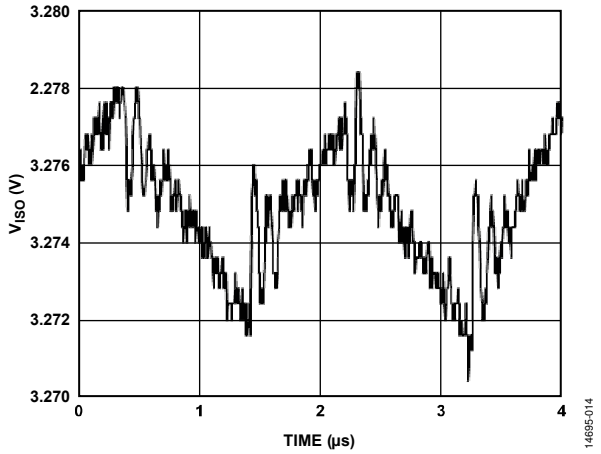

Figure 14. Output Voltage Ripple at 90% Load, V_{ISO} = 3.3 V

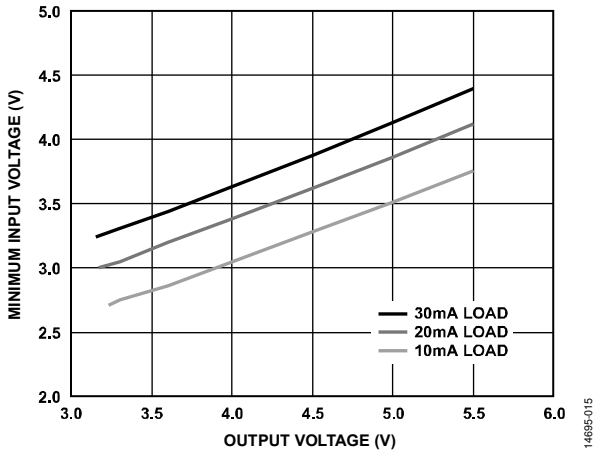

Figure 15. Relationship Between Output Voltage and Required Input Voltage, Under Load, to Maintain >80% Duty Factor in the PWM

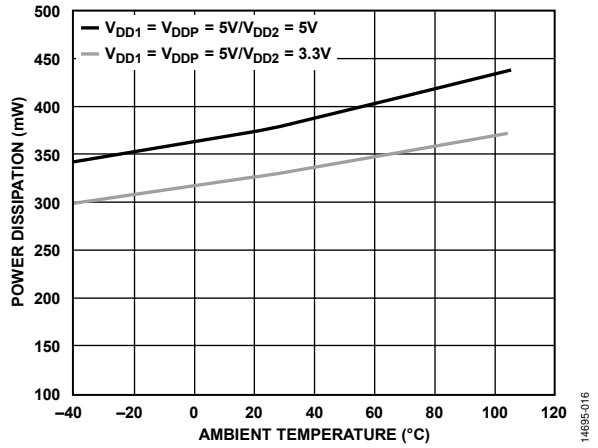

Figure 16. Power Dissipation vs. Ambient Temperature with a 30 mA Load

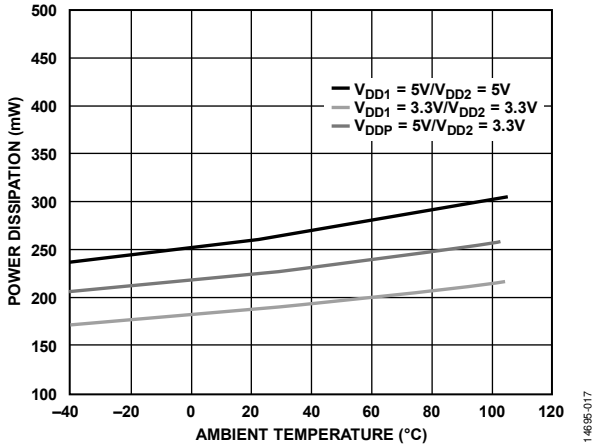

Figure 17. Power Dissipation vs. Ambient Temperature with a 20 mA Load

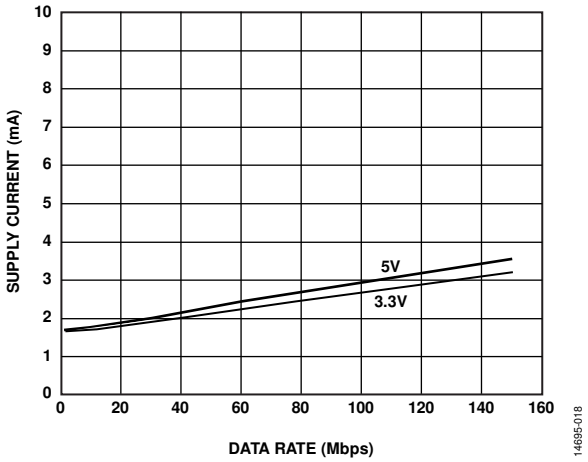

Figure 18. Supply Current per Input Channel vs. Data Rate for 5 V and 3.3 V Operation

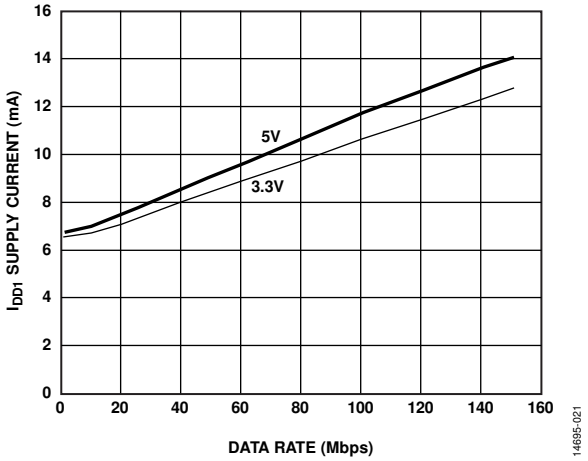

Figure 21. ADuM5410 V_{DD1} Supply Current (I_{DD1}) vs. Data Rate for 5 V and 3.3 V Operation

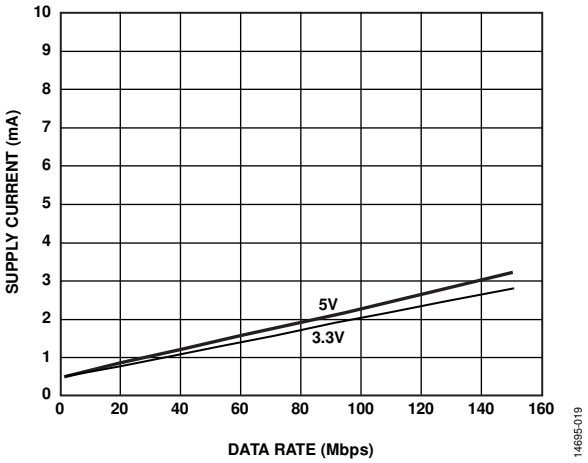

Figure 19. Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

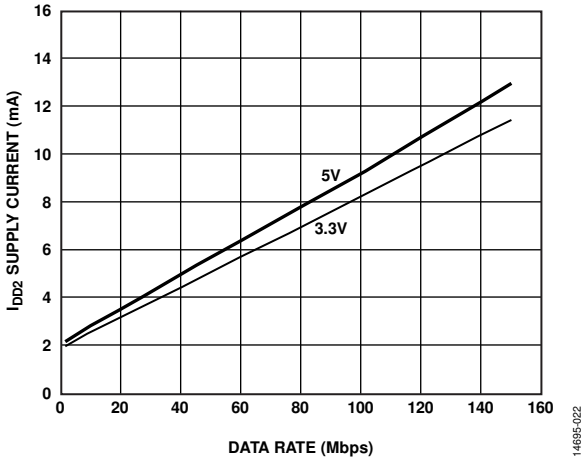

Figure 22. ADuM5410 V_{DD2} Supply Current (I_{DD2}) vs. Data Rate for 5 V and 3.3 V Operation

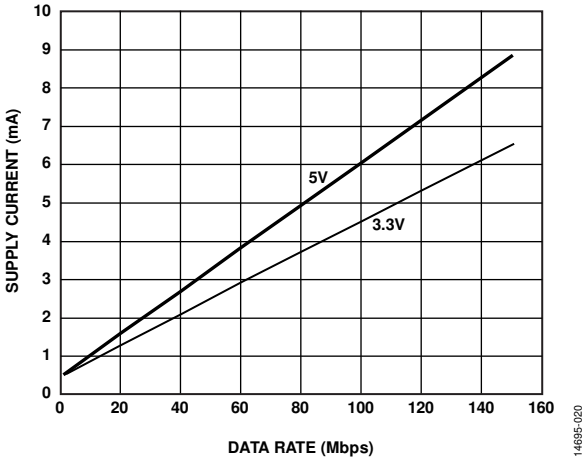

Figure 20. Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

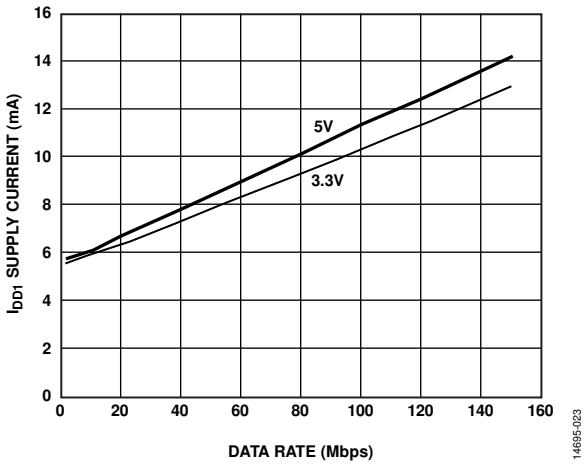

Figure 23. ADuM5411 V_{DD1} Supply Current (I_{DD1}) vs. Data Rate for 5 V and 3.3 V Operation

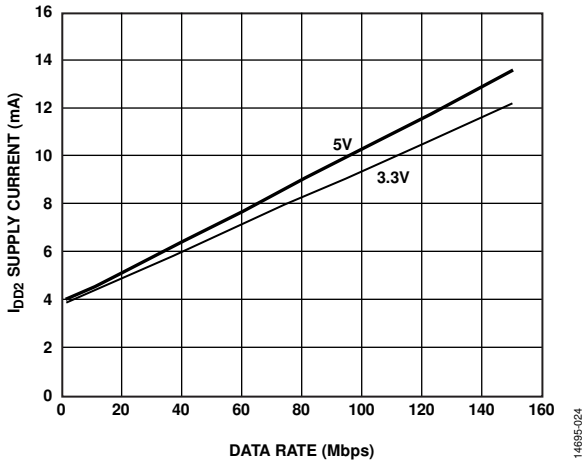

Figure 24. ADuM5411 V_{DD2} Supply Current (I_{DD2}) vs. Data Rate for 5 V and 3.3 V Operation

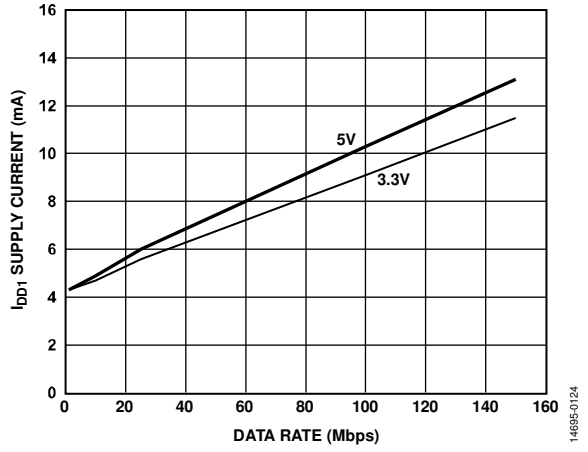

Figure 25. ADuM5412 V_{DD1} Supply Current (I_{DD1}) vs. Data Rate for 5 V and 3.3 V Operation

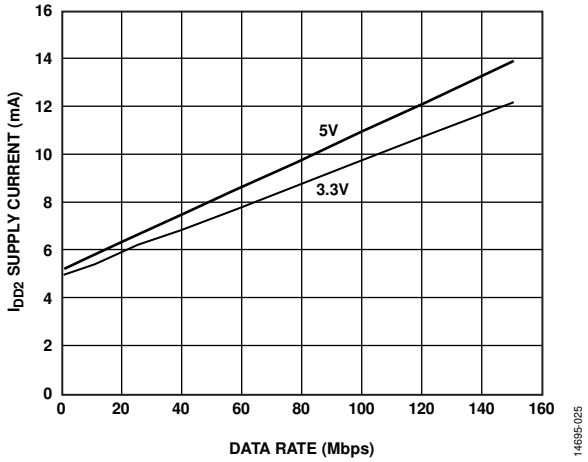

Figure 26. ADuM5412 V_{DD2} Supply Current (I_{DD2}) vs. Data Rate for 5 V and 3.3 V Operation

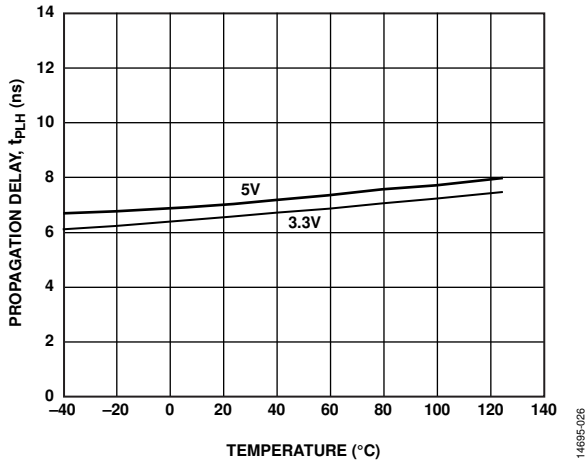

Figure 27. Propagation Delay, t_{PLH} vs. Temperature for 5 V and 3.3 V Operation

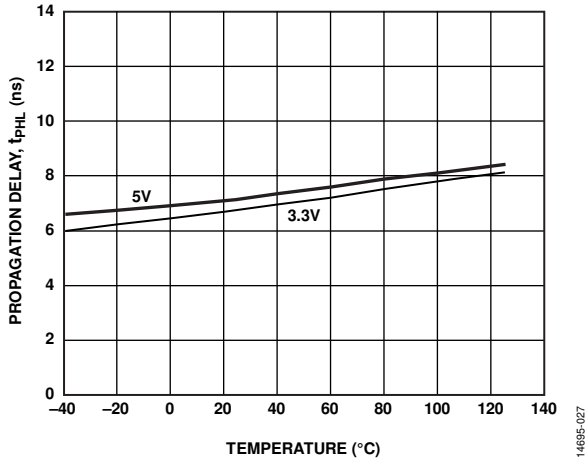

Figure 28. Propagation Delay, t_{PHL} vs. Temperature for 5 V and 3.3 V Operation

TERMINOLOGY

$I_{DD1 (Q)}$
$I_{DD1 (Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the input/output pins are operating below 2 Mbps, requiring no additional dynamic supply current. $I_{DD1 (Q)}$ reflects the minimum current operating condition.

$I_{DD1 (D)}$
$I_{DD1 (D)}$ is the typical input supply current with all channels simultaneously driven at a maximum data rate of 33 Mbps with full capacitive load representing the maximum dynamic load conditions. Treat resistive loads on the outputs separately from the dynamic load.

$I_{DD1 (MAX)}$
$I_{DD1 (MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

$I_{SO (LOAD)}$
$I_{SO (LOAD)}$ is the current available to load.

Propagation Delay, t_{PHL}
t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

Propagation Delay, t_{PLH}
t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew, t_{PSK}
t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel to Channel Matching, t_{PSKCD}/t_{PSKOD}
Channel to channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate
The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

THEORY OF OPERATION

The dc-to-dc converter section of the ADuM5410/ADuM5411/ADuM5412 works on principles that are common to most modern power supplies. It has a split controller architecture with isolated PWM feedback. V_{DDP} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to a value between 3.15 V and 5.25 V, depending on the setpoint supplied by an external voltage divider (see Equation 1). The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

$$V_{ISO} = 1.225\ \text{V} \frac{(R1 + R2)}{R1} \quad (1)$$

where:
R1 is a resistor between V_{SEL} and GND_{ISO}.
R2 is a resistor between V_{SEL} and V_{ISO}.

Because the output voltage can be adjusted continuously, there are an infinite number of operating conditions. This data sheet addresses three discrete operating conditions in the Specifications section. Many other combinations of input and output voltage are possible; Figure 15 shows the supported voltage combinations at room temperature. Figure 15 was generated by fixing the V_{ISO} load and decreasing the input voltage until the PWM was at 80% duty cycle. Each of the figures represents the minimum input voltage that is required for operation under this criterion. For example, if the application requires 30 mA of output current at 5 V, the minimum input voltage at V_{DDP} is 4.25 V. Figure 15 also illustrates why the V_{DDP} = 3.3 V input and V_{ISO} = 5 V configuration is not recommended. Even at 10 mA of output current, the PWM cannot maintain less than 80% duty factor, leaving no margin to support load or temperature variations.

Typically, the ADuM5410/ADuM5411/ADuM5412 dissipate about 17% more power between room temperature and maximum temperature; therefore, the 20% PWM margin covers temperature variations.

The ADuM5410/ADuM5411/ADuM5412 implement undervoltage lockout (UVLO) with hysteresis on the primary and secondary side input/output pins as well as the V_{DDP} power input. This feature ensures that the converters do not go into oscillation due to noisy input power or slow power-on ramp rates.

The digital isolator channels use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 29, the digital isolator channels have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 29 shows the waveforms of the digital isolator channels that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state sets the output to low.

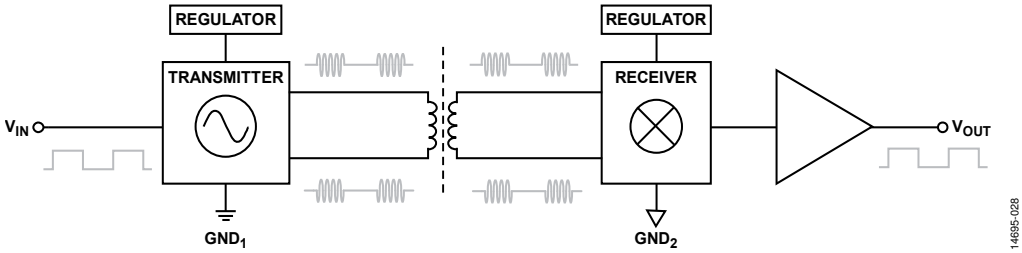

Figure 29. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State