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JPEG2000 Video Codec

Data Sheet **ADV202**

FEATURES

- Complete single-chip JPEG2000 compression and decompression solution for video and still images
- Patented SURF® (spatial ultra-efficient recursive filtering) technology enables low power and low cost wavelet-based compression
- Supports both 9/7 and 5/3 wavelet transforms with up to 6 levels of transform
- Programmable tile/image size with widths up to 2048 pixels in 3-component 4:2:2 interleaved mode, and up to 4096 pixels in single-component mode
- Maximum tile/image width: 4096 pixels
- Video interface directly supporting ITU.R-BT656, SMPTE125M PAL/ NTSC, SMPTE274M, SMPTE293M (525p), ITU.R-BT1358 (625p) or any video format with a maximum input rate of 65 MSPS for irreversible mode or 40 MSPS for reversible mode
- Two or more ADV202s can be combined to support full-frame SMPTE274M HDTV (1080i) or SMPTE296M (720p)
- Flexible asynchronous SRAM-style host interface allows glueless connection to most 16-/32-bit microcontrollers and ASICs
- 2.5 V to 3.3 V I/O and 1.5 V core supply
- 12 mm × 12 mm 121-lead CSPBGA, speed grade 115 MHz, or
- 13 mm × 13 mm 144-lead CSPBGA, speed grade 135 MHz, or
- 13 mm × 13 mm 144-lead CSPBGA, speed grade 150 MHz

APPLICATIONS

- Networked video and image distribution systems
- Wireless video and image distribution
- Image archival/retrieval
- Digital CCTV and surveillance systems
- Digital cinema systems
- Professional video editing and recording
- Digital still cameras
- Digital camcorders

GENERAL DESCRIPTION

The ADV202 is a single-chip JPEG2000 codec targeted for video and high bandwidth image compression applications that can benefit from the enhanced quality and feature set provided by the JPEG2000 (J2K)—ISO/IEC15444-1 image compression standard. The part implements the computationally intensive operations of the JPEG2000 image compression standard as well as providing fully compliant code-stream generation for most applications.

The ADV202's dedicated video port provides glueless connection to common digital video standards such as ITU.R-BT656, SMPTE125M, SMPTE293M (525p), ITU.R-BT1358 (625p), SMPTE274M (1080i), or SMPTE296M (720p). A variety of other high speed, synchronous pixel and video formats can also be supported using the programmable framing and validation signals.

(continued on Page 4)

FUNCTIONAL BLOCK DIAGRAM

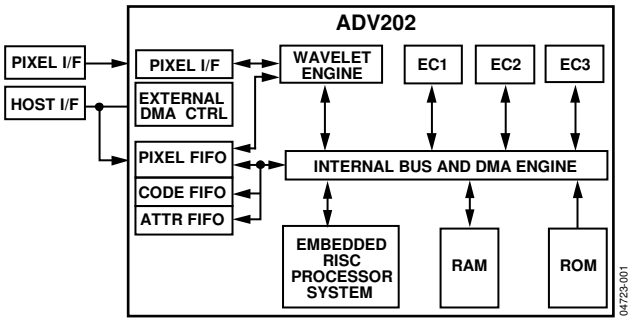

Figure 1.

Rev. D

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Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

ADV202* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-790: How to Use the ADV202
- AN-796: Using the ADV202 in a Multichip Application
- AN-799: ADV202 Test Modes

Data Sheet

- ADV202: JPEG2000 Video Codec Data Sheet

REFERENCE MATERIALS

Technical Articles

- ADV202 Technical Documentation
- Digital 3-D at a Theater Near You
- HDTV Over UWB: Wireless Video Streaming Trials and Quality of Service Analysis
- Implementing JPEG2000 compression
- IP Centric Calls for Scalable Compression
- JPEG2000 Codec for Robust, Scalable Pro and Consumer Video

DESIGN RESOURCES

- ADV202 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADV202 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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GENERAL DESCRIPTION

(continued from Page 1)

The ADV202 can process images at a rate of 40 MSPS in reversible mode and at higher rates when used in irreversible mode. The ADV202 contains a dedicated wavelet transform engine, three entropy codecs, an on-board memory system, and an embedded RISC processor that can provide a complete JPEG2000 compression/decompression solution.

The wavelet processor supports the 9/7 irreversible wavelet transform and the 5/3 wavelet transform in reversible and irreversible modes. The entropy codecs support all features in the JPEG2000 Part 1 specification, except Maxshift ROI.

The ADV202 operates on a rectangular array of pixel samples called a tile. A tile can contain a complete image, up to the maximum supported size, or some portion of an image. The maximum horizontal tile size supported depends on the wavelet transform selected and the number of samples in the tile. Images larger than the ADV202's maximum tile size can be broken into individual tiles and then sent sequentially to the chip while still maintaining a single, fully compliant JPEG2000 code stream for the entire image.

JPEG2000 FEATURE SUPPORT

The ADV202 supports a broad set of features that are included in Part 1 of the JPEG2000 standard (ISO/IEC 15444). See *Getting Started with ADV202* for information on the JPEG2000 features that the ADV202 currently supports.

Depending on the particular application requirements, the ADV202 can provide varying levels of JPEG2000 compression support. It can provide raw code-block and attribute data output, which allow the host software to have complete control over the generation of the JPEG2000 code stream and other aspects of the compression process such as bit-rate control. Otherwise, the ADV202 can create a complete, fully compliant JPEG2000 code stream (.j2c) and enhanced file formats such as .jp2 and .j2c. See *Getting Started with ADV202* for information on the formats that the ADV202 currently supports.

Application notes and other ADV202 support documents can be accessed over the ADV202 product page at:

- http://www.analog.com/ADV202Notes or from
- ftp://ftp.analog.com/pub/Digital_Imaging/ADV202_FTP_site_contents_3.html

SPECIFICATIONS

SUPPLY VOLTAGES AND CURRENT

Table 1.

Parameter	Description	Min	Typ	Max	Unit
VDD	DC Supply Voltage, Core	1.425	1.5	1.575	V
IOVDD	DC Supply Voltage, I/O	2.375	3.3	3.63	V
PLLVDD	DC Supply Voltage, PLL	1.425	1.5	1.575	V
V_{INPUT}	Input Range	−0.3		$V_{DDI/O}$ + 0.3	V
Temp	Operating Ambient Temperature Range in Free Air	−40	+25	+85	°C
I_{DD}	Static Current[1]			300	mA
	Dynamic Current, Core (JCLK Frequency = 150 MHz)[2]			570	mA
	Dynamic Current, Core (JCLK Frequency = 108 MHz)			420	mA
	Dynamic Current, Core (JCLK Frequency = 81 MHz)			325	mA
	Dynamic Current, I/O			20	mA
	Dynamic Current, PLL			2.6	mA

[1] No clock or I/O activity.
[2] ADV202-150 only.

INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$V_{IH (3.3 V)}$	High Level Input Voltage	VDD = max	2.2			V
$V_{IH (2.5 V)}$	High Level Input Voltage	VDD = max	1.9			V
$V_{IL (3.3 V, 2.5 V)}$	Low Level Input Voltage	VDD = min			0.6	V
$V_{OH (3.3 V)}$	High Level Output Voltage	VDD = min, I_{OH} = −0.5 mA	2.4			V
$V_{OH (2.5 V)}$	High Level Output Voltage	VDD = min, I_{OH} = −0.5 mA	2.0			V
$V_{OL (3.3 V, 2.5 V)}$	Low Level Output Voltage	VDD = min, I_{OL} = 2 mA			0.4	V
I_{IH}	High Level Input Current	VDD = max, V_{IN} = VDD	1.0			µA
I_{IL}	Low Level Input Current	VDD = max, V_{IN} = 0 V			1	µA
I_{OZH}	High Level Three-State Leakage Current	VDD = max, V_{IN} = VDD	1.0			µA
I_{OZL}	Low Level Three-State Leakage Current	VDD = max, V_{IN} = 0 V			1.0	µA
C_I	Input Pin Capacitance				8	pF
C_O	Output Pin Capacitance				8	pF

CLOCK AND $\overline{\text{RESET}}$ SPECIFICATIONS

Table 3.

Parameter	Description	Min	Typ	Max	Unit
t_{MCLK}	MCLK[1] Period	13.3		100	ns
t_{MCLKL}	MCLK Width Low	6			ns
t_{MCLKH}	MCLK Width High	6			ns
t_{VCLK}	VCLK Period	13.4		50	ns
t_{VCLKL}	VCLK Width Low	5			ns
t_{VCLKH}	VCLK Width High	5			ns
t_{RST}	$\overline{\text{RESET}}$ Width Low	5			MCLK cycles

[1] For a definition of MCLK, see the PLL section.

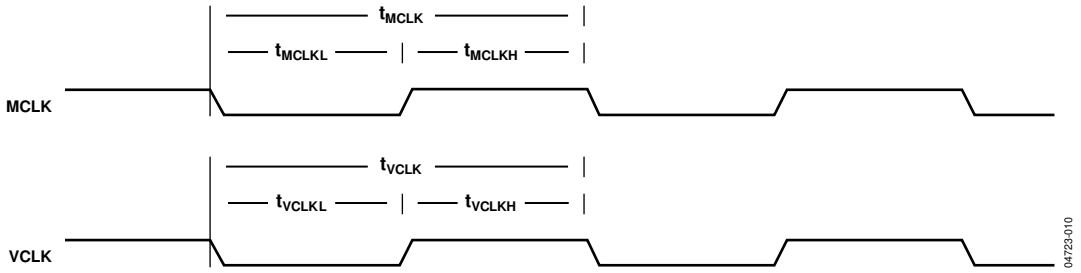

Figure 2. Input Clock

NORMAL HOST MODE—READ OPERATION

Table 4.

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{ACK}}$ [dir]	$\overline{RD}$ to $\overline{ACK}$, Direct Registers and FIFO Accesses	5		1.5 × JCLK[1] + 7.0	ns
$t_{\overline{ACK}}$ [indir]	$\overline{RD}$ to $\overline{ACK}$, Indirect Registers	10.5 × JCLK		15.5 × JCLK + 7.0	ns
t_{DRD} [dir]	Read Access Time, Direct Registers	5		1.5 × JCLK + 7.0	ns
t_{DRD} [indir]	Read Access Time, Indirect Registers	10.5 × JCLK		15.5 × JCLK + 7.0	ns
t_{HZRD}	Data Hold	2		8.5	ns
t_{SC}	$\overline{CS}$ to $\overline{RD}$ Setup	0			ns
t_{SA}	Address Setup	2			ns
t_{HC}	$\overline{CS}$ Hold	0			ns
t_{HA}	Address Hold	2			ns
t_{RH}	Read Inactive Pulse Width	2.5			JCLK
t_{RL}	Read Active Pulse Width	2.5			JCLK
t_{RCYC}	Read Cycle Time, Direct Registers	5.0			JCLK

[1] For a definition of JCLK, see the PLL section.

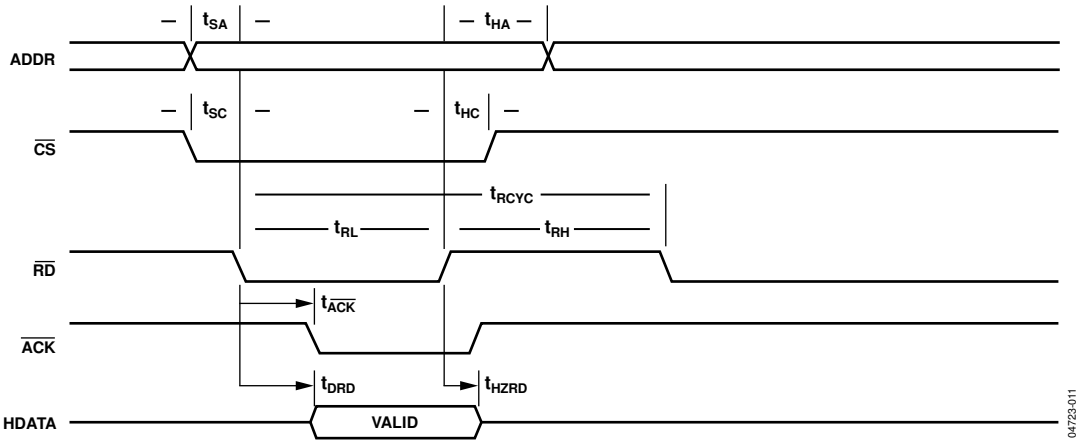

Figure 3. Normal Host Mode—Read Operation

NORMAL HOST MODE—WRITE OPERATION

Table 5.

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{ACK}}$ (Direct)	$\overline{WE}$ to $\overline{ACK}$, Direct Registers and FIFO Accesses	5		1.5 × JCLK[1] + 7.0	ns
$t_{\overline{ACK}}$ (Indirect)	$\overline{WE}$ to $\overline{ACK}$, Indirect Registers	5		2.5 × JCLK + 7.0	ns
t_{SD}	Data Setup	3.0			ns
t_{HD}	Data Hold	1.5			ns
t_{SA}	Address Setup	2			ns
t_{HA}	Address Hold	2			ns
t_{SC}	$\overline{CS}$ to $\overline{WE}$ Setup	0			ns
t_{HC}	$\overline{CS}$ Hold	0			ns
t_{WH}	Write Inactive Pulse Width (Minimum Time Until Next $\overline{WE}$ Pulse)	2.5			JCLK
t_{WL}	Write Active Pulse Width	2.5			JCLK
t_{WCYC}	Write Cycle Time	5			JCLK

[1] For a definition of JCLK, see the PLL section.

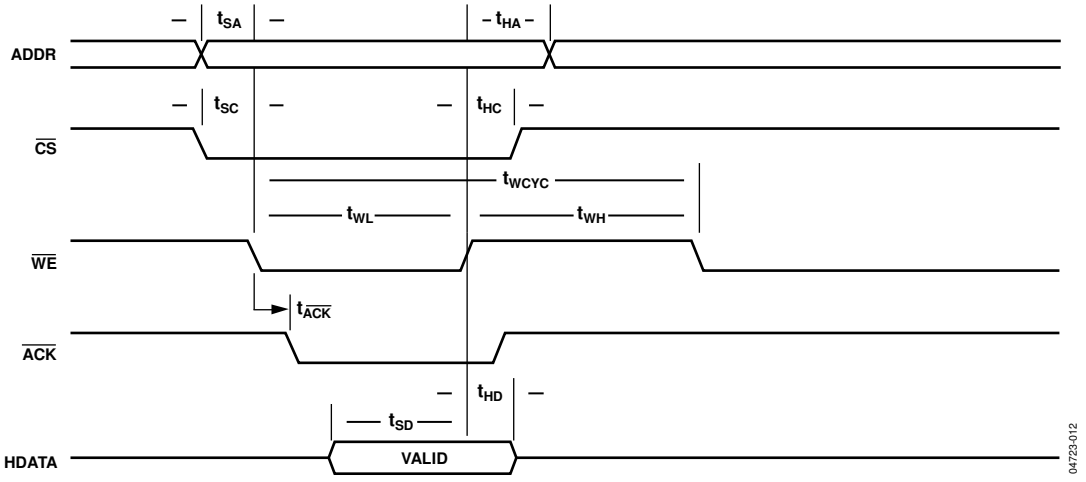

Figure 4. Nor/ mal Host Mode—Write Operation

$\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA MODE—SINGLE FIFO WRITE OPERATION

Table 6.

Parameter	Description	Min	Typ	Max	Unit
$\overline{\text{DREQ}}_{\text{PULSE}}$[1]	$\overline{\text{DREQ}}$ Pulse Width	1		15	JCLK cycles[2]
$t_{\overline{\text{DREQ}}}$	$\overline{\text{DACK}}$ Assert to Subsequent $\overline{\text{DREQ}}$ Delay	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{\text{WE}}\text{SU}}$	$\overline{\text{WE}}$ to $\overline{\text{DACK}}$ Setup	0			ns
t_{SU}	Data to $\overline{\text{DACK}}$ Deassert Setup	2			ns
t_{HD}	Data to $\overline{\text{DACK}}$ Deassert Hold	2			ns
$\overline{\text{DACK}}_{\text{LO}}$	$\overline{\text{DACK}}$ Assert Pulse Width	2			JCLK cycles
$\overline{\text{DACK}}_{\text{HI}}$	$\overline{\text{DACK}}$ Deassert Pulse Width	2			JCLK cycles
$t_{\overline{\text{WE}}\text{HD}}$	$\overline{\text{WE}}$ Hold After $\overline{\text{DACK}}$ Deassert	0			ns
$\overline{\text{WFSRQ}}$	$\overline{\text{WE}}$ Assert to $\overline{\text{FSRQ}}$ Deassert (FIFO Full)	1.5		2.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{\text{DREQ}}\text{RTN}}$	$\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Deassert (DR × PULS = 0)	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles

[1] Applies to assigned DMA channel, if EDMOD0 or EDMOD1[14:11] is programmed to a value that is not 0. Pulse width depends on the value programmed
[2] For a definition of JCLK, see the PLL section.

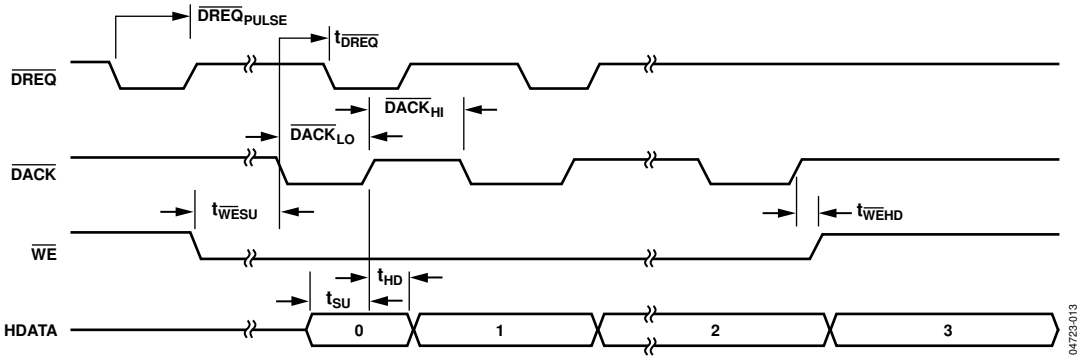

Figure 5. Single Write for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] NOT Programmed to a Value of 0000)

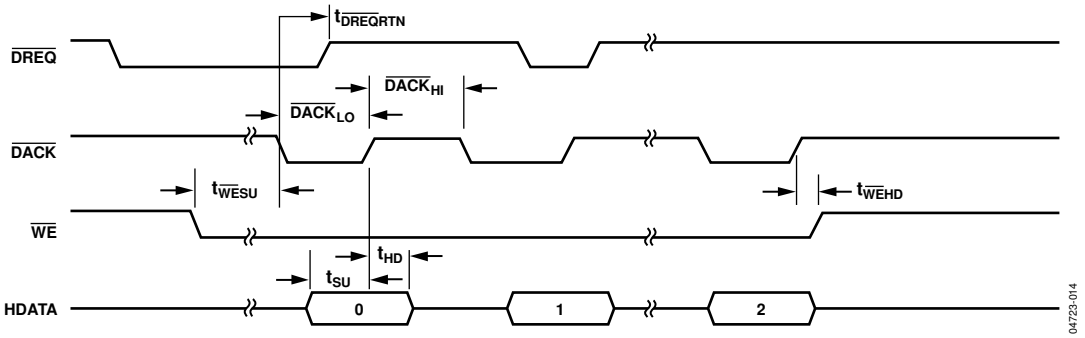

Figure 6. Single Write for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

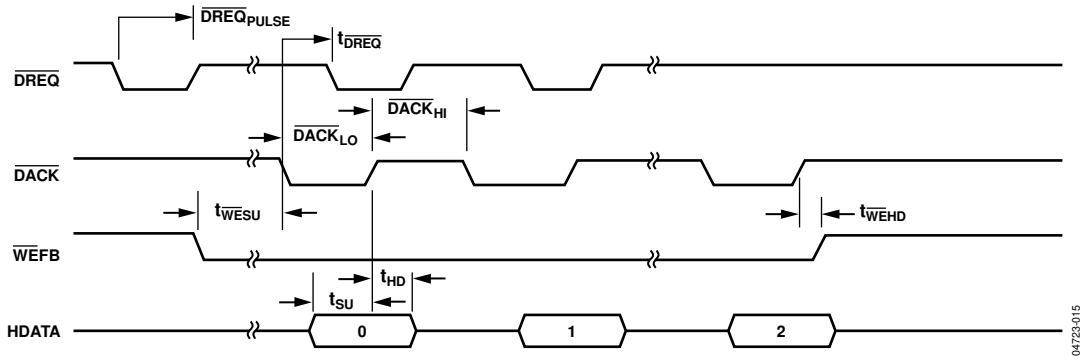

Figure 7. Fly-By DMA Mode—Single Write Cycle (DREQ Pulse Width Is Programmable)

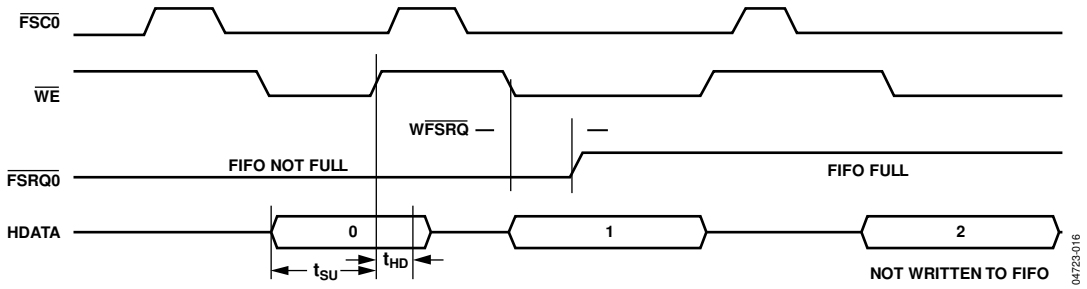

Figure 8. DCS DMA Mode—Single Write Access (Rev. 0.1 and Higher)

$\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA MODE—SINGLE FIFO READ OPERATION

Table 7.

Parameter	Description	Min	Typ	Max	Unit
$\overline{\text{DREQ}}_{\text{PULSE}}$	$\overline{\text{DREQ}}$ Pulse Width[1]	1		15	JCLK cycles[2]
$t_{\overline{\text{DREQ}}}$	$\overline{\text{DACK}}$ Assert to Subsequent $\overline{\text{DREQ}}$ Delay	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{\text{RD}}\text{SU}}$	$\overline{\text{RD}}$ to $\overline{\text{DACK}}$ Setup	0			ns
$t_{\overline{\text{RD}}}$	$\overline{\text{DACK}}$ to Data Valid	2.5		11	ns
t_{HD}	Data Hold	1.5			ns
$\overline{\text{DACK}}_{\text{LO}}$	$\overline{\text{DACK}}$ Assert Pulse Width	2			JCLK cycles
$\overline{\text{DACK}}_{\text{HI}}$	$\overline{\text{DACK}}$ Deassert Pulse Width	2			JCLK cycles
$t_{\overline{\text{RD}}\text{HD}}$	$\overline{\text{RD}}$ Hold After $\overline{\text{DACK}}$ Deassert	0			ns
$\overline{\text{RDFSRQ}}$	$\overline{\text{RD}}$ Assert to $\overline{\text{FSRQ}}$ Deassert (FIFO Empty)	1.5		2.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{\text{DREQ}}\text{RTN}}$	$\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Deassert (DR × PULS = 0)	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles

[1] Applies to assigned DMA channel, if EDMOD0 or EDMOD1[14:11] is programmed to a nonzero value.
[2] For a definition of JCLK, see the PLL section.

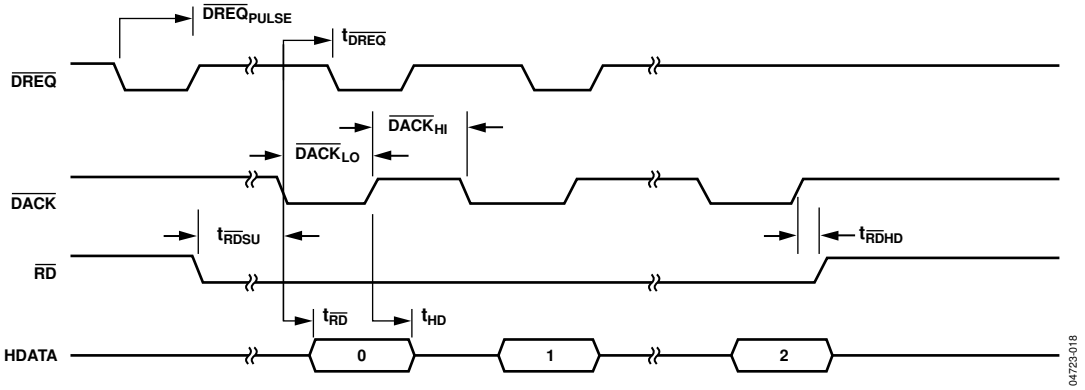

Figure 9. Single Read for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Not Programmed to a Value of 0000)

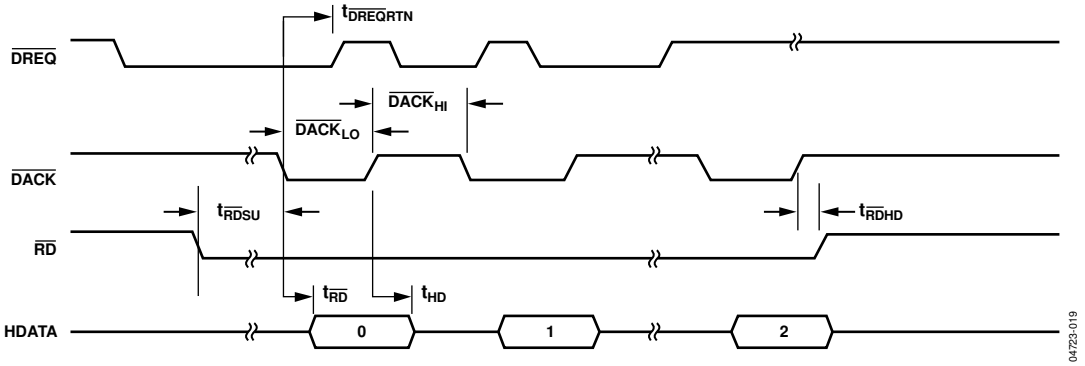

Figure 10. Single Read for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

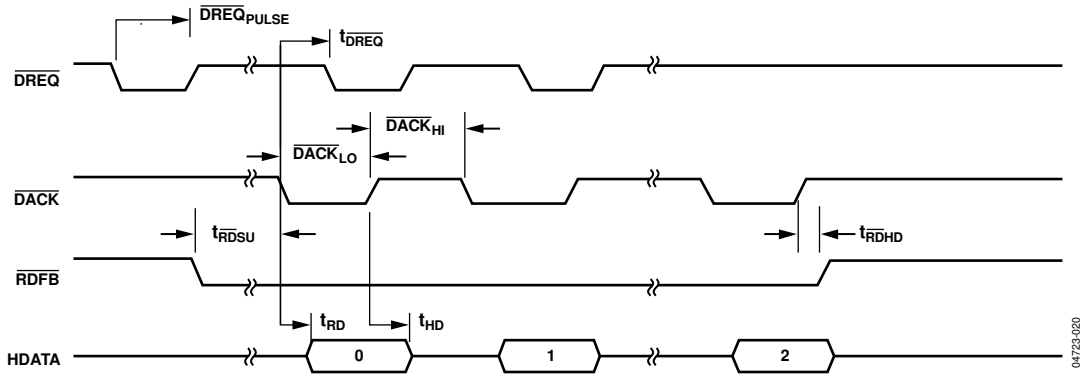

Figure 11. Fly-By DMA Mode—Single Read Cycle (DREQ Pulse Width Is Programmable)

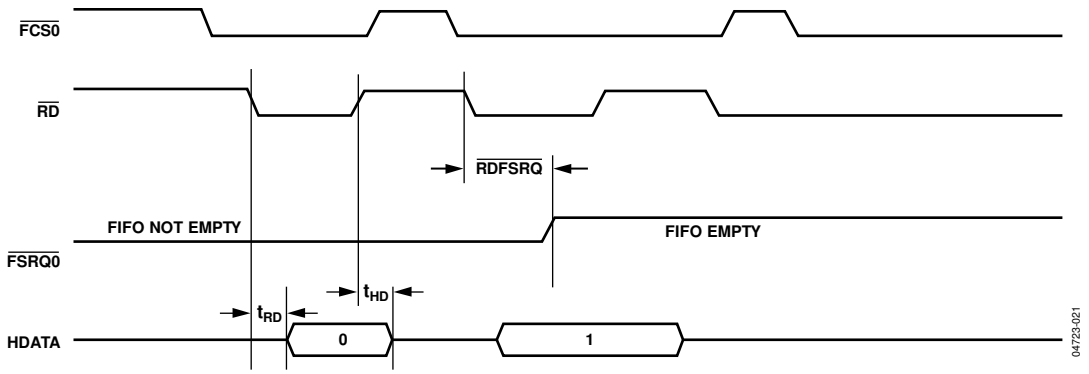

Figure 12. DCS DMA Mode—Single Read Access (Rev. 0.1 and Higher)

EXTERNAL DMA MODE—FIFO WRITE, BURST MODE

Table 8.

Parameter	Description	Min	Typ	Max	Unit
$\overline{DREQ}_{PULSE}$	$\overline{DREQ}$ Pulse Width[1]	1		15	JCLK[2] cycles
$t_{\overline{DREQ}RTN}$	$\overline{WE}$ to $\overline{DREQ}$ Deassert (DR × Pulse = 0)	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{DACK}SU}$	$\overline{DACK}$ to $\overline{WE}$ Setup	0			ns
t_{SU}	Data Setup	2.5			ns
t_{HD}	Data Hold	2			ns
$\overline{WE}_{LO}$	$\overline{WE}$ Assert Pulse Width	1.5			JCLK cycles
$\overline{WE}_{HI}$	$\overline{WE}$ Deassert Pulse Width	1.5			JCLK cycles
$t_{\overline{DREQ}WAIT}$	Last Burst Access to Next $\overline{DREQ}$	2.5		4.5 × JCLK + 7.5 ns[3]	JCLK cycles

[1] Applies to assigned DMA channel, if EDMOD0 or EDMOD1[14:11] is programmed to a value that is not 0. Pulse width depends on the value programmed.
[2] For a definition of JCLK, see the PLL section.
[3] If sufficient space is available in FIFO.

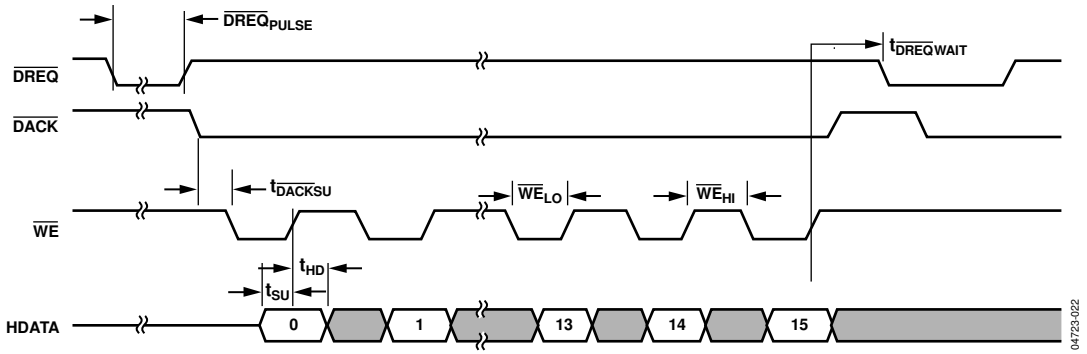

Figure 13. Burst Write Cycle for $\overline{DREQ}$/DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] NOT Programmed to a Value of 0000)

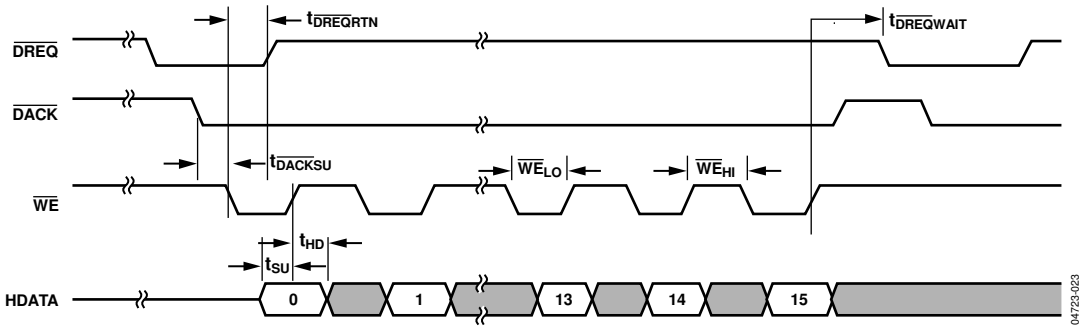

Figure 14. Burst Write Cycle for $\overline{DREQ}$/DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

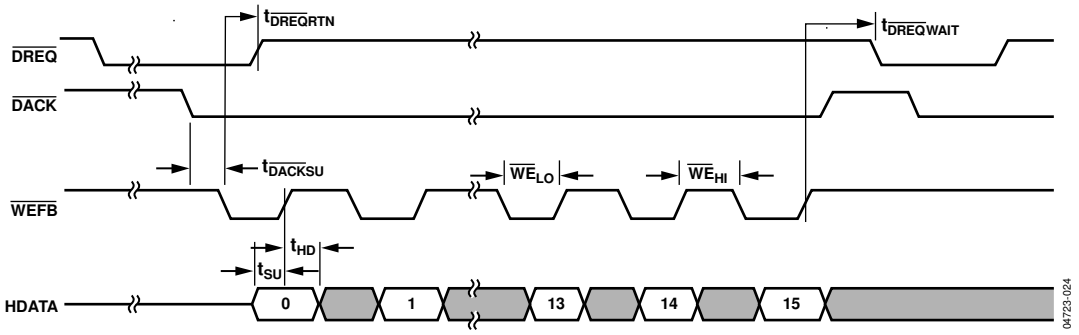

Figure 15. Burst Write Cycle for Fly-By DMA Mode (DREQ Pulse Width Is Programmable)

EXTERNAL DMA MODE—FIFO READ, BURST MODE

Table 9.

Parameter	Description	Min	Typ	Max	Unit
$\overline{DREQ}_{PULSE}$	$\overline{DREQ}$ Pulse Width[1]	1		15	JCLK cycles[2]
$t_{\overline{DREQ}RTN}$	$\overline{RD}$ to $\overline{DREQ}$ Deassert (DR × PULS = 0)	2.5		3.5 × JCLK + 7.5 ns	JCLK cycles
$t_{\overline{DACK}SU}$	$\overline{DACK}$ to $\overline{RD}$ Setup	0			ns
$t_{\overline{RD}}$	$\overline{RD}$ to Data Valid	2.5		9.7	ns
t_{HD}	Data Hold	2.5			ns
$\overline{RD}_{LO}$	$\overline{RD}$ Assert Pulse Width	1.5			JCLK cycles
$\overline{RD}_{HI}$	$\overline{RD}$ Deassert Pulse Width	1.5			JCLK cycles
$t_{\overline{DREQ}WAIT}$	Last Burst Access to Next $\overline{DREQ}$	2.5		3.5 × JCLK + 7.5 ns[3]	JCLK cycles

[1] Applies to assigned DMA channel, if EDMOD0 or EDMOD1[14:11] is programmed to a value that is not 0. Pulse width depends on the value programmed.
[2] For a definition of JCLK, see the PLL section.
[3] If sufficient space is available in FIFO.

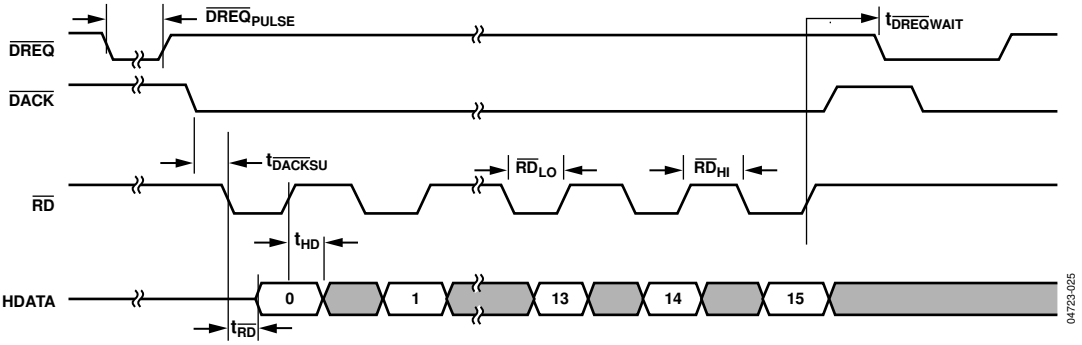

Figure 16. Burst Read Cycle for $\overline{DREQ}$/$\overline{DACK}$ DMA Mode for Assigned DMA Channel (EMOD0/EDMOD1[14:11] NOT Programmed to a Value of 0)

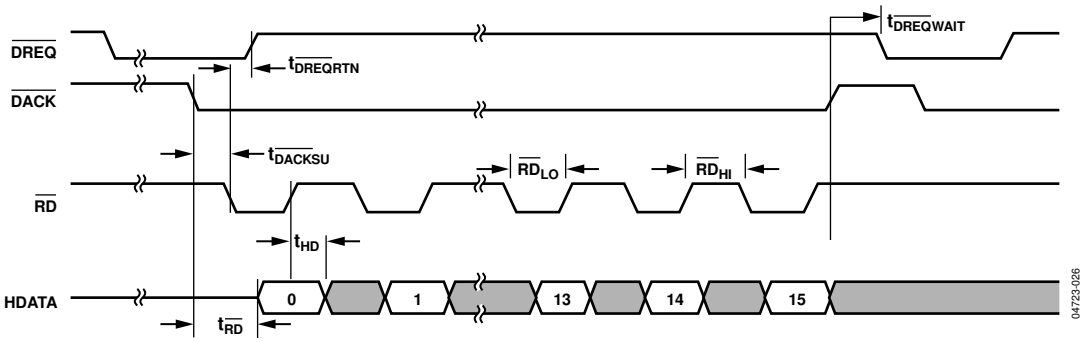

Figure 17. Burst Read Cycle for DREQ/DACK DMA Mode for Assigned DMA Channel (EMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

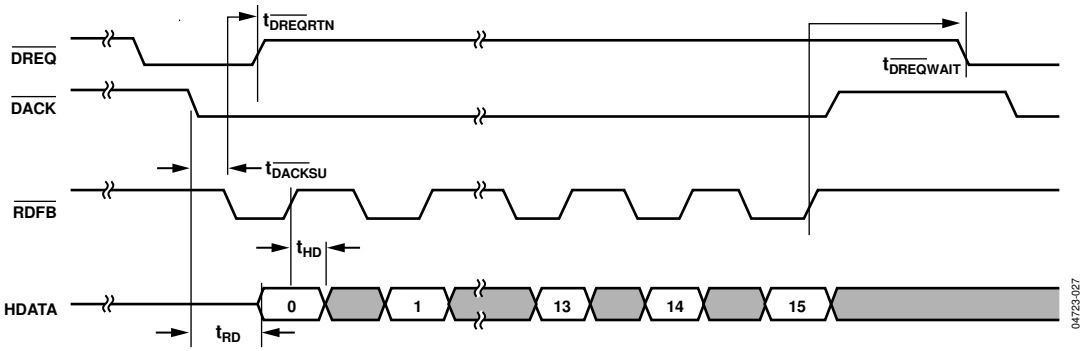

Figure 18. Burst Read Cycle, Fly-By DMA Mode (DREQ Pulse Width Is Programmable)

STREAMING MODE (JDATA)—FIFO READ/WRITE

Table 10.

Parameter	Description	Min	Typ	Max	Unit
$JDATA_{TD}$	MCLK to JDATA Valid	1.5		2.5 × JCLK + 7.0 ns	JCLK cycles[1]
$VALID_{TD}$	MCLK to VALID Assert/Deassert	1.5		2.5 × JCLK + .7.0 ns	JCLK cycles
$HOLD_{SU}$	HOLD Setup to Rising MCLK	3			ns
$HOLD_{HD}$	HOLD Hold from Rising MCLK	3			ns
$JDATA_{SU}$	JDATA Setup to Rising MCLK	3			ns
$JDATA_{HD}$	JDATA Hold from Rising MCLK	3			ns

[1] For a definition of JCLK, see the PLL section.

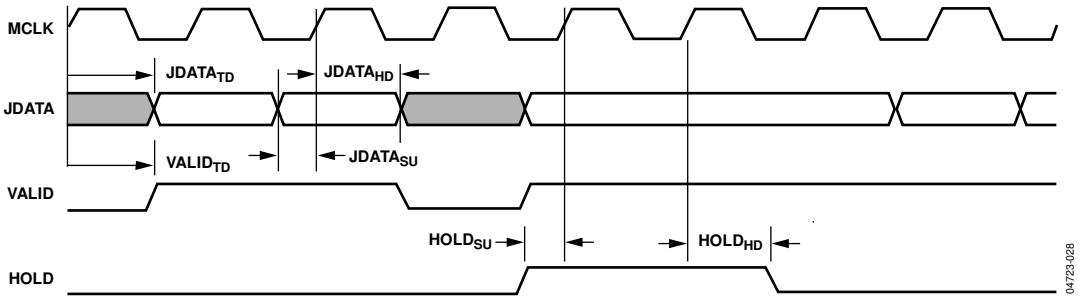

Figure 19. Streaming Mode Timing—Encode Mode JDATA Output

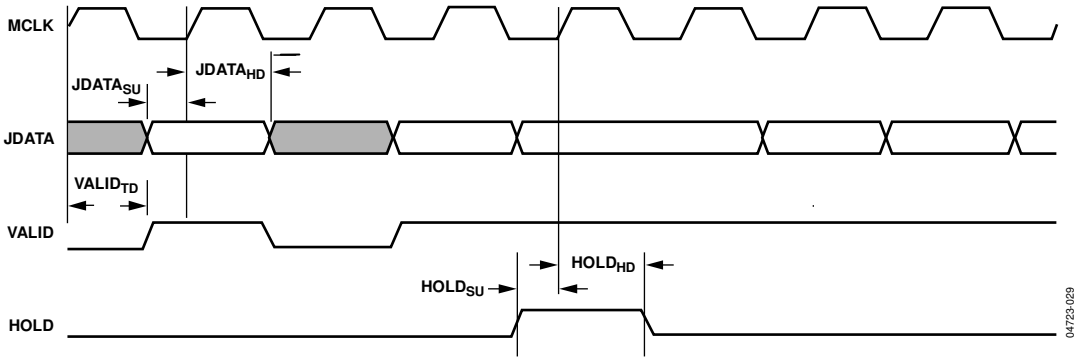

Figure 20. Streaming Mode Timing—Decode Mode JDATA Input

VDATA MODE TIMING

Table 11.

Parameter	Description	Min	Typ	Max	Unit
$VDATA_{TD}$	VCLK to VDATA Valid Delay (VDATA Output)			12	ns
$VDATA_{SU}$	VDATA Setup to Rising VCLK (VDATA Input)	4			ns
$VDATA_{HD}$	VDATA Hold from Rising VCLK (VDATA Input)	4			ns
$HSYNC_{SU}$	HSYNC Setup to Rising VCLK	3			ns
$HSYNC_{HD}$	HSYNC Hold from Rising VCLK	4			ns
$HSYNC_{TD}$	VCLK to HSYNC Valid Delay			12	ns
$VSYNC_{SU}$	VSYNC Setup to Rising VCLK	3			ns
$VSYNC_{HD}$	VSYNC Hold from Rising VCLK	4			ns
$VSYNC_{TD}$	VCLK to VSYNC Valid Delay			12	ns
$FIELD_{SU}$	FIELD Setup to Rising VCLK	4			ns
$FIELD_{HD}$	FIELD Hold from Rising VCLK	3			ns
$FIELD_{TD}$	VCLK to FIELD Valid			12	ns
SYNC DELAY	Decode Data Sync Delay for HD Input with EAV/SAV Codes		7		VCLK cycles
	Decode Data Sync Delay for SD Input with EAV/SAV Codes		9		VCLK cycles
	Decode Data Sync Delay for HVF Input (from First Rising VCLK after HSYNC Low to First Data Sample)		10		VCLK cycles

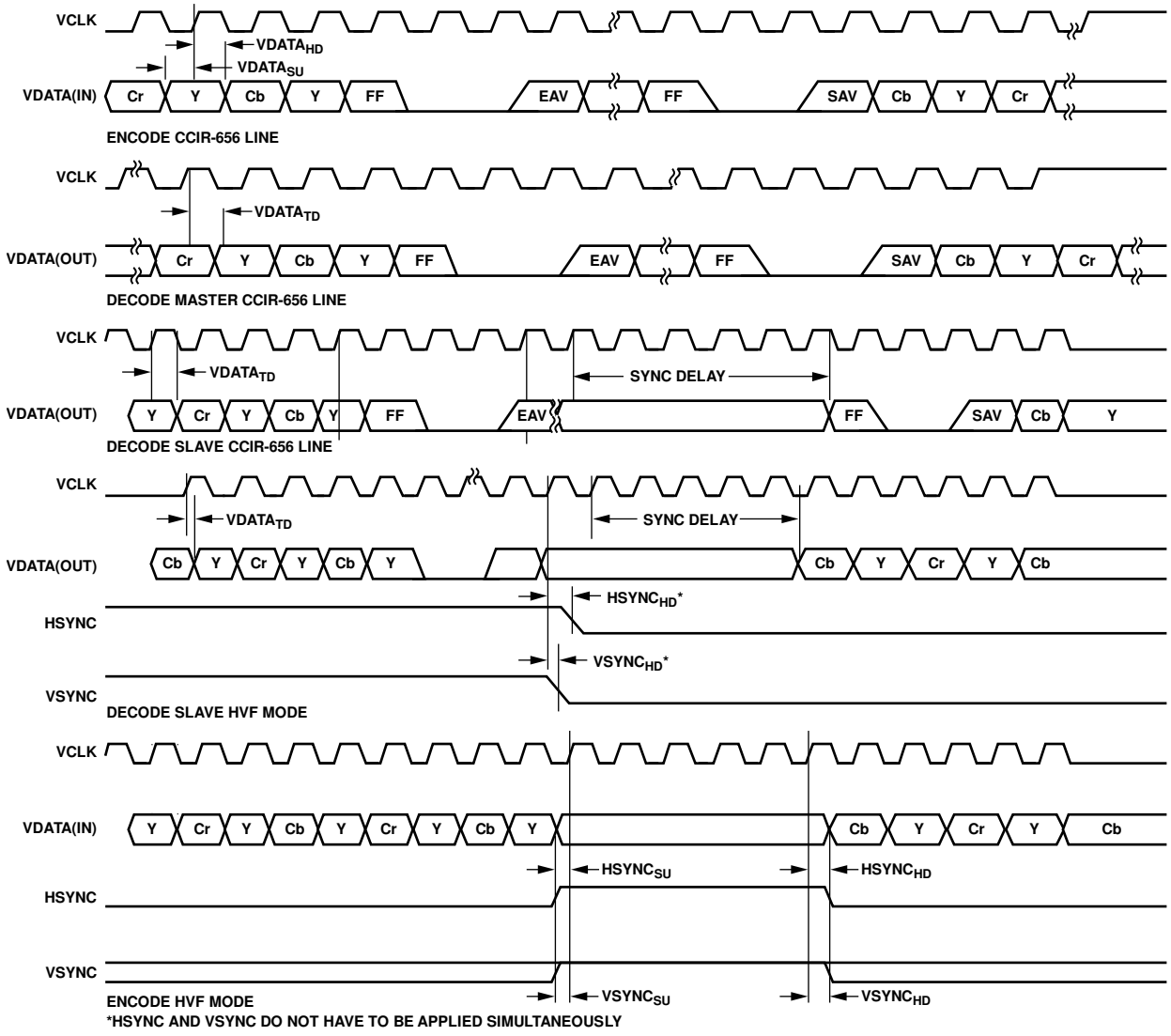

Figure 21. Video Mode Timing

RAW PIXEL MODE TIMING

Table 12.

Parameter	Description	Min	Typ	Max	Unit
$VDATA_{TD}$	VCLK to PIXELDATA Valid Delay (PIXELDATA Output)			12	ns
$VDATA_{SU}$	PIXELDATA Setup to Rising VCLK (PIXELDATA Input)	4			ns
$VDATA_{HD}$	PIXELDATA Hold from Rising VCLK (PIXELDATA Input)	4			ns
$VRDY_{TD}$	VCLK to VRDY Valid Delay			12	ns
$VFRM_{SU}$	VFRM Setup to Rising VCLK (VFRAME Input)	3			ns
$VFRM_{HD}$	VFRM Hold from Rising VCLK (VFRAME Input)	4			ns
$VFRM_{TD}$	VCLK to VFRM Valid Delay (VFRAME Output)			12	ns
$VSTRB_{SU}$	VSTRB Setup to Rising VCLK	4			ns
$VSTRB_{HD}$	VSTRB Hold from Rising VCLK	3			ns

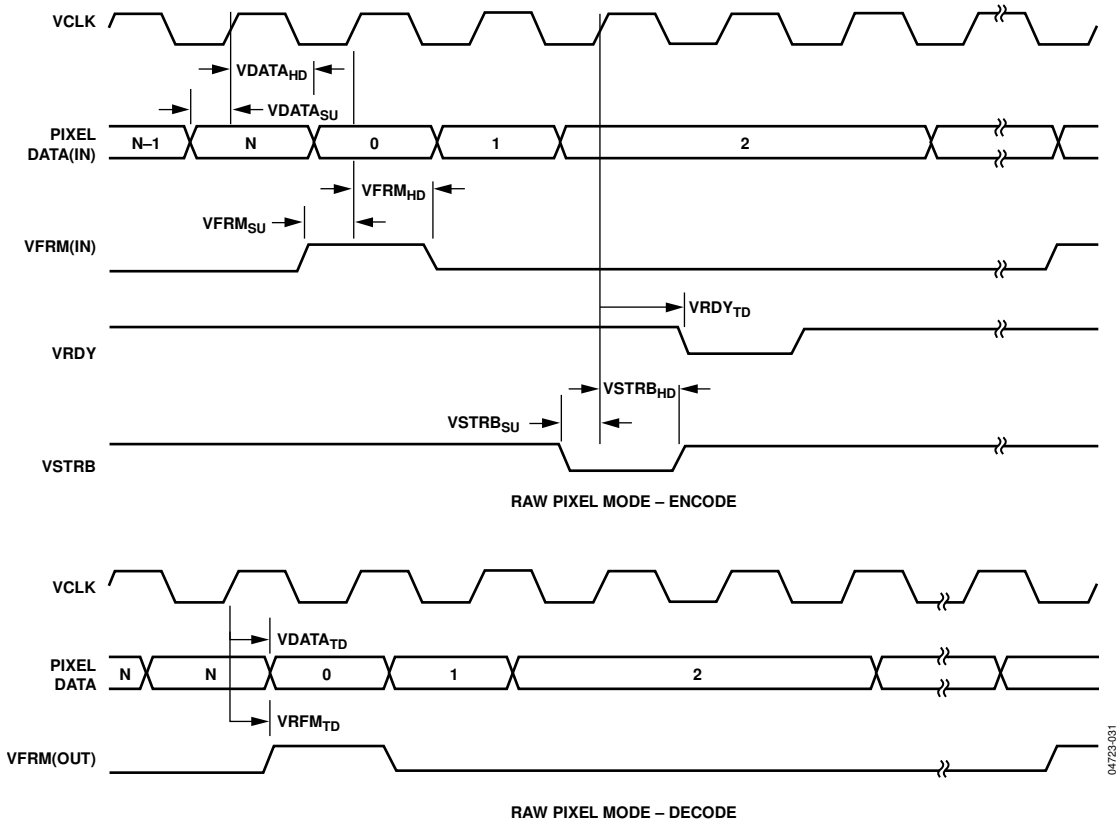

Figure 22. Raw Pixel Mode Timing

ABSOLUTE MAXIMUM RATINGS

Table 13.

Parameter	Rating
VDD (Supply Voltage, Core)	−0.3 V to +1.65 V
IOVDD (Supply Voltage, I/O)	−0.3 V to +IOVDD + 0.3 V
PLLVDD (Supply Voltage, PLL)	−0.3 V to +1.65 V
Storage Temperature (T_S) Range	−65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 14. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ADV202 (144-Lead)	22.5°	3.8°	C/W
ADV202 (121-Lead)	32.8°	7.92°	C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN BGA ASSIGNMENTS AND FUNCTION DESCRIPTIONS

PIN BGA ASSIGNMENTS

Table 15. Pin BGA Assignments for 121-Lead Package

Pin. No.	Pin Location	Pin Description
1	A1	DGND
2	A2	HDATA[2]
3	A3	VDD
4	A4	DGND
5	A5	HDATA[0]
6	A6	HDATA[1]
7	A7	VDATA[1]
8	A8	VDD
9	A9	DGND
10	A10	VDATA[0]
11	A11	DGND
12	B1	HDATA[3]
13	B2	HDATA[4]
14	B3	HDATA[5]
15	B4	HDATA[7]
16	B5	HDATA[8]
17	B6	IOVDD
18	B7	VDATA[6]
19	B8	VDATA[5]
20	B9	VDATA[4]
21	B10	VDATA[2]
22	B11	VDATA[3]
23	C1	DGND
24	C2	HDATA[6]
25	C3	HDATA[9]
26	C4	HDATA[10]
27	C5	HDATA[11]
28	C6	IOVDD
29	C7	VDATA[9]
30	C8	IOVDD
31	C9	VDATA[8]
32	C10	VDATA[7]
33	C11	DGND
34	D1	HDATA[12]
35	D2	HDATA[13]
36	D3	HDATA[14]
37	D4	HDATA[15]
38	D5	IOVDD
39	D6	DGND
40	D7	VDD
41	D8	VSYNC
42	D9	HSYNC
43	D10	VDATA[10]
44	D11	VDATA[11]
45	E1	DGND
46	E2	HDATA[18]_VDATA[14]
47	E3	HDATA[17]_VDATA[13]
48	E4	HDATA[16]_VDATA[12]
49	E5	DGND
50	E6	DGND
51	E7	DGND
52	E8	IOVDD
53	E9	VCLK
54	E10	FIELD
55	E11	DGND
56	F1	DGND
57	F2	HDATA[19]_VDATA[15]
58	F3	HDATA[20]
59	F4	HDATA[21]
60	F5	DGND
61	F6	DGND
62	F7	DGND
63	F8	$\overline{\text{DREQ0}}$
64	F9	$\overline{\text{DACK0}}$
65	F10	$\overline{\text{DREQ1}}$
66	F11	DGND
67	G1	DGND
68	G2	HDATA[22]
69	G3	HDATA[23]
70	G4	HDATA[24]_JDATA[0]
71	G5	DGND
72	G6	DGND
73	G7	DGND
74	G8	IOVDD
75	G9	$\overline{\text{DACK1}}$
76	G10	$\overline{\text{IRQ}}$
77	G11	DGND
78	H1	HDATA[28]_JDATA[4]
79	H2	HDATA[27]_JDATA[3]
80	H3	HDATA[26]_JDATA[2]
81	H4	HDATA[25]_JDATA[1]
82	H5	IOVDD
83	H6	DGND
84	H7	VDD
85	H8	$\overline{\text{ACK}}$
86	H9	$\overline{\text{RD}}$
87	H10	ADDR[1]
88	H11	ADDR[3]
89	J1	DGND
90	J2	HDATA[31]_JDATA[7]
91	J3	HDATA[30]_JDATA[6]
92	J4	HDATA[29]_JDATA[5]
93	J5	IOVDD
94	J6	TEST1
95	J7	$\overline{\text{WE}}$
96	J8	$\overline{\text{CS}}$
97	J9	ADDR[0]

Pin. No.	Pin Location	Pin Description
98	J10	TEST3
99	J11	DGND
100	K1	SCOMM[4]
101	K2	SCOMM[3]
102	K3	SCOMM[0]
103	K4	SCOMM[1]
104	K5	IOVDD
105	K6	IOVDD
106	K7	IOVDD
107	K8	ADDR[2]
108	K9	TEST2
109	K10	TEST5
110	K11	DGND
111	L1	DGND
112	L2	SCOMM[7]
113	L3	SCOMM[6]
114	L4	SCOMM[5]
115	L5	SCOMM[2]
116	L6	TEST4
117	L7	$\overline{\text{RESET}}$
118	L8	DGND
119	L9	MCLK
120	L10	PLLVDD
121	L11	DGND

Table 16. Pin BGA Assignments for 144-Lead Package

Pin No.	Pin Location	Pin Description
1	A1	DGND
2	A2	HDATA[2]
3	A3	HDATA[1]
4	A4	HDATA[0]
5	A5	DGND
6	A6	DGND
7	A7	DGND
8	A8	DGND
9	A9	VDATA[2]
10	A10	VDATA[1]
11	A11	VDATA[0]
12	A12	DGND
13	B1	HDATA[5]
14	B2	HDATA[4]
15	B3	HDATA[3]
16	B4	IOVDD
17	B5	DGND
18	B6	VDD
19	B7	VDD
20	B8	DGND
21	B9	IOVDD
22	B10	VDATA[5]
23	B11	VDATA[4]
24	B12	VDATA[3]
25	C1	HDATA[8]
26	C2	HDATA[7]
27	C3	HDATA[6]
28	C4	IOVDD
29	C5	DGND
30	C6	VDD
31	C7	VDD
32	C8	DGND
33	C9	IOVDD
34	C10	VDATA[8]
35	C11	VDATA[7]
36	C12	VDATA[6]
37	D1	HDATA[11]
38	D2	HDATA[10]
39	D3	HDATA[9]
40	D4	IOVDD
41	D5	DGND
42	D6	VDD
43	D7	VDD
44	D8	DGND
45	D9	IOVDD
46	D10	VDATA[11]
47	D11	VDATA[10]
48	D12	VDATA[9]
49	E1	HDATA[14]
50	E2	HDATA[13]
51	E3	HDATA[12]
52	E4	DGND
53	E5	DGND
54	E6	DGND
55	E7	DGND
56	E8	DGND
57	E9	FIELD
58	E10	VSYNC
59	E11	HSYNC
60	E12	VCLK
61	F1	HDATA[18]_VDATA[14]
62	F2	HDATA[17]_VDATA[13]
63	F3	HDATA[16]_VDATA[12]
64	F4	HDATA[15]
65	F5	DGND
66	F6	DGND
67	F7	DGND
68	F8	DGND
69	F9	$\overline{\text{DACK1}}$
70	F10	$\overline{\text{DREQ1}}$
71	F11	$\overline{\text{DACK0}}$
72	F12	$\overline{\text{DREQ0}}$
73	G1	HDATA[22]
74	G2	HDATA[21]

Pin No.	Pin Location	Pin Description
75	G3	HDATA[20]
76	G4	HDATA[19]_VDATA[15]
77	G5	DGND
78	G6	DGND
79	G7	DGND
80	G8	DGND
81	G9	DGND
82	G10	$\overline{\text{IRQ}}$
83	G11	$\overline{\text{ACK}}$
84	G12	$\overline{\text{RD}}$
85	H1	HDATA[26]_JDATA[2]
86	H2	HDATA[25]_JDATA[1]
87	H3	HDATA[24]_JDATA[0]
88	H4	HDATA[23]
89	H5	DGND
90	H6	DGND
91	H7	DGND
92	H8	DGND
93	H9	DGND
94	H10	$\overline{\text{WR}}$
95	H11	$\overline{\text{CS}}$
96	H12	ADDR[0]
97	J1	HDATA[30]_JDATA[6]
98	J2	HDATA[29]_JDATA[5]
99	J3	HDATA[28]_JDATA[4]
100	J4	HDATA[27]_JDATA[3]
101	J5	DGND
102	J6	VDD
103	J7	VDD
104	J8	DGND
105	J9	DGND
106	J10	ADDR[1]
107	J11	ADDR[2]
108	J12	ADDR[3]
109	K1	SCOMM[1]

Pin No.	Pin Location	Pin Description
110	K2	SCOMM[0]
111	K3	HDATA[31]_JDATA[7]
112	K4	IOVDD
113	K5	DGND
114	K6	VDD
115	K7	VDD
116	K8	DGND
117	K9	IOVDD
118	K10	TEST3
119	K11	TEST2
120	K12	TEST1
121	L1	SCOMM[4]
122	L2	SCOMM[3]
123	L3	SCOMM[2]
124	L4	IOVDD
125	L5	DGND
126	L6	VDD
127	L7	VDD
128	L8	DGND
129	L9	IOVDD
130	L10	TEST5
131	L11	$\overline{\text{RESET}}$
132	L12	MCLK
133	M1	DGND
134	M2	SCOMM[7]
135	M3	SCOMM[6]
136	M4	SCOMM[5]
137	M5	DGND
138	M6	DGND
139	M7	DGND
140	M8	DGND
141	M9	TEST4
142	M10	PLLVDD
143	M11	DGND
144	M12	DGND

PIN FUNCTION DESCRIPTIONS

Table 17.

Mnemonic	Pins Used	121-Lead Package	144-Lead Package	I/O	Description
MCLK	1	L9	L12	I	System Input Clock. For details, see the PLL section. Maximum input frequency on MCLK is 74.25 MHz.
$\overline{\text{RESET}}$	1	L7	L11	I	Reset. Causes the ADV202 to immediately reset. $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WE}}$, $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DREQ0}}$, and $\overline{\text{DREQ1}}$ must be held high when a $\overline{\text{RESET}}$ is applied.
HDATA[15:0]	16	D4 to D1, C5 to C3, B5, B4, C2, B3 to B1, A2, A6 to A5	F4, E1 to E3, D1 to D3, C1 to C3, B1 to B3, A2, A3, A4	I/O	Host Data Bus. With HDATA[23:16], [27:24], [31:28], these pins make up the 32-bit wide host data bus. The async host interface is interfaced together with ADDR[3:0], $\overline{\text{CS}}$, $\overline{\text{WE}}$, $\overline{\text{RD}}$, and $\overline{\text{ACK}}$. Unused HDATA pins should be pulled down via a 10 kΩ resistor.
ADDR[3:0]	4	H11, K8, H10, J9	J12, J11, J10, H12	I	Address Bus for the Host Interface.
$\overline{\text{CS}}$	1	J8	H11	I	Chip Select. This signal is used to qualify addressed read and write access to the ADV202 using the host interface.
$\overline{\text{WE}}$	1	J7	H10	I	Write Enable Used with the Host Interface.
$\overline{\text{RDFB}}$					Read Enable When Fly-By DMA Is Enabled. Note: Simultaneous assertion of $\overline{\text{WE}}$ and $\overline{\text{DACK}}$ low activates the HDATA bus, even if the DMA channels are disabled.
$\overline{\text{RD}}$	1	H9	G12	I	Read Enable. Used with the host interface.
$\overline{\text{WEFB}}$					Write Enable When Fly-By DMA Is Enabled. Note: Simultaneous assertion of $\overline{\text{RD}}$ and $\overline{\text{DACK}}$ low activates the HDATA bus, even if the DMA channels are disabled.
$\overline{\text{ACK}}$	1	H8	G11	O	Acknowledge. Used for direct register accesses. This signal indicates that the last register access was successful. Note: Due to synchronization issues, control and status register accesses can incur an additional delay, so the host software should wait for acknowledgment from the ADV202. Accesses to the FIFOs (external DMA modes), on the other hand, are guaranteed to occur immediately, if space is available, and should not wait for $\overline{\text{ACK}}$, if the timing constraints are observed. If $\overline{\text{ACK}}$ is shared with more than one device, $\overline{\text{ACK}}$ should be connected to a pull-up resistor (10 kΩ) and the PLL_HI register, Bit 4, must be set to 1.
$\overline{\text{IRQ}}$	1	G10	G10	O	Interrupt. This pin indicates that the ADV202 requires the attention of the host processor. This pin can be programmed to indicate the status of the internal interrupt conditions within the ADV202. The interrupt sources are enabled via bits in Register EIRQIE.
$\overline{\text{DREQ0}}$	1	F8	F12	O	Data Request for External DMA Interface. Indicates that the ADV202 is ready to send/receive data to/from the FIFO assigned to DMA Channel 0.
$\overline{\text{FSRQ0}}$				O	Used in DCS-DMA Mode. Service request from the FIFO assigned to Channel 0 (asynchronous mode).
$\overline{\text{VALID}}$				O	Valid Indication for JDATA Input/Output Stream. Polarity of this pin is programmable in the EDMOD0 register. $\overline{\text{VALID}}$ is always an output.
CFG[1]				I	Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to IOVDD or DGND through a 10 kΩ resistor.
$\overline{\text{DACK0}}$	1	F9	F11	I	Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request ($\overline{\text{DREQ0}}$) has been acknowledged and data transfer can proceed. This pin must be held high at all times if the DMA interface is not used, even if the DMA channels are disabled.

Mnemonic	Pins Used	121-Lead Package	144-Lead Package	I/O	Description
$\overline{\text{HOLD}}$				I	External Hold Indication for JDATA Input/Output Stream. Polarity is programmable in the EDMOD0 register. This pin is always an input.
$\overline{\text{FCS0}}$				I	Used in DCS-DMA Mode. Chip select for the FIFO assigned to Channel 0 (asynchronous mode).
$\overline{\text{DREQ1}}$	1	F10	F10	O	Data Request for External DMA Interface. Indicates that the ADV202 is ready to send/receive data to/from the FIFO assigned to DMA Channel 1.
$\overline{\text{FSRQ1}}$				O	Used in DCS-DMA Mode. Service request from the FIFO assigned to Channel 1 (asynchronous mode).
CFG[2]				I	Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to IOVDD or DGND through a 10 kΩ resistor.
$\overline{\text{DACK1}}$	1	G9	F9	I	Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request ($\overline{\text{DREQ1}}$) has been acknowledged and data transfer can proceed. This pin must be held high at all times unless a DMA or JDATA access is occurring. This pin must be held high at all times if the DMA interface is not used, even if the DMA channels are disabled.
$\overline{\text{FCS1}}$				I	Used in DCS-DMA Mode. Chip select for the FIFO assigned to Channel 1 (asynchronous mode).
HDATA[31:28]	4	J2 to J4, H1	K3, J1 to J3	I/O	Host Expansion Bus.
JDATA[7:4]				I/O	JDATA Bus (JDATA Mode).
HDATA[27:24]	4	H2 to H4, G4	J4, H1 to H3	I/O	Host Expansion Bus.
JDATA[3:0]				I/O	JDATA Bus (JDATA Mode).
HDATA[23:16]	8	G3, G2, F4, F3, F2 E2, E3, E4	H4, G1 to G4, F1 to F3	I/O	Host Expansion Bus.
SCOMM[7]	8	L2	M2	I/O	When not used, this pin should be tied low via a 10 kΩ resistor.
SCOMM[6]		L3	M3	I/O	When not used, this pin should be tied low via a 10 kΩ resistor.
SCOMM[5]		L4	M4	I/O	This pin must be used in multiple chip mode to align the outputs of two or more ADV202s. For details, see the Applications section and AN-796 *ADV202 Multichip Application* application note. When not used, this pin should be tied low via a 10 kΩ resistor.
SCOMM[4]		K1	L1	O	LCODE Output in Encode Mode. When LCODE is enabled, the output on this pin indicates on a high transition that the last data-word for a field has been read from the FIFO. For an 8-bit interface, such as JDATA, LCODE is asserted for four consecutive bytes and is enabled by default.
SCOMM[3]		K2	L2	O	This pin should be tied low via a 10 kΩ resistor.
SCOMM[2]		L5	L3	O	This pin should be tied low via a 10 kΩ resistor.
SCOMM[1]		K4	K1	I	This pin should be tied low via a 10 kΩ resistor.
SCOMM[0]		K3	K2	O	This pin should be tied low via a 10 kΩ resistor.
VCLK	1	E9	E12	I	Video Data Clock. Must be supplied if video data is input/output on the VDATA bus.
VDATA[11:0]	12	D11, D10, C7, C9, C10, B7, B8, B9, B11, B10, A7, A10	D10 to D12, C10 to C12, B10 to B12, A9 to A11	I/O	Video Data. Unused pins should be pulled down via a 10 kΩ resistor.
VSYNC	1	D8	E10	I/O	Vertical Sync for Video Mode.
VFRM					Raw Pixel Mode Framing Signal. Indicates first sample of a tile when asserted high.
HSYNC	1	D9	E11	I/O	Horizontal Sync for Video Mode.
VRDY				O	Raw Pixel Mode Ready Signal.