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Wavescale Video Codec

ADV212

FEATURES

- Implementation of a JPEG2000-compatible video CODEC for video and still images through the ADV212 Wavescale video compression/decompression engine
- Identical pinout and footprint to the ADV202; and support for all the functionality of the ADV202
- Power reduction of at least 30% compared with ADV202
- JTAG/boundary scan support
- Patented spatial ultraefficient recursive filtering (SURF) technology for low power, low cost wavelet-based compression
- Support for both 9/7 and 5/3 wavelet transforms with up to 5 levels of transform
- 9/7 wavelet support for tiles up to 1.048 million samples
- 5/3 wavelet support for tiles up to 262,144 samples
- Video interface direct support for ITU-R BT.656, SMPTE 125M PAL/NTSC, SMPTE 274M, SMPTE 293M (525p), and ITU-R BT.1358 (625p) or any video format with a maximum input rate of 65 MSPS for irreversible mode or 40 MSPS for reversible mode
- Programmable tile/image size with widths of up to 4096 pixels in single-component mode; maximum tile/image height of 4096 pixels
- Ability to combine 2 or more ADV212s to support full-frame SMPTE 274M HDTV (1080i) or SMPTE 296M (720p)
- Flexible, asynchronous SRAM-style host interface support for glueless connection to most 16-/32-bit microcontrollers and ASICs
- 2.5 V or 3.3 V input/output and 1.5 V core supply
- 2 package and speed grade options
  - 12 mm × 12 mm, 121-ball CSP_BGA with a speed grade of 115 MHz
  - 13 mm × 13 mm, 144-ball CSP_BGA with a speed grade of 150 MHz

APPLICATIONS

- Networked video and image distribution systems
- Wireless video and image distribution
- Image archival/retrieval
- Digital CCTV and surveillance systems
- Digital cinema systems
- Professional video editing and recording
- Digital still cameras
- Digital camcorders

GENERAL DESCRIPTION

The ADV212 Wavescale® video compression/decompression (CODEC) is a single-chip JPEG2000 CODEC targeted for video and high bandwidth image compression applications that can benefit from the enhanced quality and features provided by the JPEG2000 (J2K) ISO/IEC15444-1 image compression standard. The part implements the computationally intensive operations of the JPEG2000 image compression standard and provides fully compliant code stream generation for most applications.

The dedicated video port of the ADV212 provides glueless connection to common digital video standards such as ITU-R BT.656, SMPTE 125M, SMPTE 293M (525p), ITU-R BT.1358 (625p), SMPTE 274M (1080i), and SMPTE 296M (720p). A variety of other high speed, synchronous pixel and video formats can also be supported by using the programmable framing and validation signals.

The ADV212 is an upgrade version of the ADV202, which is identical in pinout and footprint. It supports all of the functionality of the ADV202 and has the following additional options: JTAG/boundary scan support and power reduction of at least 30% compared with the ADV202.

Advantiv® Advanced Television Solutions by Analog Devices | Wavescale® Compression Technology by Analog Devices

Rev. B

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DOCUMENTATION

Data Sheet

- ADV212: JPEG 2000 Video Codec Data Sheet

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- Advantiv™ Advanced TV Solutions

Technical Articles

- Implementing JPEG2000 compression
- JPEG2000 Codec for Robust, Scalable Pro and Consumer Video

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- ADV212 Material Declaration
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4/08—Rev. 0 to Rev. A

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10/06—Revision 0: Initial Version

The ADV212 can process images at a rate of 40 MSPS in reversible mode and at higher rates when used in irreversible mode. The ADV212 contains a dedicated wavelet transform engine, three entropy CODECs, an on-board memory system, and an embedded reduced instruction set computer (RISC) processor that can provide a complete JPEG2000 compression/decompression solution.

The wavelet processor supports the 9/7 irreversible wavelet transform and the 5/3 wavelet transform in reversible and irreversible modes. The entropy CODECs support all features in the JPEG2000 Part 1 specification except maximum shift region of interest (ROI).

The ADV212 operates on a rectangular array of pixel samples called a tile. A tile can contain a complete image, up to the maximum supported size, or some portion of an image. The maximum horizontal tile size supported depends on the wavelet transform selected and the number of samples in the tile. Images larger than the ADV212 maximum tile size can be broken into individual tiles and then sent sequentially to the chip while maintaining a single, fully compliant JPEG2000 code stream for the entire image.

JPEG2000 FEATURE SUPPORT

The ADV212 supports a broad set of features that are included in Part 1 of the JPEG2000 standard (ISO/IEC 15444).

Depending on the particular application requirements, the ADV212 can provide varying levels of JPEG2000 compression support. It can provide raw code block and attribute data output, which allows the host software to have complete control over generation of the JPEG2000 code stream and other aspects of the compression process such as bit-rate control. Additionally, the ADV212 can create a complete, fully compliant JPEG2000 code stream (J2C) and enhanced file formats such as JP2.

FUNCTIONAL BLOCK DIAGRAM

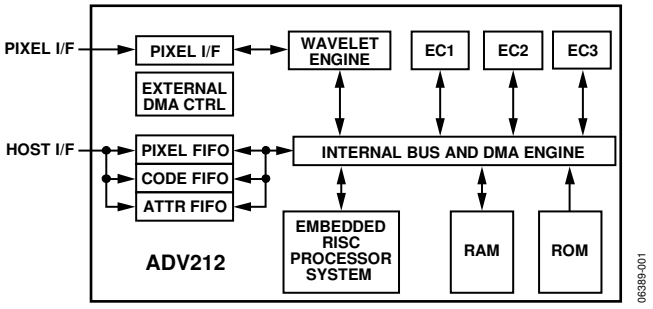

Figure 1.

SPECIFICATIONS

Specifications apply to IOVDD = 2.5 V or 3.3 V over the operating temperature range, unless otherwise specified.

SUPPLY VOLTAGES AND CURRENT

Table 1.

Parameter	Mnemonic	Min	Typ	Max	Unit
DC Supply Voltage, Core	V_{DD}	1.425	1.5	1.575	V
DC Supply Voltage, Input/Output	IOVDD	2.375	2.5	2.625	V
	IOVDD	3.135	3.3	3.465	V
Input Range	V_{IN}	−0.3		$V_{DDI/O}$ + 0.3	V
Operating Ambient Temperature Range in Free Air	T	−40	+25	+85	°C
Static Current[1]	I_{DD}		60		mA
Dynamic Current, Core (JCLK[2] Frequency = 150 MHz)[3]			380	440	mA
Dynamic Current, Core (JCLK[2] Frequency = 108 MHz)			280	320	mA
Dynamic Current, Core (JCLK[2] Frequency = 81 MHz)			210	290	mA
Dynamic Current, Input/Output			40	50	mA

[1] No clock or input/output activity.
[2] For a definition of JCLK, see Figure 32.
[3] ADV212-150 only.

INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Mnemonic	Min	Typ	Max	Unit	Test Conditions
High Level Input Voltage	$V_{IH\ (3.3\ V)}$	2.2			V	V_{DD} = maximum
	$V_{IH\ (2.5\ V)}$	1.9			V	V_{DD} = maximum
Low Level Input Voltage	$V_{IL\ (3.3\ V,\ 2.5\ V)}$			0.6	V	V_{DD} = minimum
High Level Output Voltage	$V_{OH\ (3.3\ V)}$	2.4			V	V_{DD} = minimum, I_{OH} = −0.5 mA
	$V_{OH\ (2.5\ V)}$	2.0			V	V_{DD} = minimum, I_{OH} = −0.5 mA
Low Level Output Voltage	$V_{OL\ (3.3\ V,\ 2.5\ V)}$			0.4	V	V_{DD} = minimum, I_{OL} = +2 mA
High Level Input Current	I_{IH}			1.0	µA	V_{DD} = maximum, V_{IN} = V_{DD}
Low Level Input Current	I_{IL}			1.0	µA	V_{DD} = maximum, V_{IN} = 0 V
High Level Three-State Leakage Current	I_{OZH}			1.0	µA	V_{DD} = maximum, V_{IN} = V_{DD}
Low Level Three-State Leakage Current	I_{OZL}			1.0	µA	V_{DD} = maximum, V_{IN} = 0 V
Input Pin Capacitance	C_I			8	pF	
Output Pin Capacitance	C_O			8	pF	

CLOCK AND $\overline{\text{RESET}}$ SPECIFICATIONS

Table 3.

Parameter	Mnemonic	Min	Typ	Max	Unit
MCLK Period	t_{MCLK}	13.3		100	ns
MCLK Frequency	f_{MCLK}	10		75.18	MHz
MCLK Width Low	t_{MCLKL}	6			ns
MCLK Width High	t_{MCLKH}	6			ns
VCLK Period	t_{VCLK}	13.4		50	ns
VCLK Frequency	f_{VCLK}	20		74.60	MHz
VCLK Width Low	t_{VCLKL}	5			ns
VCLK Width High	t_{VCLKH}	5			ns
$\overline{\text{RESET}}$ Width Low	$t_{\overline{RESET}}$	5			MCLK cycles[1]

[1] For a definition of MCLK, see Figure 32.

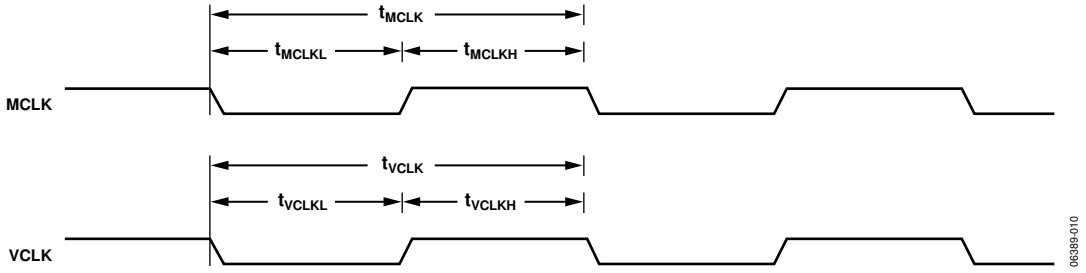

Figure 2. Input Clock

NORMAL HOST MODE—WRITE OPERATION

Table 4.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{WE}$ to $\overline{ACK}$, Direct Registers and FIFO Accesses	$t_{\overline{ACK}}$ (direct)	5		1.5 × JCLK + 7.0[1]	ns
$\overline{WE}$ to $\overline{ACK}$, Indirect Registers	$t_{\overline{ACK}}$ (indirect)	5		2.5 × JCLK + 7.0[1]	ns
Data Setup	t_{SD}	3.0			ns
Data Hold	t_{HD}	1.5			ns
Address Setup	t_{SA}	2			ns
Address Hold	t_{HA}	2			ns
$\overline{CS}$ to $\overline{WE}$ Setup	t_{SC}	0			ns
$\overline{CS}$ Hold	t_{HC}	0			ns
Write Inactive Pulse Width (Minimum Time Until Next $\overline{WE}$ Pulse)	t_{WH}	2.5 JCLK[1]			ns
Write Active Pulse Width	t_{WL}	2.5 JCLK[1]			ns
Write Cycle Time	t_{WCYC}	5 JCLK[1]			ns

[1] For a definition of JCLK, see Figure 32.

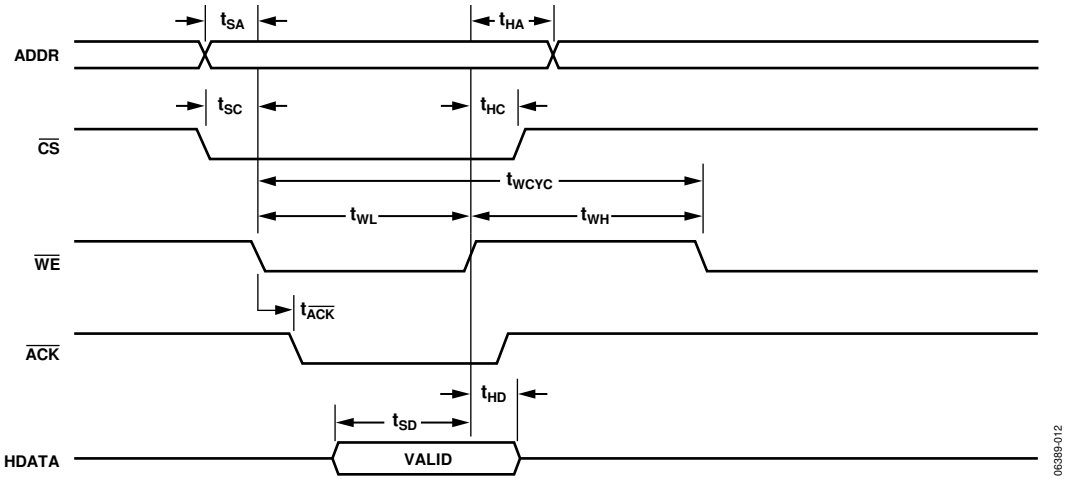

Figure 3. Normal Host Mode—Write Operation

NORMAL HOST MODE—READ OPERATION

Table 5.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{RD}$ to $\overline{ACK}$, Direct Registers and FIFO Accesses	$t_{\overline{ACK}}$ (direct)[1]	5		1.5 × JCLK + 7.0[2]	ns
$\overline{RD}$ to $\overline{ACK}$, Indirect Registers	$t_{\overline{ACK}}$ (indirect)[1]	10.5 JCLK[2]		15.5 × JCLK + 7.0[2]	ns
Read Access Time, Direct Registers	t_{DRD} (direct)	5		1.5 × JCLK + 7.0[2]	ns
Read Access Time, Indirect Registers	t_{DRD} (indirect)	10.5 JCLK[2]		15.5 × JCLK + 7.0[2]	ns
Data Hold	t_{HZRD}	2		8.5	ns
$\overline{CS}$ to $\overline{RD}$ Setup	t_{SC}	0			ns
Address Setup	t_{SA}	2			ns
$\overline{CS}$ Hold	t_{HC}	0			ns
Address Hold	t_{HA}	2			ns
Read Inactive Pulse Width	t_{RH}	2.5 JCLK[2]			ns
Read Active Pulse Width	t_{RL}	2.5 JCLK[2]			ns
Read Cycle Time, Direct Registers	t_{RCYC}	5.0 JCLK[2]			ns

[1] Timing relationship between $\overline{ACK}$ falling transition and HDATA valid is not guaranteed. HDATA valid hold time is guaranteed with respect to $\overline{RD}$ rising transition. A minimum of three JCLK cycles is recommended between $\overline{ACK}$ assert and $\overline{RD}$ deassert.
[2] For a definition of JCLK, see Figure 32.

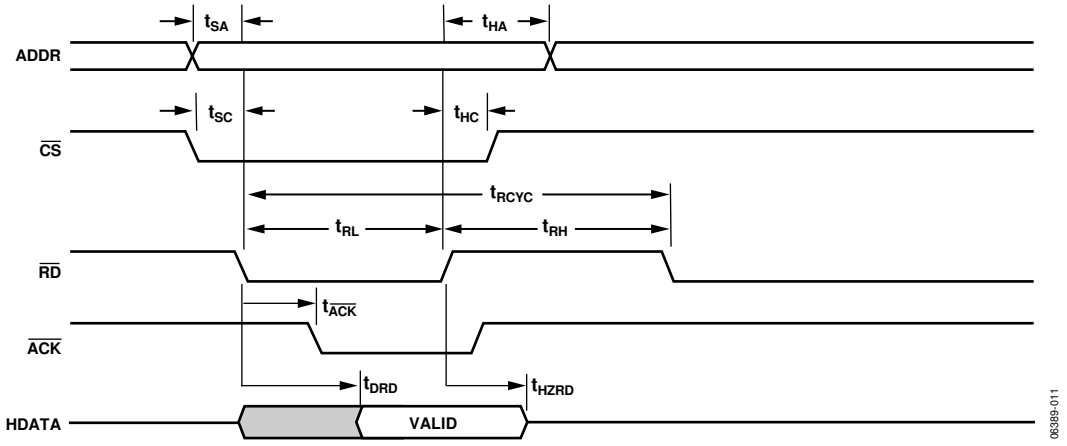

Figure 4. Normal Host Mode—Read Operation

$\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA MODE—SINGLE FIFO WRITE OPERATION

Table 6.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{\text{DREQ}}$ Pulse Width	$\overline{\text{DREQ}}_{\text{PULSE}}$	1 JCLK[1]		15 JCLK[1]	ns
$\overline{\text{DACK}}$ Assert to Subsequent $\overline{\text{DREQ}}$ Delay	$t_{\overline{\text{DREQ}}}$	2.5 JCLK[1]		3.5 × JCLK + 8.5[1]	ns
$\overline{\text{WE}}$ to $\overline{\text{DACK}}$ Setup	$t_{\overline{\text{WE}}_{\text{SU}}}$	0			ns
Data to $\overline{\text{DACK}}$ Deassert Setup	t_{SU}	2			ns
Data to $\overline{\text{DACK}}$ Deassert Hold	t_{HD}	2			ns
$\overline{\text{DACK}}$ Assert Pulse Width	$\overline{\text{DACK}}_{\text{LOW}}$	2 JCLK[1]			ns
$\overline{\text{DACK}}$ Deassert Pulse Width	$\overline{\text{DACK}}_{\text{HIGH}}$	2 JCLK[1]			ns
$\overline{\text{WE}}$ Hold After $\overline{\text{DACK}}$ Deassert	$t_{\overline{\text{WE}}_{\text{HD}}}$	0			ns
$\overline{\text{WE}}$ Assert to $\overline{\text{FSRQ}}$ Deassert (FIFO Full)	$\overline{\text{WFSRQ}}$	1.5 JCLK[1]		2.5 × JCLK + 7.5[1]	ns
$\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Deassert (DR × PULS = 0)	$t_{\overline{\text{DREQ}}_{\text{RTN}}}$	2.5 JCLK[1]		3.5 × JCLK + 9.0[1]	ns

[1] For a definition of JCLK, see Figure 32.

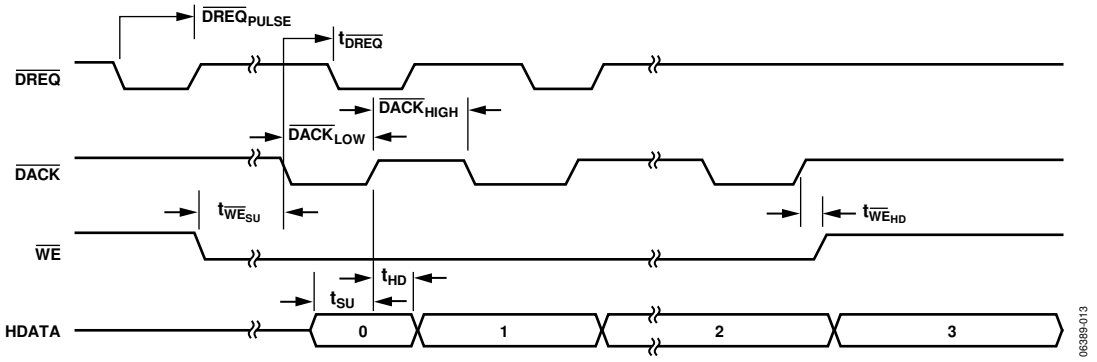

Figure 5. Single Write for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:1] Not Programmed to a Value of 0000)

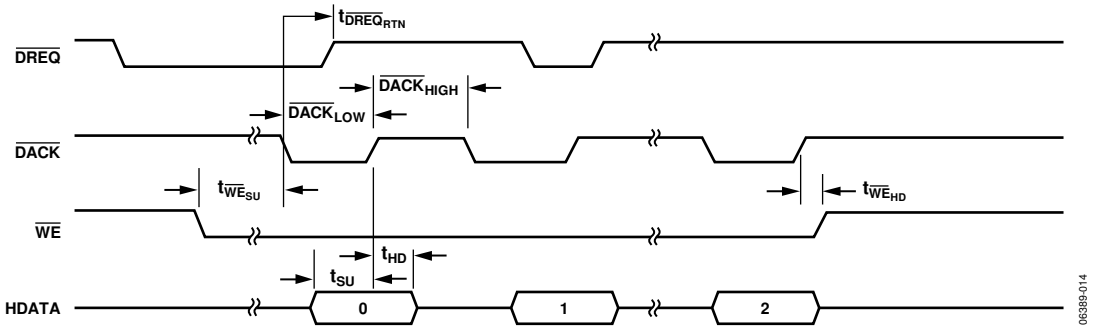

Figure 6. Single Write for $\overline{\text{DREQ}}/\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

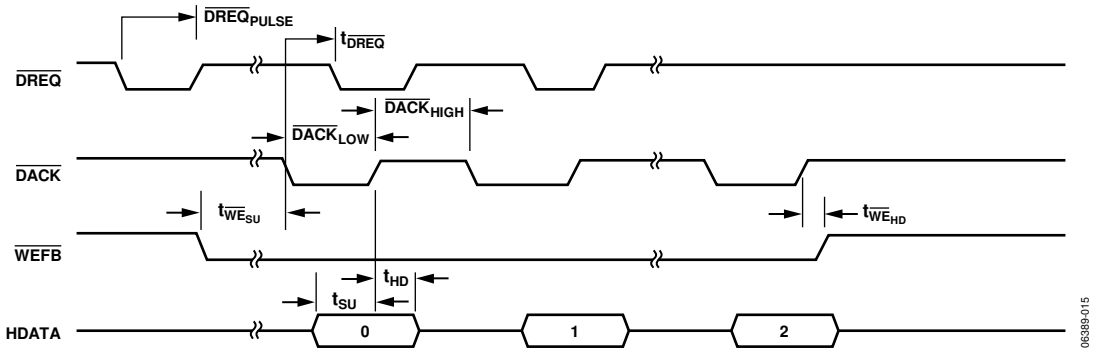

Figure 7. Single Write Cycle for Fly-By DMA Mode (DREQ Pulse Width Is Programmable)

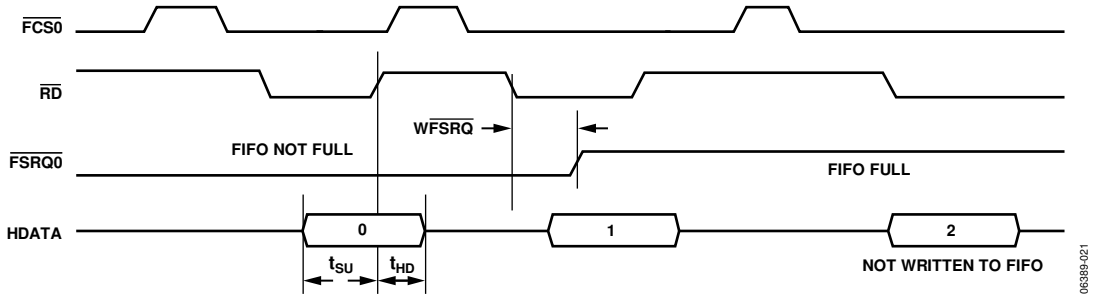

Figure 8. Single Write Access for DCS DMA Mode

$\overline{\text{DREQ}}$/$\overline{\text{DACK}}$ DMA MODE—SINGLE FIFO READ OPERATION

Table 7.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{\text{DREQ}}$ Pulse Width	$\overline{\text{DREQ}}_{\text{PULSE}}$	1 JCLK [1]		15 JCLK[1]	ns
$\overline{\text{DACK}}$ Assert to Subsequent $\overline{\text{DREQ}}$ Delay	$t_{\overline{\text{DREQ}}}$	2.5 JCLK[1]		3.5 × JCLK + 9.0[1]	ns
$\overline{\text{RD}}$ to $\overline{\text{DACK}}$ Setup	$t_{\overline{\text{RD}}_{\text{SU}}}$	0			ns
$\overline{\text{DACK}}$ to Data Valid	$t_{\overline{\text{RD}}}$	2.5		11	ns
Data Hold	t_{HD}	1.5			ns
$\overline{\text{DACK}}$ Assert Pulse Width	$\overline{\text{DACK}}_{\text{LOW}}$	2 JCLK[1]			ns
$\overline{\text{DACK}}$ Deassert Pulse Width	$\overline{\text{DACK}}_{\text{HIGH}}$	2 JCLK[1]			ns
$\overline{\text{RD}}$ Hold after $\overline{\text{DACK}}$ Deassert	$t_{\overline{\text{RD}}_{\text{HD}}}$	0			ns
$\overline{\text{RD}}$ Assert to $\overline{\text{FSRQ}}$ Deassert (FIFO Empty)	$\overline{\text{RDFSRQ}}$	1.5 JCLK[1]		2.5 × JCLK + 9.0[1]	ns
$\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Deassert (DR × PULS = 0)	$t_{\overline{\text{DREQ}}_{\text{RTN}}}$	2.5 JCLK[1]		3.5 × JCLK + 9.0[1]	ns

[1] For a definition of JCLK, see Figure 32.

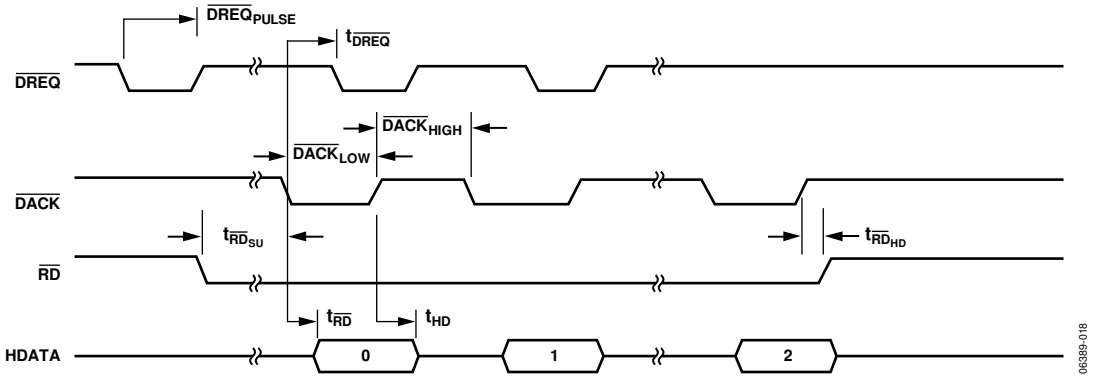

Figure 9. Single Read for $\overline{\text{DREQ}}$/$\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Not Programmed to a Value of 0000)

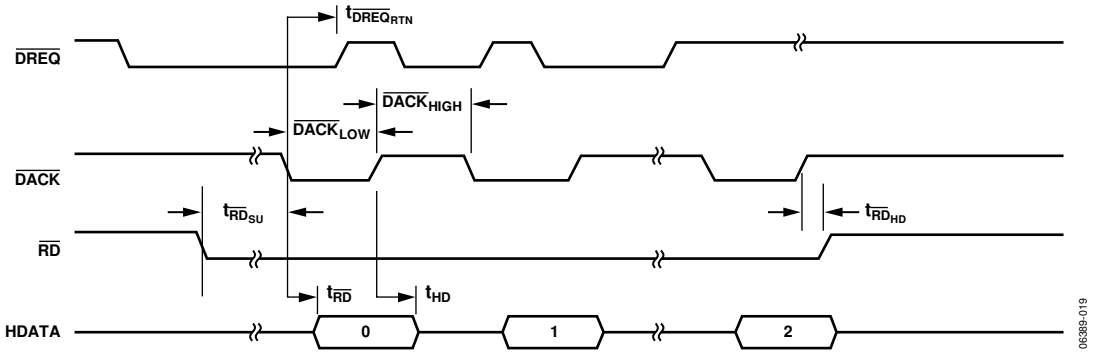

Figure 10. Single Read for $\overline{\text{DREQ}}$/$\overline{\text{DACK}}$ DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

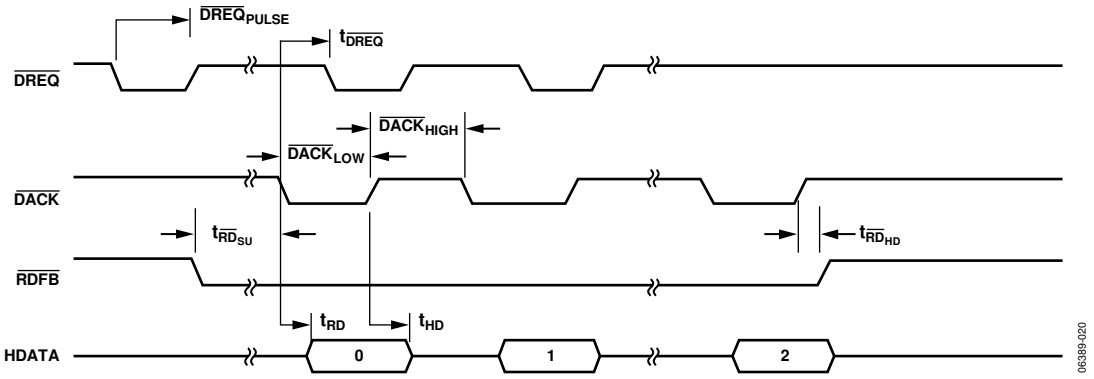

Figure 11. Single Read Cycle for Fly-By DMA Mode (DREQ Pulse Width Is Programmable)

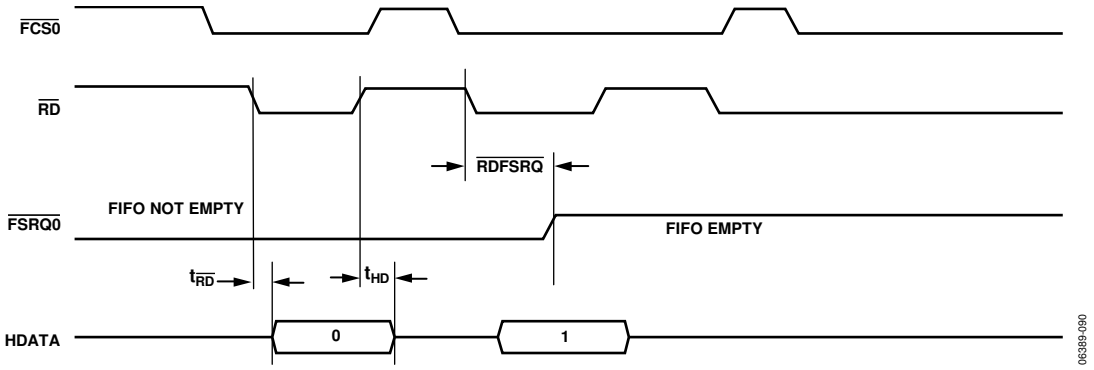

Figure 12. Single Read Access for DCS DMA Mode

EXTERNAL DMA MODE—FIFO WRITE, BURST MODE

Table 8.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{\text{DREQ}}$ Pulse Width[1]	$\overline{\text{DREQ}}_{\text{PULSE}}$	1 JCLK [2]		15 JCLK[2]	ns
$\overline{\text{WE}}$ to $\overline{\text{DREQ}}$ Deassert (DR × PULS = 0)	$t_{\overline{\text{DREQ}}_{\text{RTN}}}$	2.5 JCLK[2]		3.5 × JCLK + 7.5[2]	ns
$\overline{\text{DACK}}$ to $\overline{\text{WE}}$ Setup	$t_{\overline{\text{DACK}}_{\text{SU}}}$	0			ns
Data Setup	t_{SU}	2.5			ns
Data Hold	t_{HD}	2			ns
$\overline{\text{WE}}$ Assert Pulse Width	$\overline{\text{WE}}_{\text{LOW}}$	1.5 JCLK[2]			ns
$\overline{\text{WE}}$ Deassert Pulse Width	$\overline{\text{WE}}_{\text{HIGH}}$	1.5 JCLK[2]			ns
$\overline{\text{WE}}$ Deassert to Next $\overline{\text{DREQ}}$	$t_{\overline{\text{DREQ}}_{\text{WAIT}}}$	2.5 JCLK[2]		4.5 × JCLK + 9.0[2]	ns
$\overline{\text{WE}}$ Deassert to $\overline{\text{DACK}}$ Deassert	$t_{\overline{\text{WE\_DACK}}}$	0			ns

[1] Applies to assigned DMA channel, if EDMOD0/EDMOD1[14:11] is programmed to a nonzero value.
[2] For a definition of JCLK, see Figure 32.

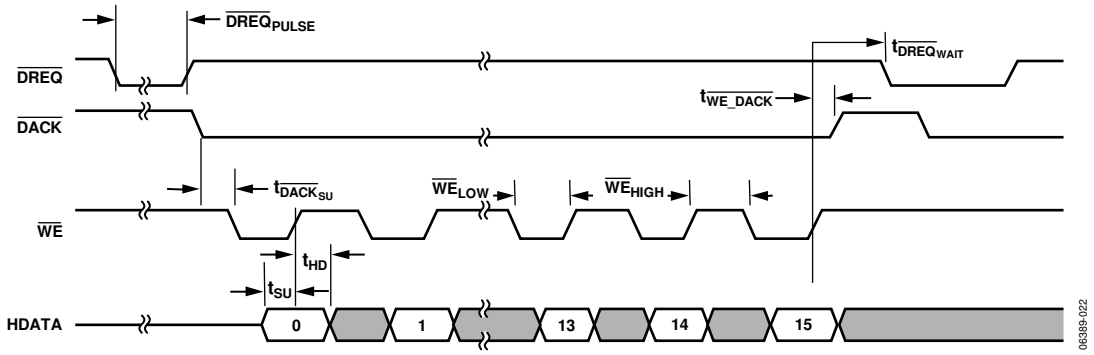

Figure 13. Burst Write Cycle for $\overline{\text{DREQ}}$/DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:1] Not Programmed to a Value of 0000)

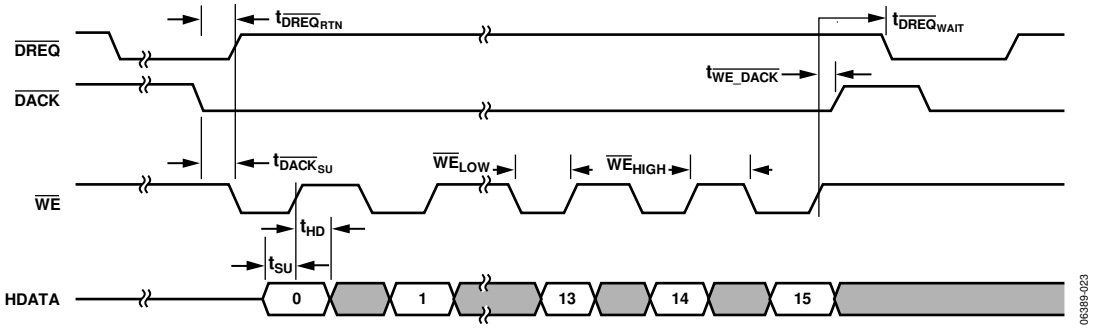

Figure 14. Burst Write Cycle for $\overline{\text{DREQ}}$/DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

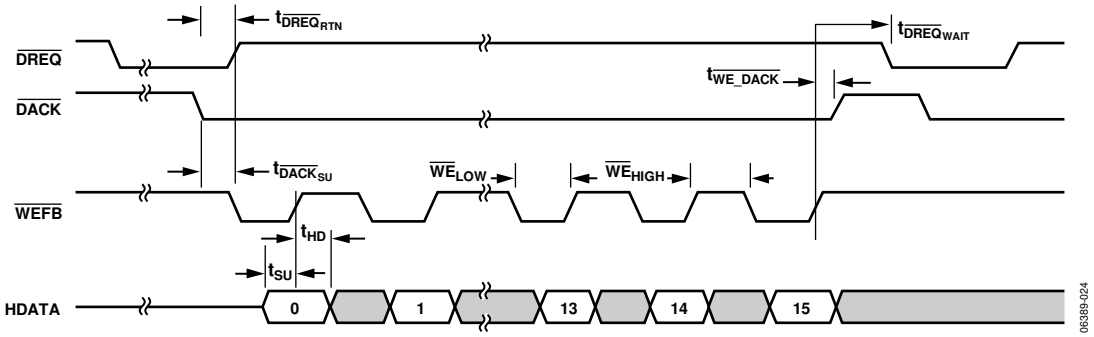

Figure 15. Burst Write Cycle for Fly-By DMA Mode

EXTERNAL DMA MODE—FIFO READ, BURST MODE

Table 9.

Parameter	Mnemonic	Min	Typ	Max	Unit
$\overline{DREQ}$ Pulse Width[1]	$\overline{DREQ}_{PULSE}$	1 JCLK [2]		15 JCLK[2]	ns
$\overline{RD}$ to $\overline{DREQ}$ Deassert (DR × PULS = 0)	$t_{\overline{DREQ}_{RTN}}$	2.5 JCLK[2]		3.5 × JCLK + 7.5[2]	ns
$\overline{DACK}$ to $\overline{RD}$ Setup	$t_{\overline{DACK}_{SU}}$	0			ns
$\overline{RD}$ to Data Valid	$t_{\overline{RD}}$	2.5		9.7	ns
Data Hold	t_{HD}	2.5			ns
$\overline{RD}$ Assert Pulse Width	$\overline{RD}_{LOW}$	1.5 JCLK[2]			ns
$\overline{RD}$ Deassert Pulse Width	$\overline{RD}_{HIGH}$	1.5 JCLK[2]			ns
$\overline{RD}$ Deassert to Next $\overline{DREQ}$	$t_{\overline{DREQ}_{WAIT}}$	2.5 JCLK[2]		3.5 × JCLK + 7.5[2]	ns
$\overline{RD}$ Deassert to $\overline{DACK}$ Deassert	$t_{\overline{RD\_DACK}}$	0			ns

[1] Applies to assigned DMA channel if EDMOD0 or EDMOD1 <14:11> is programmed to a nonzero value.
[2] For a definition of JCLK, see Figure 32.

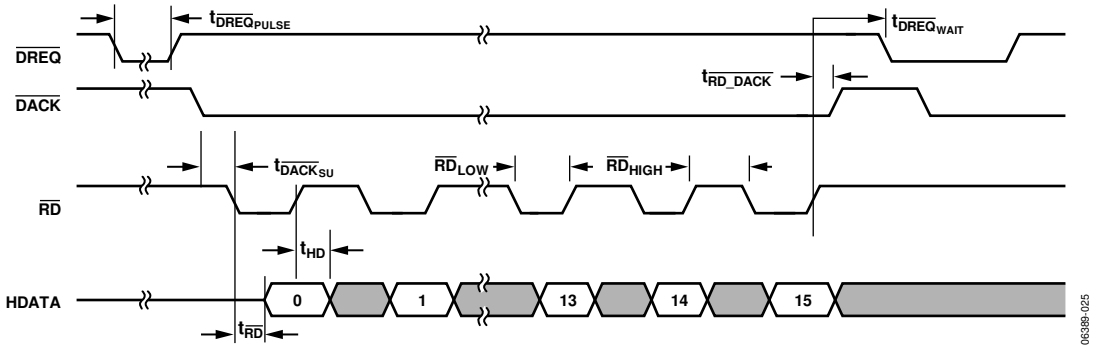

Figure 16. Burst Read Cycle for $\overline{DREQ}/\overline{DACK}$ DMA Mode for Assigned DMA Channel (EMOD0/EDMOD1[14:11] Not Programmed to a Value of 0

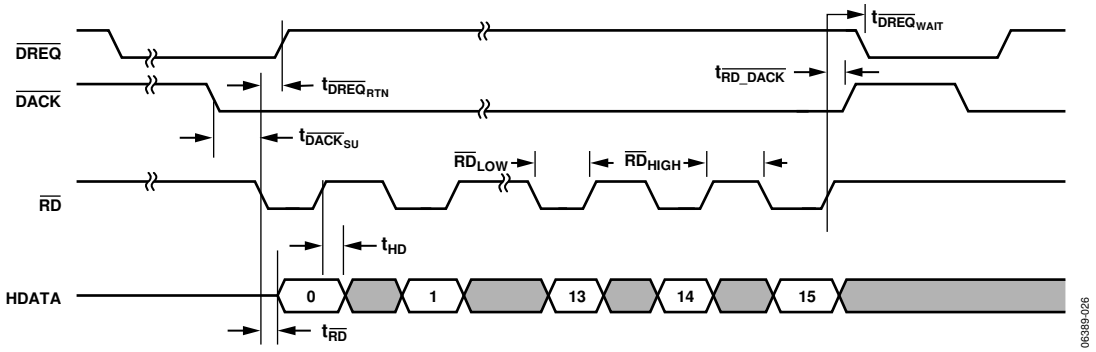

Figure 17. Burst Read Cycle for $\overline{DREQ}/\overline{DACK}$ DMA Mode for Assigned DMA Channel (EMOD0/EDMOD1[14:11] Programmed to a Value of 0000)

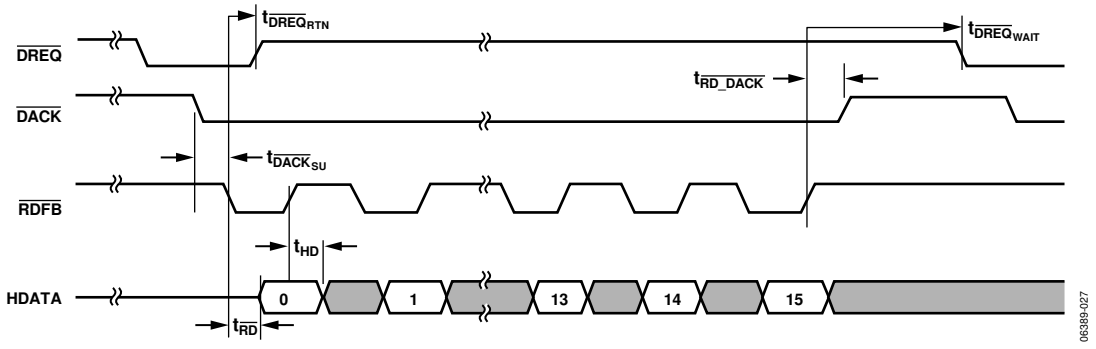

Figure 18. Burst Read Cycle for Fly-By DMA Mode

STREAMING MODE (JDATA)—FIFO READ/WRITE

Table 10.

Parameter	Mnemonic	Min	Typ	Max	Unit
MCLK to JDATA Valid	$JDATA_{TD}$	1.5 JCLK[1]		2.5 × JCLK + 9.5[1]	ns
MCLK to VALID Assert/Deassert	$VALID_{TD}$	1.5 JCLK[1]		2.5 × JCLK + 8.0[1]	ns
HOLD Setup to Rising MCLK	$HOLD_{SU}$	3			ns
HOLD Hold from Rising MCLK	$HOLD_{HD}$	3			ns
JDATA Setup to Rising MCLK	$JDATA_{SU}$	3			ns
JDATA Hold from Rising MCLK	$JDATA_{HD}$	3			ns

[1] For a definition of JCLK, see Figure 32.

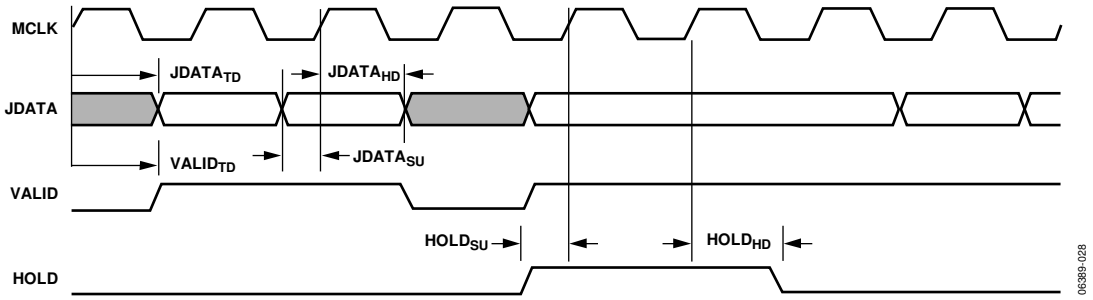

Figure 19. Streaming Mode Timing—Encode Mode JDATA Output

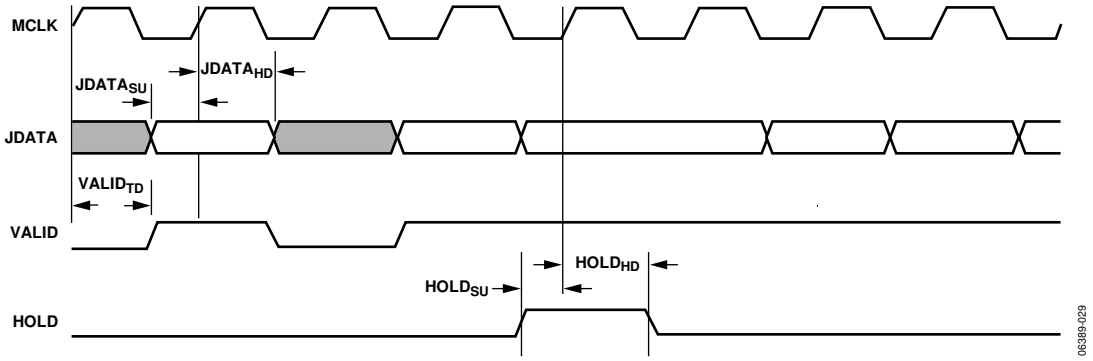

Figure 20. Streaming Mode Timing—Decode Mode JDATA Input

VDATA MODE TIMING

Table 11.

Parameter	Mnemonic	Min	Typ	Max	Unit
VCLK to VDATA Valid Delay (VDATA Output)	$VDATA_{TD}$			12	ns
VDATA Setup to Rising VCLK (VDATA Input)	$VDATA_{SU}$	4			ns
VDATA Hold from Rising VCLK (VDATA Input)	$VDATA_{HD}$	4			ns
HSYNC Setup to Rising VCLK	$HSYNC_{SU}$	3			ns
HSYNC Hold from Rising VCLK	$HSYNC_{HD}$	4			ns
VCLK to HSYNC Valid Delay	$HSYNC_{TD}$			12	ns
VSYNC Setup to Rising VCLK	$VSYNC_{SU}$	3			ns
VSYNC Hold from Rising VCLK	$VSYNC_{HD}$	4			ns
VCLK to VSYNC Valid Delay	$VSYNC_{TD}$			12	ns
FIELD Setup to Rising VCLK	$FIELD_{SU}$	4			ns
FIELD Hold from Rising VCLK	$FIELD_{HD}$	3			ns
VCLK to FIELD Valid	$FIELD_{TD}$			12	
Decode Slave Data Sync Delay (HSYNC Low to First 0xFF of EAV/SAV Code)	SYNC DELAY		8[1]		VCLK cycles
Decode Slave Data Sync Delay (HSYNC Low to First Data for HVF Mode)			10[1]		VCLK cycles

[1] The sync delay value varies according to the application.

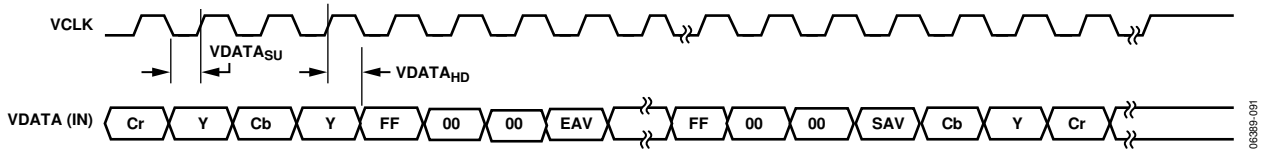

Figure 21. Encode Video Mode Timing—CCIR 656 Mode

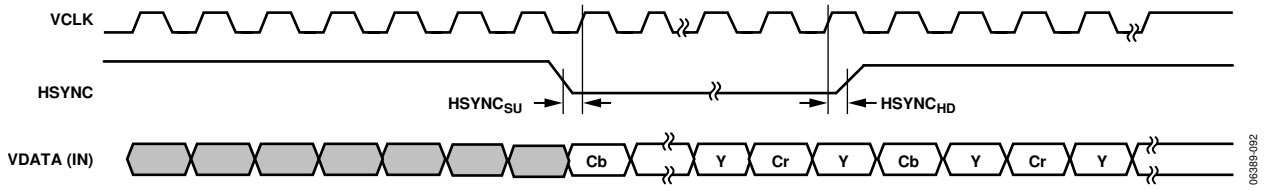

Figure 22. Encode Video Mode Timing—HVF Mode (HSYNC Timing)
(HSYNC Programmed for Negative Polarity)

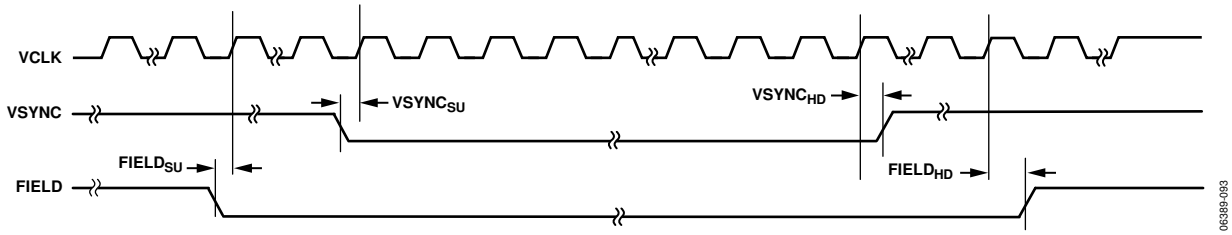

Figure 23. Encode Video Mode Timing—HVF Mode (VSYNC and FIELD Timing)
(VSYNC and FIELD Programmed for Negative Polarity)

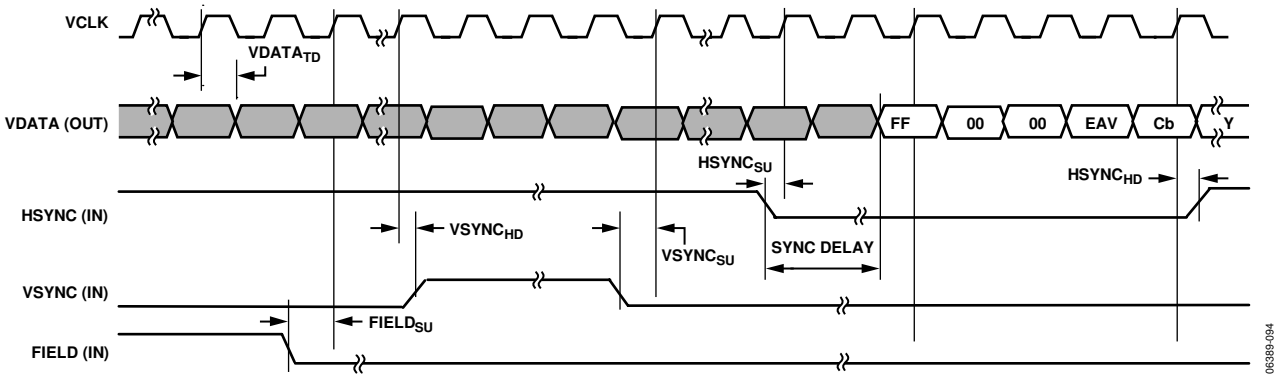

Figure 24. Decode Video Mode Timing—CCIR 656 Mode, Decode Slave (HSYNC, VSYNC, and FIELD Programmed to Negative Polarity)

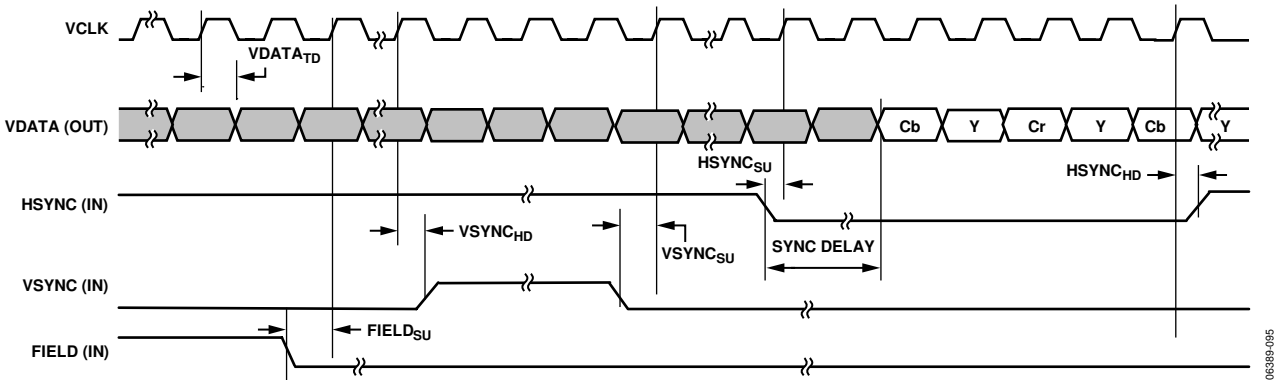

Figure 25. Decode Video Mode Timing—HVF Mode, Decode Slave (HSYNC, VSYNC, and FIELD Programmed to Negative Polarity)

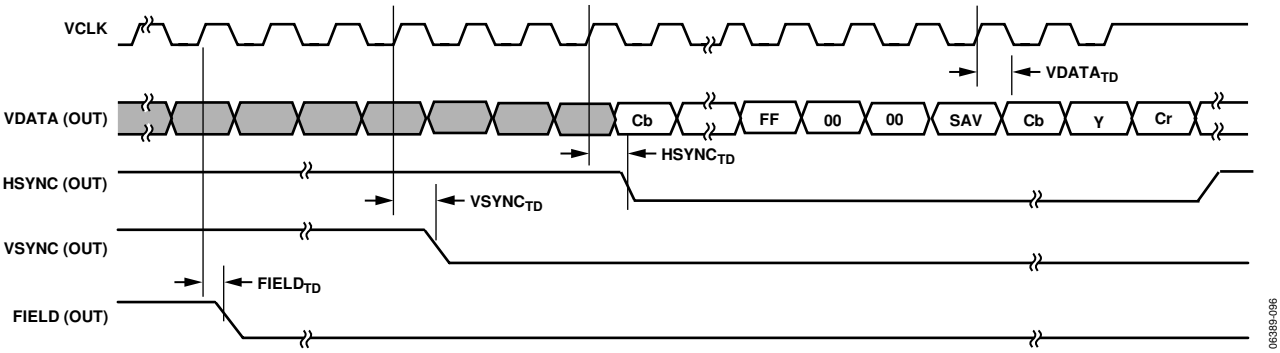

Figure 26. Decode Video Mode Timing—CCIR 656 Mode, Decode Master (HSYNC, VSYNC, and FIELD Programmed to Negative Polarity)

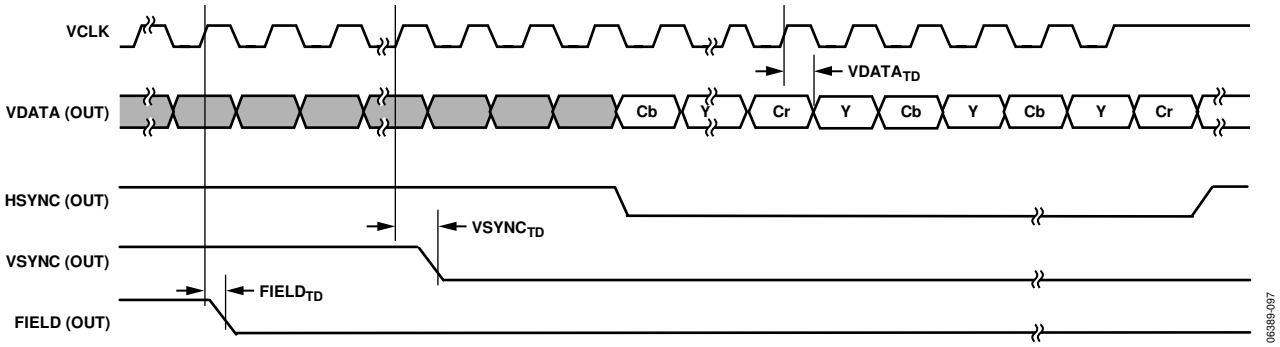

Figure 27. Decode Video Mode Timing—HVF Mode, Decode Master (HSYNC, VSYNC, and FIELD Programmed to Negative Polarity)

RAW PIXEL MODE TIMING

Table 12.

Parameter	Mnemonic	Min	Typ	Max	Unit
VCLK to PIXELDATA Valid Delay (PIXELDATA Output)[1]	$VDATA_{TD}$			12	ns
PIXELDATA Setup to Rising VCLK (PIXELDATA Input)	$VDATA_{SU}$	4			ns
PIXELDATA Hold from Rising VCLK (PIXELDATA Input)	$VDATA_{HD}$	4			ns
VCLK to VRDY Valid Delay	$VRDY_{TD}$			12	ns
VFRM Setup to Rising VCLK (VFRAME Input)	$VFRM_{SU}$	3			ns
VFRM Hold from Rising VCLK (VFRAME Input)	$VFRM_{HD}$	4			ns
VCLK to VFRM Valid Delay (VFRAME Output)	$VFRM_{TD}$			12	ns
VSTRB Setup to Rising VCLK	$VSTRB_{SU}$	4			ns
VSTRB Hold from Rising VCLK	$VSTRB_{HD}$	3			ns

[1] PIXELDATA is the actual data on the VDATA bus; pins and bus width depend on it but timing does not.

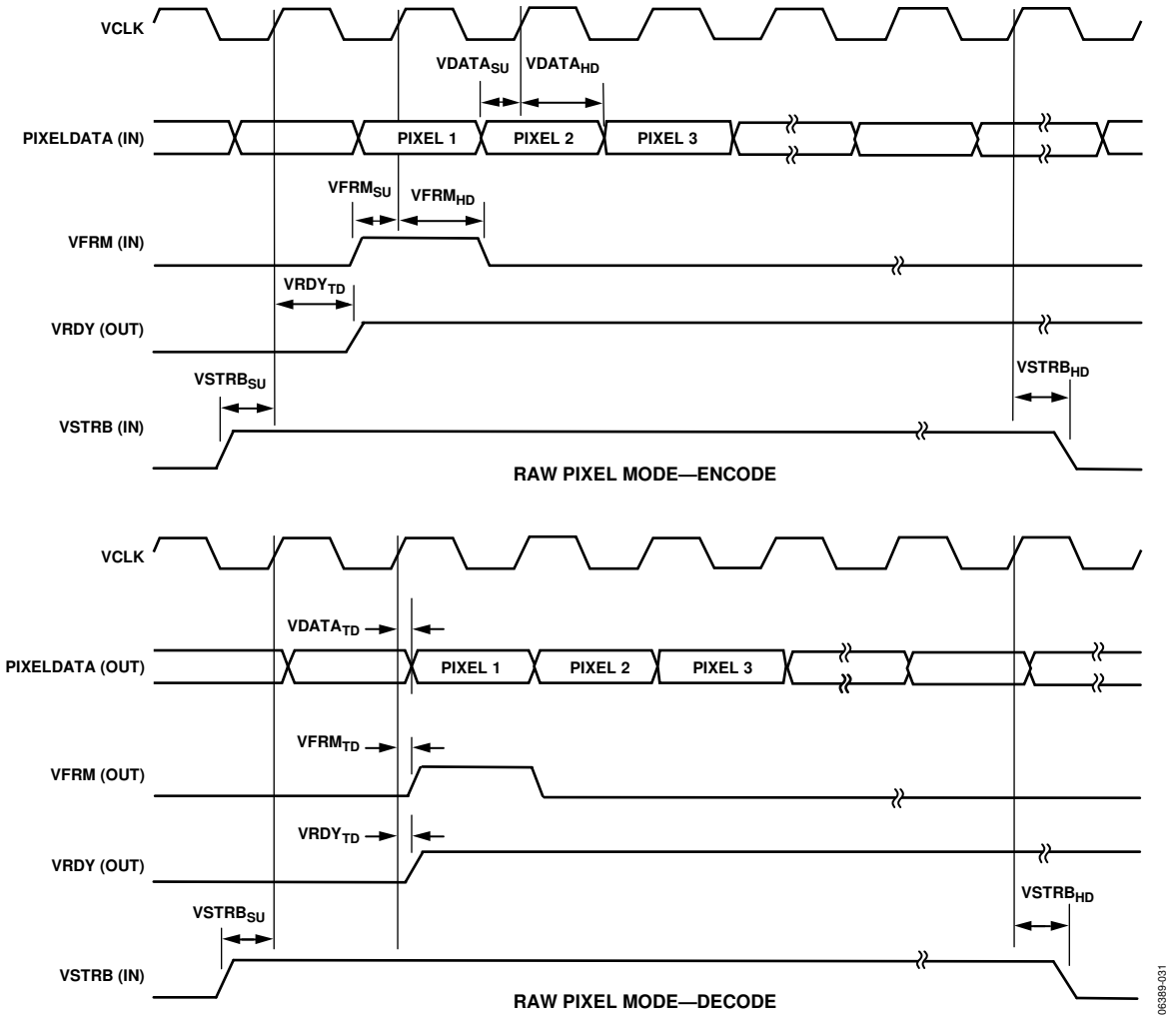

Figure 28. Raw Pixel Modes

JTAG TIMING

Table 13.

Parameter	Mnemonic	Min	Typ	Max	Unit
TCK Period	TCK	134			ns
TDI or TMS Setup Time	TDI_{SU}	4.0			ns
TDI or TMS Hold Time	TDI_{HD}	4.0			ns
TDO Hold Time	TDO_{HD}	0.0			ns
TDO Valid	TDO_{VALID}			10.0	ns
TRS Hold Time	TRS_{HD}	4.0			ns
TRS Setup Time	TRS_{SU}	4.0			ns
TRS Pulse Width Low	TRS_{LOW}	4			TCK cycles

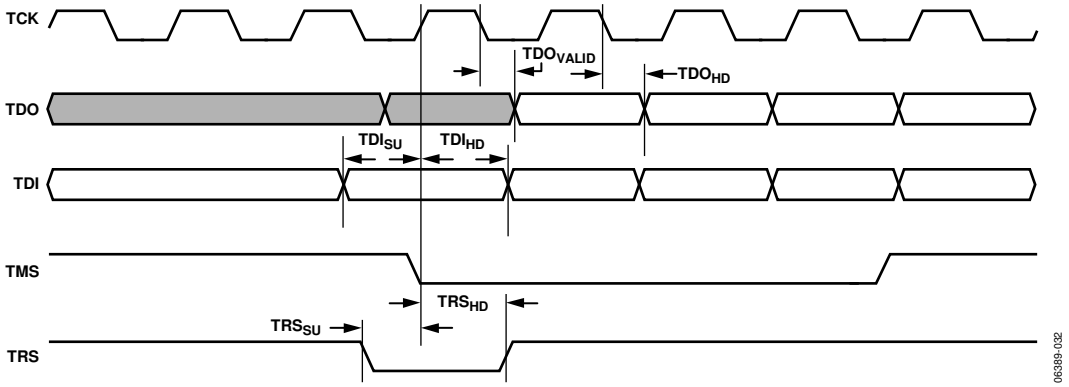

Figure 29. JTAG Timing

ABSOLUTE MAXIMUM RATINGS

Table 14.

Parameter	Rating
V_{DD} – Supply Voltage, Core	–0.3 V to +1.65 V
IOVDD – Supply Voltage, Input/Output	–0.3 V to +3.63 V
Storage Temperature (T_S)	–65°C to +150°C
Reflow Soldering	
RoHS-Compliant, 121-Ball	260°C (20 sec to 40 sec)
RoHS-Compliant, 144-Ball	260°C (20 sec to 40 sec)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 15. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
144-Ball ADV212BBCZ	22.5	3.8	°C/W
121-Ball ADV212BBCZ	32.8	7.92	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

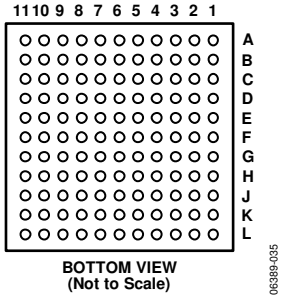

Figure 30.121-Ball Pin Configuration

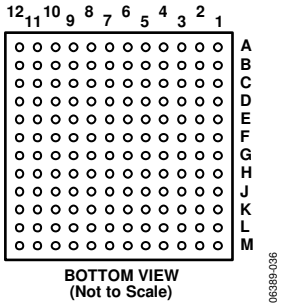

Figure 31. 144-Ball Pin Configuration

Table 16. Pin Function Descriptions

121-Ball Package		144-Ball Package					
Pin No.	**Location**	**Pin No.**	**Location**	**Mnemonic**	**Pins Used**	**Type**	**Description**
119	L9	132	L12	MCLK	1	I	System Input Clock. See the PLL Registers section.
117	L7	131	L11	$\overline{\text{RESET}}$	1	I	Reset. Causes the ADV212 to immediately reset. $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WE}}$, $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DREQ0}}$, and $\overline{\text{DREQ1}}$ must be held high when a $\overline{\text{RESET}}$ is applied.
37 to 34, 27 to 25, 16, 15, 24, 14 to 12, 2, 6, 5	D4 to D1, C5 to C3, B5, B4, C2, B3 to B1, A2, A6, A5	64, 49 to 51, 37 to 39, 25 to 27, 13 to 15, 2 to 4	F4, E1 to E3, D1 to D3, C1 to C3, B1 to B3, A2 to A4	HDATA[15:0]	16	I/O	Host Data Bus. With HDATA[23:16], HDATA[27:24], and HDATA[31:28], these pins make up the 32-bit wide host data bus. The async host interface is interfaced together with ADDR[3:0], $\overline{\text{CS}}$, $\overline{\text{WE}}$, $\overline{\text{RD}}$, and $\overline{\text{ACK}}$. Unused HDATA pins should be pulled down via a 10 kΩ resistor.
88, 107, 87, 97	H11, K8, H10, J9	108 to 106, 96	J12 to J10, H12	ADDR[3:0]	4	I	Address Bus for the Host Interface.
96	J8	95	H11	$\overline{\text{CS}}$	1	I	Chip Select. This signal is used to qualify addressed read and write access to the ADV212 using the host interface.
95	J7	94	H10	$\overline{\text{WE}}$[1]	1	I	Write Enable Used with the Host Interface.
				$\overline{\text{RDFB}}$[2]			Read Enable When Fly-By DMA Is Enabled. Simultaneous assertion of $\overline{\text{WE}}$ and $\overline{\text{DACK}}$ low activates the HDATA bus, even if the DMA channels are disabled.
86	H9	84	G12	$\overline{\text{RD}}$[1]	1	I	Read Enable Used with the Host Interface.
				$\overline{\text{WEFB}}$[3]			Write Enable When Fly-By DMA Is Enabled. Simultaneous assertion of $\overline{\text{RD}}$ and $\overline{\text{DACK}}$ low activates the HDATA bus, even if the DMA channels are disabled.

121-Ball Package		144-Ball Package					
Pin No.	Location	Pin No.	Location	Mnemonic	Pins Used	Type	Description
85	H8	83	G11	$\overline{ACK}$	1	O	Acknowledge. Used for direct register accesses. This signal indicates that the last register access was successful. Due to synchronization issues, control and status register accesses may incur an additional delay; therefore, the host software should wait for acknowledgment from the ADV212 before attempting another register access. Accesses to the FIFOs (external DMA modes), on the other hand, are guaranteed to occur immediately, provided that space is available; therefore, the host software does not need to wait for $\overline{ACK}$ before attempting another register access, provided that the timing constraints are observed. If $\overline{ACK}$ is shared with more than one device, $\overline{ACK}$ should be connected to a pull-up resistor (10 kΩ) and the PLL_HI register, Bit 4, must be set to 1.
76	G10	82	G10	$\overline{IRQ}$	1	O	Interrupt. This pin indicates that the ADV212 requires the attention of the host processor. This pin can be programmed to indicate the status of the internal interrupt conditions within the ADV212. The interrupt sources are enabled via the bits in the EIRQIE register.
63	F8	72	F12	$\overline{DREQ0}$	1	O	Data Request for External DMA Interface. Indicates that the ADV212 is ready to send/receive data to/from the FIFO assigned to DMA Channel 0.
				$\overline{FSRQ0}$		O	FIFO Service Request. Used in DCS-DMA mode. Service request from the FIFO assigned to Channel 0 (asynchronous mode).
				VALID		O	Valid Indication for JDATA Input/Output Stream. Polarity of this pin is programmable in the EDMOD0 register. VALID is always an output.
				CFG1		I	Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to IOVDD through a 10 kΩ resistor.
64	F9	71	F11	$\overline{DACK0}$	1	I	Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request ($\overline{DREQ0}$) has been acknowledged and that the data transfer can proceed. This pin must be held high at all times if the DMA interface is not used, even if the DMA channels are disabled.
				HOLD		I	External Hold Indication for JDATA Input/Output Stream. Polarity is programmable in the EDMOD0 register. This pin is always an input.
				$\overline{FCS0}$		I	FIFO Chip Select. Used in DCS-DMA mode. Chip select for the FIFO assigned to Channel 0 (asynchronous mode).

121-Ball Package		144-Ball Package					
Pin No.	Location	Pin No.	Location	Mnemonic	Pins Used	Type	Description
65	F10	70	F10	$\overline{\text{DREQ1}}$	1	O	Data Request for External DMA Interface. Indicates that the ADV212 is ready to send/receive data to/from the FIFO assigned to DMA Channel 1.
				$\overline{\text{FSRQ1}}$		O	FIFO Service Request. Used in DCS-DMA mode. Service request from the FIFO assigned to Channel 1 (asynchronous mode).
				CFG2		I	Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to DGND through a 10 kΩ resistor.
75	G9	69	F9	$\overline{\text{DACK1}}$	1	I	Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request ($\overline{\text{DREQ1}}$) has been acknowledged and data transfer can proceed. This pin must be held high at all times unless a DMA or JDATA access is occurring. This pin must be held high at all times if the DMA interface is not used, even if the DMA channels are disabled.
				$\overline{\text{FCS1}}$		I	FIFO Chip Select. Used in DCS-DMA mode. Chip select for the FIFO assigned to Channel 1 (asynchronous mode).
90 to 92, 78	J2 to J4, H1	111, 97 to 99	K3, J1 to J3	HDATA[31:28]	4	I/O	Host Expansion Bus.
				JDATA[7:4]		I/O	JDATA Bus (JDATA Mode).
79 to 81, 70	H2 to H4, G4	100, 85 to 87	J4, H1 to H3	HDATA[27:24]	4	I/O	Host Expansion Bus.
				JDATA[3:0]		I/O	JDATA Bus (JDATA Mode).
69, 68, 59, 58	G3, G2, F4, F3	88, 73 to 75	H4, G1 to G3	HDATA[23:20]	4	I/O	Host Expansion Bus.
57, 46 to 48	F2, E2, E3, E4	76, 61 to 63	G4, F1 to F3	HDATA[19:16]	4	I/O	Host Expansion Bus.
				VDATA[15:12]		I/O	Video Data. Used only for raw pixel video mode. Unused pins should be pulled down via a 10 kΩ resistor.
112	L2	134	M2	SCOMM7	8	I/O	Serial Communication. For internal use only. This pin should be tied low via a 10 kΩ resistor.
113	L3	135	M3	SCOMM6		I/O	Serial Communication. For internal use only. This pin should be tied low via a 10 kΩ resistor.
114	L4	136	M4	SCOMM5		I/O	Serial Communication. This pin must be used in multiple chip mode to align the outputs of two or more ADV212s. For details, see the Applications Information section. When not used, this pin should be tied low via a 10 kΩ resistor.
100	K1	121	L1	SCOMM4		O	LCODE Output in Encode Mode. When LCODE is enabled, the output on this pin indicates on a high transition that the last data-word for a field has been read from the FIFO. For an 8-bit interface, such as JDATA, LCODE is asserted for four consecutive bytes and is enabled by default.

121-Ball Package		144-Ball Package					
Pin No.	Location	Pin No.	Location	Mnemonic	Pins Used	Type	Description
101	K2	122	L2	SCOMM3		I	Serial Communication. For internal use only. This pin should be tied low via a 10 kΩ resistor.
115	L5	123	L3	SCOMM2		O	Serial Communication. For internal use only. This pin should be tied low via a 10 kΩ resistor.
103	K4	109	K1	SCOMM1		I	Serial Communication. For internal use only. This pin should be tied low via a 10 kΩ resistor.
102	K3	110	K2	SCOMM0		O	Serial Communication. This pin should be tied low via a10 kΩ resistor.
53	E9	60	E12	VCLK	1	I	Video Data Clock. This pin must be supplied if video data is input/output on the VDATA bus.
44, 43, 29, 31, 32, 18 to 20, 22, 21, 7, 10	D11, D10, C7, C9, C10, B7, B8, B9, B11, B10, A7, A10	46 to 48, 34 to 36, 22 to 24, 9 to 11	D10 to D12, C10 to C12, B10 to B12, A9 to A11	VDATA[11:0]	12	I/O	Video Data. Unused pins should be pulled down via a 10 kΩ resistor.
41	D8	58	E10	VSYNC	1	I/O	Vertical Sync for Video Mode.
				VFRM			Raw Pixel Mode Framing Signal. When this pin is asserted high, it indicates the first sample of a tile.
42	D9	59	E11	HSYNC	1	I/O	Horizontal Sync for Video Mode.
				VRDY		O	Raw Pixel Mode Ready Signal.
54	E10	57	E9	FIELD	1	I/O	Field Sync for Video Mode.
				VSTRB		I	Raw Pixel Mode Transfer Strobe.
94	J6	120	K12	TCK	1	I	JTAG Clock. If not used, this pin should be connected to ground via a pull-down resistor.
108	K9	119	K11	TRS	1	I	JTAG Reset. If the JTAG is used, this pin must be toggled low to high. If JTAG is not used, this pin must be held low.
98	J10	118	K10	TMS	1	I	JTAG Mode Select. If JTAG is used, connect a 10 kΩ pull-up resistor to this pin. If not used, this pin should be connected to ground via a pull-down resistor.
116	L6	141	M9	TDI	1	I	JTAG Serial Data Input. If JTAG is used, connect a 10 kΩ pull-up resistor to this pin. If JTAG is not used, this pin should be connected to ground via a pull-down resistor.
109	K10	130	L10	TDO	1	O	JTAG Serial Data Output. If this pin is not used, do not connect it.
3, 8, 40, 84, 120	A3, A8, D7, H7, L10	18, 19, 30, 31, 42, 43, 102, 103, 114, 115, 126, 127, 142	B6, B7, C6, C7, D6, D7, J6, J7, K6, K7, L6, L7, M10	VDD	5/13	V	Positive Supply for Core.

121-Ball Package		144-Ball Package					
Pin No.	Location	Pin No.	Location	Mnemonic	Pins Used	Type	Description
1, 4, 9,11, 23, 33, 39, 45, 49 to 51, 55, 56, 60 to 62, 66, 67, 71 to 73, 77, 83, 89, 99, 110, 111, 118, 121	A1, A4, A9, A11, C1, C11, D6, E1, E5 to E7, E11, F1, F5 to F7, F11, G1, G5 to G7, G11, H6, J1, J11, K11, L1, L8, L11	1, 5 to 8, 12, 17, 20, 29, 32, 41, 44, 52 to 56, 65 to 68, 77 to 81, 89 to 93, 101, 104, 105, 113, 116, 125, 128, 133, 137 to 140, 143, 144	A1, A5 to A8, A12, B5, B8, C5, C8, D5, D8, E4 to E8, F5 to F8, G5 to G9, H5 to H9, J5, J8, J9, K5, K8, L5, L8, M1, M5 to M8, M11, M12	DGND	29/45	GND	Ground.
17, 28, 30, 38, 52, 74, 82, 93, 104 to 106	B6, C6, C8, D5, E8, G8, H5, J5, K5 to K7	16, 21, 28, 33, 40, 45, 112, 117, 124, 129	B4, B9, C4, C9, D4, D9, K4, K9, L4, L9	IOVDD	11/10	V	Positive Supply for Input/Output.

[1] In fly-by mode DMA, the functions of the $\overline{RD}$ and $\overline{WE}$ signals (for DMA only) are reversed. This allows a host to move data between an external device and the ADV212 with the use of a single strobe.

[2] In encode mode with fly-by DMA, the host can use the $\overline{RDFB}$ signal ($\overline{WE}$ pin) to simultaneously read from the ADV212 and write to an external device such as memory.

[3] In decode mode with fly-by DMA, the host can use the $\overline{WEFB}$ signal ($\overline{RD}$ pin) to simultaneously read from the external device and write to the ADV212.