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300 MHz, 32 × 32 Buffered Analog Crosspoint Switch

ADV3200/ADV3201

FEATURES

- Large, 32 × 32, nonblocking switch array
- G = +1 (ADV3200) or G = +2 (ADV3201) operation
- Pin-compatible 32 × 16 versions available (ADV3202/ADV3203)
- Single 5 V supply, dual ±2.5 V supply, or dual ±3.3 V supply (G = +2)
- Serial programming of switch array
- 2:1 OSD insertion mux per output
- Input sync-tip clamp
- High impedance output disable allows connection of multiple devices with minimal output bus load
- Excellent video performance
  - 60 MHz, 0.1 dB gain flatness
  - 0.1% differential gain error (R_L = 150 Ω)
  - 0.1° differential phase error (R_L = 150 Ω)
- Excellent ac performance
  - Bandwidth: >300 MHz
  - Slew rate: >400 V/µs
- Low power: 1.25 W
- Low all hostile crosstalk of −48 dB @ 5 MHz
- Reset pin allows disabling of all outputs
  - Connected through a capacitor to ground, provides power-on reset capability
- 176-lead exposed pad LQFP (24 mm × 24 mm)

APPLICATIONS

- CCTV surveillance
- Routing of high speed signals including
  - Composite video (NTSC, PAL, S, SECAM)
  - RGB and component video routing
  - Compressed video (MPEG, Wavelet)
- Video conferencing

FUNCTIONAL BLOCK DIAGRAM

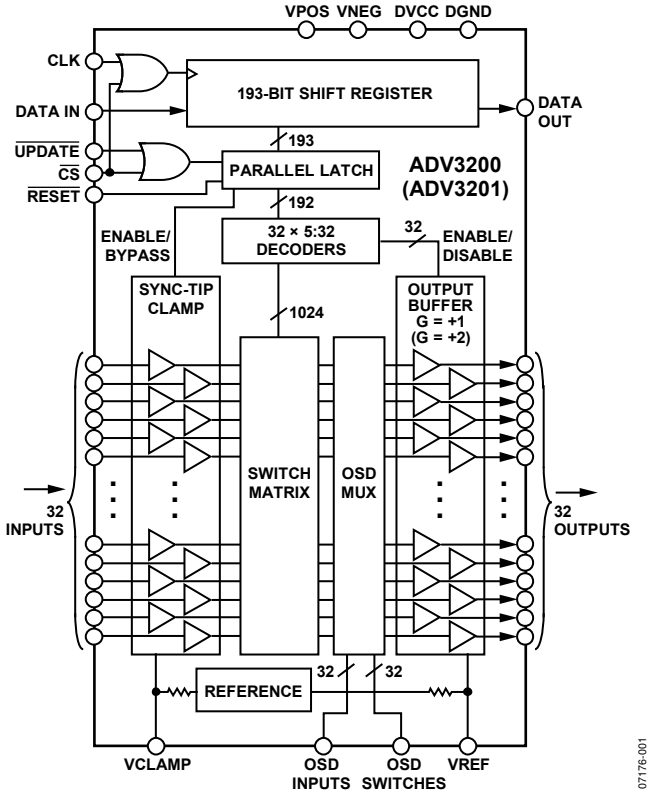

Figure 1.

GENERAL DESCRIPTION

The ADV3200/ADV3201 are 32 × 32 analog crosspoint switch matrices. They feature a selectable sync-tip clamp input for ac-coupled applications and an on-screen display (OSD) insertion mux. With −48 dB of crosstalk and −80 dB isolation at 5 MHz, the ADV3200/ADV3201 are useful in many high density routing applications. The 0.1 dB flatness out to 60 MHz makes the ADV3200/ADV3201 ideal for composite video switching.

The 32 independent output buffers of the ADV3200/ADV3201 can be placed into a high impedance state for paralleling cross-point outputs so that off channels present minimal loading to an output bus if building a larger array. The part is available in a gain of +1 (ADV3200) or +2 (ADV3201) for ease of use in back-terminated load applications. A single 5 V supply, dual ±2.5 V supplies, or dual ±3.3 V supplies (G = +2) can be used while consuming only 250 mA of idle current with all outputs enabled. The channel switching is performed via a double buffered, serial digital control, which can accommodate daisy chaining of several devices.

The ADV3200/ADV3201 are packaged in a 176-lead exposed pad LQFP (24 mm × 24 mm) and are available over the extended industrial temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

OSD DISABLED

V_S = ±2.5 V (ADV3200), V_S = ±3.3 V (ADV3201) at T_A = 25°C, G = +1 (ADV3200), G = +2 (ADV3201), R_L = 150 Ω, all configurations, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p		300		MHz
	2 V p-p		120		MHz
Gain Flatness	0.1 dB, 200 mV p-p		60		MHz
	0.1 dB, 2 V p-p		40		MHz
Settling Time	1%, 2 V step		6		ns
Slew Rate	2 V step, peak		400		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL				
ADV3200			0.06		%
ADV3201			0.1		%
Differential Phase Error	NTSC or PAL				
ADV3200			0.06		Degrees
ADV3201			0.03		Degrees
Crosstalk, All Hostile, RTI	f = 5 MHz, R_L = 150 Ω		−48		dB
	f = 5 MHz, R_L = 1 kΩ		−65		dB
	f = 100 MHz, R_L = 150 Ω		−23		dB
	f = 100 MHz, R_L = 1 kΩ		−30		dB
Off Isolation, Input-to-Output, RTI	f = 5 MHz, one channel		−80		dB
Input Voltage Noise	0.1 MHz to 50 MHz				
ADV3200			25		nV/√Hz
ADV3201			22		nV/√Hz
DC PERFORMANCE					
Gain Error					
ADV3200	No load (broadcast mode)		±0.5	±1.75	%
	Broadcast mode		±0.5	±2.2	%
ADV3201	No load (broadcast mode)		±0.5	±2.2	%
	Broadcast mode		±0.5	±2.7	%
Gain Matching	No load, channel-to-channel		±0.5	±2.8	%
	Channel-to-channel		±0.8	±3.4	%
OUTPUT CHARACTERISTICS					
Output Impedance	DC, enabled		0.15		Ω
ADV3200	DC, disabled	900	1000		kΩ
ADV3201	DC, disabled	3.2	4		kΩ
Output Capacitance	Disabled		3.7		pF
Output Voltage Range					
ADV3200		−1.1 to +1.1	−1.2 to +1.2		V
ADV3201		−1.5 to +1.5	−1.6 to +2.0		V
	No output load	−1.5 to +1.5	−2.0 to +2.0		V
INPUT CHARACTERISTICS					
Input Offset Voltage			±5	±30	mV
Input Voltage Range					
ADV3200		−1.1 to +1.1	−1.2 to +1.2		V
ADV3201		−0.75 to +0.75	−0.8 to +1.0		V
	No output load	−0.75 to +0.75	−1.0 to +1.0		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Capacitance			3		pF
Input Resistance		1	4		MΩ
Input Bias Current	Sync-tip clamp enabled, V_{IN} = VCLAMP + 0.1 V	0.1	3	12	µA
	Sync-tip clamp enabled, V_{IN} = VCLAMP − 0.1 V	−2.9	−1	−0.25	mA
	Sync-tip clamp disabled	−10	−3		µA
SWITCHING CHARACTERISTICS					
Enable On Time	50% update to 1% settling		50		ns
Switching Time, 2 V Step	50% update to 1% settling		40		ns
Switching Transient (Glitch)	IN00 to IN31, RTI		300		mV p-p
POWER SUPPLIES					
Supply Current					
ADV3200	VPOS or VNEG, outputs enabled, no load		250	300	mA
	VPOS or VNEG, outputs disabled		120	155	mA
ADV3201	VPOS or VNEG, outputs enabled, no load		260	310	mA
	VPOS or VNEG, outputs disabled		130	165	mA
DVCC			2.5	3.5	mA
Supply Voltage Range	VPOS − VNEG		5 ± 10% to 6.6 ± 10%		V
PSR	VNEG, VPOS, f = 1 MHz				
ADV3200			−50		dB
ADV3201			−45		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		−40 to +85		°C
θ_{JA}	Operating (still air)		16		°C/W

OSD ENABLED

V_S = ±2.5 V (ADV3200), V_S = ±3.3 V (ADV3201) at T_A = 25°C, G = +1 (ADV3200), G = +2 (ADV3201), R_L = 150 Ω, all configurations, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OSD DYNAMIC PERFORMANCE					
−3 dB Bandwidth					
ADV3200	200 mV p-p		170		MHz
	2 V p-p		135		MHz
ADV3201	200 mV p-p		150		MHz
	2 V p-p		130		MHz
Gain Flatness	0.1 dB, 200 mV p-p		35		MHz
	0.1 dB, 2 V p-p		35		MHz
Settling Time	1%, 2 V step		6		ns
Slew Rate	2 V step, peak		400		V/µs
OSD NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL				
ADV3200			0.12		%
ADV3201			0.35		%
Differential Phase Error	NTSC or PAL				
ADV3200			0.06		Degrees
ADV3201			0.04		Degrees
Input Voltage Noise	0.5 MHz to 50 MHz				
ADV3200			27		nV/√Hz
ADV3201			25		nV/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OSD DC PERFORMANCE					
Gain Error					
ADV3200	No load		±0.1	±2.3	%
			±0.1	±2.7	%
ADV3201	No load		±0.1	±2.2	%
			±0.1	±2.7	%
OSD INPUT CHARACTERISTICS					
Input Offset Voltage			±5	±30	mV
Input Bias Current		−10	−4		µA
OSD SWITCHING CHARACTERISTICS					
OSD Switch Delay, 2 V Step	50% OSD switch to 1% settling		20		ns
OSD Switching Transient (Glitch)					
ADV3200			15		mV p-p
ADV3201			40		mV p-p

TIMING CHARACTERISTICS (SERIAL MODE)

Table 3.

		Limit			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Serial Data Setup Time	t_1	40			ns
CLK Pulse Width	t_2	50			ns
Serial Data Hold Time	t_3	50			ns
CLK Pulse Separation	t_4	150			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5		50	160	ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	40			ns
CLK to DATA OUT Valid	t_7			130	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			50		ns
Data Load Time, CLK = 5 MHz, Serial Mode			38.6		µs
$\overline{\text{RESET}}$ Time			160		ns

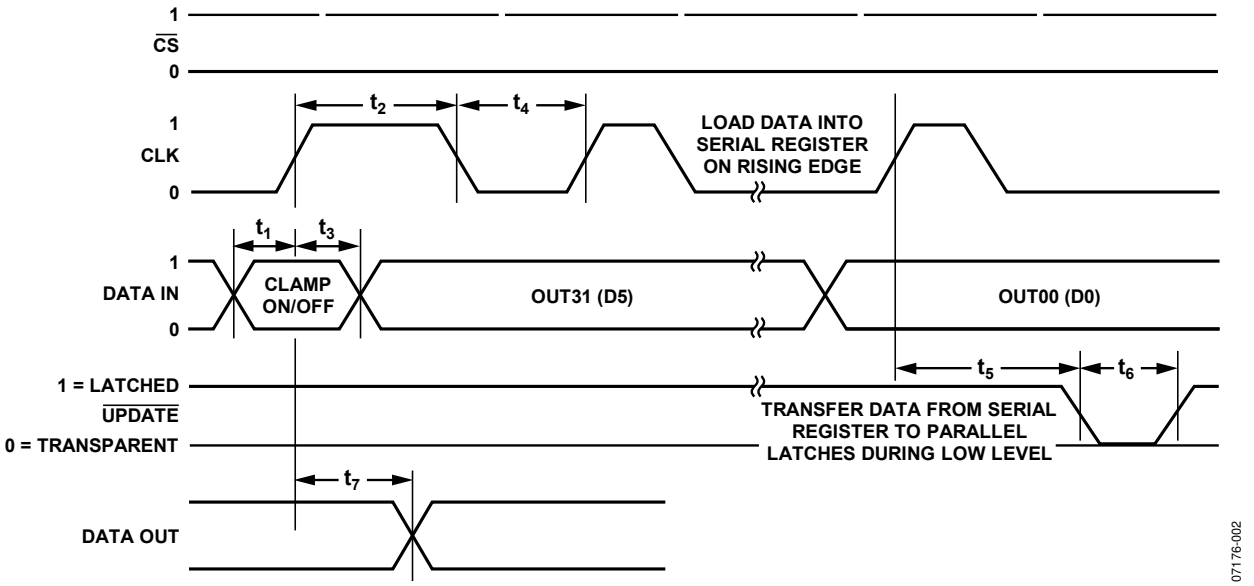


Figure 2. Timing Diagram, Serial Mode

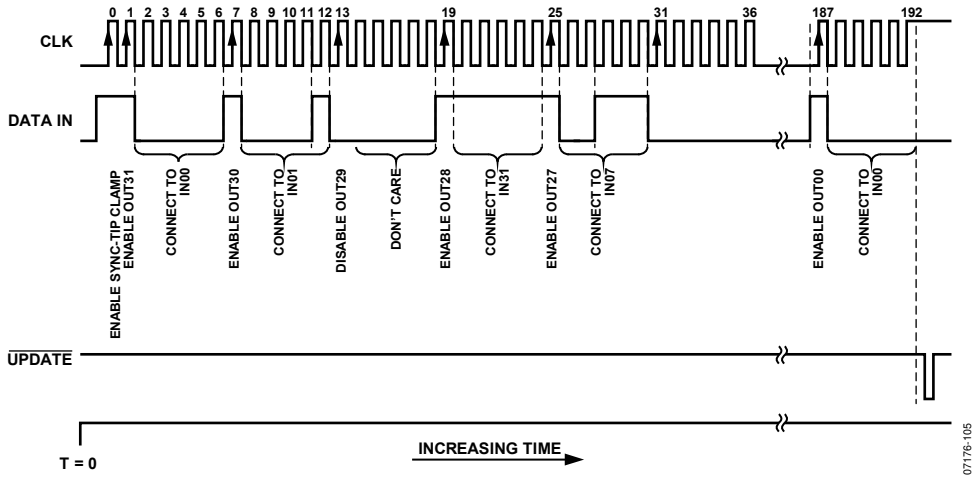


Figure 3. Programming Example

Table 4. Logic Levels, DVCC = 3.3 V

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{CS}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, OSDS	$\overline{\text{RESET}}$, $\overline{\text{CS}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, OSDS	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{CS}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, OSDS	$\overline{\text{RESET}}$, $\overline{\text{CS}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, OSDS	DATA OUT	DATA OUT
2.5 V min	0.8 V max	2.7 V min	0.5 V max	0.5 µA typ	−0.5 µA typ	3 mA typ	−3 mA typ

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Supply Voltage (VPOS – VNEG)	7.5 V
Digital Supply Voltage (DVCC – DGND)	6 V
Ground Potential Difference (VNEG – DGND)	+0.5 V to –4 V
Maximum Potential Difference	
DVCC – VNEG	9.4 V
Disabled Outputs	
ADV3200 ($\|V_{OSD} - V_{OUT}\|$)	<3 V
ADV3201 ($\|V_{OSD} - (V_{OUT} + VREF)/2\|$)	<3 V
$\|VCLAMP - V_{INxx}\|$	6 V
VREF Input Voltage	
ADV3200	VPOS – 3.5 V to VNEG + 3.5 V
ADV3201	VPOS – 4 V to VNEG + 4 V
Analog Input Voltage	VNEG to VPOS
Digital Input Voltage	DVCC
Output Voltage (Disabled Analog Output)	(VPOS – 1 V) to (VNEG + 1 V)
Output Short-Circuit Duration	Momentary
Output Short-Circuit Current	45 mA
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
176-Lead LQFP_EP	16	°C/W

POWER DISSIPATION

The ADV3200/ADV3201 are operated with ±2.5 V, 5 V, or ±3.3 V supplies and can drive loads down to 150 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken to derate the operating conditions based on ambient temperature.

The ADV3200/ADV3201 are packaged in a 176-lead exposed pad LQFP. The junction-to-ambient thermal impedance (θ_{JA}) of the ADV3200/ADV3201 is 16°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. Figure 4 shows the range of allowed internal die power dissipations that meet these conditions over the –40°C to +85°C ambient temperature range. When using Figure 4, do not include external load power in the maximum power calculation, but do include load current dropped on the die output transistors.

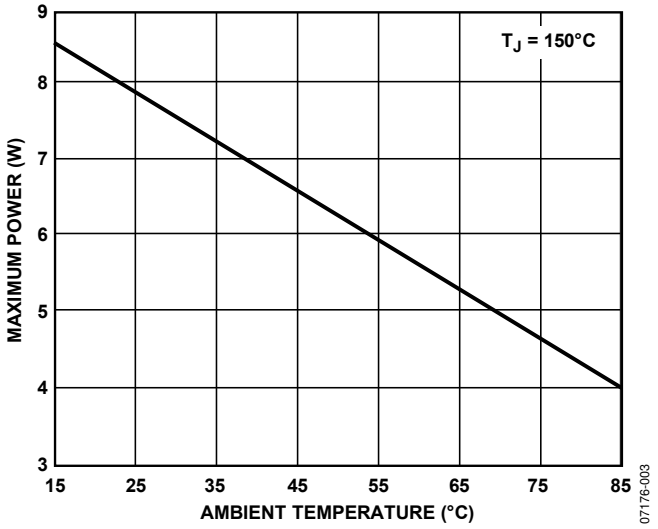
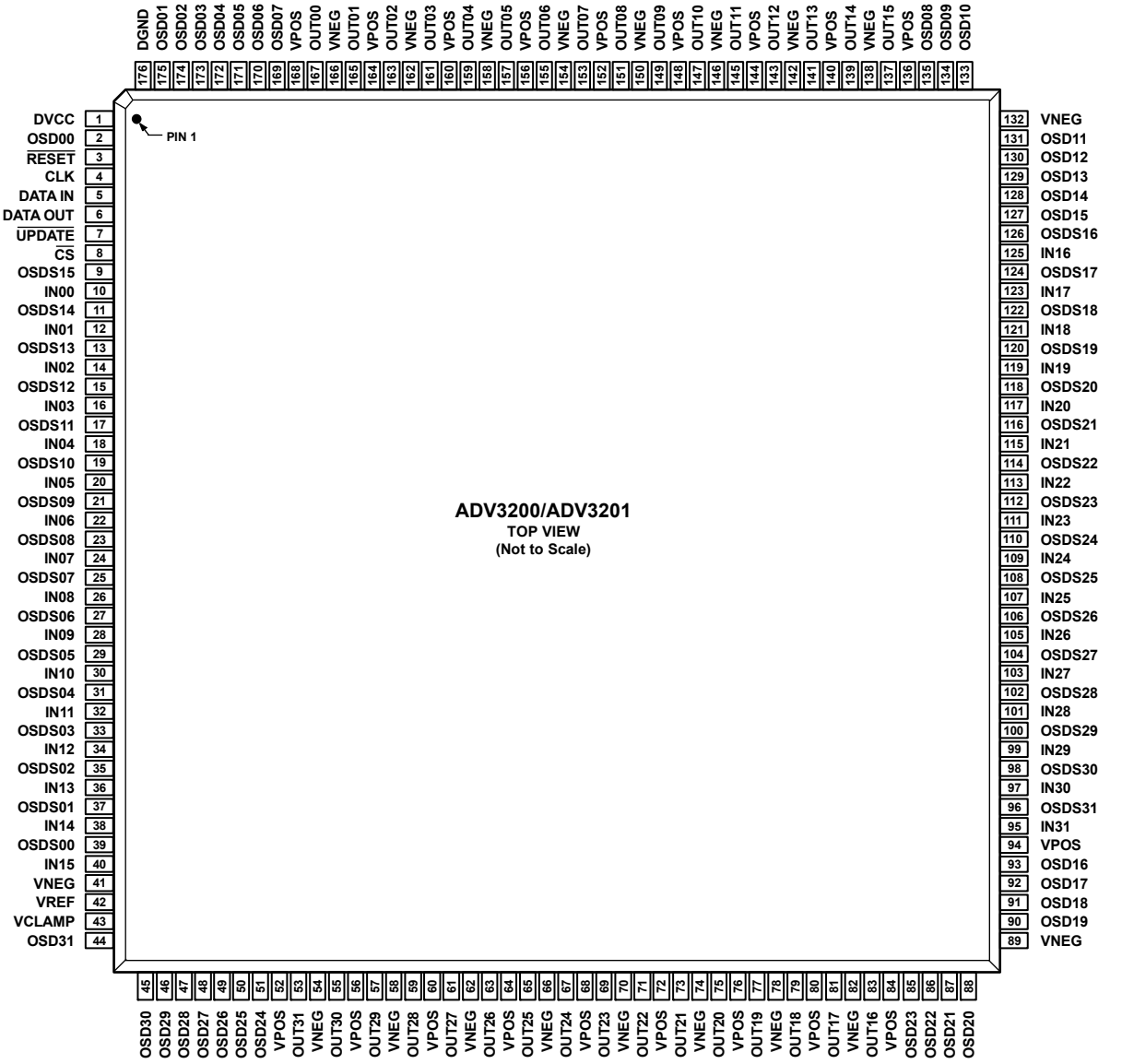


Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. OSDSxx: OSD SELECT FOR OUTxx
   OSDxx: OSD VIDEO INPUT FOR OUTxx
2. THE EXPOSED PAD SHOULD BE CONNECTED TO ANALOG GROUND.

Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin	Mnemonic	Description
1	DVCC	Digital Positive Power Supply.
2	OSD00	OSD Input Number 0.
3	$\overline{\text{RESET}}$	Control Pin: First and Second Rank Reset.
4	CLK	Control Pin: Serial Data Clock.
5	DATA IN	Control Pin: Serial Data In.
6	DATA OUT	Control Pin: Serial Data Out.
7	$\overline{\text{UPDATE}}$	Control Pin: Second Rank Write Strobe.
8	$\overline{\text{CS}}$	Control Pin: Chip Select.
9	OSDS15	Control Pin: OSD Select Number 15.
10	IN00	Input Number 0.
11	OSDS14	Control Pin: OSD Select Number 14.
12	IN01	Input Number 1.
13	OSDS13	Control Pin: OSD Select Number 13.
14	IN02	Input Number 2.
15	OSDS12	Control Pin: OSD Select Number 12.
16	IN03	Input Number 3.
17	OSDS11	Control Pin: OSD Select Number 11.
18	IN04	Input Number 4.
19	OSDS10	Control Pin: OSD Select Number 10.
20	IN05	Input Number 5.
21	OSDS09	Control Pin: OSD Select Number 9.
22	IN06	Input Number 6.
23	OSDS08	Control Pin: OSD Select Number 8.
24	IN07	Input Number 7.
25	OSDS07	Control Pin: OSD Select Number 7.
26	IN08	Input Number 8.
27	OSDS06	Control Pin: OSD Select Number 6.
28	IN09	Input Number 9.
29	OSDS05	Control Pin: OSD Select Number 5.
30	IN10	Input Number 10.
31	OSDS04	Control Pin: OSD Select Number 4.
32	IN11	Input Number 11.
33	OSDS03	Control Pin: OSD Select Number 3.
34	IN12	Input Number 12.
35	OSDS02	Control Pin: OSD Select Number 2.
36	IN13	Input Number 13.
37	OSDS01	Control Pin: OSD Select Number 1.
38	IN14	Input Number 14.
39	OSDS00	Control Pin: OSD Select Number 0.
40	IN15	Input Number 15.
41	VNEG	Analog Negative Power Supply.
42	VREF	Reference Voltage. See the Theory of Operation section for details.
43	VCLAMP	Sync-Tip Clamp Voltage. See the Theory of Operation section for details.
44	OSD31	OSD Input Number 31.
45	OSD30	OSD Input Number 30.
46	OSD29	OSD Input Number 29.
47	OSD28	OSD Input Number 28.
48	OSD27	OSD Input Number 27.
49	OSD26	OSD Input Number 26.
50	OSD25	OSD Input Number 25.
51	OSD24	OSD Input Number 24.
52	VPOS	Analog Positive Power Supply.
53	OUT31	Output Number 31.
54	VNEG	Analog Negative Power Supply.
55	OUT30	Output Number 30.
56	VPOS	Analog Positive Power Supply.
57	OUT29	Output Number 29.
58	VNEG	Analog Negative Power Supply.
59	OUT28	Output Number 28.
60	VPOS	Analog Positive Power Supply.
61	OUT27	Output Number 27.
62	VNEG	Analog Negative Power Supply.
63	OUT26	Output Number 26.
64	VPOS	Analog Positive Power Supply.
65	OUT25	Output Number 25.
66	VNEG	Analog Negative Power Supply.
67	OUT24	Output Number 24.
68	VPOS	Analog Positive Power Supply.
69	OUT23	Output Number 23.
70	VNEG	Analog Negative Power Supply.
71	OUT22	Output Number 22.
72	VPOS	Analog Positive Power Supply.
73	OUT21	Output Number 21.
74	VNEG	Analog Negative Power Supply.
75	OUT20	Output Number 20.
76	VPOS	Analog Positive Power Supply.
77	OUT19	Output Number 19.
78	VNEG	Analog Negative Power Supply.
79	OUT18	Output Number 18.
80	VPOS	Analog Positive Power Supply.
81	OUT17	Output Number 17.
82	VNEG	Analog Negative Power Supply.
83	OUT16	Output Number 16.
84	VPOS	Analog Positive Power Supply.
85	OSD23	OSD Input Number 23.
86	OSD22	OSD Input Number 22.
87	OSD21	OSD Input Number 21.
88	OSD20	OSD Input Number 20.
89	VNEG	Analog Negative Power Supply.
90	OSD19	OSD Input Number 19.
91	OSD18	OSD Input Number 18.
92	OSD17	OSD Input Number 17.
93	OSD16	OSD Input Number 16.
94	VPOS	Analog Positive Power Supply.
95	IN31	Input Number 31.
96	OSDS31	Control Pin: OSD Select Number 31.
97	IN30	Input Number 30.
98	OSDS30	Control Pin: OSD Select Number 30.
99	IN29	Input Number 29.
100	OSDS29	Control Pin: OSD Select Number 29.

Pin	Mnemonic	Description
101	IN28	Input Number 28.
102	OSDS28	Control Pin: OSD Select Number 28.
103	IN27	Input Number 27.
104	OSDS27	Control Pin: OSD Select Number 27.
105	IN26	Input Number 26.
106	OSDS26	Control Pin: OSD Select Number 26.
107	IN25	Input Number 25.
108	OSDS25	Control Pin: OSD Select Number 25.
109	IN24	Input Number 24.
110	OSDS24	Control Pin: OSD Select Number 24.
111	IN23	Input Number 23.
112	OSDS23	Control Pin: OSD Select Number 23.
113	IN22	Input Number 22.
114	OSDS22	Control Pin: OSD Select Number 22.
115	IN21	Input Number 21.
116	OSDS21	Control Pin: OSD Select Number 21.
117	IN20	Input Number 20.
118	OSDS20	Control Pin: OSD Select Number 20.
119	IN19	Input Number 19.
120	OSDS19	Control Pin: OSD Select Number 19.
121	IN18	Input Number 18.
122	OSDS18	Control Pin: OSD Select Number 18.
123	IN17	Input Number 17.
124	OSDS17	Control Pin: OSD Select Number 17.
125	IN16	Input Number 16.
126	OSDS16	Control Pin: OSD Select Number 16.
127	OSD15	OSD Input Number 15.
128	OSD14	OSD Input Number 14.
129	OSD13	OSD Input Number 13.
130	OSD12	OSD Input Number 12.
131	OSD11	OSD Input Number 11.
132	VNEG	Analog Negative Power Supply.
133	OSD10	OSD Input Number 10.
134	OSD09	OSD Input Number 9.
135	OSD08	OSD Input Number 8.
136	VPOS	Analog Positive Power Supply.
137	OUT15	Output Number 15.
138	VNEG	Analog Negative Power Supply.
139	OUT14	Output Number 14.
140	VPOS	Analog Positive Power Supply.
141	OUT13	Output Number 13.
142	VNEG	Analog Negative Power Supply.
143	OUT12	Output Number 12.
144	VPOS	Analog Positive Power Supply.
145	OUT11	Output Number 11.
146	VNEG	Analog Negative Power Supply.
147	OUT10	Output Number 10.
148	VPOS	Analog Positive Power Supply.
149	OUT09	Output Number 9.
150	VNEG	Analog Negative Power Supply.
151	OUT08	Output Number 8.
152	VPOS	Analog Positive Power Supply.
153	OUT07	Output Number 7.
154	VNEG	Analog Negative Power Supply.
155	OUT06	Output Number 6.
156	VPOS	Analog Positive Power Supply.
157	OUT05	Output Number 5.
158	VNEG	Analog Negative Power Supply.
159	OUT04	Output Number 4.
160	VPOS	Analog Positive Power Supply.
161	OUT03	Output Number 3.
162	VNEG	Analog Negative Power Supply.
163	OUT02	Output Number 2.
164	VPOS	Analog Positive Power Supply.
165	OUT01	Output Number 1.
166	VNEG	Analog Negative Power Supply.
167	OUT00	Output Number 0.
168	VPOS	Analog Positive Power Supply.
169	OSD07	OSD Input Number 7.
170	OSD06	OSD Input Number 6.
171	OSD05	OSD Input Number 5.
172	OSD04	OSD Input Number 4.
173	OSD03	OSD Input Number 3.
174	OSD02	OSD Input Number 2.
175	OSD01	OSD Input Number 1.
176	DGND	Digital Negative Power Supply.
	Exposed Pad	Connect to analog ground.

TRUTH TABLE AND LOGIC DIAGRAM

Table 8. Operation Truth Table

$\overline{CS}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	Operation/Comment
X[1]	X	X	X	X	0	Asynchronous reset. All outputs are disabled. The 193-bit shift register is reset to all 0s.
0	1	↑	$Data_i$[2]	$Data_{i-193}$	1	The data on the serial DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 193 clock cycles later.
0	0	X	X	X	1	Switch matrix update. Data in the 193-bit shift register is transferred into the parallel latches that control the switch array and sync-tip clamps.
1	X	X	X	X	1	Chip is not selected. No change in logic.

[1] X = don't care.
[2] $Data_i$: serial data.

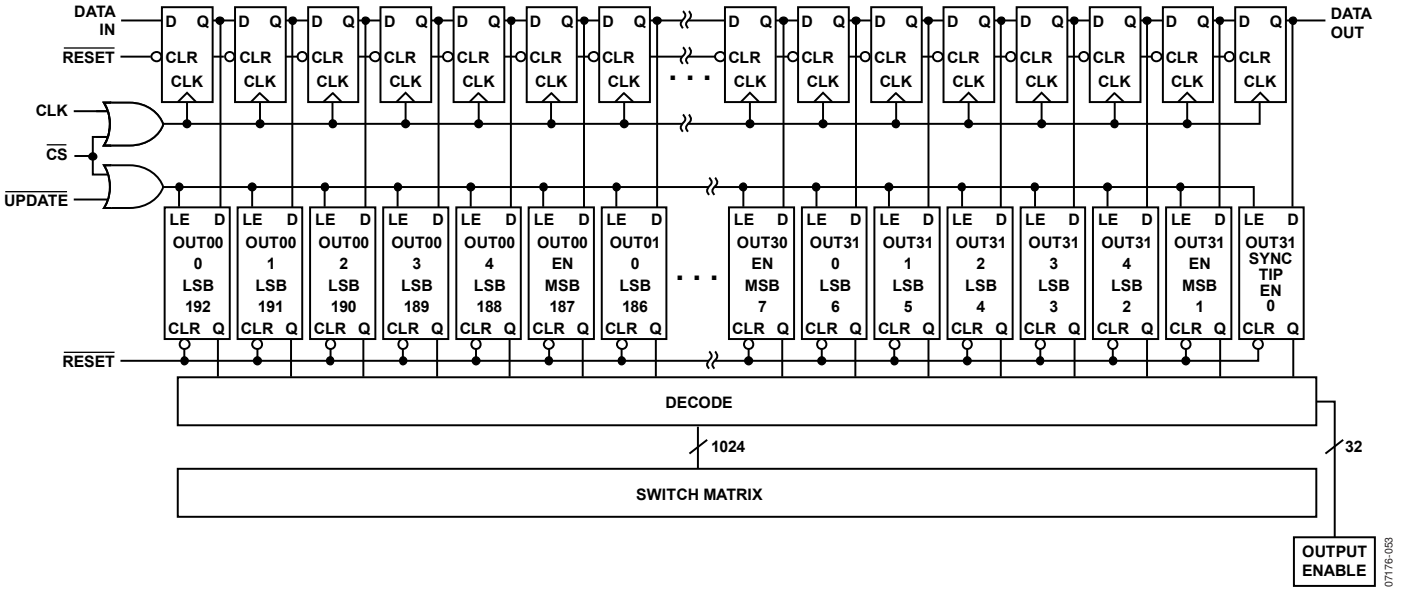


Figure 6. Logic Diagram

I/O SCHEMATICS

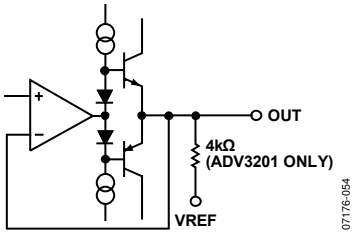


Figure 7. Enabled Output
(See Also Figure 16)

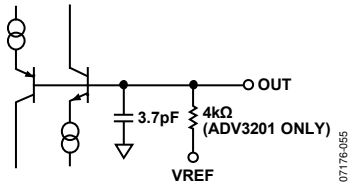


Figure 8. Disabled Output
(See Also Figure 16)

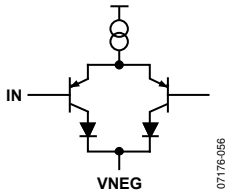


Figure 9. Receiver
(See Also Figure 16)

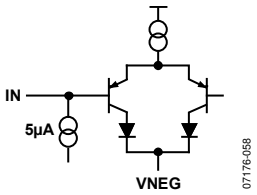


Figure 10. Receiver with Sync-Tip Clamp Enabled
(See Also Figure 16)

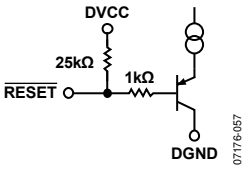


Figure 11. Reset Input
(See Also Figure 16)

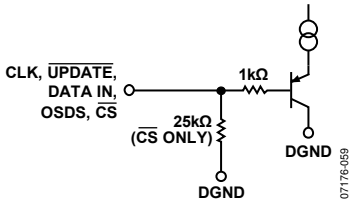


Figure 12. Logic Input
(See Also Figure 16)

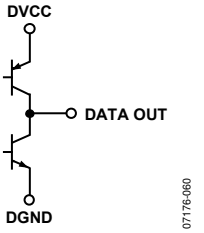


Figure 13. Logic Output
(See Also Figure 16)

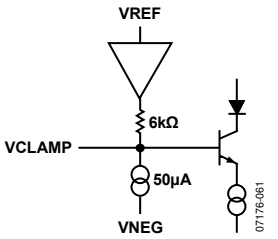


Figure 14. VCLAMP Input
(See Also Figure 16)

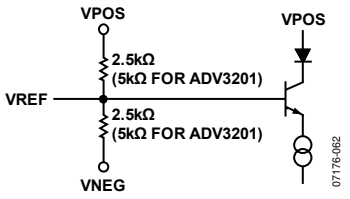


Figure 15. VREF Input
(See Also Figure 16)

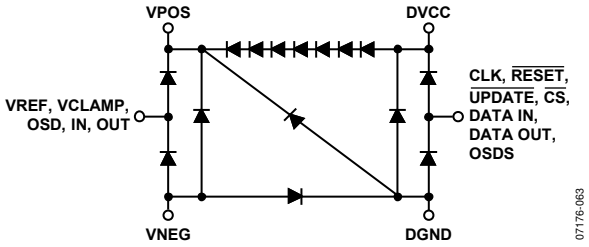


Figure 16. ESD Protection Map

TYPICAL PERFORMANCE CHARACTERISTICS

ADV3200

V_S = ±2.5 V at T_A = 25°C, R_L = 150 Ω.

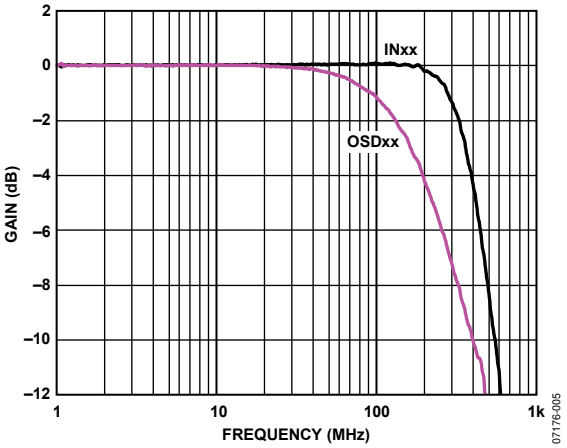


Figure 17. ADV3200 Small Signal Frequency Response, 200 mV p-p

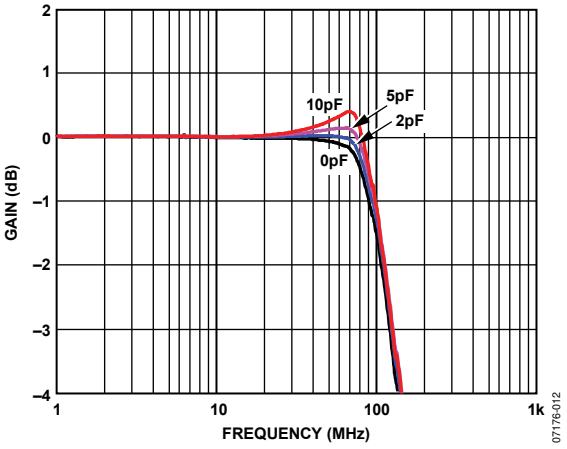


Figure 20. ADV3200 Large Signal Frequency Response with Capacitive Loads, 2 V p-p

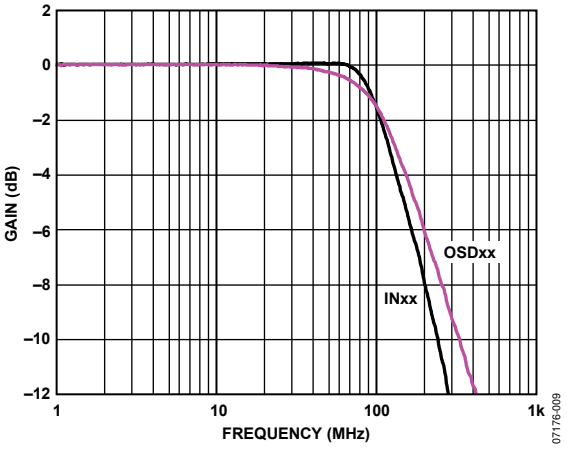


Figure 18. ADV3200 Large Signal Frequency Response, 2 V p-p

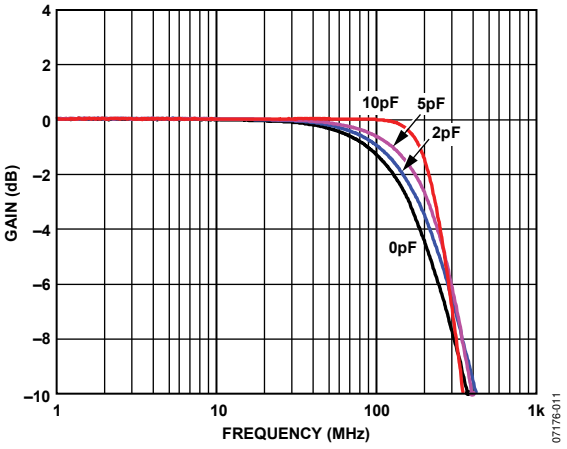


Figure 21. ADV3200 OSD Small Signal Frequency Response with Capacitive Loads, 200 mV p-p

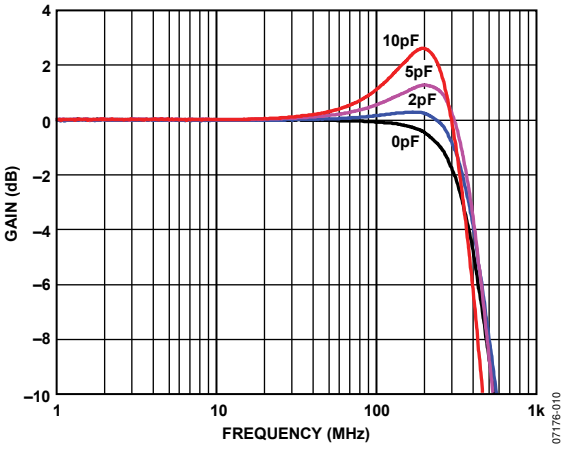


Figure 19. ADV3200 Small Signal Frequency Response with Capacitive Loads, 200 mV p-p

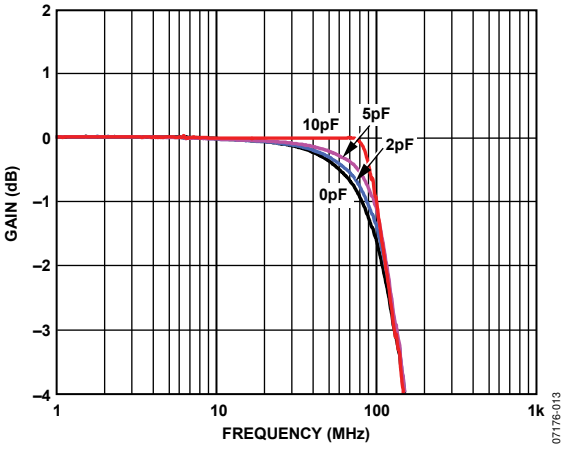


Figure 22. ADV3200 OSD Large Signal Frequency Response with Capacitive Loads, 2 V p-p

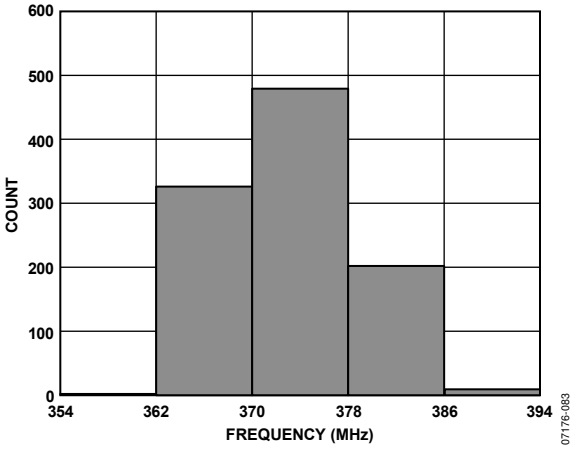


Figure 23. ADV3200 −3 dB Bandwidth Histogram, One Device, All 1024 Channels

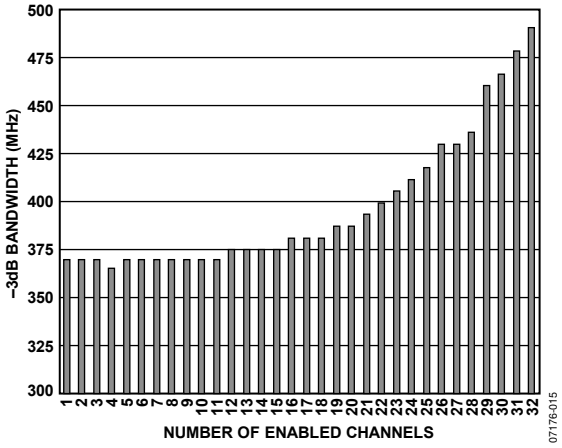


Figure 24. ADV3200 Small Signal Bandwidth vs. Enabled Channels

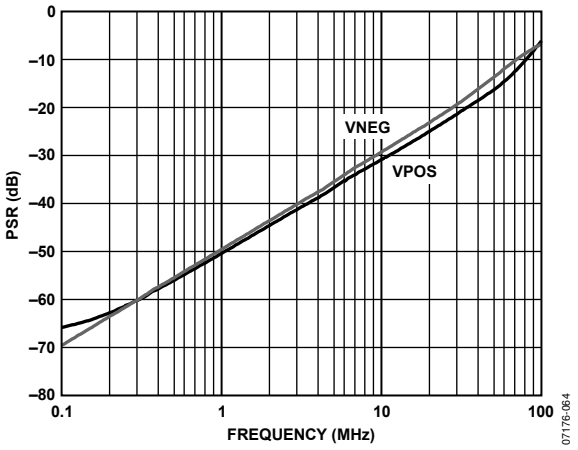


Figure 25. ADV3200 Power Supply Rejection

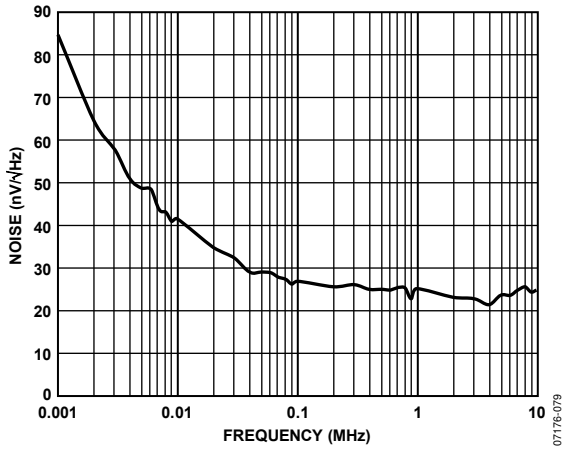


Figure 26. ADV3200 Output Noise

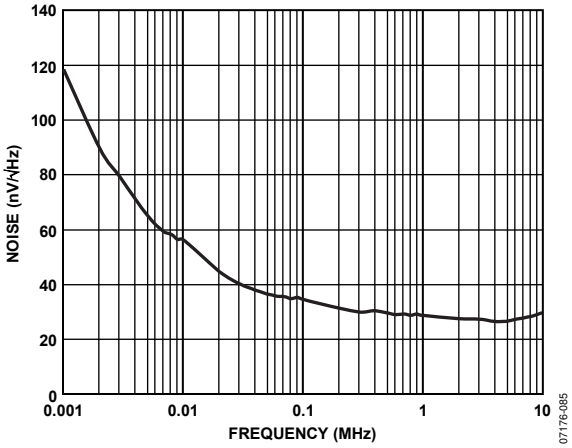


Figure 27. ADV3200 OSD Output Noise

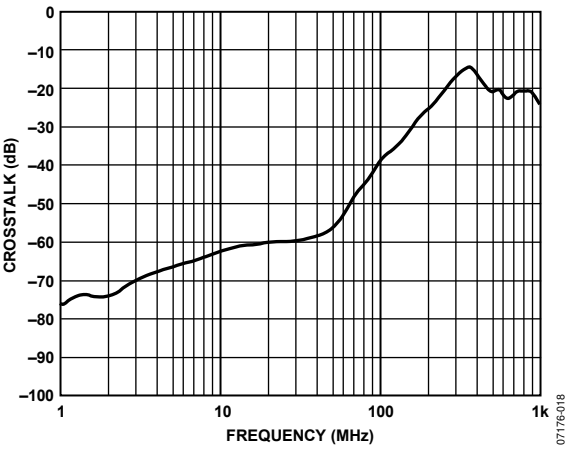


Figure 28. ADV3200 Crosstalk, One Adjacent Channel, RTO

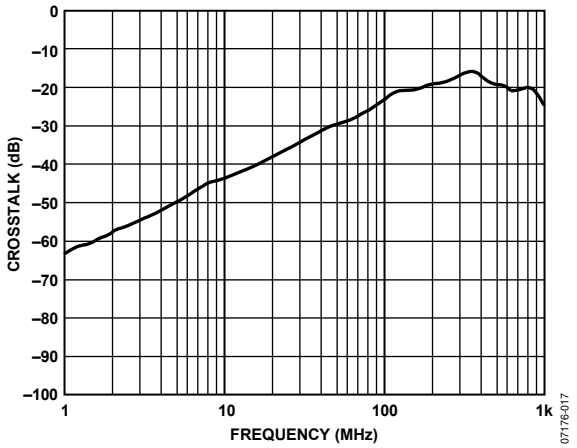


Figure 29. ADV3200 Crosstalk, All Hostile, RTO

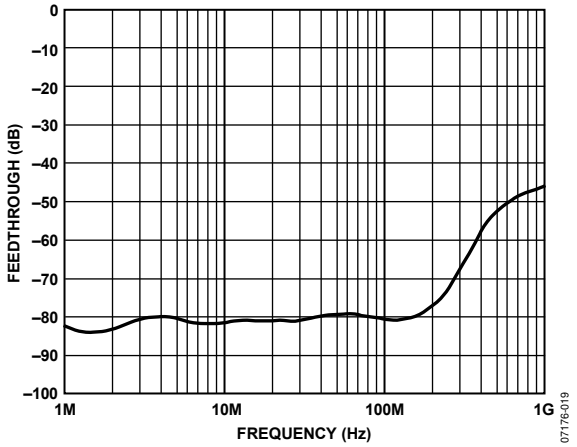


Figure 30. ADV3200 Off Isolation, RTO

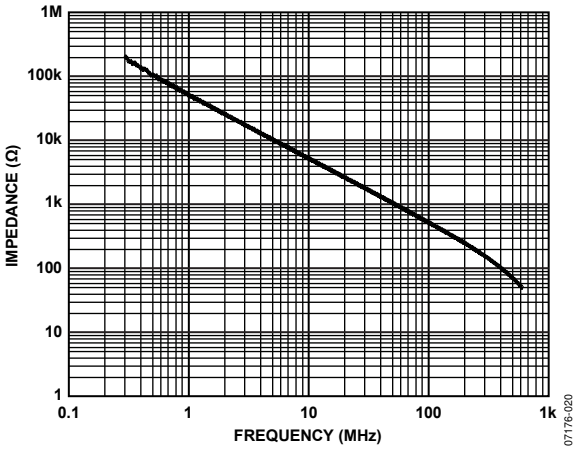


Figure 31. ADV3200 Input Impedance

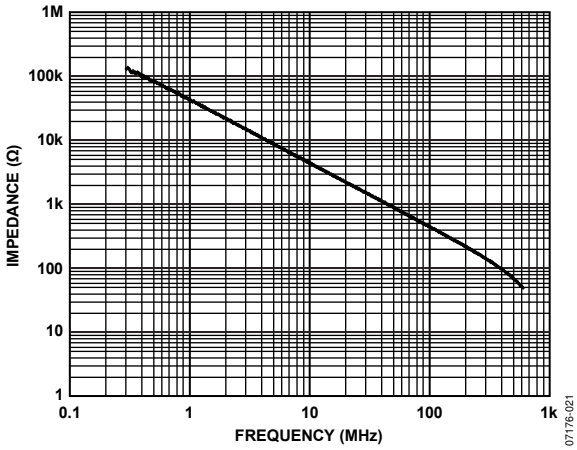


Figure 32. ADV3200 Output Impedance, Disabled

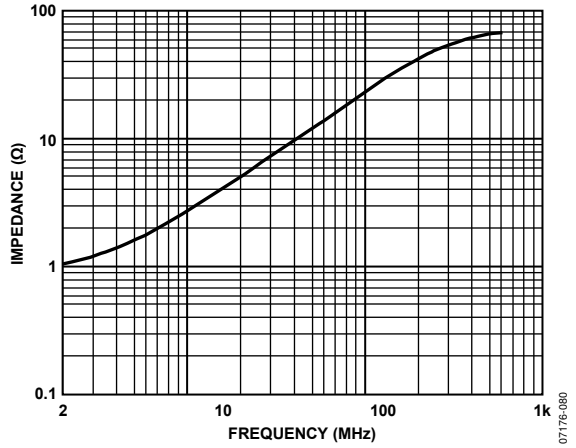


Figure 33. ADV3200 Output Impedance, Enabled

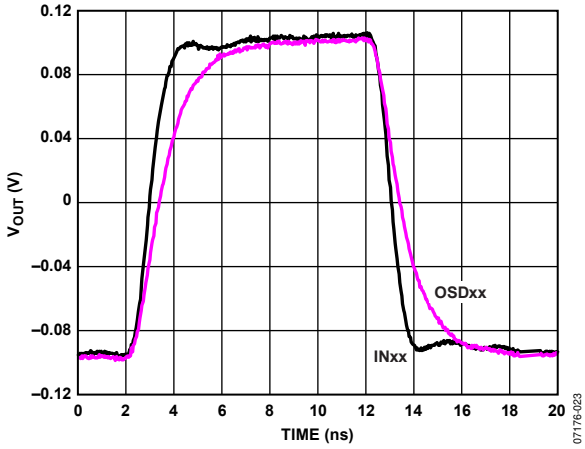


Figure 34. ADV3200 Small Signal Pulse Response, 200 mV p-p

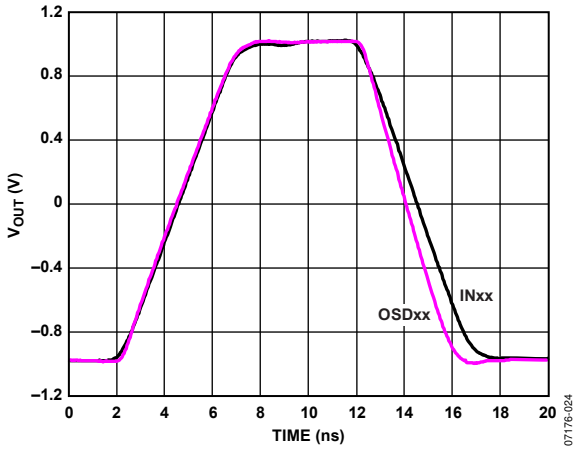


Figure 35. ADV3200 Large Signal Pulse Response, 2 V p-p

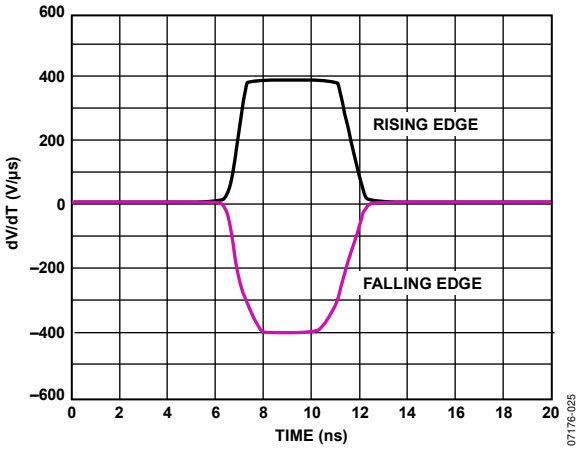


Figure 38. ADV3200 Slew Rate

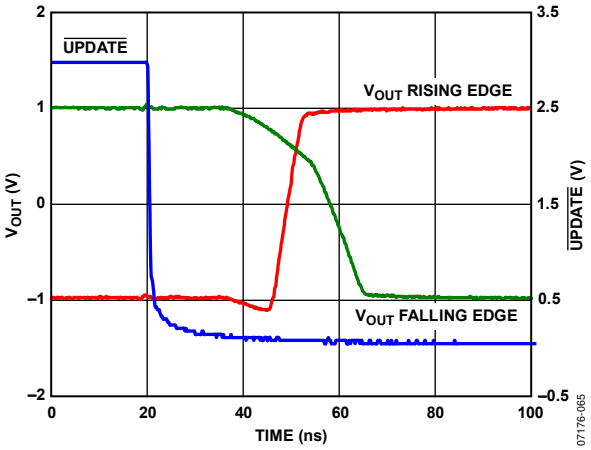


Figure 36. ADV3200 Switching Time

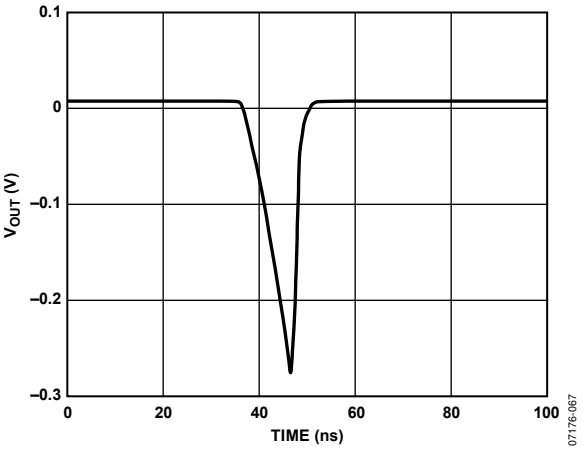


Figure 39. ADV3200 Switching Glitch

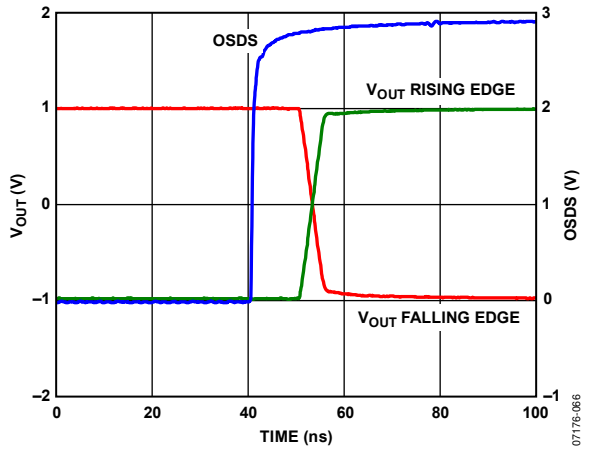


Figure 37. ADV3200 OSD Switching Time

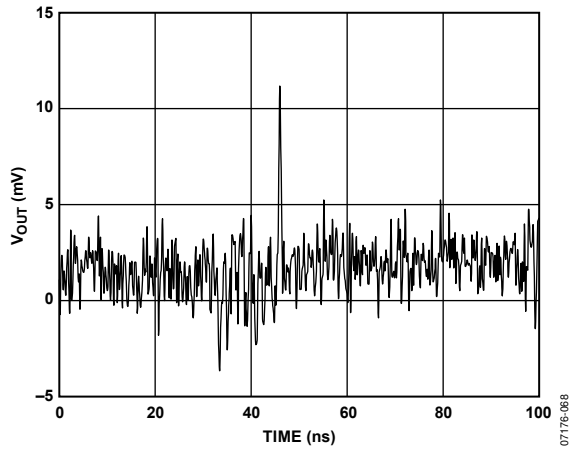


Figure 40. ADV3200 OSD Switching Glitch

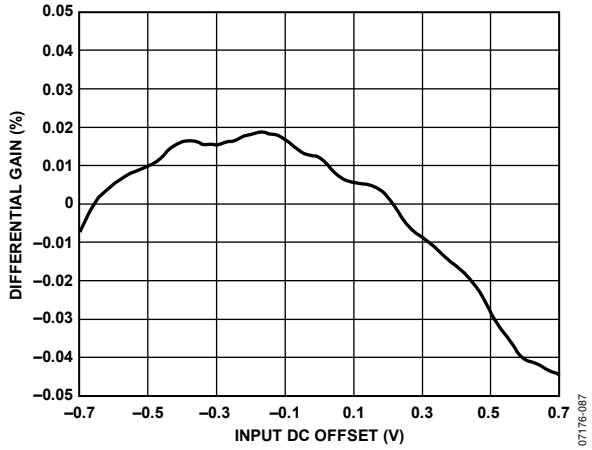


Figure 41. ADV3200 Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

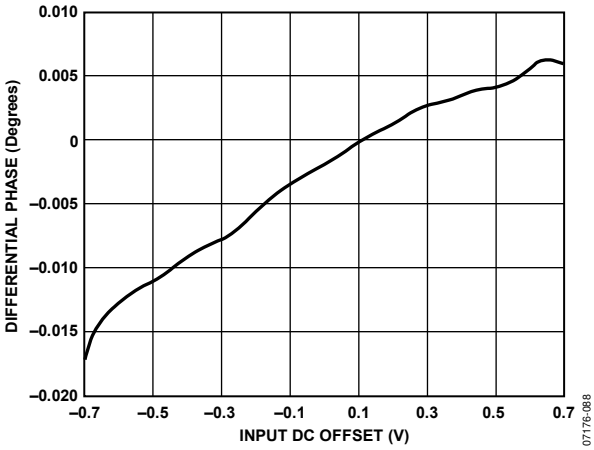


Figure 42. ADV3200 Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

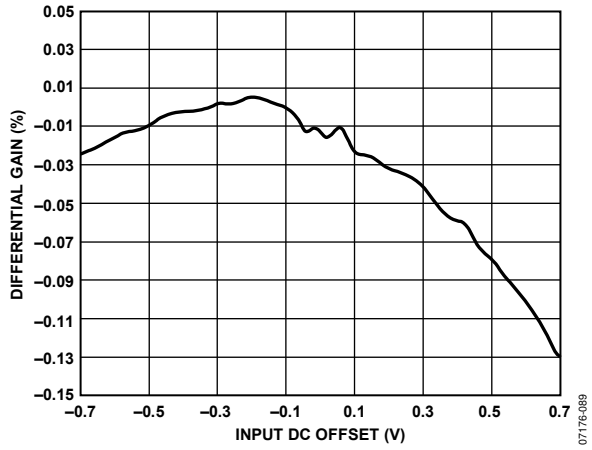


Figure 43. ADV3200 OSD Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

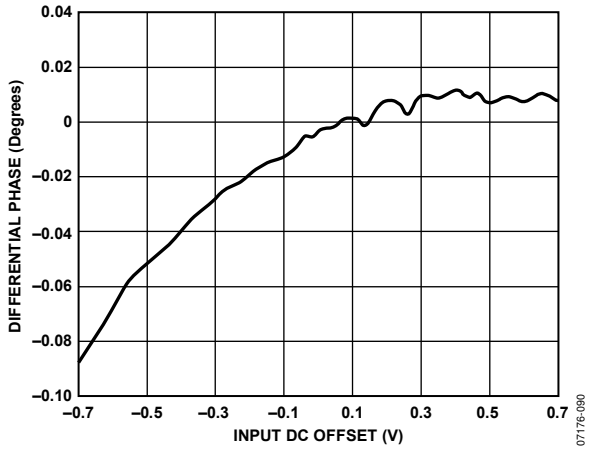


Figure 44. ADV3200 OSD Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

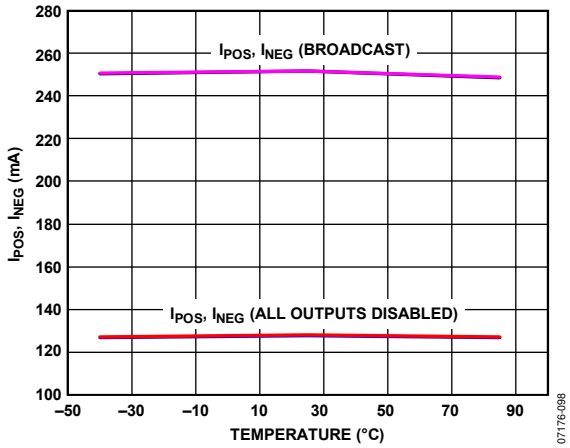


Figure 45. ADV3200 Supply Current vs. Temperature

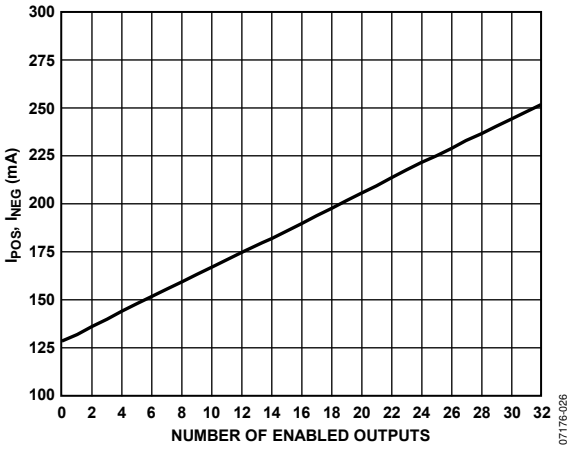


Figure 46. ADV3200 Supply Current vs. Enabled Outputs

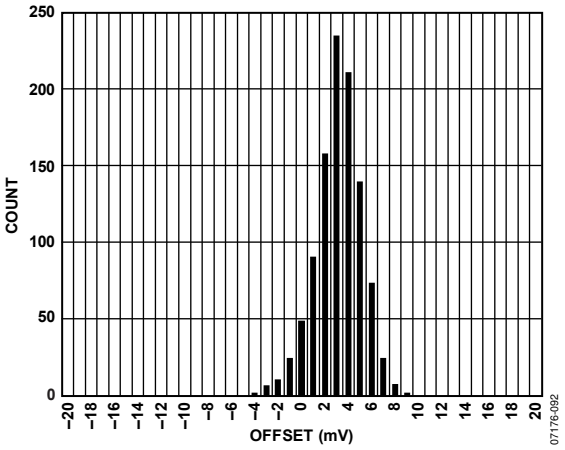


Figure 47. ADV3200 Input Offset Distribution, One Device, All 1024 Channels

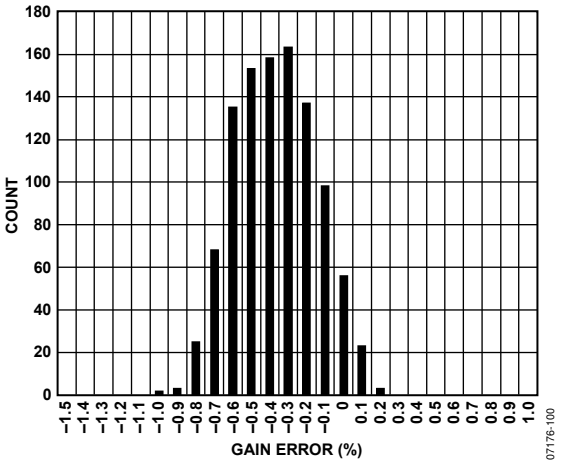


Figure 50. ADV3200 Gain Error Distribution, One Device, All 1024 Channels

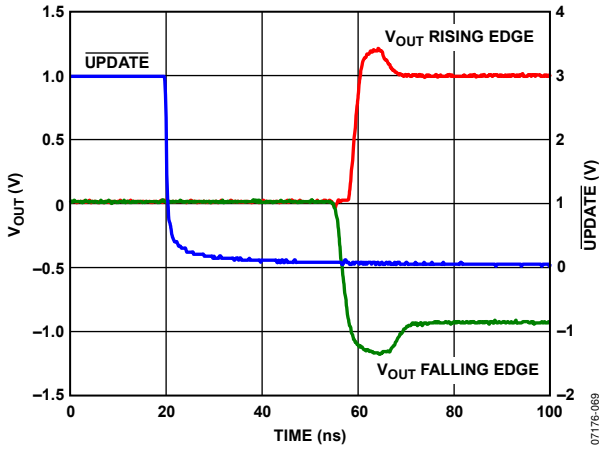


Figure 48. ADV3200 Enable Time

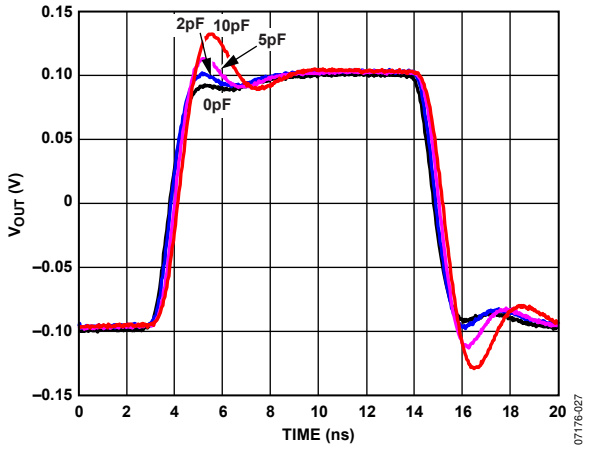


Figure 51. ADV3200 Small Signal Pulse with Capacitive Loads, 200 mV p-p

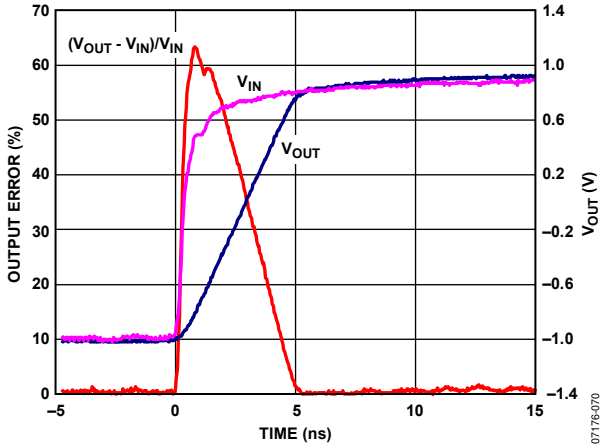


Figure 49. ADV3200 Settling Time

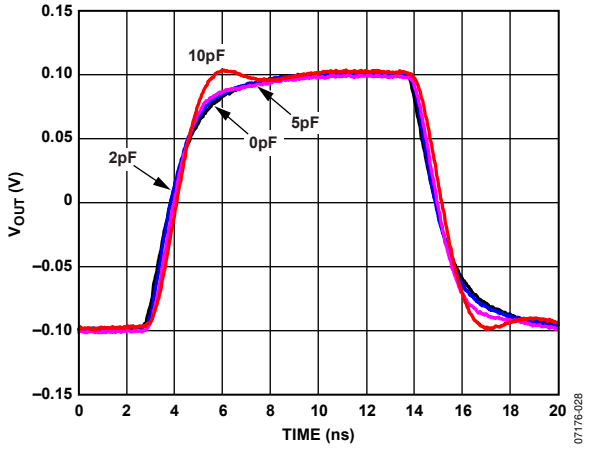


Figure 52. ADV3200 OSD Small Signal Pulse with Capacitive Loads, 200 mV p-p

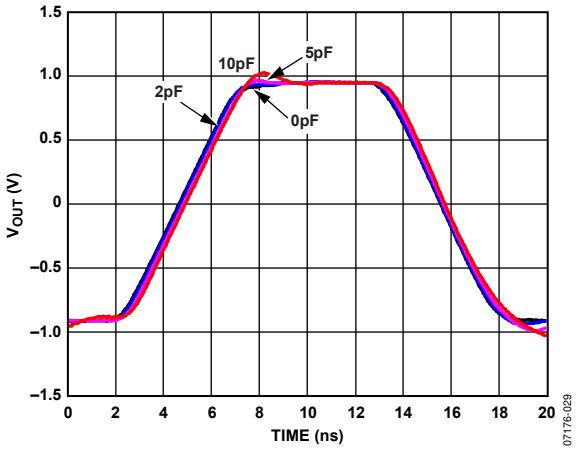


Figure 53. ADV3200 Large Signal Pulse with Capacitive Loads, 2 V p-p

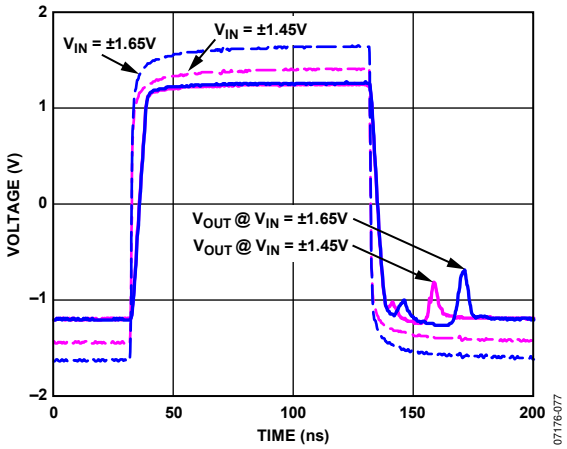


Figure 55. ADV3200 Overdrive Recovery

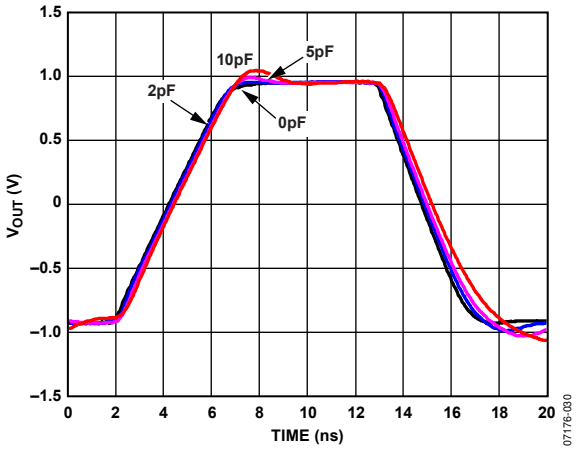


Figure 54. ADV3200 OSD Large Signal Pulse with Capacitive Loads, 2 V p-p

ADV3201

V_S = ±3.3 V at T_A = 25°C, R_L = 150 Ω.

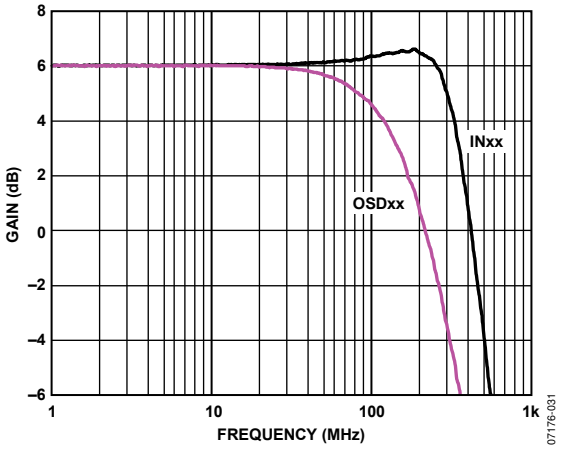


Figure 56. ADV3201 Small Signal Frequency Response, 200 mV p-p

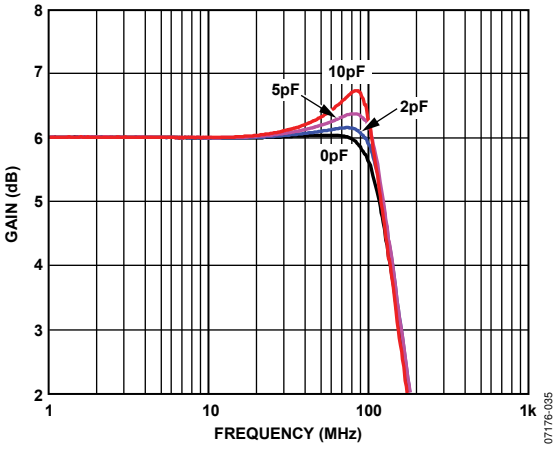


Figure 59. ADV3201 Large Signal Frequency Response with Capacitive Loads, 2 V p-p

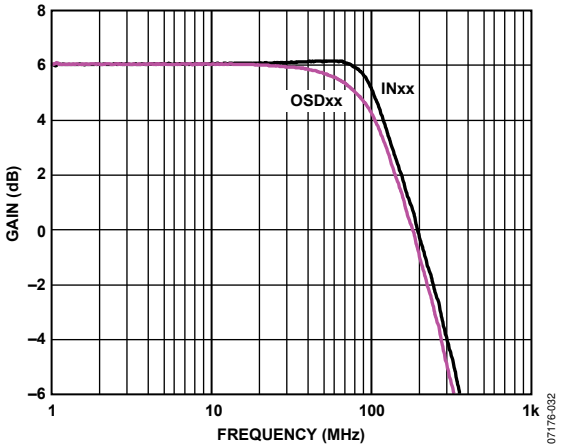


Figure 57. ADV3201 Large Signal Frequency Response, 2 V p-p

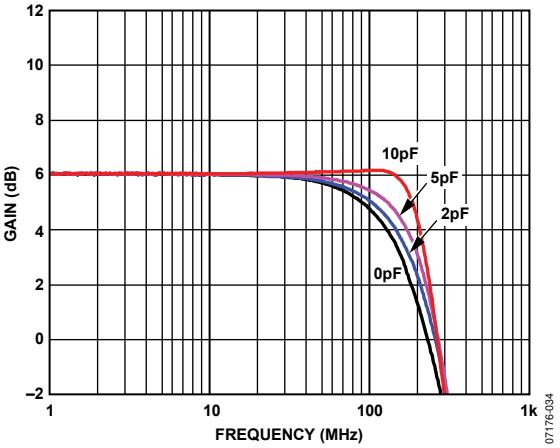


Figure 60. ADV3201 OSD Small Signal Frequency Response with Capacitive Loads, 200 mV p-p

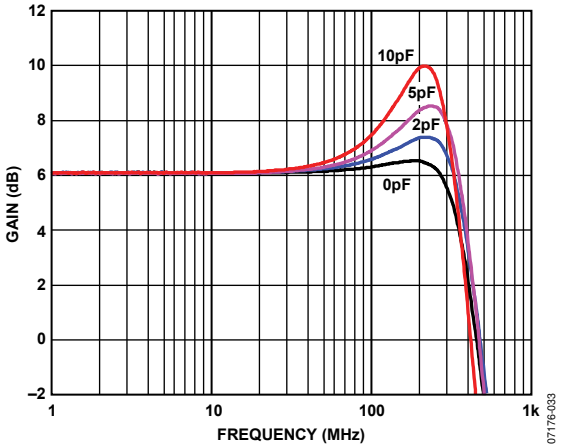


Figure 58. ADV3201 Small Signal Frequency Response with Capacitive Loads, 200 mV p-p

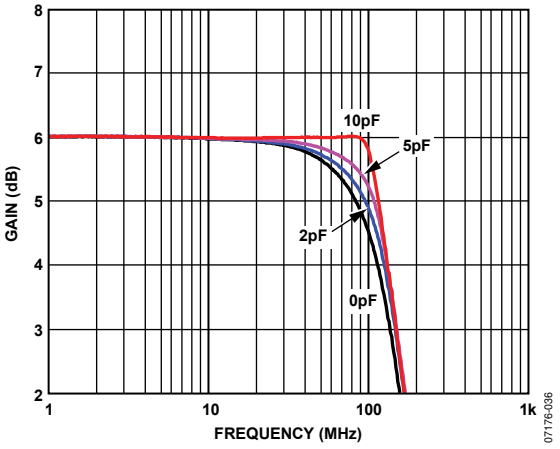


Figure 61. ADV3201 OSD Large Signal Frequency Response with Capacitive Loads, 2 V p-p

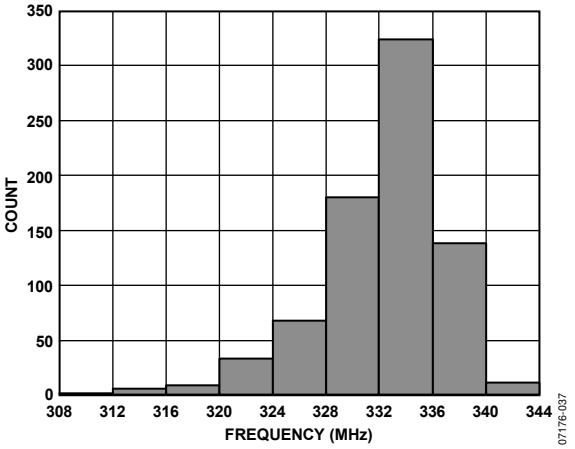


Figure 62. ADV3201 −3 dB Bandwidth Histogram, One Device, All 1024 Channels

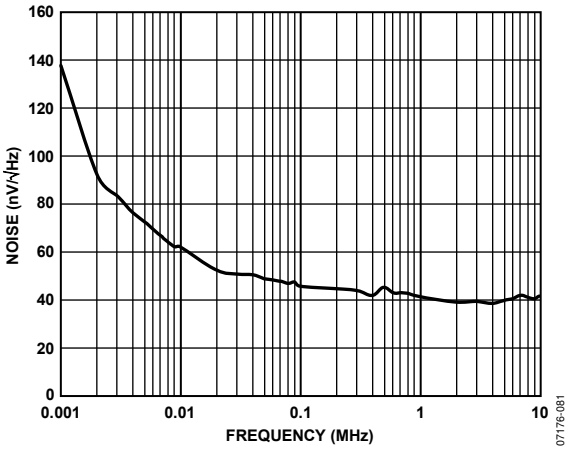


Figure 65. ADV3201 Output Noise

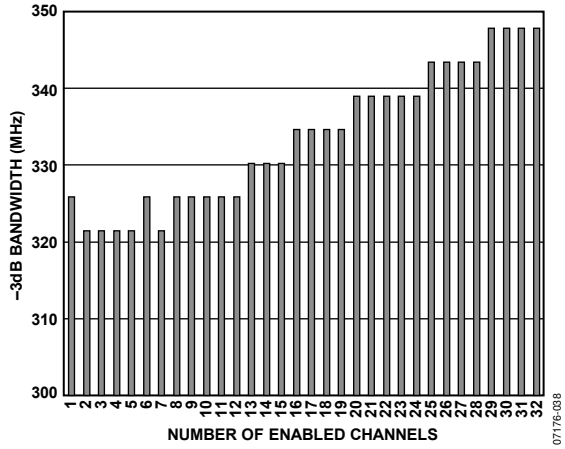


Figure 63. ADV3201 Small Signal Bandwidth vs. Enabled Channels

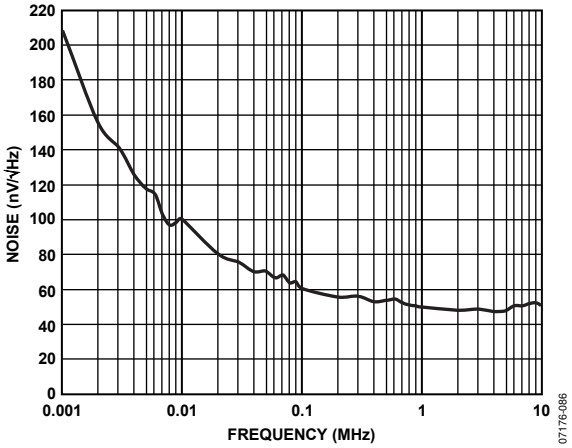


Figure 66. ADV3201 OSD Output Noise

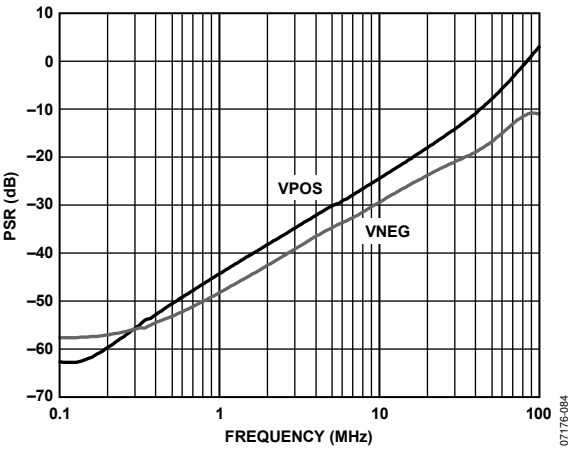


Figure 64. ADV3201 Power Supply Rejection

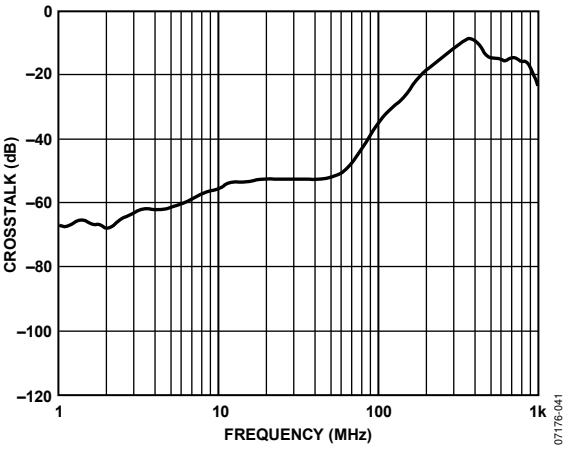


Figure 67. ADV3201 Crosstalk, One Adjacent Channel, RTO

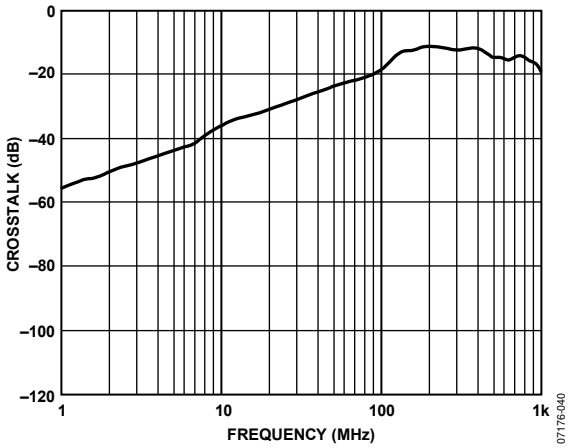


Figure 68. ADV3201 Crosstalk, All Hostile, RTO

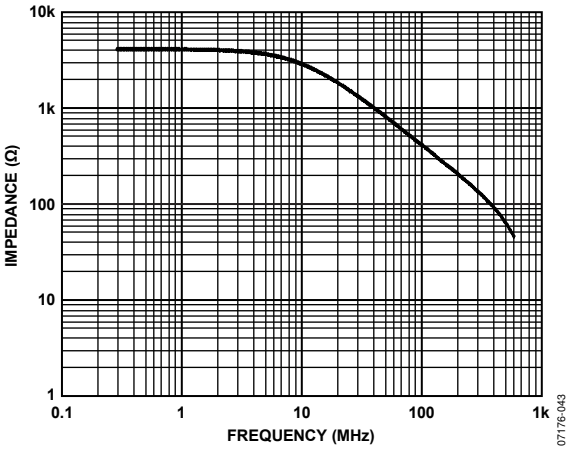


Figure 71. ADV3201 Output Impedance, Disabled

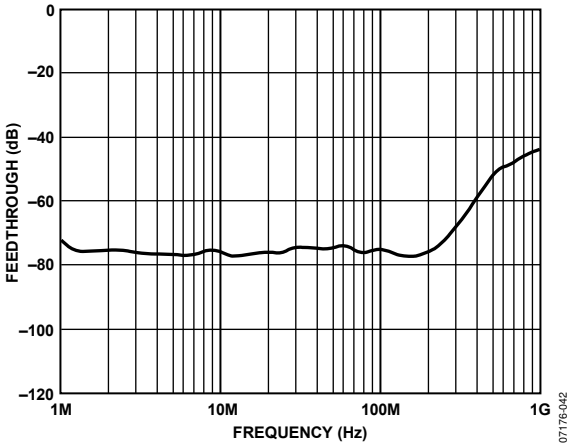


Figure 69. ADV3201 Off Isolation, RTO

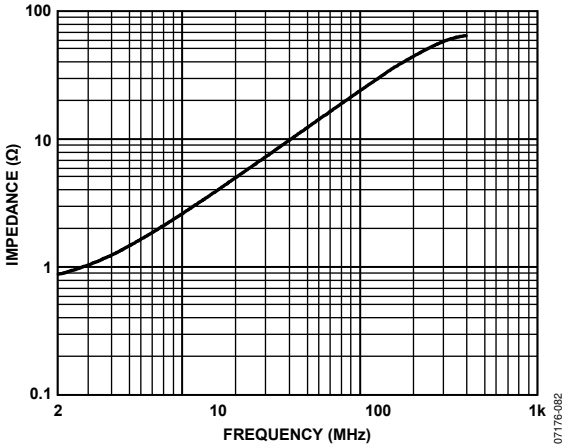


Figure 72. ADV3201 Output Impedance, Enabled

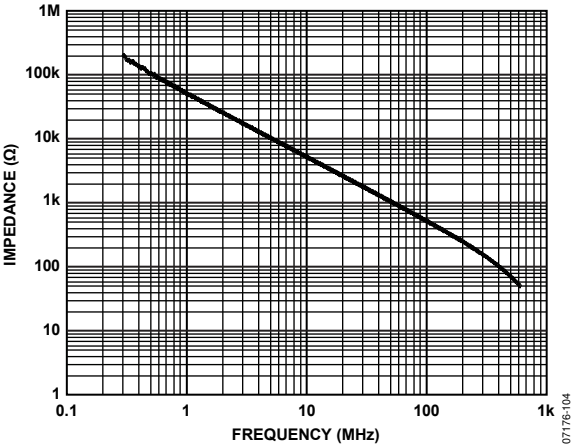


Figure 70. ADV3201 Input Impedance

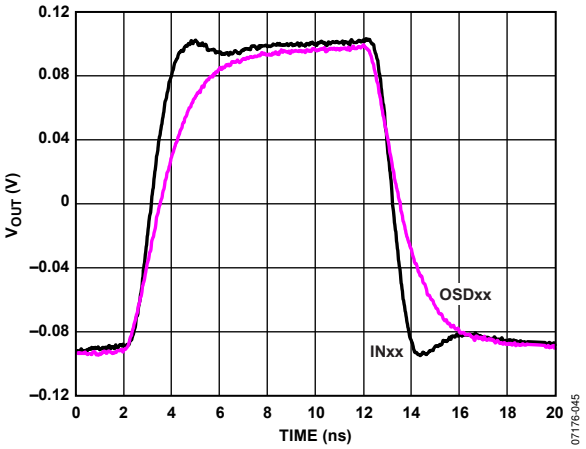


Figure 73. ADV3201 Small Signal Pulse Response, 200 mV p-p

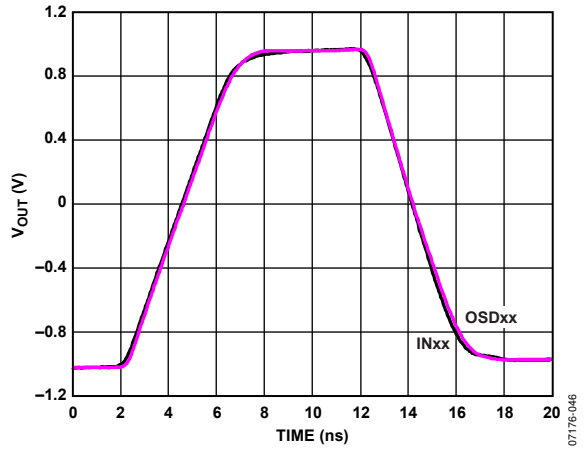


Figure 74. ADV3201 Large Signal Pulse Response, 2 V p-p

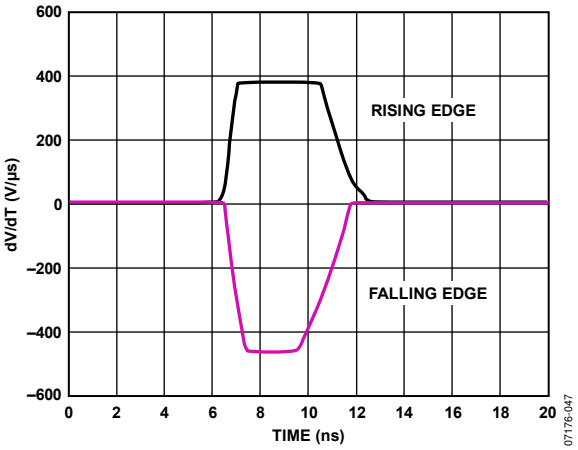


Figure 77. ADV3201 Slew Rate

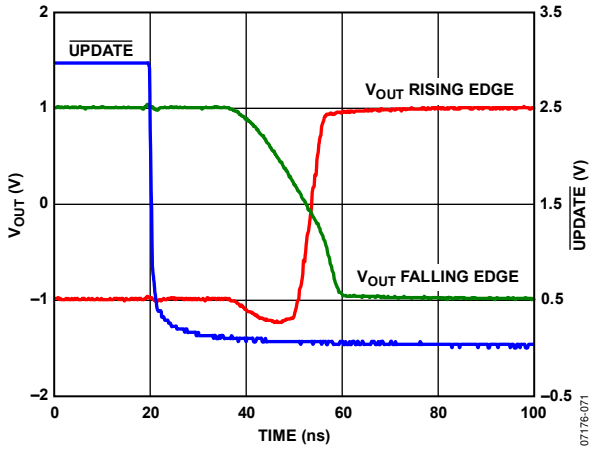


Figure 75. ADV3201 Switching Time

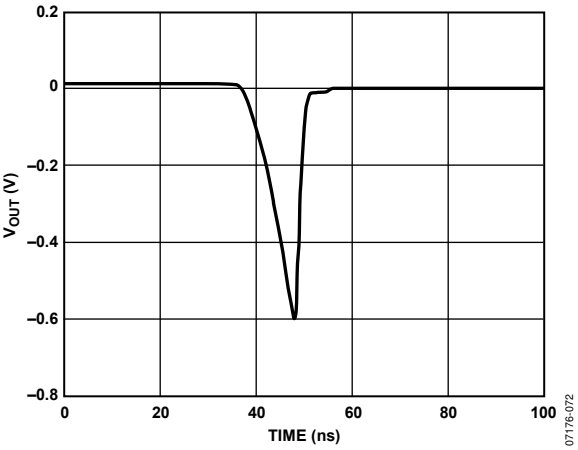


Figure 78. ADV3201 Switching Glitch

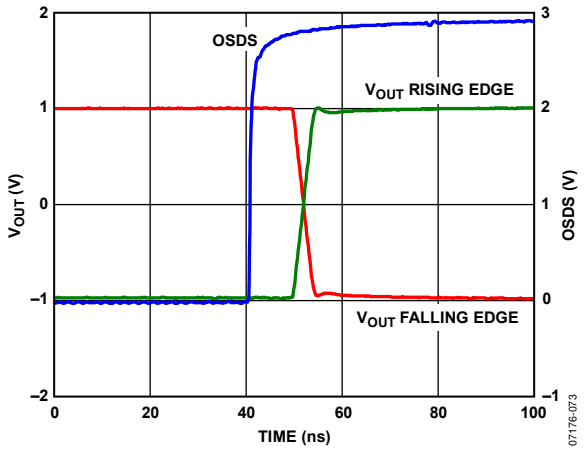


Figure 76. ADV3201 OSD Switching Time

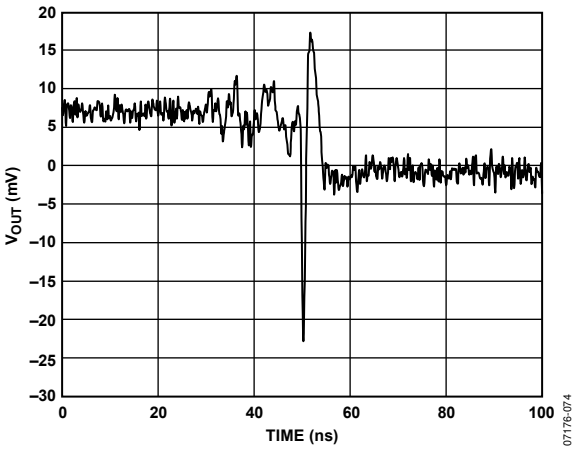


Figure 79. ADV3201 OSD Switching Glitch

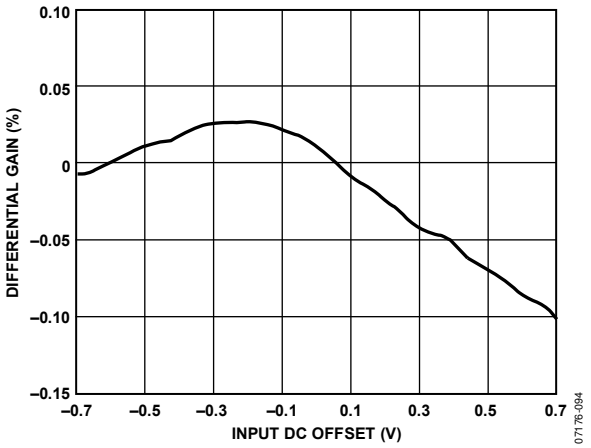


Figure 80. ADV3201 Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

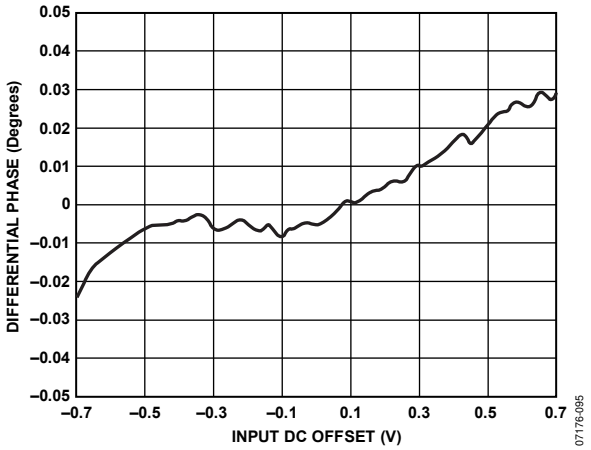


Figure 81. ADV3201 Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

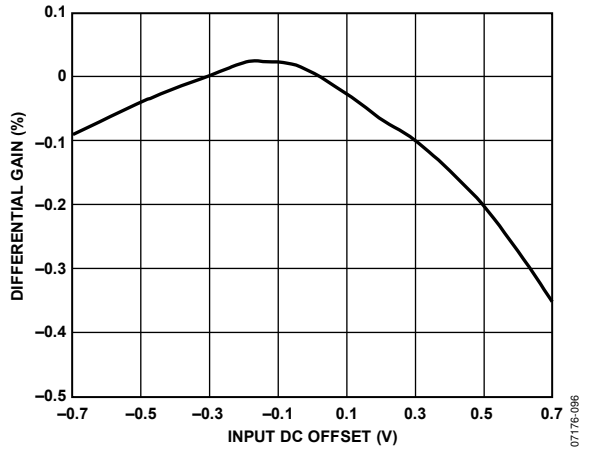


Figure 82. ADV3201 OSD Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

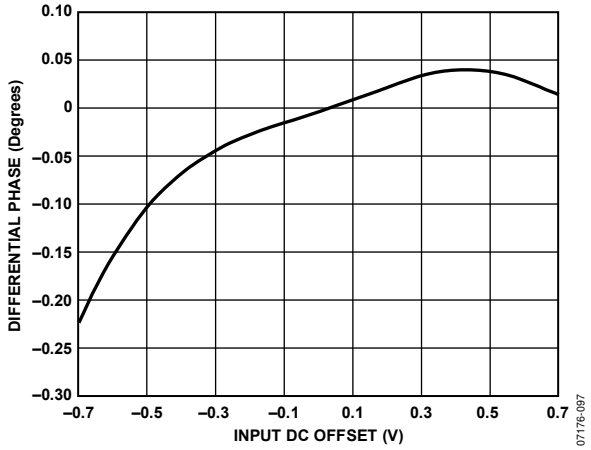


Figure 83. ADV3201 OSD Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

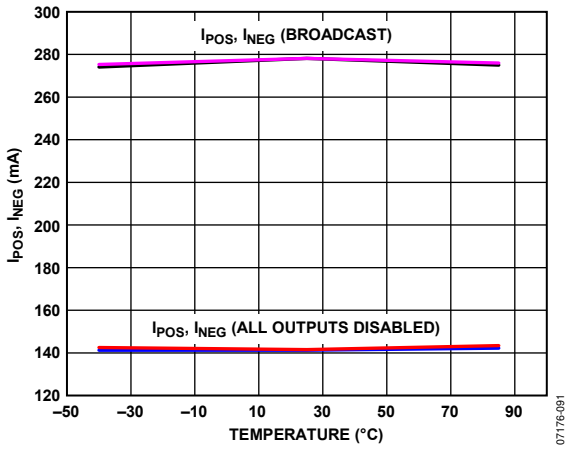


Figure 84. ADV3201 Supply Current vs. Temperature

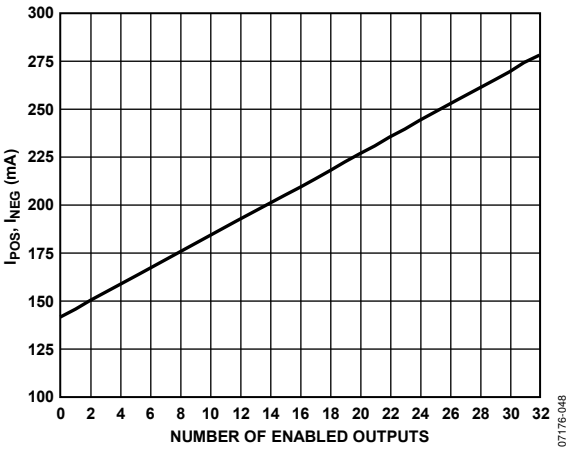


Figure 85. ADV3201 Supply Current vs. Enabled Outputs

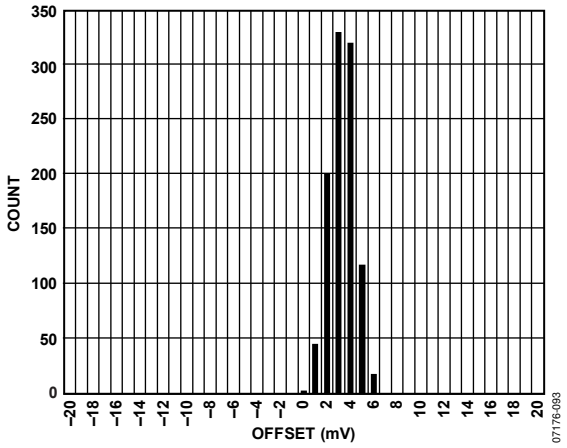


Figure 86. ADV3201 Input Offset Distribution, One Device, All 1024 Channels

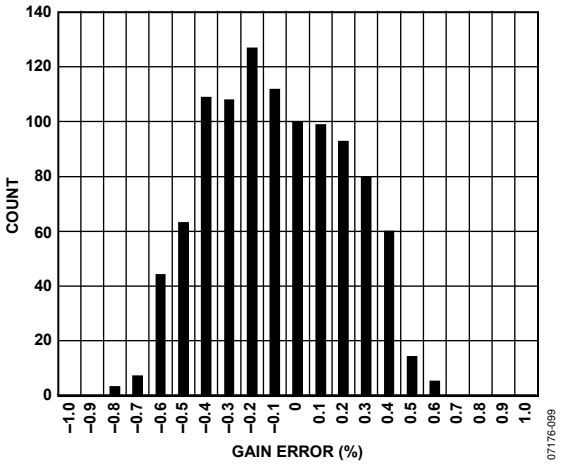


Figure 89. ADV3201 Gain Error Distribution, One Device, All 1024 Channels

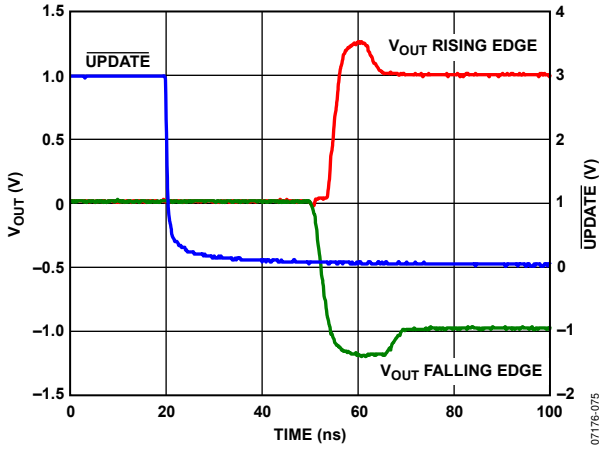


Figure 87. ADV3201 Enable Time

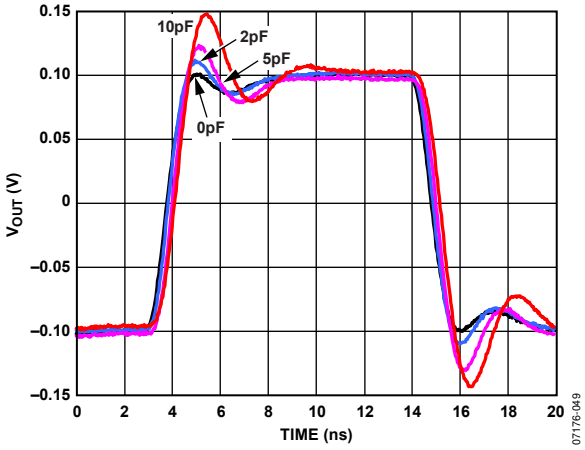


Figure 90. ADV3201 Small Signal Pulse with Capacitive Loads, 200 mV p-p

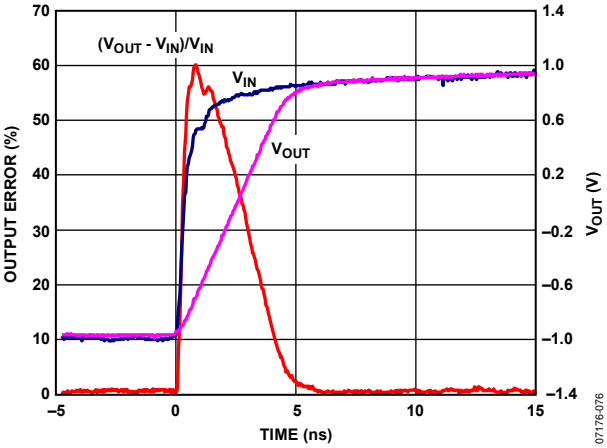


Figure 88. ADV3201 Settling Time

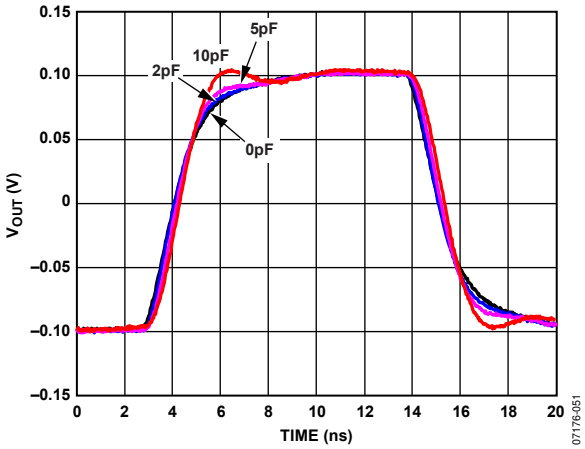


Figure 91. ADV3201 OSD Small Signal Pulse with Capacitive Loads, 200 mV p-p