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Digital PAL/NTSC Video Encoder with 10-Bit SSAF™ and Advanced Power Management

ADV7170/ADV7171

FEATURES

- ITU-R[1] BT601/656 YCrCb to PAL/NTSC video encoder
- High quality 10-bit video DACs
- SSAF (super sub-alias filter)
- Advanced power management features
- CGMS (copy generation management system)
- WSS (wide screen signalling)
- Simultaneous Y, U, V, C output format
- NTSC M, PAL M/N[2], PAL B/D/G/H/I, PAL60
- Single 27 MHz clock required (×2 oversampling)
- 80 dB video SNR
- 32-bit direct digital synthesizer for color subcarrier
- Multistandard video output support
  - Composite (CVBS)
  - Components S-Video (Y/C), YUV, and RGB
  - EuroSCART output (RGB + CVBS/LUMA)
  - Component YUV + CHROMA
- Video input data port supports
  - CCIR-656 4:2:2 8-bit parallel input format
  - 4:2:2 16-bit parallel input format
- Programmable simultaneous composite and S-Video or RGB (SCART)/YUV video outputs
- Programmable luma filters (low-pass [PAL/NTSC]) notch, extended (SSAF, CIF, and QCIF)
- Programmable chroma filters (low-pass [0.65 MHz, 1.0 MHz, 1.2 MHz and 2.0 MHz], CIF and QCIF)
- Programmable VBI (vertical blanking interval)
- Programmable subcarrier frequency and phase
- Programmable LUMA delay
- Individual on/off control of each DAC
- CCIR and square pixel operation
- Integrated subcarrier locking to external video source
- Color signal control/burst signal control
- Interlaced/noninterlaced operation
- Complete on-chip video timing generator
- Programmable multimode master/slave operation
- Macrovision® AntiTaping Rev. 7.1 (ADV7170 only)[3]
- Closed captioning support
- Teletext insertion port (PAL-WST)
- On-board color bar generation
- On-board voltage reference
- 2-wire serial MPU interface (I²C®-compatible and Fast I²C)
- Single supply 5 V or 3.3 V operation
- Small 44-lead MQFP/TQFP packages
- Industrial temperature grade = −40°C to +85°C[4]

APPLICATIONS

- High performance DVD playback systems, portable video equipment including digital still cameras and laptop PCs, video games, PC video/multimedia and digital satellite/cable systems (set-top boxes/IRD)

[1] ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).
[2] Throughout the document N is referenced to PAL- Combination -N.
[3] Protected by U.S. Patents 4,631,603;, 4,577,216, 4,819,098; and other intellectual property rights. The Macrovision anticopy process is licensed for noncommercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available.
[4] Refer to Table 8 for complete operating details.

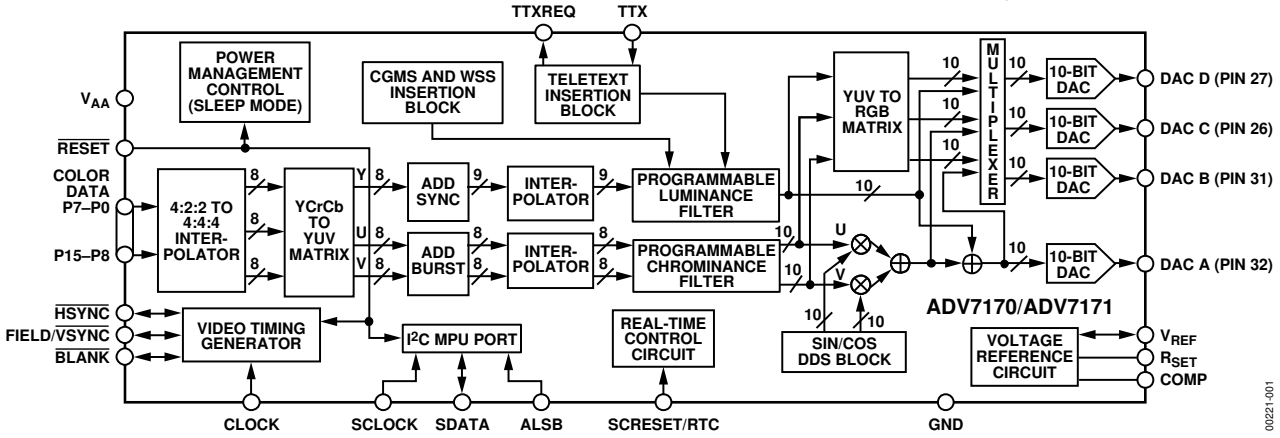

Figure 1. Functional Block Diagram

Rev. C

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Fax: 781.461.3113

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SPECIFICATIONS

V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 1.

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		±0.6		LSB
Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]	R_{SET} = 150 Ω, R_L = 37.5 Ω	3	34.7	37	mA
Output Current[4]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching			1.5		%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.142	1.235	1.327	V
POWER REQUIREMENTS[5]					
V_{AA}		4.75	5.0	5.25	V
Normal Power Mode					
I_{DAC} (max)[6]	R_{SET} = 150 Ω, R_L = 37.5 Ω		150	155	mA
I_{DAC} (min)[6]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		20		mA
I_{CCT}[7]			75	95	mA
Low Power Mode					
I_{DAC} (max)[6]			80		mA
I_{DAC} (min)[6]			20		mA
I_{CCT}[7]			75	95	mA
Sleep Mode					
I_{DAC}[8]			0.1		μA
I_{CCT}[9]			0.001		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] The min/max specifications are guaranteed over this range. The min/max values are typical over 4.75 V to 5.25 V.
[2] Ambient temperature range T_{MIN} to T_{MAX}: −40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] Full drive into 37.5 Ω doubly terminated load.
[4] Minimum drive current (used with buffered/scaled output load).
[5] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[6] I_{DAC} is the total current (min corresponds to 5 mA output per DAC; max corresponds to 37 mA output per DAC) to drive all four DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[7] I_{CCT} (circuit current) is the continuous current required to drive the device.
[8] Total DAC current in sleep mode.
[9] Total continuous current during sleep mode.

V_{AA} = 3.0 V to 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 2.

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		±0.6		LSB
Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}[3, 4]	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current[4, 5]	R_{SET} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current[6]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching			2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 7]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (max)[8]	R_{SET} = 150 Ω, R_L = 37.5 Ω		150	155	mA
I_{DAC} (min)[8]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		20		mA
I_{CCT}[9]			35		mA
Low Power Mode					
I_{DAC} (max)[8]			80		mA
I_{DAC} (min)[8]			20		mA
I_{CCT}[9]			35		mA
Sleep Mode					
I_{DAC}[10]			0.1		μA
I_{CCT}[11]			0.001		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] The min/max specifications are guaranteed over this range. The min/max values are typical over 3.0 V to 3.6 V.
[2] Ambient temperature range T_{MIN} to T_{MAX}: –40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] Guaranteed by characterization.
[4] Full drive into 37.5 Ω load.
[5] DACs can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 37.5 Ω); optimum performance obtained at 18 mA DAC current (R_{SET} = 300 Ω and R_L = 75 Ω).
[6] Minimum drive current (used with buffered/scaled output load).
[7] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[8] I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 38 mA output per DAC) to drive all four DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[9] I_{CCT} (circuit current) is the continuous current required to drive the device.
[10] Total DAC current in sleep mode.
[11] Total continuous current during sleep mode.

DYNAMIC SPECIFICATIONS

V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 3.

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3, 4]	Normal power mode		0.3	0.7	%
Differential Phase[3, 4]	Normal power mode		0.4	0.7	Degrees
Differential Gain[3, 4]	Lower power mode		1.0	2.0	%
Differential Phase[3, 4]	Lower power mode		1.0	2.0	Degrees
SNR[3, 4](Pedestal)	RMS		80		dB rms
SNR[3, 4](Pedestal)	Peak periodic		70		dB p-p
SNR[3, 4](Ramp)	RMS		60		dB rms
SNR[3, 4](Ramp)	Peak periodic		58		dB p-p
Hue Accuracy[3, 4]			0.7	1.2	Degrees
Color Saturation Accuracy[3, 4]			0.9	1.4	%
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		0.6		±%
Chroma Nonlinear Phase[3 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%
Chroma/Luma Gain Inequality[3, 4]			1.0	1.4	±%
Chroma/Luma Delay Inequality[3, 4]			0.5	2.0	ns
Luminance Nonlinearity[3, 4]			0.8	1.4	±%
Chroma AM Noise[3, 4]		82	85		dB
Chroma PM Noise[3, 4]		79	81		dB

[1] The min/max specifications are guaranteed over this range. The min/max values are typical over 4.75 V to 5.25 V.
[2] Ambient temperature range T_{MIN} to T_{MAX}: −40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] Guaranteed by characterization.
[4] These specifications are for the low-pass filter only and are guaranteed by design.

V_{AA} = 3.0 V to 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 4.

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3]	Normal power mode		1.0		%
Differential Phase[3]	Normal power mode		0.5		Degrees
Differential Gain[3]	Lower power mode		0.6		%
Differential Phase[3]	Lower power mode		0.5		Degrees
SNR3 (Pedestal)	RMS		78		dB rms
SNR3 (Pedestal)	Peak periodic		70		dB p-p
SNR3 (Ramp)	RMS		60		dB rms
SNR3 (Ramp)	Peak periodic		58		dB p-p
Hue Accuracy[3]			1.0		Degrees
Color Saturation Accuracy[3]			1.0		%
Luminance Nonlinearity[3, 4]			1.4		±%
Chroma AM Noise[3, 4]			80		dB
Chroma PM Noise[3, 4]			79		dB
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		0.6		±%
Chroma Nonlinear Phase[3, 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%

[1] The min/max specifications are guaranteed over this range. The min/max values are typical over 4.75 V to 5.25 V.
[2] Ambient temperature range T_{MIN} to T_{MAX}: −40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] Guaranteed by characterization.
[4] These specifications are for the low-pass filter only and are guaranteed by design. For other internal filters, see Table 10.

TIMING SPECIFICATIONS

V_{AA} = 4.75 V to 5.25 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulse Width, t_1		0.6			µs
SCLOCK Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the first clock is generated	0.6			µs
Setup Time (Start Condition), t_4	Relevant for repeated start condition	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			11	16	ns
Digital Output Hold Time, t_{14}[4]			8		ns
Pipeline Delay, t_{15}[4]			48		Clock cycles
TELETEXT[3, 4, 7]					
Digital Output Access Time, t_{16}			20		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

[1] The min/max specifications are guaranteed over this range. The min/max values are typical over 4.75 V to 5.25 V range.
[2] Ambient temperature range T_{MIN} to T_{MAX}: –40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] TTL input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.
[4] Guaranteed by characterization
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
[6] Pixel port consists of the following:
Pixel inputs: P15–P0
Pixel controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock input: CLOCK
[7] Teletext port consists of the following:
Teletext output: TTXREQ
Teletext input: TTX

V_{AA} = 3.0 V to 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulse Width, t_1		0.6			µs
SCLOCK Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the first clock is generated	0.6			µs
Setup Time (Start Condition), t_4	Relevant for repeated start condition	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			12		ns
Digital Output Hold Time, t_{14}			8		ns
Pipeline Delay, t_{15}			48		Clock cycles
TELETEXT[3, 4, 7]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V range.
[2] Ambient temperature range T_{MIN} to T_{MAX}: −40°C to +85°C. The die temperature, T_J, must always be kept below 110°C.
[3] TTL input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF.
[4] Guaranteed by characterization
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition
[6] Pixel Port consists of the following:
Pixel inputs: P15–P0
Pixel controls: HSYNC, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock input: CLOCK
[7] Teletext port consists of the following:
Teletext output: TTXREQ
Teletext input: TTX

TIMING DIAGRAMS

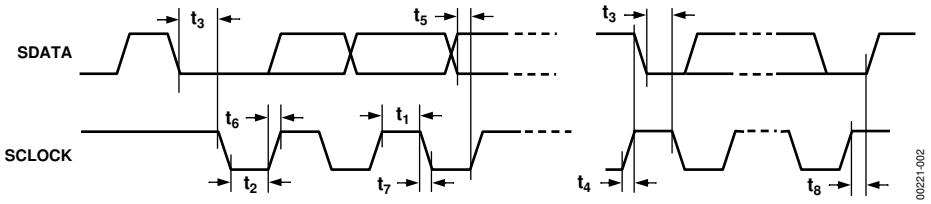


Figure 2. MPU Port Timing Diagram

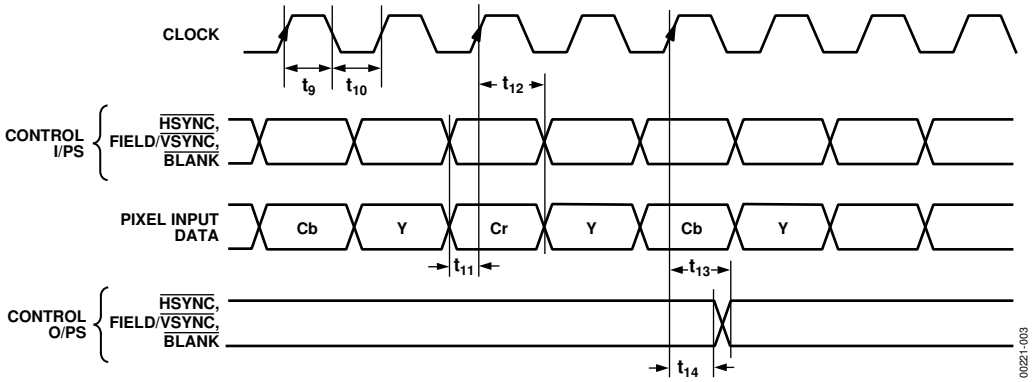


Figure 3. Pixel and Control Data Timing Diagram

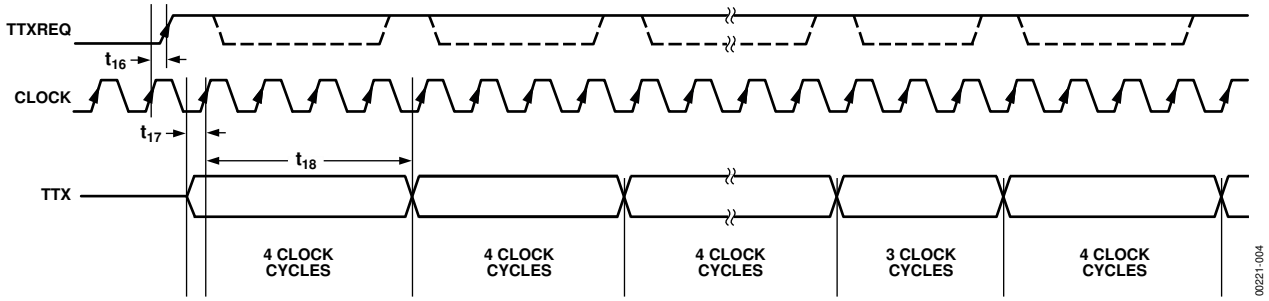


Figure 4. Teletext Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
V_{AA} to GND	7 V
Voltage on Any Digital Input Pin	GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S)	–65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	260°C
Analog Outputs to GND[1]	GND – 0.5 V to V_{AA}

[1] Analog output short circuit to any power supply or GND can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PACKAGE THERMAL PERFORMANCE

The 44-MQFP package used for this device takes advantage of an ADI patented thermal coastline lead frame construction. This maximizes heat transfer into the leads and reduces the package thermal resistance.

For the MQFP package, the junction-to-ambient (θ_{JA}) thermal resistance in still air on a four-layer PCB is 35.5°C/W. The junction-to-case thermal resistance (θ_{JC}) is 13.75°C/W. For the TQFP package, θ_{JA} in still air on a four-layer PCB is 53.2°C/W. θ_{JC} is 11.1°C/W. Junction Temperature = $T_J = [V_{AA} (\Sigma \text{ DAC Output Current} + I_{CCT}) \times \theta_{JA}]$ + Ambient Temperature.

Table 8. Allowable Operating Conditions for KS and KSU Package Options

	KS, WBS		KSU	
Conditions	**3 V**	**5 V**	**3 V**	**5 V**
4 DAC ON Double 75R[1]	Yes	+70°C max	+70°C max	No
4 DAC ON Low Power[2]	Yes	Yes	Yes	No
4 DAC ON Buffering[3]	Yes	Yes	Yes	Yes
3 DAC ON Double 75R	Yes	Yes	Yes	No
3 DAC ON Low Power	Yes	Yes	Yes	Yes
3 DAC ON Buffering	Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes	Yes
Yes	Yes	Yes		
4 DAC ON Buffering	Yes	Yes		

[1] DAC ON Double 75R refers to a condition where the DACs are terminated in a double 75R load and low power mode is disabled.
[2] DAC ON Low Power refers to a condition where the DACs are terminated in a double 75R load and low power mode is enabled.
[3] DAC ON Buffering refers to a condition where the DAC current is reduced to 5 mA and external buffers are used to drive the video load.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

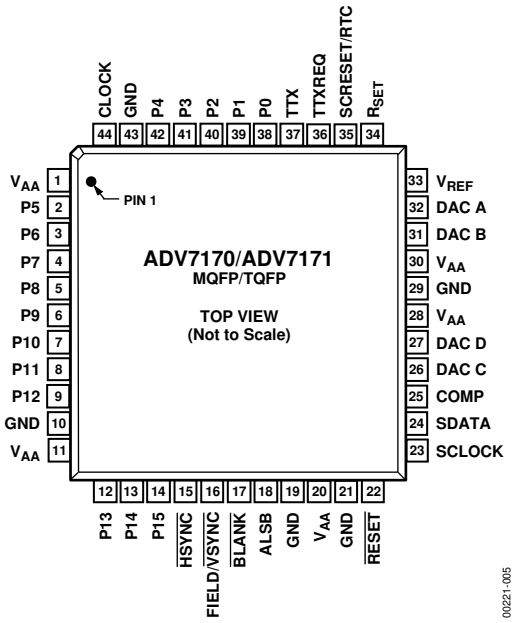


Figure 5. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Description
1, 11, 20, 28, 30	V_{AA}	P	Power Supply (3 V to 5 V).
2 to 9, 12 to 14, 38 to 42	P15 to P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7 to P0) or 16-Bit YCrCb Pixel Port (P15 to P0). P0 represents the LSB.
10, 19, 21, 29, 43	GND	G	Ground Pin.
15	$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Mode 1 and Mode 2) Control Signal. This pin may be configured to output (master mode) or accept (slave mode) sync signals.
16	FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (master mode) or accept (slave mode) these control signals.
17	$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level 0. This signal is optional.
18	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
22	$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7170/ADV7171 into default mode. This is NTSC operation, Timing Slave Mode 0, 8-bit operation, 2 × composite and S-Video out, and DAC B powered on and DAC D powered off.
23	SCLOCK	I	MPU Port Serial Interface Clock Input.
24	SDATA	I/O	MPU Port Serial Data Input/Output.
25	COMP	O	Compensation Pin. Connect a 0.1 µF capacitor from COMP to V_{AA}. For optimum dynamic performance in low power mode, the value of the COMP capacitor can be lowered to as low as 2.2 nF.
26	DAC C	O	RED/S-Video C/V Analog Output.
27	DAC D	O	GREEN/S-Video Y/Y Analog Output.
31	DAC B	O	BLUE/Composite/U Analog Output.
32	DAC A	O	PAL/NTSC Composite Video Output. Full-scale output is 180 IRE (1286 mV) for NTSC and 1300 mV for PAL.
33	V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
34	R_{SET}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the video signals.

Pin No.	Mnemonic	Input/ Output	Description
35	SCRESET/RTC	I	This pin can be configured as an input by setting MR22 and MR21 of Mode Register 2. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin resets the subcarrier to Field 0. Alternatively, it may be configured as a real-time control (RTC) input.
36	TTXREQ	O	Teletext Data Request Signal. Defaults to GND when teletext not selected. Enables backward compatibility to ADV7175/ADV7176.
37	TTX	I	Teletext Data. Defaults to V_{AA} when teletext not selected. Enables backward compatibility to ADV7175/ADV7176.
44	CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.

GENERAL DESCRIPTION

The ADV7170/ADV7171 are integrated digital video encoders that convert digital CCIR-601 4:2:2 8- or 16-bit component video data into a standard analog baseband television signal compatible with worldwide standards.

The on-board SSAF (super sub-alias filter) with extended luminance frequency response and sharp stop band attenuation enables studio-quality video playback on modern TVs, giving optimal horizontal line resolution.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes and power-down or sleep modes.

The ADV7170/ADV7171 support both PAL and NTSC square pixel operation. The parts also incorporate WSS and CGMS-A data control generation.

The output video frames are synchronized with the incoming data timing reference codes. Optionally, the encoder accepts and can generate $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD timing signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The encoder requires a single, two-times pixel rate (27 MHz) clock for standard operation. Alternatively, the encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7170/ADV7171 modes are set up over a 2-wire, serial bidirectional port (I^2C-compatible) with two slave addresses.

Functionally, the ADV7170 and ADV7171 are the same with the exception that the ADV7170 can output the Macrovision anticopy algorithm.

The ADV7170/ADV7171 are packaged in a 44-lead MQFP package and a 44-lead TQFP package.

DATA PATH DESCRIPTION

For PAL B/D/G/H/I/M/N, and NTSC M and N modes, YcrCb 4:2:2 data is input via the CCIR-656 compatible pixel port at a 27 MHz data rate. The pixel data is demultiplexed to form three data paths. Y typically has a range of 16 to 235; Cr and Cb typically have a range of 128 ± 112. However, it is possible to input data from 1 to 254 on Y, Cb, and Cr. The ADV7170/ADV7171 support PAL (B, D, G, H, I, M, N) and NTSC (with and without pedestal) standards. The appropriate SYNC, $\overline{\text{BLANK}}$, and burst levels are added to the YCrCb data. Macrovision antitaping (ADV7170 only), closed-captioning, and teletext levels are also added to Y, and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate sub-carrier sine/cosine phases and added together to make up the chrominance signal. The luma (Y) signal can be delayed 1 to 3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate SYNC and $\overline{\text{BLANK}}$ levels. The RGB data is in synchronization with the composite video output. Alternatively, analog YUV data can be generated instead of RGB.

The four 10-bit DACs can be used to output the following:

Composite video + RGB video.

Composite video + YUV video.

Two composite video signals + LUMA and CHROMA (Y/C) signals.

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in Appendix 6—Waveforms.

INTERNAL FILTER RESPONSE

The Y filter supports several different frequency responses, including two low-pass responses, two notch responses, an extended (SSAF) response, a CIF response, and a QCIF response. The UV filter supports several different frequency responses, including four low-pass responses, a CIF response, and a QCIF response that are shown in Table 10 and Table 11 and Figure 6 to Figure 18.

Table 10. Luminance Internal Filter Specifications

Filter Type	Filter Selection MR04	MR03	MR02	Pass-Band Ripple (dB)	3 dB Bandwidth (MHz)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)
Low Pass (NTSC)	0	0	0	0.091	4.157	7.37	–56
Low Pass (PAL)	0	0	1	0.15	4.74	7.96	–64
Notch (NTSC)	0	1	0	0.015	6.54	8.3	–68
Notch (PAL)	0	1	1	0.095	6.24	8.0	–66
Extended (SSAF)	1	0	0	0.051	6.217	8.0	–61
CIF	1	0	1	0.018	3.0	7.06	–61
QCIF	1	1	0	Monotonic	1.5	7.15	–50

Table 11. Chrominance Internal Filter Specifications

Filter Type	Filter Selection MR07	MR06	MR05	Pass-Band Ripple (dB)	3 dB Bandwidth (MHz)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)
1.3 MHz Low Pass	0	0	0	0.084	1.395	3.01	–45
.65 MHz Low Pass	0	0	1	Monotonic	0.65	3.64	–58.5
1.0 MHz Low Pass	0	1	0	Monotonic	1.0	3.73	–49
2.0 MHz Low Pass	0	1	1	0.0645	2.2	5.0	–40
Reserved	1	0	0				
CIF	1	0	1	0.084	0.7	3.01	–45
QCIF	1	1	0	Monotonic	0.5	4.08	–50

TYPICAL PERFORMANCE CHARACTERISTICS

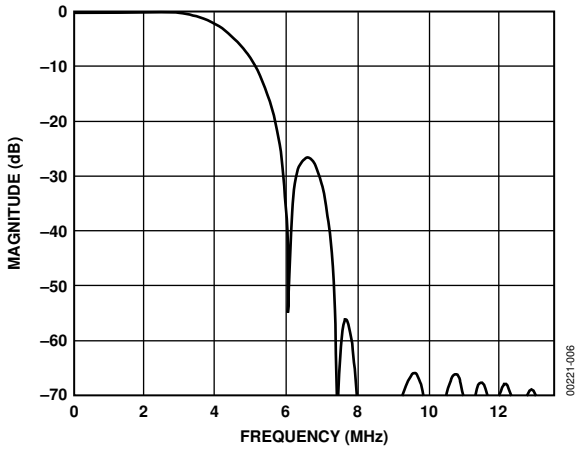


Figure 6. NTSC Low-Pass Luma Filter

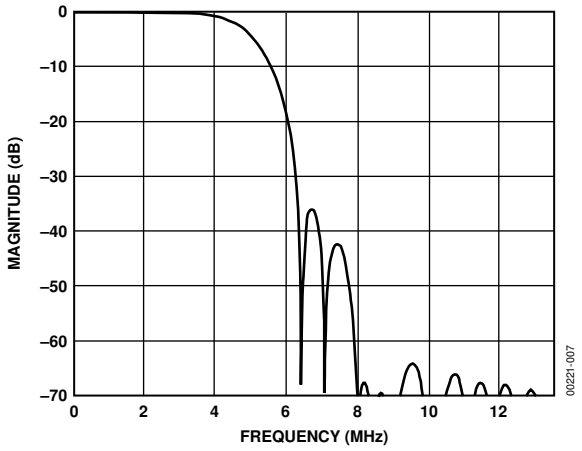


Figure 7. PAL Low-Pass Luma Filter

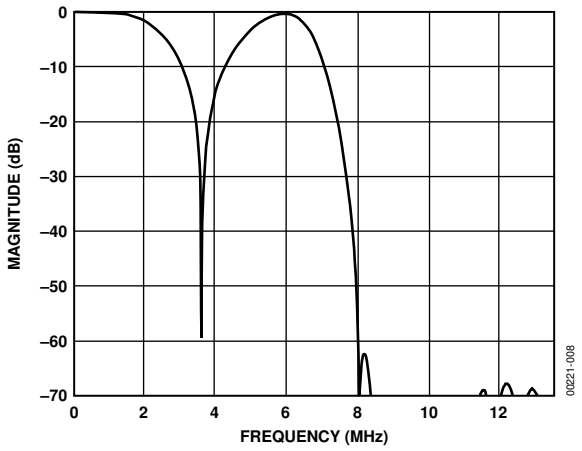


Figure 8. NTSC Notch Luma Filter

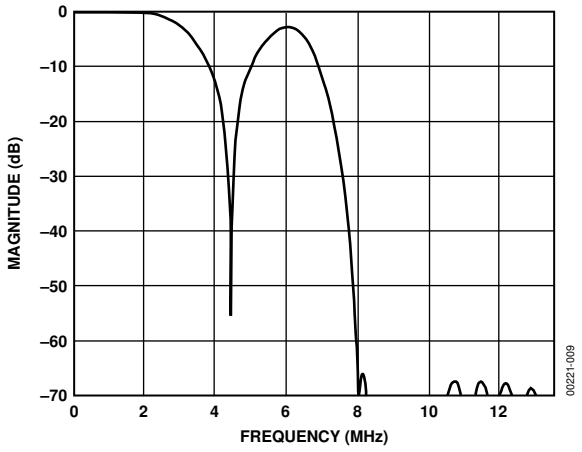


Figure 9. PAL Notch Luma Filter

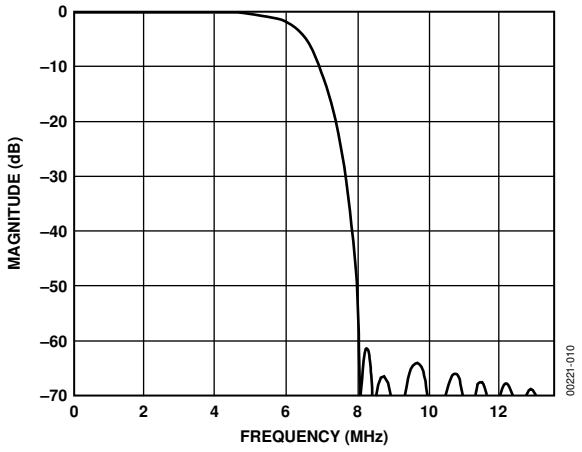


Figure 10. Extended Mode (SSAF) Luma Filter

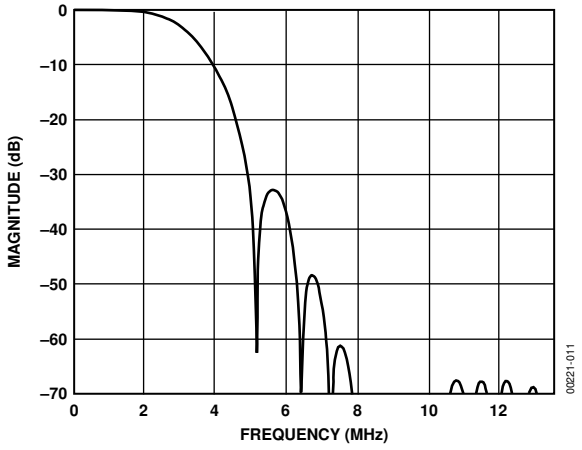


Figure 11. CIF Luma Filter

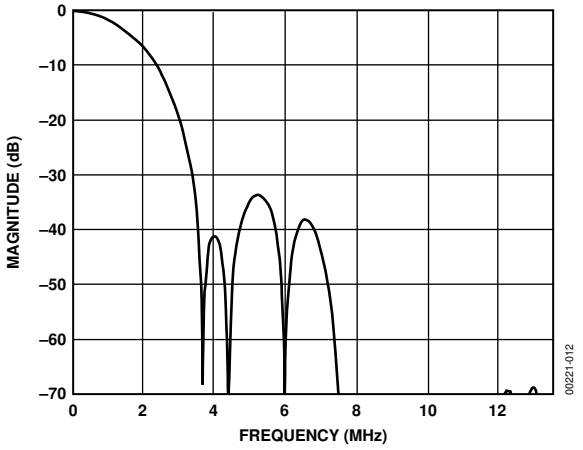


Figure 12. QCIF Luma Filter

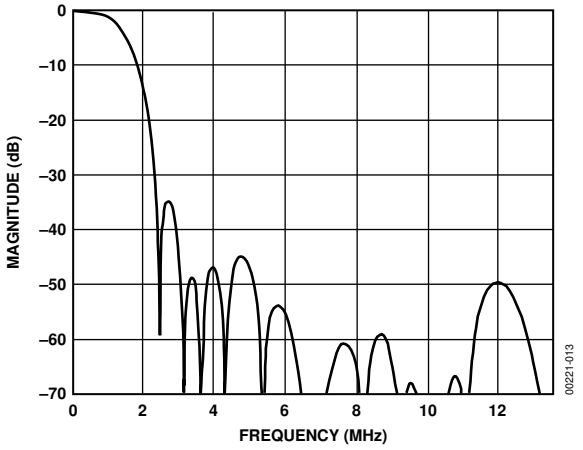


Figure 13. 1.3 MHz Low-Pass Chroma Filter

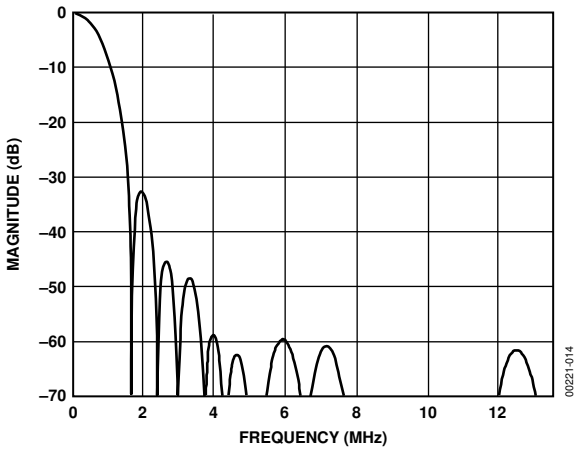


Figure 14. 0.65 MHz Low-Pass Chroma Filter

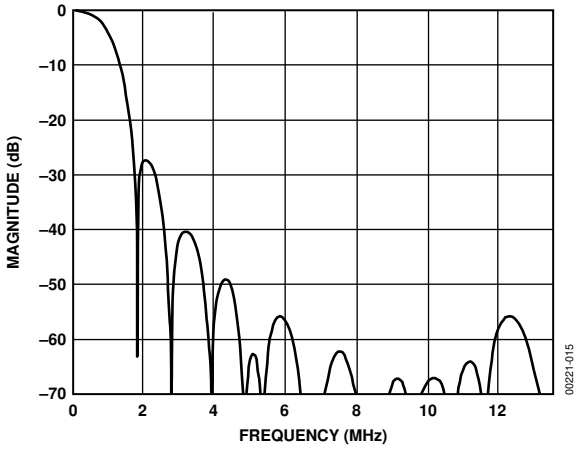


Figure 15. 1.0 MHz Low-Pass Chroma Filter

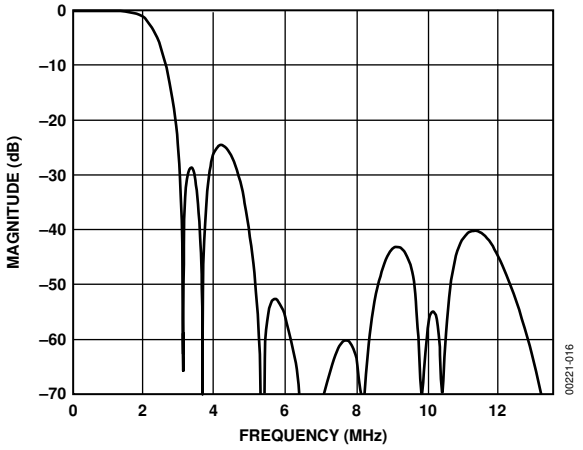


Figure 16. 2.0 MHz Low-Pass Chroma Filter

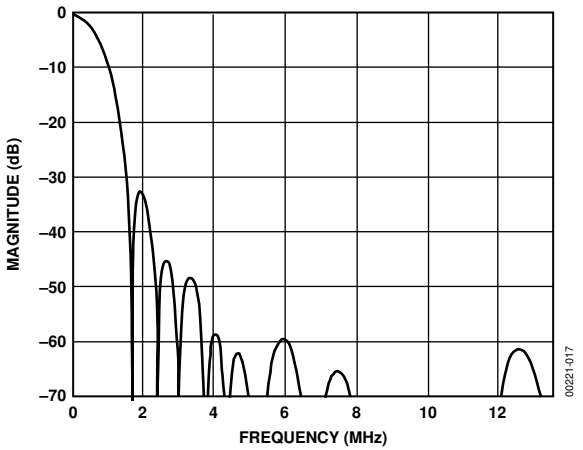


Figure 17. CIF Chroma Filter

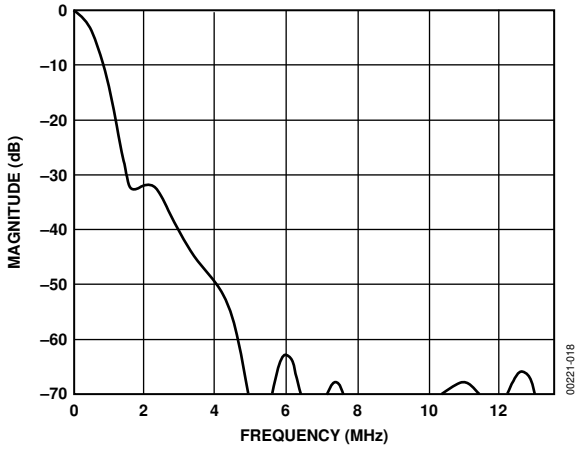


Figure 18. QCIF Chroma Filter

FEATURES

COLOR BAR GENERATION

The ADV7170/ADV7171 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 color bars for PAL. These are enabled by setting MR17 of Mode Register 1 to Logic Level 1.

SQUARE PIXEL MODE

The ADV7170/ADV7171 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation. When the ADV7171 is configured for PAL square pixel mode, it supports 768 active pixels per line. NTSC square pixel mode supports 640 active pixels per line.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL

The pedestal on both odd and even fields can be controlled on a line-by-line basis using the NTSC pedestal control registers. This allows the pedestals to be controlled during the vertical blanking interval.

PIXEL TIMING DESCRIPTION

The ADV7170/ADV7171 operate in either 8-bit or 16-bit YCrCb mode.

8-Bit YCrCb Mode

This default mode accepts multiplexed YCrCb inputs through the P7 to P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, and so on. The Y, Cb, and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode

This mode accepts Y inputs through the P7 to P0 pixel inputs and multiplexed CrCb inputs through the P15 to P8 pixel inputs. The data is loaded on every second rising edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, and so on.

SUBCARRIER RESET

Together with the SCRESET/RTC pin and Bit MR22 and Bit MR21 of Mode Register 2, the ADV7170/ADV7171 can be used in subcarrier reset mode. The subcarrier resets to Field 0 at the start of the following field when a low-to-high transition occurs on this input pin.

REAL-TIME CONTROL

Together with the SCRESET/RTC pin and Bit MR22 and Bit MR21 of Mode Register 2, the ADV7170/ADV7171 can be used to lock to an external video source. The real-time control mode allows the ADV7170/ADV7171 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7185 video decoder, shown in Figure 19), the part automatically changes to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide, and the subcarrier is contained in Bit 0 to Bit 21. Each bit is 2 clock cycles long. 00Hex should be written into all four subcarrier frequency registers when using this mode.

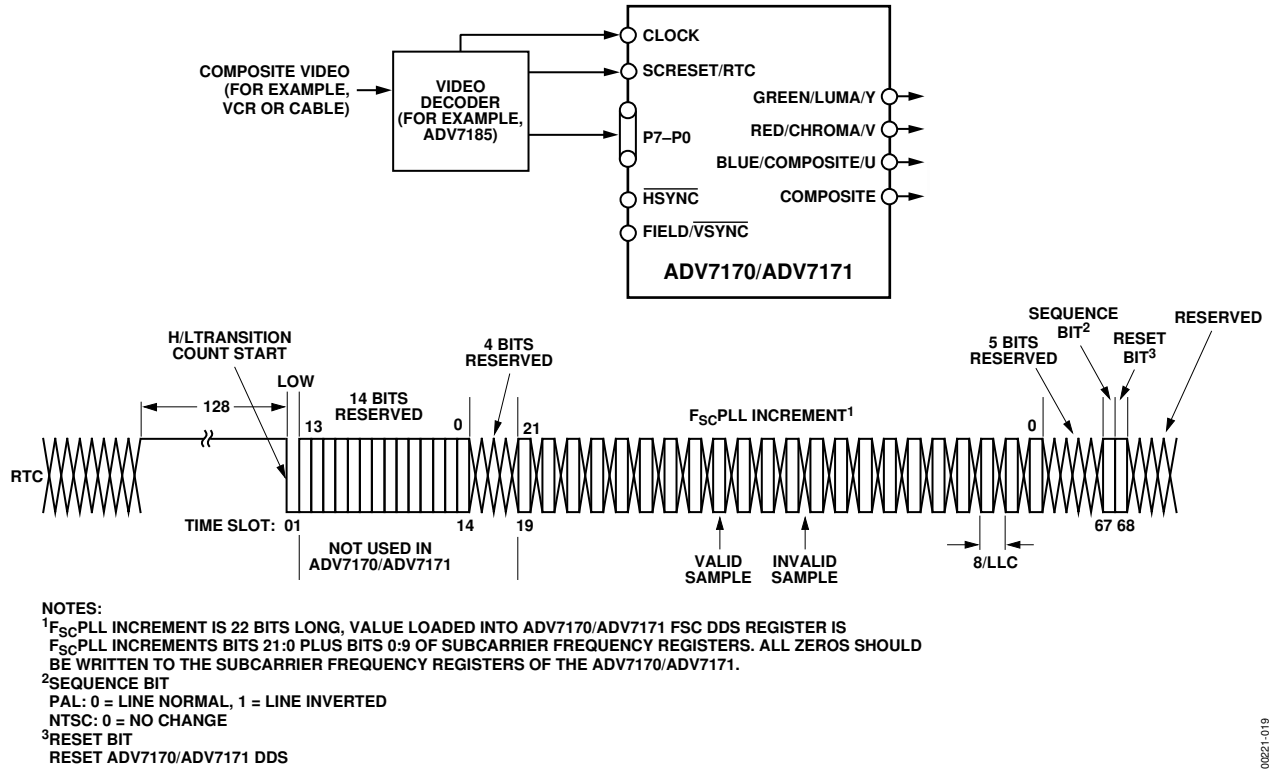
VIDEO TIMING DESCRIPTION

The ADV7170/ADV7171 are intended to interface to off-the-shelf MPEG1 and MPEG2 decoders. Consequently, the ADV7170/ADV7171 accept 4:2:2 YCrCb pixel data via a CCIR-656 pixel port, and they have several video timing modes of operation that allow them to be configured as either system master video timing generators or as slaves to the system video timing generator. The ADV7170/ADV7171 generate all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7170/ADV7171 calculate the width and placement of analog sync pulses, blanking levels, and color burst envelopes. Color bursts are disabled on appropriate lines, and serration and equalization pulses are inserted where required.

In addition, the ADV7170/ADV7171 support a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7170/ADV7171 have four distinct master and four distinct slave timing configurations. Timing Control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths where they occur in relation to each other.



NOTES:
[1]F_{SC}PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7170/ADV7171 FSC DDS REGISTER IS F_{SC}PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7170/ADV7171.
[2]SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
[3]RESET BIT
RESET ADV7170/ADV7171 DDS

Figure 19. RTC Timing and Connections

Vertical Blanking Data Insertion

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not bear line sync or pre-/post-equalization pulses (see Figure 21 to Figure 32). This mode of operation is called "partial blanking" and is selected by setting MR32 to 1. It allows the insertion of any VBI data (opened VBI) into the encoded output waveform. This data is present in the digitized incoming YcbCr data stream (for example, WSS data, CGMS, VPS, and so on). Alternatively, the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR32 to 0.

Mode 0 (CCIR-656): Slave Option

(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7170/ADV7171 are controlled by the SAV (start active video) and EAV (end active video) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is shown in Figure 20. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

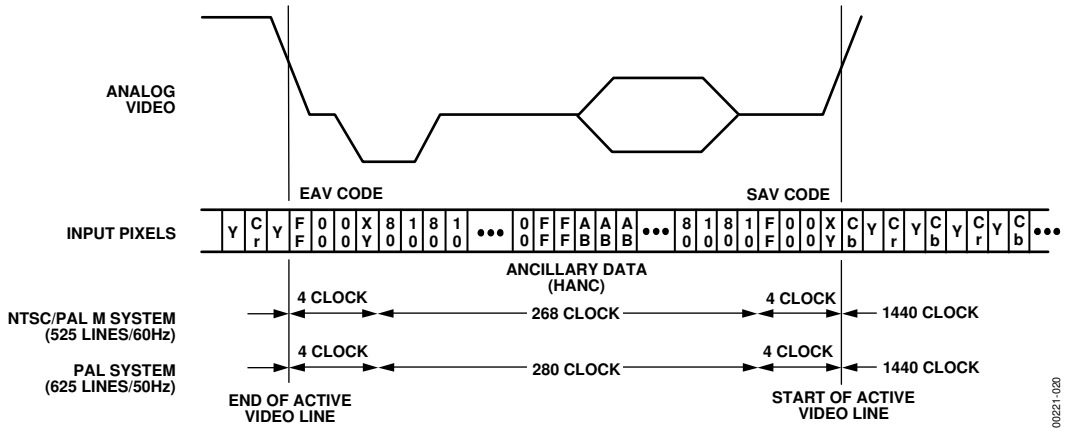


Figure 20. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR-656): Master Option

(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7170/ADV7171 generate H, V, and F signals required for the SAV (start active video) and EAV (end active video) time codes in the CCIR656 standard. The H bit is output on the HSYNC pin, the V bit is output on the BLANK pin, and the F bit is output on the FIELD/VSYNC pin. Mode 0 is illustrated in Figure 21 (NTSC) and Figure 22 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 23.

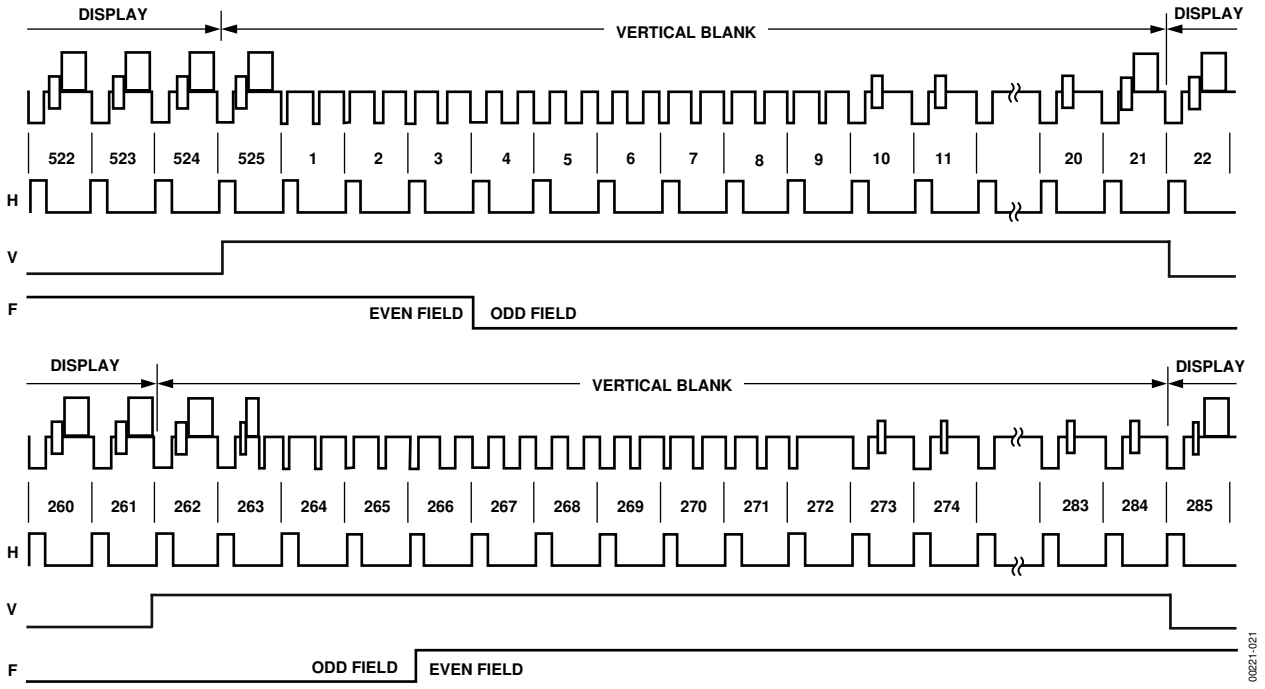


Figure 21. Timing Mode 0 (NTSC Master Mode)

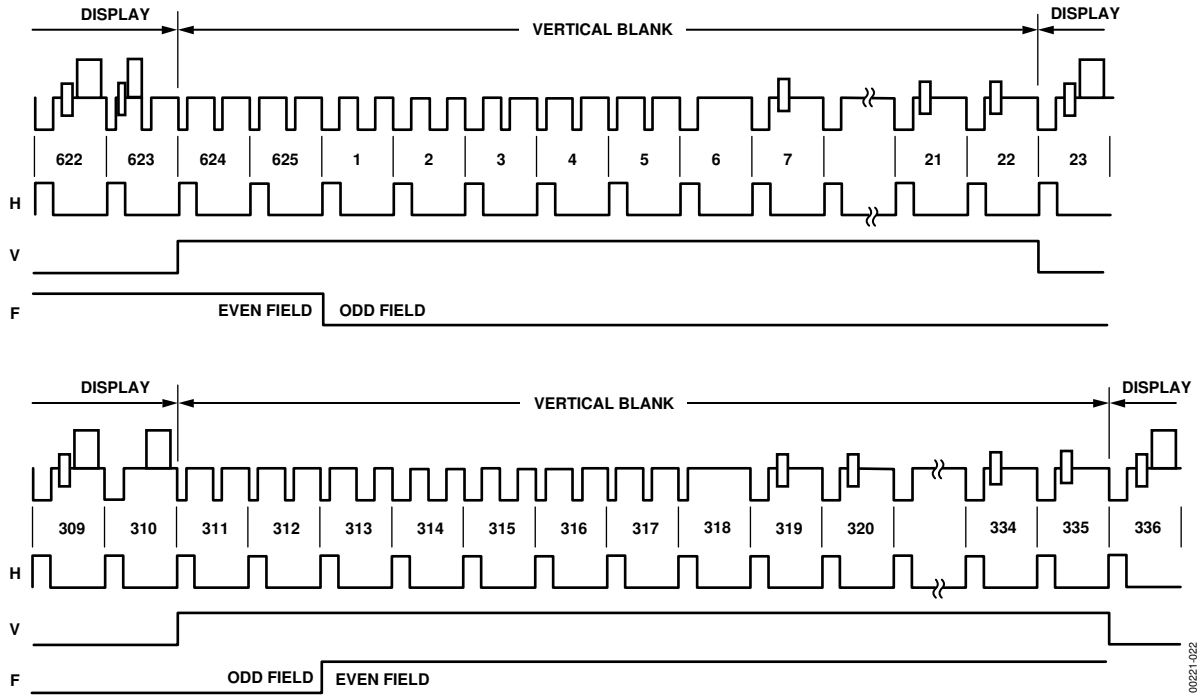


Figure 22. Timing Mode 0 (PAL Master Mode)

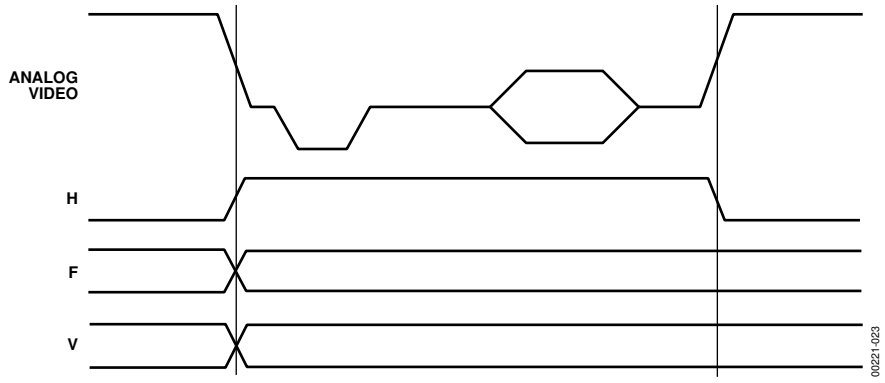


Figure 23. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7170/ADV7171 accept horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{HSYNC}$ is low indicates a new frame, that is, vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7170/ADV7171 automatically blank all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

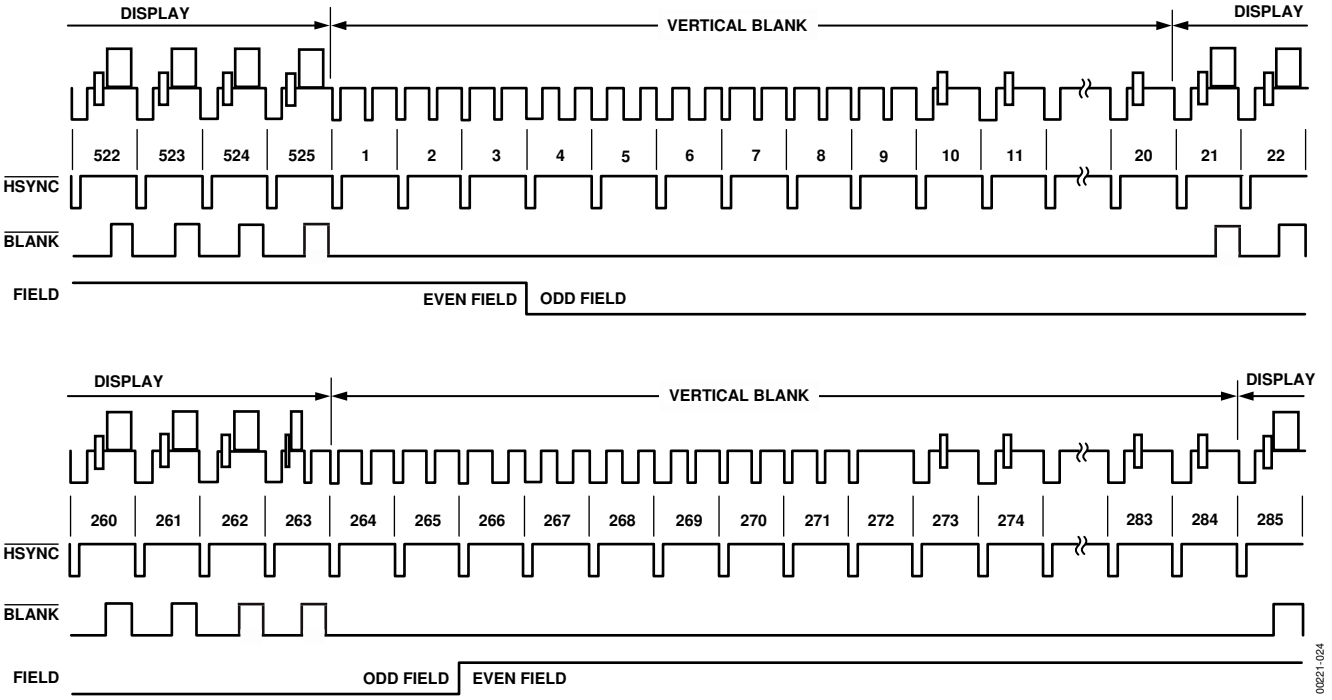


Figure 24. Timing Mode 1 (NTSC)

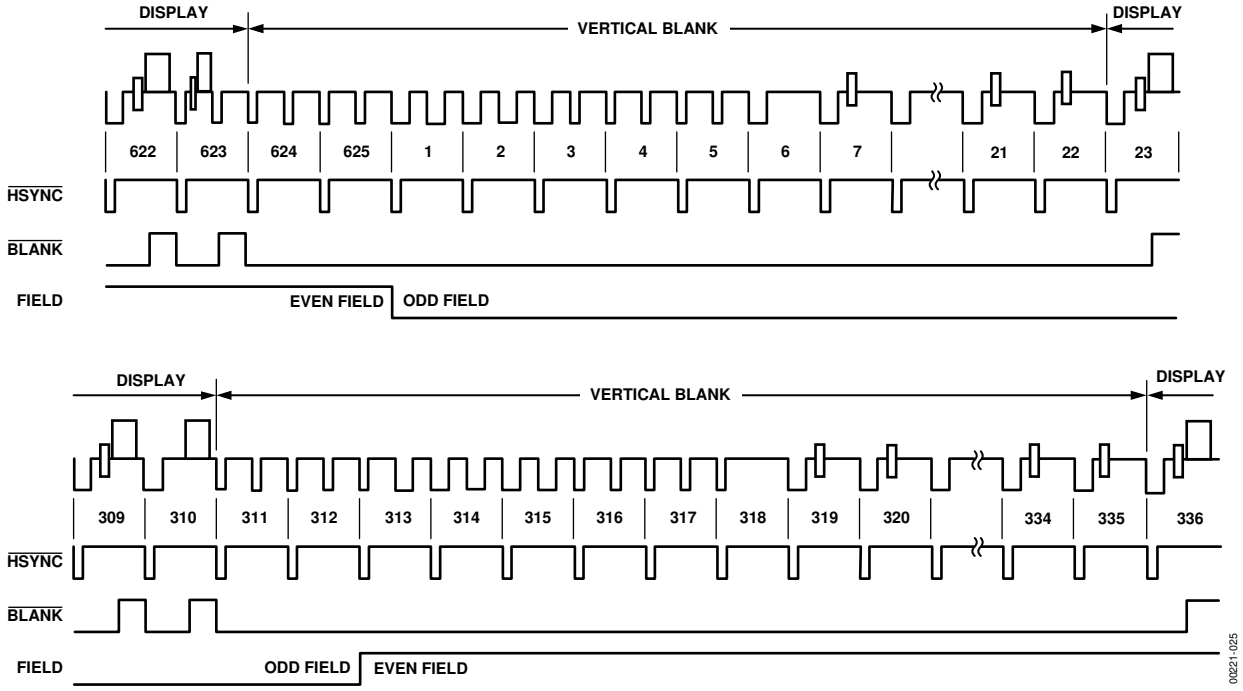


Figure 25. Timing Mode 1 (PAL)

Mode 1: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD

(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7170/ADV7171 can generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, that is, vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blank all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is shown in Figure 24 (NTSC) and Figure 25 (PAL). Figure 26 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD for an odd or even field transition relative to the pixel data.

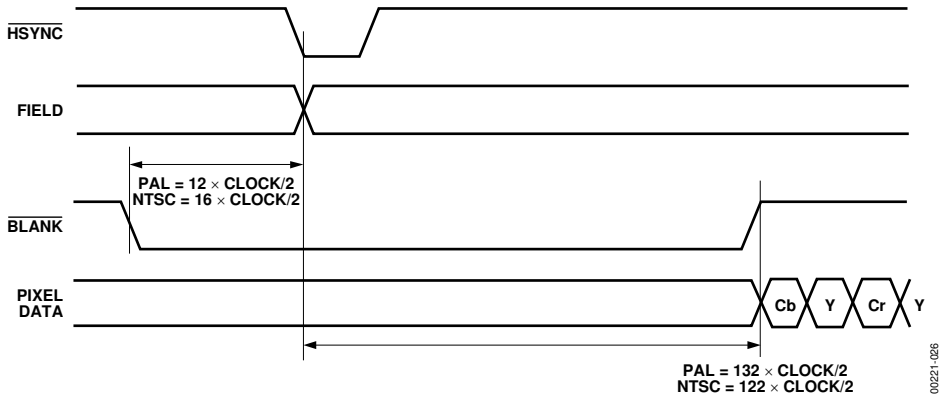


Figure 26. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$

(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7170/ADV7171 accept horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blank all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL).

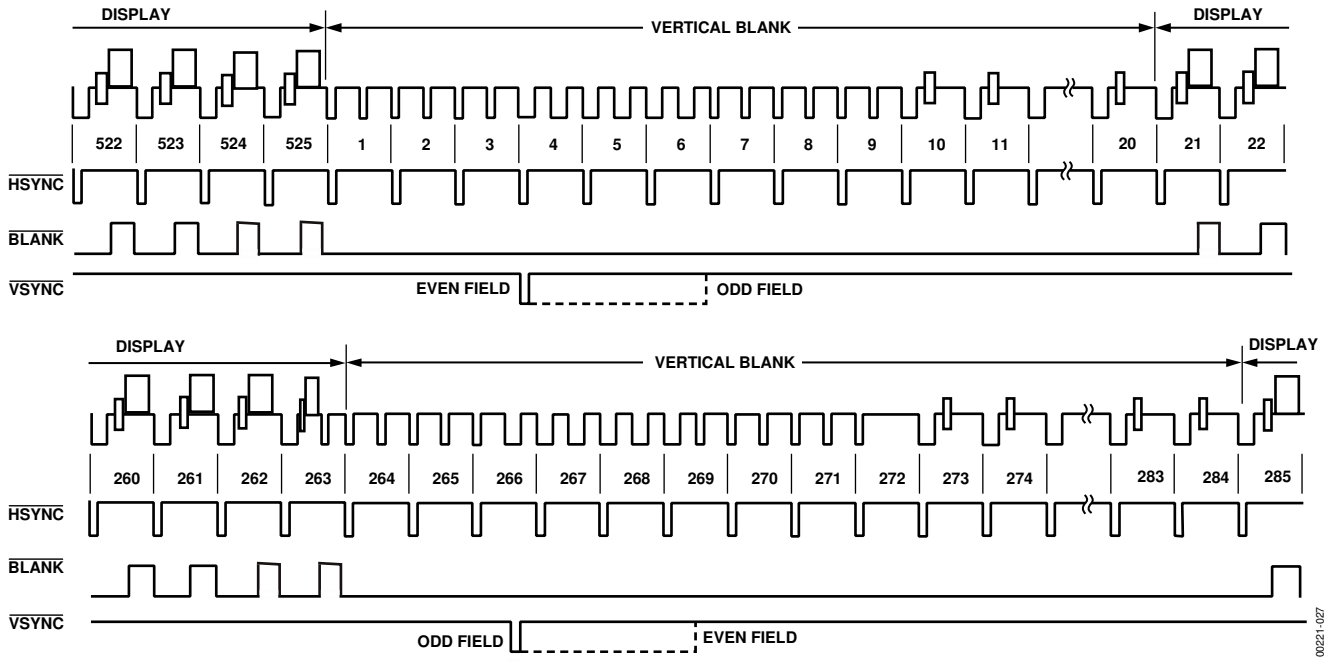


Figure 27. Timing Mode 2 (NTSC)

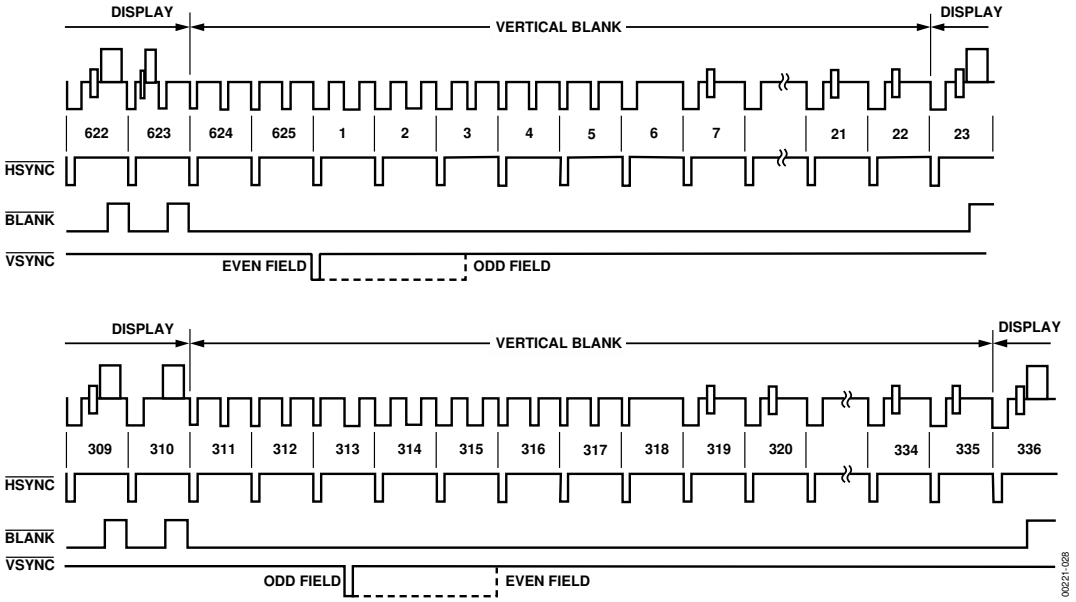


Figure 28. Timing Mode 2 (PAL)

Mode 2: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$

(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7170/ADV7171 can generate horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blank all normally blank lines as per CCIR-624. Mode 2 is shown in Figure 27 (NTSC) and Figure 28 (PAL). Figure 29 shows the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an even-to-odd field transition relative to the pixel data. Figure 30 shows the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an odd-to-even field transition relative to the pixel data.

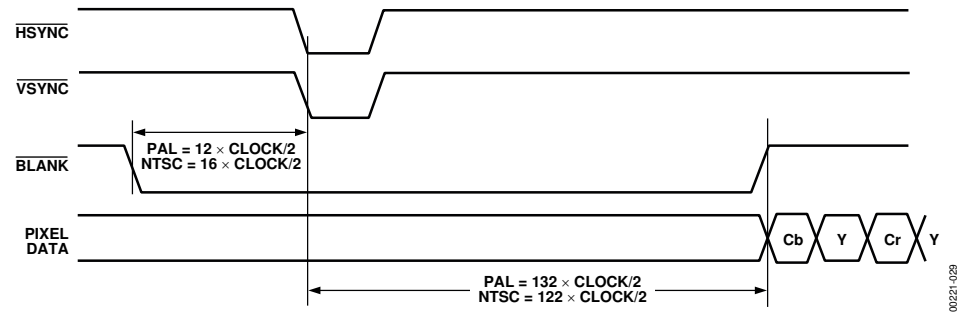


Figure 29. Timing Mode 2 Even-to-Odd Field Transition Master/Slave

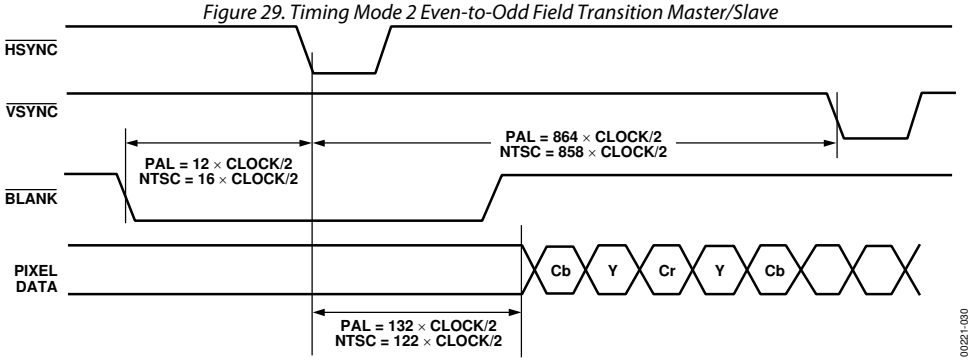


Figure 30. Timing Mode 2 Odd-to-Even Field Transition Master/Slave

Mode 3: Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD

(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7170/ADV7171 accept or generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame, that is, vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blank all normally blank lines as per CCIR-624. Mode 3 is shown in Figure 31 (NTSC) and Figure 32 (PAL).

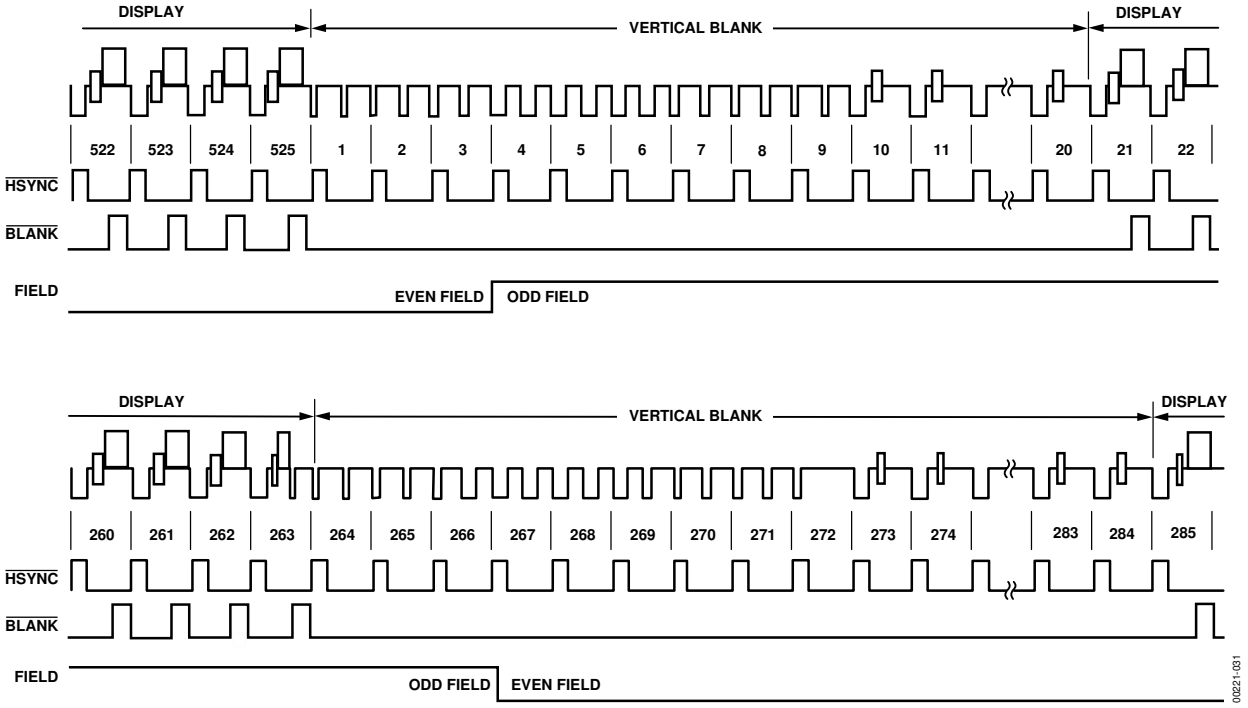


Figure 31. Timing Mode 3 (NTSC)

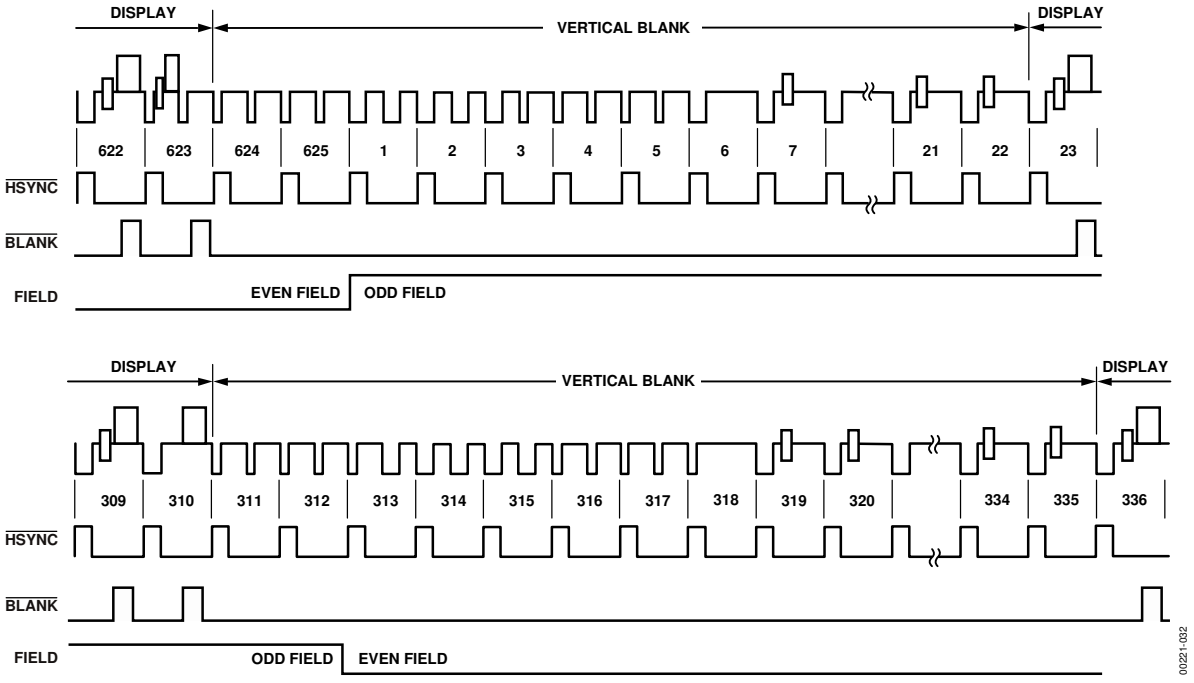


Figure 32. Timing Mode 3 (PAL)