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Digital PAL/NTSC Video Encoder with Six DACs (10 Bits), Color Control and Enhanced Power Management

ADV7172/ADV7173

FEATURES

- ITU-R[1] BT601/656 YCrCb to PAL/NTSC Video Encoder
- Six High Quality 10-Bit Video DACs
- SSAF™ (Super Sub-Alias Filter)
- Advanced Power Management Features
  - PC'98-Compliant (TV Detect with Polling and Auto Shutdown to Save On Power Consumption)
  - Low Power DAC Mode
  - Individual DAC ON/OFF Control
  - Variable DAC Output Current (5 mA–36 mA)
  - Ultralow Sleep Mode Current
- Hue, Brightness, Contrast and Saturation Controls
- CGMS (Copy Generation Management System)
- WSS (Wide Screen Signalling)
- NTSC-M, PAL-M/N, PAL-B/D/G/H/I, PAL-60
- YUV Betacam, MII and SMPTE/EBU N10 Output Levels
- Single 27 MHz Clock Required (×2 Oversampling)
- 80 dB Video SNR
- 32-Bit Direct Digital Synthesizer for Color Subcarrier
- Multistandard Video Output Support:
  - Composite (CVBS)
  - Component S-Video (Y/C)
  - Component YUV
  - EuroSCART RGB
  - Component YUV + CHROMA + LUMA + CVBS
  - EuroSCART Output RGB + CHROMA + LUMA + CVBS
- Programmable Clamping Output Signal
- Advanced Programmable Power-On Reset Sequencing
- Video Input Data Port Supports:
  - CCIR-656 4:2:2 8-Bit Parallel Input Format
  - SMPTE 170M NTSC-Compatible Composite Video
  - ITU-R BT.470 PAL-Compatible Composite Video
- Luma Sharpness Control
- Programmable Luma Filters (Low-Pass [PAL/NTSC], Notch [PAL/NTSC], Extended [SSAF], CIF and QCIF)
- Programmable Chroma Filters (Low-Pass [0.65 MHz, 1.0 MHz, 1.2 MHz and 2.0 MHz], CIF and QCIF)
- Programmable VBI (Vertical Blanking Interval)
- Programmable Subcarrier Frequency and Phase
- Programmable LUMA Delay
- CCIR and Square Pixel Operation
- Integrated Subcarrier Locking to External Video Source
- Color Signal Control/Burst Signal Control
- Interlaced/Noninterlaced Operation
- Complete On-Chip Video Timing Generator
- Programmable Multimode Master/Slave Operation
- Macrovision Antitaping Rev 7.1 (ADV7172 Only)[2]
- Closed Captioning Support
- Teletext Insertion Port (PAL-WST)
- On-Board Color Bar Generation
- On-Board Voltage Reference
- 2-Wire Serial MPU Interface (I²C®-Compatible and Fast I²C)
- Single Supply 5 V or 3.3 V Operation
- Small 48-Lead LQFP Package

APPLICATIONS

- High Performance DVD Playback Systems, Portable Video Equipment including Digital Still Cameras and Laptop PCs, Video Games, PC Video/Multimedia and Digital Satellite/Cable Systems (Set-Top Boxes/IRD)

GENERAL DESCRIPTION

The ADV7172/ADV7173 is an integrated Digital Video Encoder that converts digital CCIR-601 4:2:2 8-bit component video data into a standard analog baseband television signal compatible with worldwide standards.

There are six DACs available on the ADV7172/ADV7173. In addition to the Composite output signal there is the facility to output S-VHS Y/C Video, RGB Video and YUV Video.

The on-board SSAF (Super Sub-Alias Filter), with extended luminance frequency response and sharp stopband attenuation, enables studio quality video playback on modern TVs, giving optimal horizontal line resolution. An additional sharpness control feature allows extra luminance boost on the frequency response.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes and power down or sleep modes. A PC'98-Compliant autodetect feature has been added to allow the user to determine whether or not the DACs are correctly terminated. If not, the ADV7172/ADV7173 flags that they are not connected through the Status bit and provides the option of automatically powering them down, thereby reducing power consumption.

The ADV7172/ADV7173 also supports both PAL and NTSC square pixel operation. The parts also incorporate WSS and CGMS-A data control generation.

NOTES

[1]ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).
[2]The Macrovision anticopy process is licensed for noncommercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available.
SSAF is a trademark of Analog Devices, Inc.
I²C is a registered trademark of Philips Corporation.

REV. B

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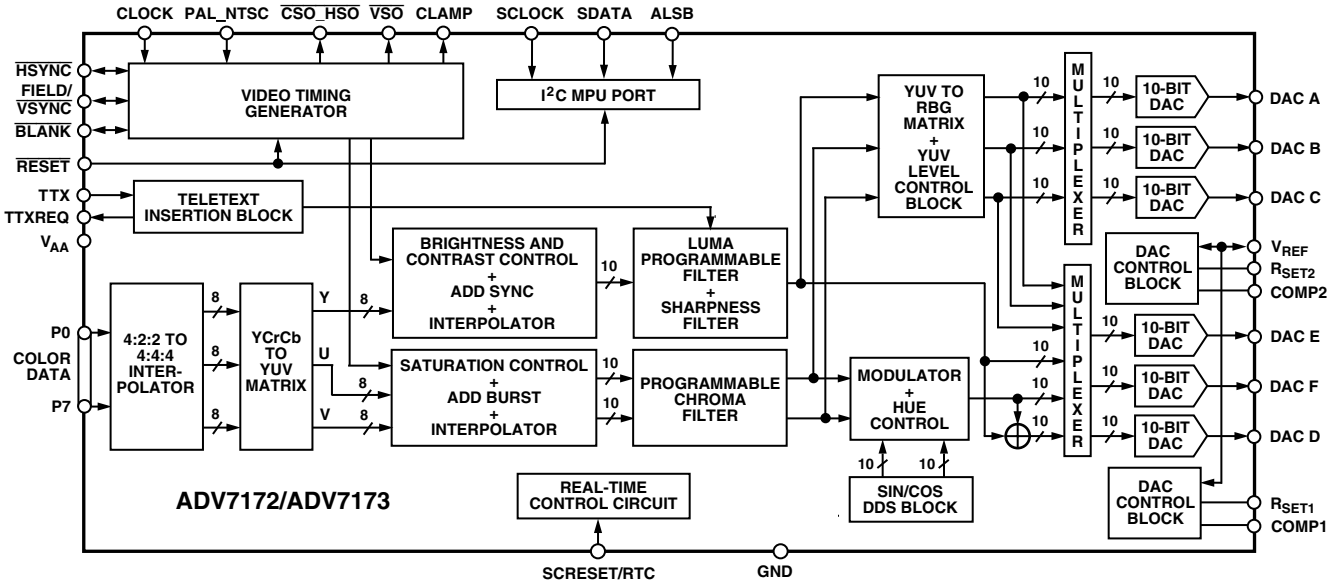
FUNCTIONAL BLOCK DIAGRAM



The ADV7172/ADV7173 is designed with four color controls (hue, contrast, brightness and saturation). All YUV formats (SMPTE/EBU N10, MII and Betacam) are supported in both PAL and NTSC.

The output video frames are synchronized with the incoming data Timing Reference Codes. Optionally the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD timing signals. These timing signals can be adjusted to change pulsewidth and position while the part is in the master mode. The Encoder requires a single two times pixel rate (27 MHz) clock for standard operation. Alternatively the Encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

HSO/CSO and VSO TTL outputs, synchronous to the analog output video, are also available. A programmable CLAMP output signal is also available to enable clamping in either the front or back porch of the video signal.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7172/ADV7173 modes are set up over a 2-wire serial bidirectional port (I^2C-Compatible) with two slave addresses. Functionally the ADV7173 and ADV7172 are the same with the exception that the ADV7172 can output the Macrovision anti-copy algorithm.

The ADV7172/ADV7173 is packaged in a 48-lead LQFP package (1.4 mm thickness).

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, M, N, and NTSC M, N modes, YCrCb 4:2:2 Data is input via the CCIR-656-Compatible Pixel Port at a 27 MHz Data Rate. The Pixel Data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, Cr, and Cb typically have a range of 128 ± 112; however, it is possible to input data from 1 to 254 on both Y, Cb, and Cr. The ADV7172/ADV7173 supports PAL (B, D, G, H, I, N, M) and NTSC (with and without pedestal) standards. The Y data is then manipulated by being scaled for contrast control and a setup level is added for brightness control. The Cr, Cb data is also scaled and saturation control is added. The appropriate Sync, Blank and Burst levels are then added to the YCrCb data. Macrovision AntiTaping (ADV7172 only), Closed-Captioning and Teletext levels are also added to Y, and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR Filters.

The U and V Signals are modulated by the appropriate subcarrier sine/cosine phases and a phase offset may be added onto the color subcarrier during active video to allow hue adjustment. The resulting U and V signals are then added together to make up the chrominance signal. The luma (Y) signal can be delayed 1–3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate Sync and Blank levels.

There are six DACs on the ADV7172/ADV7173. Three of these DACs are capable of providing 34.66 mA of current. The other three DACs provide 8.66 mA each.

The six l0-bit DACs can be used to output:

1. Composite Video + RGB Video + LUMA + CHROMA.
2. Composite Video + YUV Video + LUMA + CHROMA.

Alternatively, each DAC can be individually powered off if not required. A complete description of DAC output configurations is given in Appendix 8.

Video output levels are illustrated in Appendix 6.

SPECIFICATIONS

5 V SPECIFICATIONS (V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Test Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity[3]				±1.0	LSB
Differential Nonlinearity[3]	Guaranteed Monotonic			±1.0	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current (DACs A, B, C)[4]	R_{SET1} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current (DACs A, B, C)[5]	R_{SET1} = 1041 Ω, R_L = 262.5 Ω		5		mA
Output Current (DACs D, E, F)[6]	R_{SET2} = 600 Ω, R_L = 150 Ω	8.25	8.66	9.25	mA
Output Current (DACs D, E, F)[5]	R_{SET2} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching (DACs A, B, C)[7]			1	4.0	%
DAC-to-DAC Matching (DACs D, E, F)[7]			1	4.0	%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.112	1.235	1.359	V
POWER REQUIREMENTS					
V_{AA}		4.75	5.0	5.25	V
Normal Power Mode					
I_{DAC} (max)[8, 9]	$R_{SET1,2}$ = 600 Ω		59	65	mA
I_{DAC} (min)[8, 9]	$R_{SET1,2}$ = 1041 Ω		30		mA
I_{CCT}[10]			78	90	mA
Low Power Mode					
I_{DAC} (max)[11]	R_{SET1} = 150 Ω		64		mA
I_{DAC} (min)[11]			15		mA
I_{CCT}[10]			78	90	mA
Sleep Mode					
I_{DAC}[12]			0.1		μA
I_{CCT}[13]			0.1		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Characterized by design.

[4]Full drive into 75 Ω doubly terminated load.

[5]Minimum drive current (used with buffered/scaled output load).

[6]Full drive into 150 Ω load.

[7]Specification guaranteed by characterization.

[8]I_{DAC} is the total current (*"min" corresponds to 5 mA output per DAC, "max" corresponds to 8.66 mA output per DAC*) to drive DACs A, B, C, D, E, F. Turning off individual DACs reduces I_{DAC} correspondingly, also DACs A, B, C can be configured to output a max current of 37 mA but DAC D, E, F must be turned off.

[9]All six DACs on (DAC A, B, C, D, E, F).

[10]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[11]Only large DACs (DACs A, B, C) on per low power mode.

[12]Total DAC current in Sleep Mode.

[13]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

ADV7172/ADV7173–SPECIFICATIONS

3.3 V SPECIFICATIONS (V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Test Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				1.0	LSB
Differential Nonlinearity	Guaranteed Monotonic			1.0	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}			2		V
Input Low Voltage, V_{INL}			0.8		V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA		2.4		V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA		0.4		V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current (DACs A, B, C)[4]	R_{SET1} = 150 Ω, R_L = 37.5 Ω		34.7		mA
Output Current (DACs A, B, C)[5]	R_{SET1} = 1041 Ω, R_L = 262.5 Ω		5		mA
Output Current (DACs D, E, F)[6]	R_{SET2} = 600 Ω, R_L = 150 Ω		8.66		mA
Output Current (DACs D, E, F)[5]	R_{SET2} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching (DACs A, B, C)[3]			1	4.0	%
DAC-to-DAC Matching (DACs D, E, F)[3]			1	4.0	%
Output Compliance, V_{OC}				1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 7]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (max)[8, 9]	$R_{SET1,2}$ = 600 Ω		58	65	mA
I_{DAC} (min)[8]	$R_{SET1,2}$ = 1041 Ω		30		mA
I_{CCT}[10]			40		mA
Sleep Mode					
I_{DAC}[11]			0.1		μA
I_{CCT}[12]			0.1		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01		%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Guaranteed by characterization.

[4]Full drive into 75 Ω doubly terminated load.

[5]Minimum drive current (used with buffered/scaled output load).

[6]Full Drive into 150 Ω load.

[7]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.

[8]I_{DAC} is the total current (*"min" corresponds to 5 mA output per DAC, "max" corresponds to 8.66 mA output per DAC*) to drive DACs A, B, C, D, E, F. Turning off individual DACs reduces I_{DAC} correspondingly, also DACs A, B, C can be configured to output a max current of 37 mA.

[9]DACs A, B, C can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 37.5 Ω), optimum performance obtained at 18 mA DAC Current (R_{SET} = 300 Ω and R_L = 75 Ω).

[10]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[11]Total DAC current in Sleep Mode.

[12]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

5 V DYNAMIC SPECIFICATIONS

(V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3, 4]	Normal Power Mode		0.3	0.7	%
Differential Phase[3, 4]	Normal Power Mode		0.4	0.7	Degrees
Differential Gain[3, 4]	Lower Power Mode		0.5	1.0	%
Differential Phase[3, 4]	Lower Power Mode		2.0	3.0	Degrees
SNR[3, 4] (Pedestal)	RMS		75		dB rms
SNR[3, 4] (Pedestal)	Peak Periodic		66		dB p-p
SNR[3, 4] (Ramp)	RMS		60		dB rms
SNR[3, 4] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3, 4]			0.7		Degrees
Color Saturation Accuracy[3, 4]			0.9		%
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		1.2		±%
Chroma Nonlinear Phase[3, 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%
Chroma/Luma Gain Inequality[3, 4]			1.0		±%
Chroma/Luma Delay Inequality[3, 4]			0.5		ns
Luminance Nonlinearity[3, 4]			1.0	1.7	±%
Chroma AM Noise[3, 4]		79	82		dB
Chroma PM Noise[3, 4]		79	80		dB

NOTES
[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]These specifications are for the low-pass filter only and guaranteed by design.
[4]Guaranteed by characterization.

Specifications subject to change without notice.

3.3 V DYNAMIC SPECIFICATIONS

(V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3]	Normal Power Mode		0.6		%
Differential Phase[3]	Normal Power Mode		0.5		Degrees
Differential Gain[3]	Lower Power Mode		1.0		%
Differential Phase[3]	Lower Power Mode		0.5		Degrees
SNR[3] (Pedestal)	RMS		75		dB rms
SNR[3] (Pedestal)	Peak Periodic		70		dB p-p
SNR[3] (Ramp)	RMS		60		dB rms
SNR[3] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3]			1.0		Degrees
Color Saturation Accuracy[3]			1.0		%
Luminance Nonlinearity[3]			1.1		±%
Chroma AM Noise[3]			83		dB
Chroma PM Noise[3]			79		dB
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		1.2		±%
Chroma Nonlinear Phase[3, 4]			0.3		±Degrees
Chroma/Luma Intermod[3, 4]			0.2		±%

NOTES
[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Guaranteed by characterization.
[4]These specifications are for the low-pass filter only and guaranteed by design.

Specifications subject to change without notice.

ADV7172/ADV7173

5 V TIMING SPECIFICATIONS (V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET1} = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			µs
SCLOCK Low Pulsewidth, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the 1st clock is generated	0.6			µs
Setup Time (Start Condition), t_4	relevant for repeated Start Condition.	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		4.0			ns
Data Hold Time, t_{12}		5.0			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			15	24	ns
Digital Output Hold Time, t_{14}			10		ns
Pipeline Delay, t_{15}			37		Clock Cycles
TELETEXT PORT[3, 7]					
Digital Output Access Time, t_{16}			20		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3]					
$\overline{\text{RESET}}$ Low Time			3		ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs: P7–P0

Pixel Controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSO}}$, $\overline{\text{CSO\_HSO}}$, CLAMP

Clock Input: CLOCK

[7]Teletext Port consists of the following:

Teletext Output: TTXREQ

Teletext Input: TTX

Specifications subject to change without notice.

3.3 V TIMING SPECIFICATIONS (V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			µs
SCLOCK Low Pulsewidth, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the 1st clock is generated	0.6			µs
Setup Time (Start Condition), t_4	relevant for repeated Start Condition.	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		4.0			ns
Data Hold Time, t_{12}		5			ns
Control Setup Time, t_{11}		5			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			20		ns
Digital Output Hold Time, t_{14}			12		ns
Pipeline Delay, t_{15}			37		Clock Cycles
TELETEXT PORT[3, 4, 7]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time			3		ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs:	P7–P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSO}}$, $\overline{\text{CSO\_HSO}}$, CLAMP
Clock Input:	CLOCK

[7]Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

Specifications subject to change without notice.

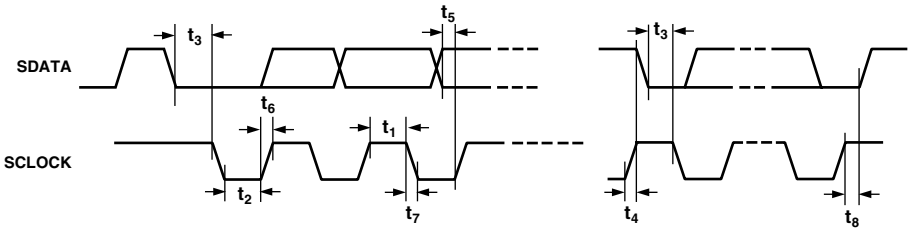


Figure 1. MPU Port Timing Diagram

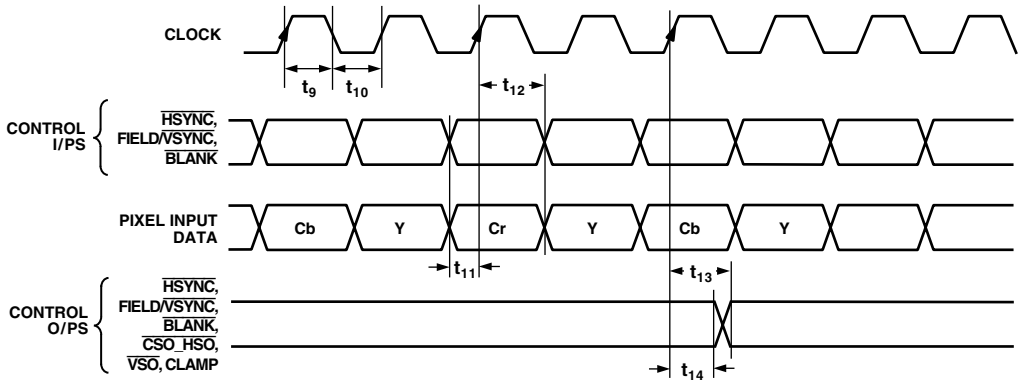


Figure 2. Pixel and Control Data Timing Diagram

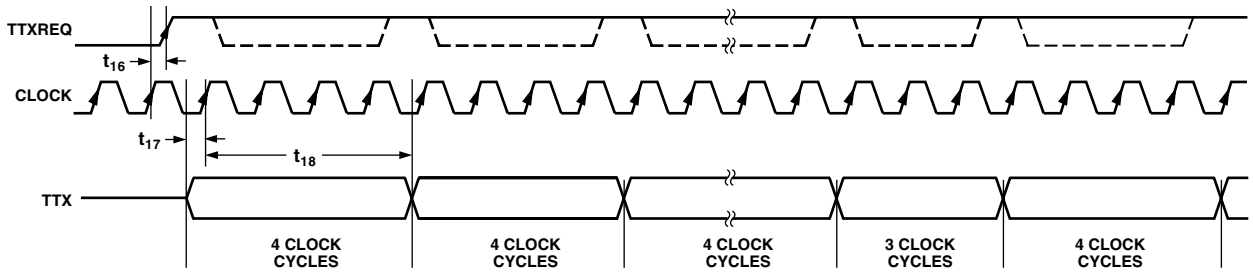


Figure 3. Teletext Timing Diagram

DAC Average Current Consumption

DAC D, E, F: The average current consumed by each DAC is the DAC output current as determined by R_{SET2}/V_{REF} (see Appendix 8).

DAC A, B, C: In *normal power mode* the average current consumed by each DAC is the DAC output current as determined by R_{SET1} (see Appendix 8).

In *Low Power Mode* the average current consumed by each DAC is approximately half the DAC output current as determined by R_{SET1}.

Consult AN-551 for detailed information on ADV7172/ADV7173 power management.

ABSOLUTE MAXIMUM RATINGS[1]

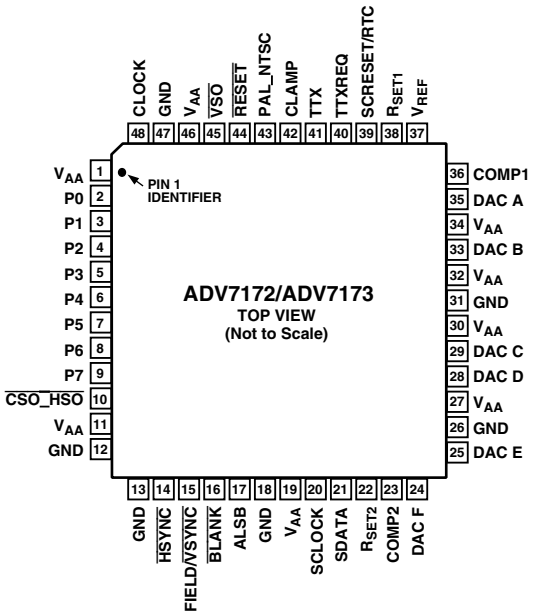
V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Input Pin . GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Lead Temperature (Soldering, 10 sec) . . . . . 260°C
Analog Outputs to GND[2] . . . . . GND – 0.5 V to V_{AA}

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

PIN CONFIGURATION



PACKAGE THERMAL PERFORMANCE

The 48-lead LQFP package is used for this device. The junction-to-ambient (θ_{JA}) thermal resistance in still air on a four layer PCB is 54.6°C/W. The junction-to-case thermal resistance (θ_{JC}) is 16.7°C.

To reduce power consumption when using this part the user is advised to run the part on a 3.3 V supply, turn off any unused DACs. However, if 5 V operation is required the user can enable Low Power mode by setting MR16 to a Logic 1. Another alternative way to further reduce power is to use external buffers that dramatically reduce the DAC currents, the current can be lowered to as low as 5 mA (see AN-551 and Appendix 8 for more details) from a nominal value of 36 mA.

The user must at all times stay below the maximum junction temperature of 110°C. The following equation shows how to calculate this junction temperature:

$$Junction\ Temperature = [V_{AA}\ (I_{DAC} + I_{CCT}) \times \theta_{JA}\ ]\ 70°C$$

where

I_{DAC} = 10 mA + (sum of the average currents consumed by each powered-on DAC).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7172KST	0°C to 70°C	Plastic Thin Quad Flatpack	ST-48
ADV7173KST	0°C to 70°C	Plastic Thin Quad Flatpack	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7172/ADV7173 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Mnemonic	Input/Output	Function
P7–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or as an input and accept (Slave Mode) Sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or as an input (Slave Mode) and accept these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level "0." This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR42 and MR41 of Mode Register 4. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier phase to Field 0. Alternatively it may be configured as a Real-Time Control (RTC) Input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET1}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs A, B, and C (the "large" DACs).
R_{SET2}	I	A 600 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs D, E, and F (the "small" DACs).
COMP1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 μF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in Low Power Mode, the value of the COMP1 capacitor can be lowered to as low as 2.2 nF.
COMP2	O	Compensation Pin for DACs D, E, and F. Connect a 0.1 μF Capacitor from COMP to V_{AA}.
DAC A	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 34.66 mA output.
DAC B	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 34.66 mA output.
DAC C	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 34.66 mA output.
DAC D	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 8.66 mA output.
DAC E	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 8.66 mA output.
DAC F	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 8.66 mA output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
CLAMP	O	TTL Output Signal to external circuitry to enable clamping of all video signals.
PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic "1" selects PAL.
$\overline{\text{VSO}}$	O	$\overline{\text{VSO}}$ TTL Output Sync Signal.
$\overline{\text{CSO\_HSO}}$	O	Dual Function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ TTL Output Sync Signal.
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7172/ADV7173 into default mode. This is NTSC operation, Timing Slave Mode 0, DACs A, B, and C powered OFF, DACs D, E, and F powered ON, Composite and S-Video out.
TTX	I	Teletext Data Input Pin.
TTXREQ	O	Teletext Data Request output signal used to control teletext data transfer.
V_{AA}	P	Power Supply (3 V to 5 V).
GND	G	Ground Pin.

(*continued from page 2*)

INTERNAL FILTER RESPONSE

The Y Filter supports several different frequency responses, including two low-pass responses, two notch responses, an Extended (SSAF) response with or without gain boost/attenuation, a CIF response and a QCIF response. The UV Filter supports several different frequency responses, including four low-pass responses, a CIF response and a QCIF response. These can be seen in Figures 4 to 18.

In Extended Mode there is the option of twelve responses in the range from –4 dB to +4 dB. The desired response can be chosen by the user by programming the correct value via the I^2C. The variation of frequency responses can be seen in Figures 19 to 21.

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR04	MR03	MR02				
LOW-PASS (NTSC)	0	0	0	0.091	4.157	7.37	–56
LOW-PASS (PAL)	0	0	1	0.15	4.74	7.96	–64
NOTCH (NTSC)	0	1	0	0.015	6.54	8.3	–68
NOTCH (PAL)	0	1	1	0.095	6.24	8.0	–66
EXTENDED (SSAF)	1	0	0	0.051	6.217	8.0	–61
CIF	1	0	1	0.018	3.0	7.06	–61
QCIF	1	1	0	MONOTONIC	1.5	7.15	–50

Figure 4. Luminance Internal Filter Specifications

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR07	MR06	MR05				
1.3MHz LOW PASS	0	0	0	0.084	1.395	3.01	–45
0.65MHz LOW PASS	0	0	1	MONOTONIC	0.65	3.64	–58.5
1.0MHz LOW PASS	0	1	0	MONOTONIC	1.0	3.73	–49
2.0MHz LOW PASS	0	1	1	0.0645	2.2	5.0	–40
RESERVED	1	0	0				
CIF	1	0	1	0.084	0.7	3.01	–45
QCIF	1	1	0	MONOTONIC	0.5	4.08	–50

Figure 5. Chrominance Internal Filter Specifications

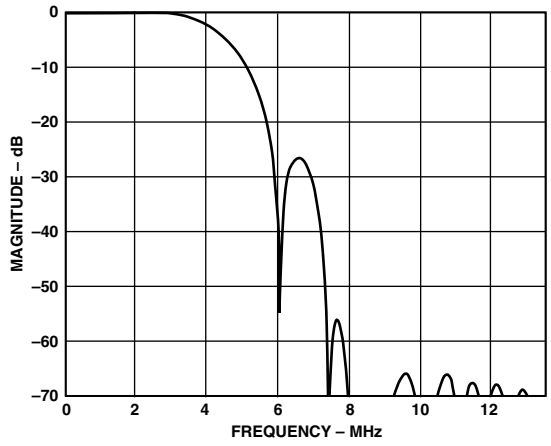


Figure 6. NTSC Low-Pass Luma Filter

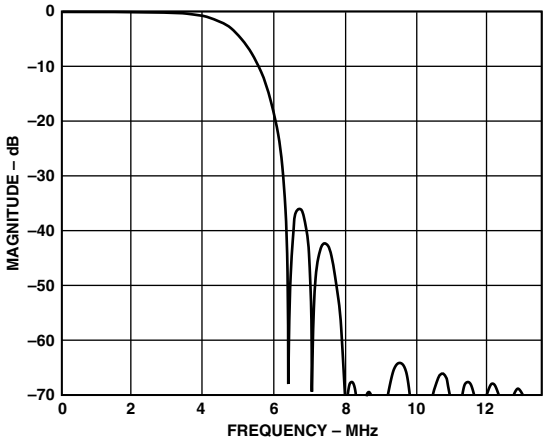


Figure 7. PAL Low-Pass Luma Filter

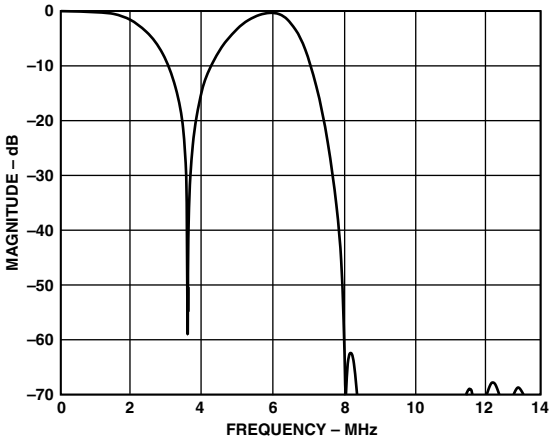


Figure 8. NTSC Notch Luma Filter

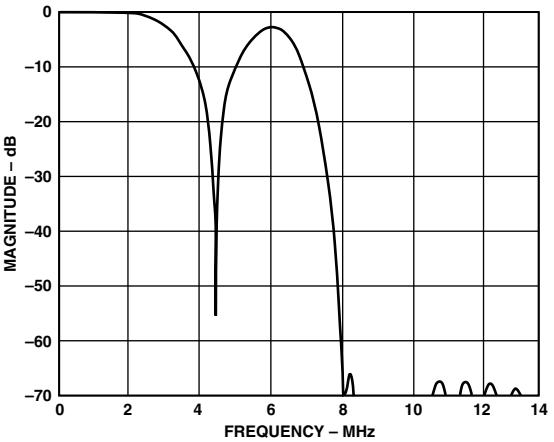


Figure 9. PAL Notch Luma Filter

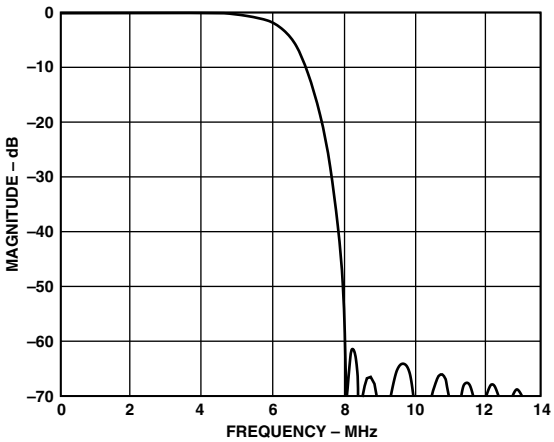


Figure 10. Extended Mode (SSAF) Luma Filter

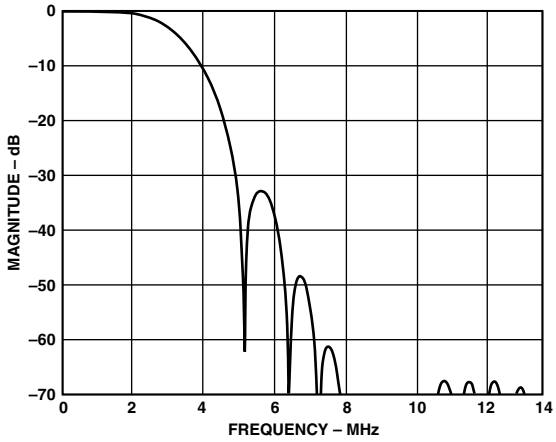


Figure 11. CIF Luma Filter

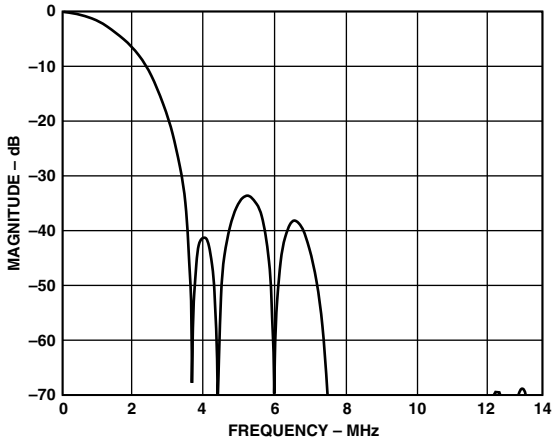


Figure 12. QCIF Luma Filter

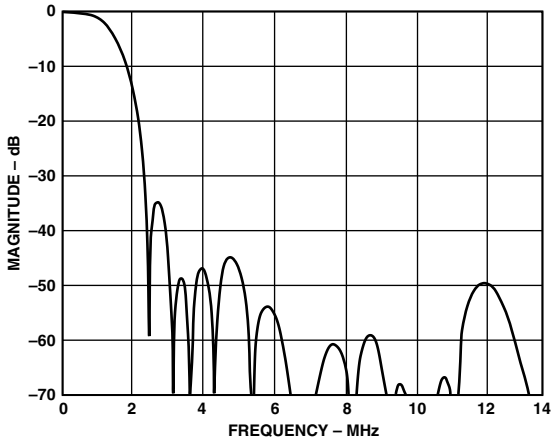


Figure 13. 1.3 MHz Low-Pass Chroma Filter

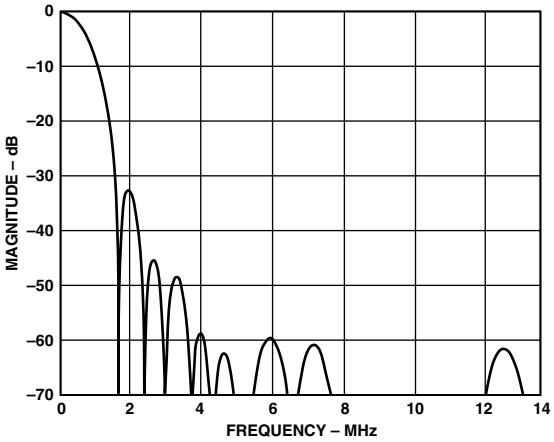


Figure 14. 0.65 MHz Low-Pass Chroma Filter

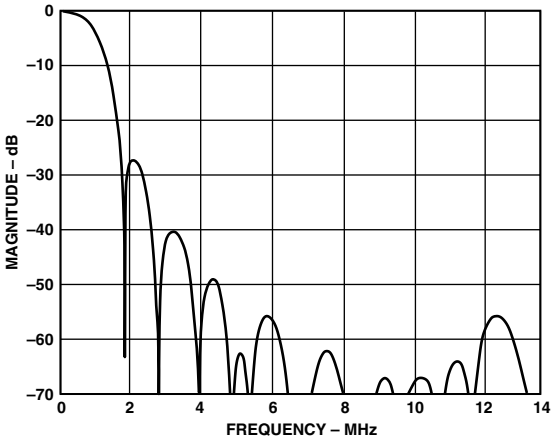


Figure 15. 1.0 MHz Low-Pass Chroma Filter

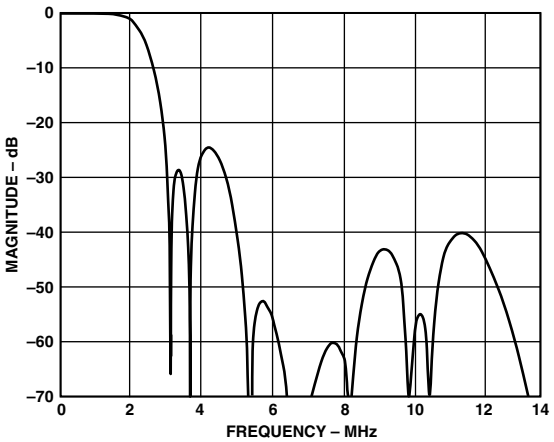


Figure 16. 2.0 MHz Low-Pass Chroma Filter

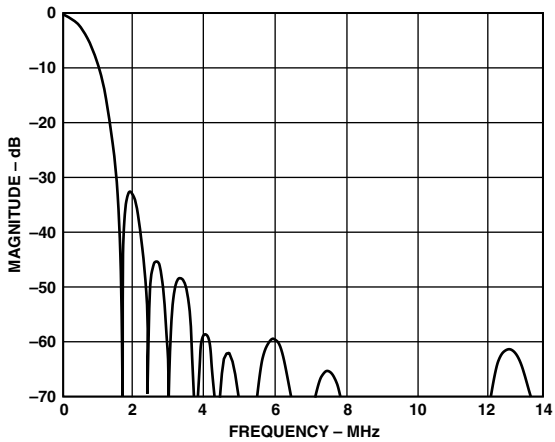


Figure 17. CIF Chroma Filter

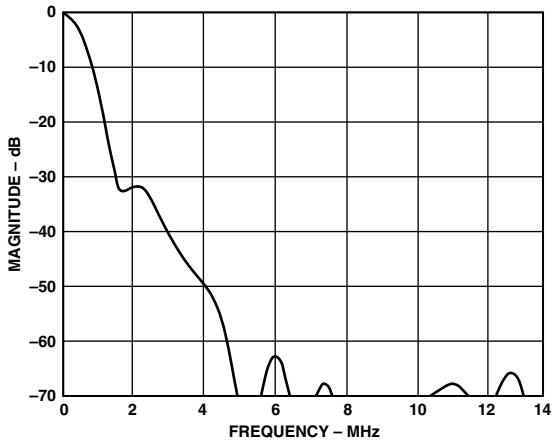


Figure 18. QCIF Chroma Filter

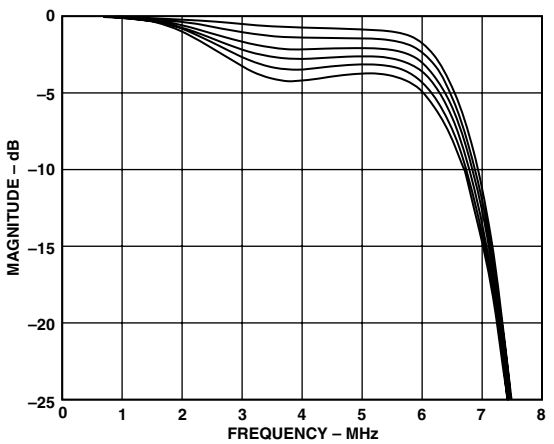


Figure 19. Extended Mode Luma Filter with Programmable Gain, Negative Response

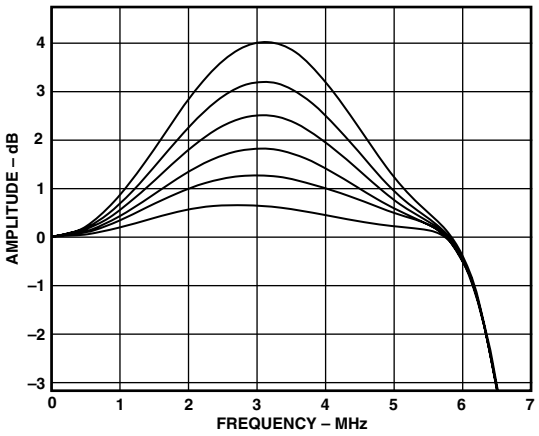


Figure 20. Extended Mode Luma Filter with Programmable Gain, Positive Response

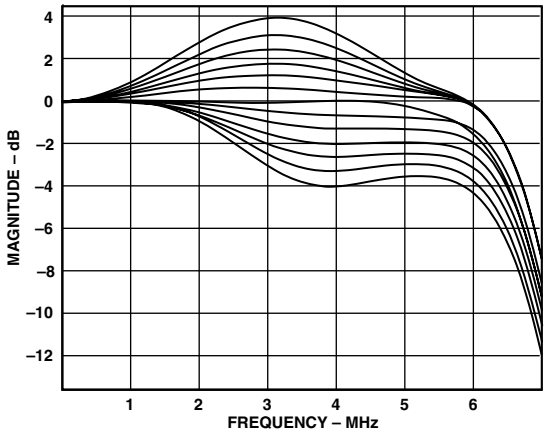


Figure 21. Extended Mode Luma Filter with Programmable Gain, Combined Response

COLOR BAR GENERATION

The ADV7172/ADV7173 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 color bars for PAL. These are enabled by setting MR46 of Mode Register 4 to Logic "1."

SQUARE PIXEL MODE

The ADV7172/ADV7173 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR44 of Mode Register 4.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR45 of Mode Register 4.

NTSC PEDESTAL CONTROL

The pedestal on both odd and even fields can be controlled on a line-by-line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the Vertical Blanking Interval.

COLOR CONTROLS

The ADV7172/ADV7173 allows the user the advantage of controlling the brightness, contrast, hue and saturation of the color.

Contrast Control

Contrast adjustment is achieved by scaling the Y input data by a factor programmed by the user into the Contrast Control Register Bits 5–0. This factor allows the data to be scaled between 75% and 125%.

Brightness Control

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the Y data in PAL mode, NTSC mode without pedestal or NTSC mode with pedestal, in which case it is added directly onto the 7.5 IRE pedestal already present.

The level added is programmed by the user into the Brightness Control Register (Bits 4–0) and the user is capable of adding from 0 IRE to a maximum of 14 IRE in 32 (2^5) steps. Because of different gains in the datapath for each mode, different values may need to be programmed to obtain the same IRE setup level in each mode. Maximum brightness is achieved when 31 is programmed into the Brightness Control Register. Table I illustrates the maximum setup/brightness amplitudes available in the various modes. Note that if a level of less than 7.5 IRE is required on the Y data in NTSC mode, then NTSC without pedestal must be the mode selected.

Table I. Maximum Brightness Levels Available

Mode	Brightness Control Register	Setup
NTSC No Pedestal	00011111	14 IRE
NTSC Pedestal	00011111	13 IRE
PAL	00011111	99 mV

Color Saturation Control

Color adjustment is achieved by scaling the Cr and Cb input data by a factor programmed by the user into the Color Control Registers 1 and 2, Bits 5–0. This factor allows the data to be scaled between 75% and 125%.

Hue Control

The hue adjustment is achieved on the composite and chroma outputs by adding a phase offset onto the color subcarrier in the active video but leaving the color burst unmodified, i.e., only the phase between the video and the color burst is modified and hence the hue is shifted. Hue adjustment is under the control of the Hue Control Register. The ADV7172/ADV7173 provides a range of ±22° change in increments of 0.17578125°.

YUV LEVELS

This functionality is under the control of Mode Register 5, Bits 2–0. Bit 0 (MR50) allows the ADV7172/ADV7173 to output SMPTE levels on the Y output when configured in NTSC mode, and Betacam levels on the Y output when configured in PAL mode and vice-versa.

	Video	Sync
Betacam	286 mV	714 mV
SMPTE	300 mV	700 mV
MII	300 mV	700 mV

As the datapath is branched at the output of the filters, the luma signal relating to the CVBS or S-Video Y/C output is unaltered. Only the Y output of the YUV outputs is scaled. Bits 2–1 (MR52–MR51) allow UV levels to have a peak-peak amplitude of 700 mV or 1000 mV, or the default values of 934 mV in NTSC and 700 mV in PAL.

AUTODETECT CONTROL

The ADV7172/ADV7173 provides the option of automatically powering down the DACs A, B and C if they are not correctly terminated (i.e., the 75 Ω cable is not connected to the DAC). The voltage at the output of DACs A and B are compared to a selected reference level. This reference voltage (MR64) will depend on whether the user terminates with 37.5 Ω (75 Ω connected on the DAC end and 75 Ω connected at TV end of cable, i.e., combined load of 37.5 Ω) or 75 Ω. It cannot operate in a DAC buffering configuration. There are two modes of autodetect operation provided by the ADV7172/ADV7173:

(1) Mode 0: The state of termination of the DAC may be read by reading the status bits in Mode Register 6. MR67 status bit indicates whether or not the composite DAC is terminated, MR66 status bit indicates whether or not the luma DAC is terminated. The user may then decide whether or not to power down the DACs using MR15–MR0.

(2) Mode 1: The state of the DACs may be read as in Mode 0. If either of the DACs is unterminated, they are automatically powered down. If the luma DAC, DAC B is powered down then DAC C, the chroma DAC, will also be powered down. The state of termination of the DAC is checked each frame to decide whether or not it is to be powered up or down.

Mode Register 6, Bits 3–2, indicates which mode of operation is used. Note that Mode Register 1, Bits 5-3, must be enabled ("1") for autodetect functionality to work. (DACs A, B, C are enabled.)

Vertical Blanking Data Insertion

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not have line sync or pre-/post-equalization pulses (see Figures 24 to 25). This mode of operation is called "Partial Blanking" and is selected by setting MR32 to "1." It allows the insertion of any VBI data (Opened VBI) into the encoded output waveform. This data is present in digitized incoming YCbCr data stream (e.g., WSS data, CGMS, VPS etc.). Alternatively the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR32 to "0."

SUBCARRIER RESET

Together with the SCRESET/RTC PIN and Bits MR42 and MR41 of Mode Register 4, the ADV7172/ADV7173 can be used in subcarrier reset mode. The subcarrier phase will reset to Field 0 at the start of the following field when a low to high transition occurs on this input pin.

REAL-TIME CONTROL

Together with the SCRESET/RTC PIN and Bits MR42 and MR41 of Mode Register 4, the ADV7172/ADV7173 can be used to lock to an external video source. The real-time control mode allows the ADV7172/ADV7173 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7185 video decoder, see Figure 22), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00Hex should be written into all four subcarrier frequency registers when using this mode.

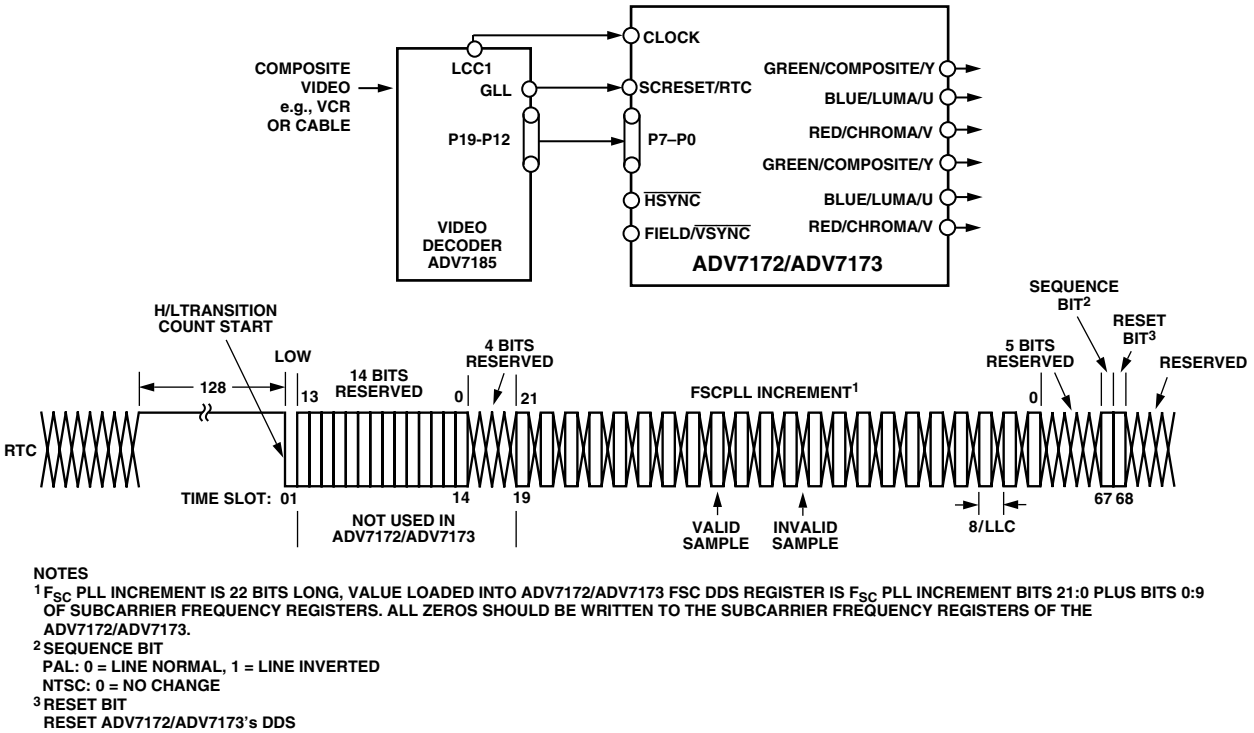
VIDEO TIMING DESCRIPTION

The ADV7172/ADV7173 is intended to interface to off-the-shelf MPEG1 and MPEG2 Decoders. As a consequence, the ADV7172/ADV7173 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 pixel port and has several video timing modes of operation that allow it to be configured as either system master video timing generator or a slave to the system video timing generator. The ADV7172/ADV7173 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7172/ADV7173 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalization pulses are inserted where required.

In addition, the ADV7172/ADV7173 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7172/ADV7173 has four distinct master and four distinct slave timing configurations. Timing control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulsewidths and where they occur in relation to each other.



NOTES
[1] F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7172/ADV7173 FSC DDS REGISTER IS F_{SC} PLL INCREMENT BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7172/ADV7173.
[2] SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
[3] RESET BIT
RESET ADV7172/ADV7173's DDS

Figure 22. RTC Timing and Connections

Mode 0 (CCIR–656): Slave Option
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7172/ADV7173 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data. All timing information is transmitted using a 4-byte Synchronization Pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 23. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

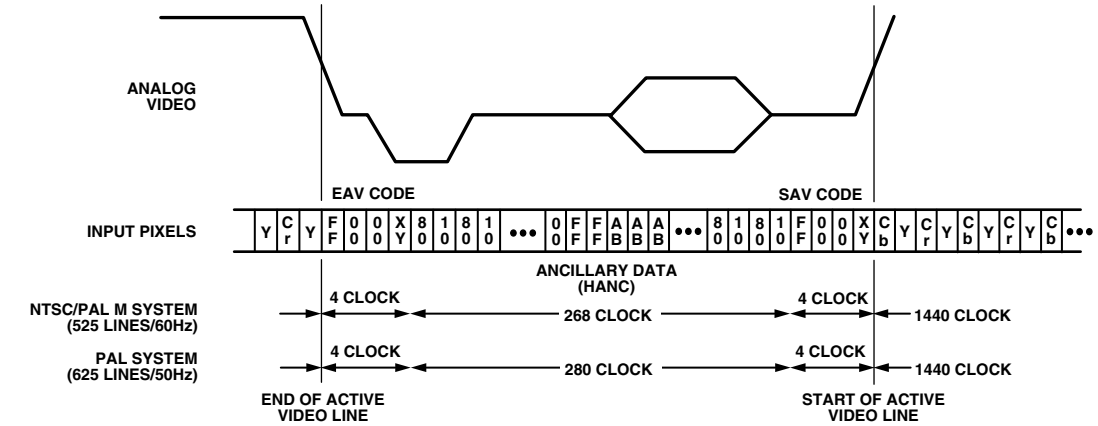


Figure 23. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR–656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7172/ADV7173 generates H, V, and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 26.

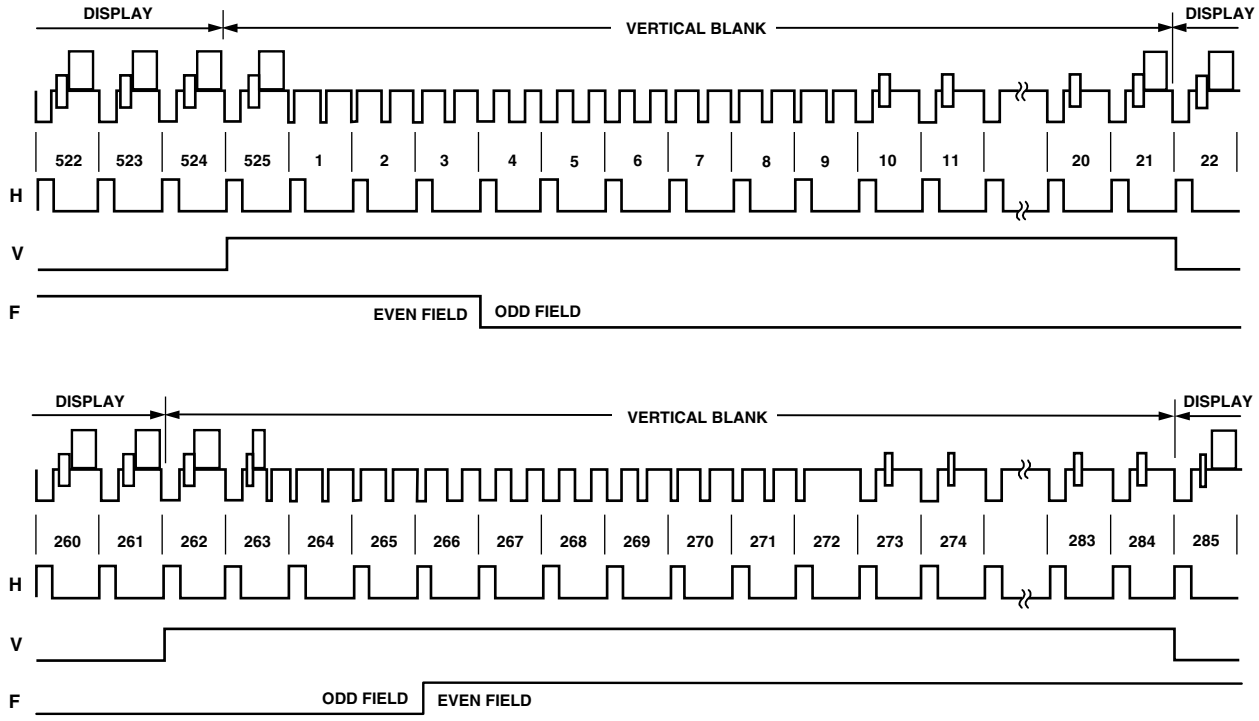


Figure 24. Timing Mode 0 (NTSC Master Mode)

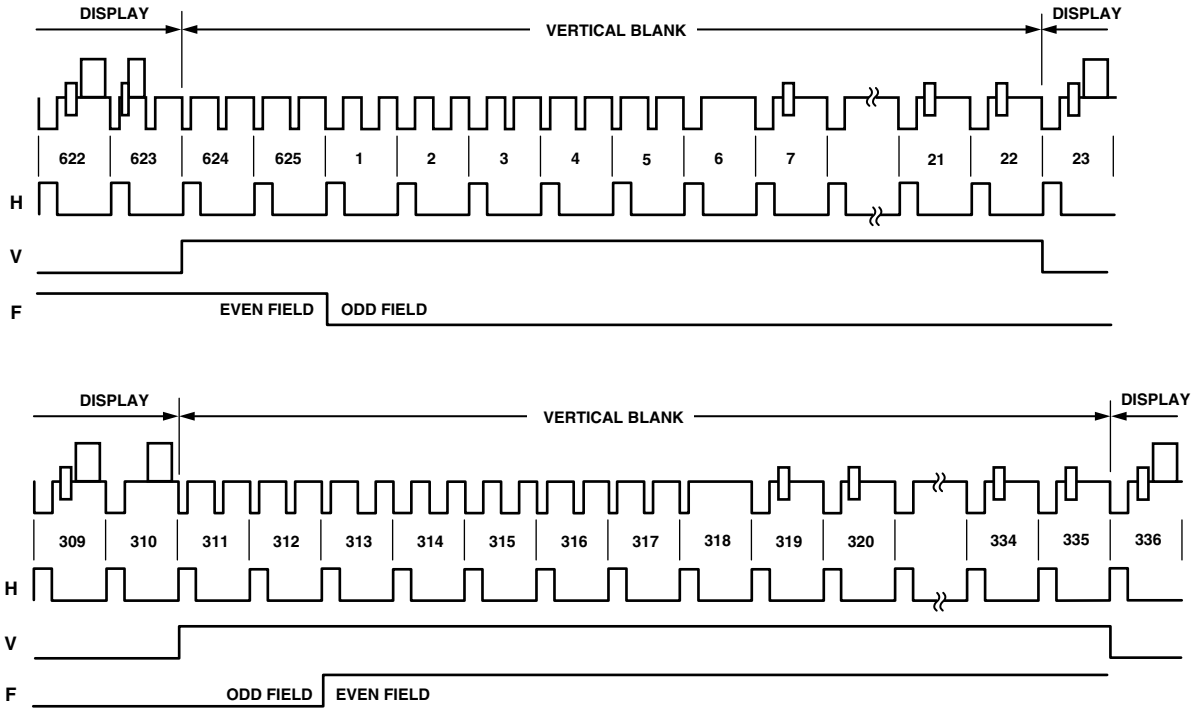


Figure 25. Timing Mode 0 (PAL Master Mode)

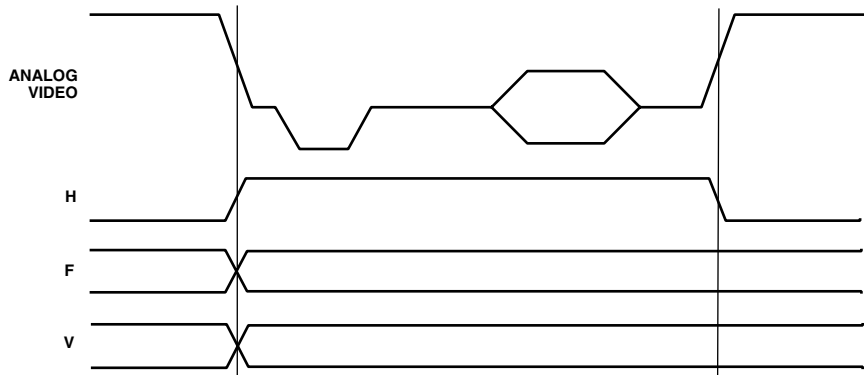


Figure 26. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7172/ADV7173 accepts horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL).

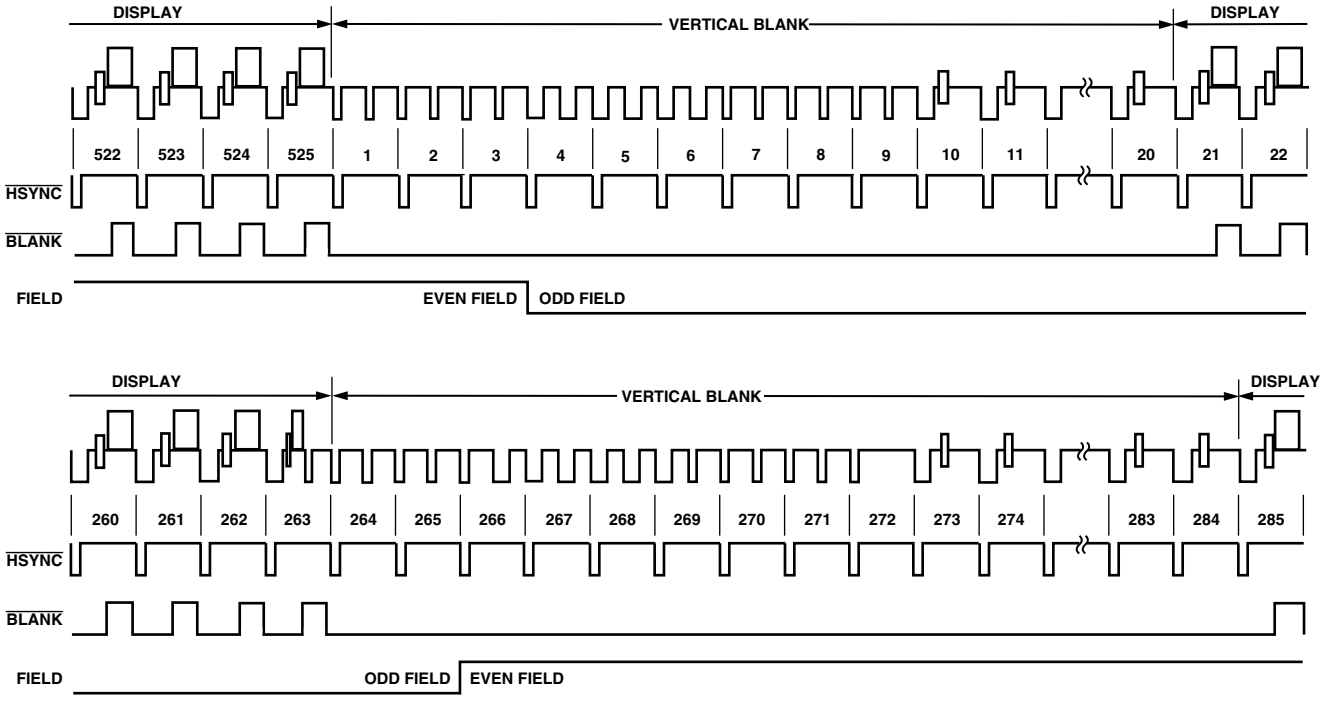


Figure 27. Timing Mode 1 (NTSC)

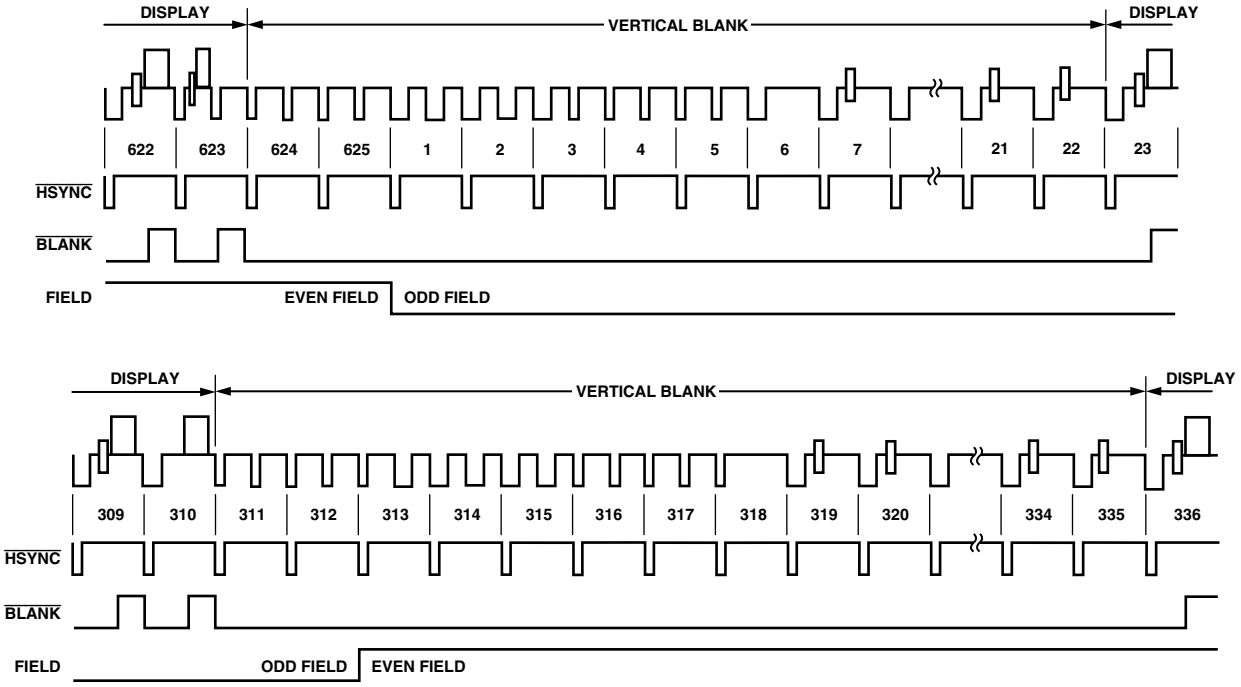


Figure 28. Timing Mode 1 (PAL)

Mode 1: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7172/ADV7173 can generate horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL). Figure 29 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD for an odd-or-even field transition relative to the pixel data.

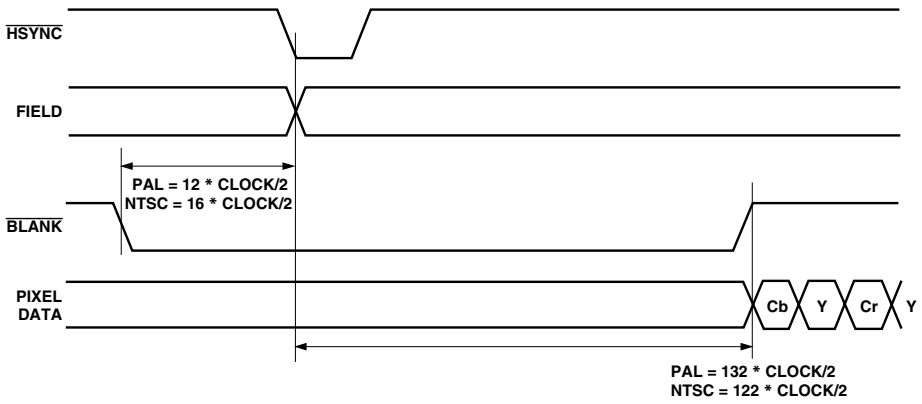


Figure 29. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7172/ADV7173 accepts horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an Even Field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 30 (NTSC) and Figure 31 (PAL).

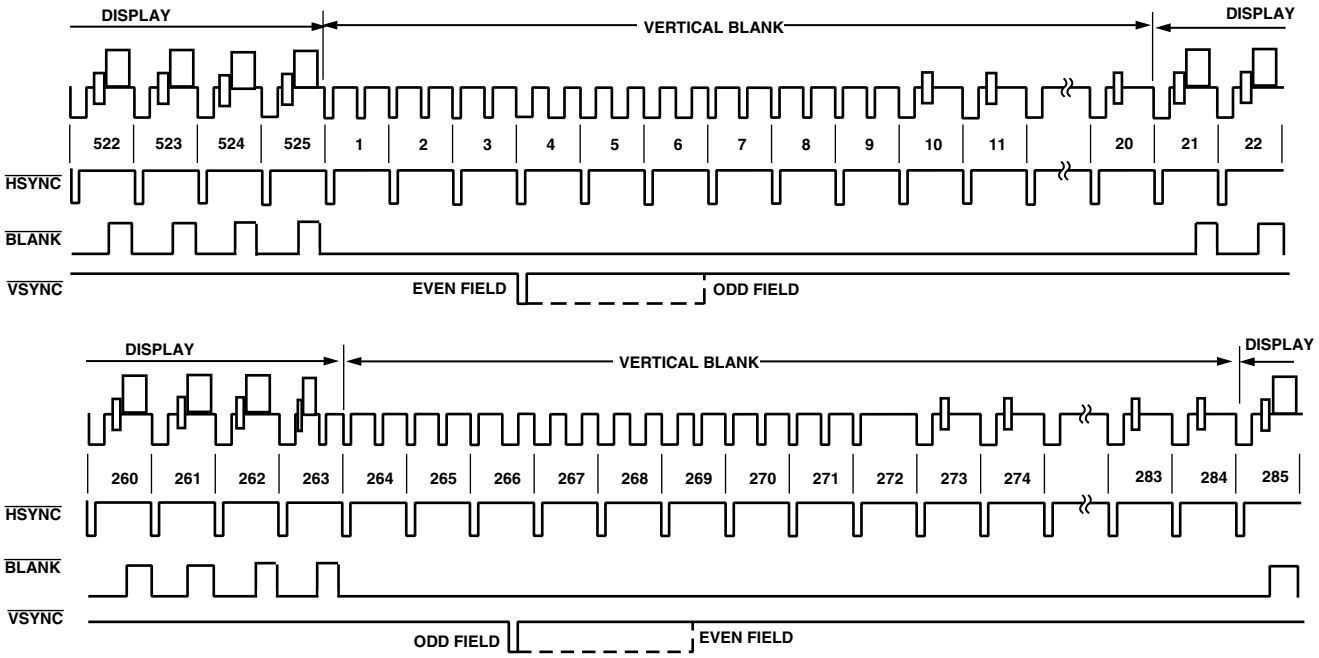


Figure 30. Timing Mode 2 (NTSC)

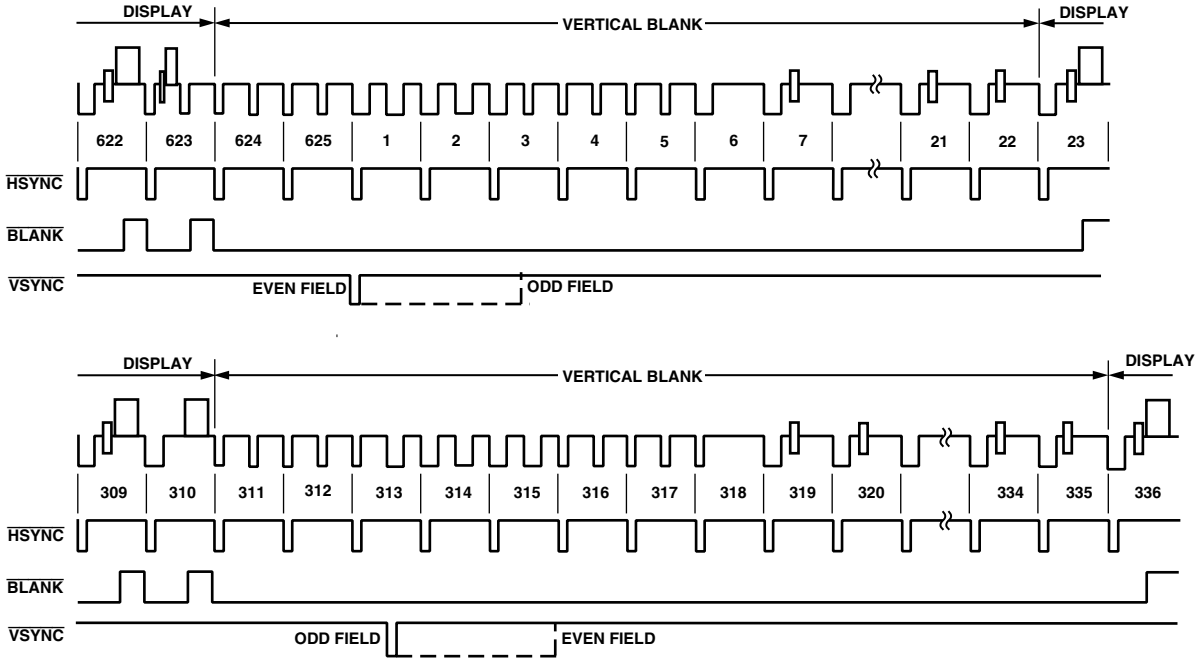


Figure 31. Timing Mode 2 (PAL)

Mode 2: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7172/ADV7173 can generate horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 30 (NTSC) and Figure 31 (PAL). Figure 32 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an even-to-odd field transition relative to the pixel data. Figure 33 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an odd-to-even field transition relative to the pixel data.

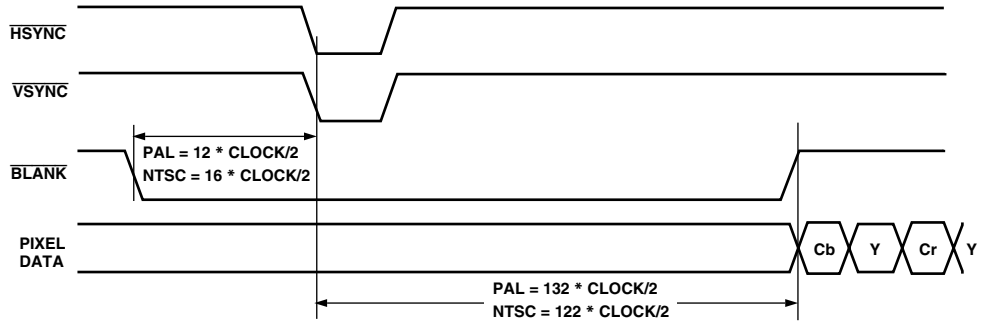


Figure 32. Timing Mode 2 Even-to-Odd Field Transition Master/Slave

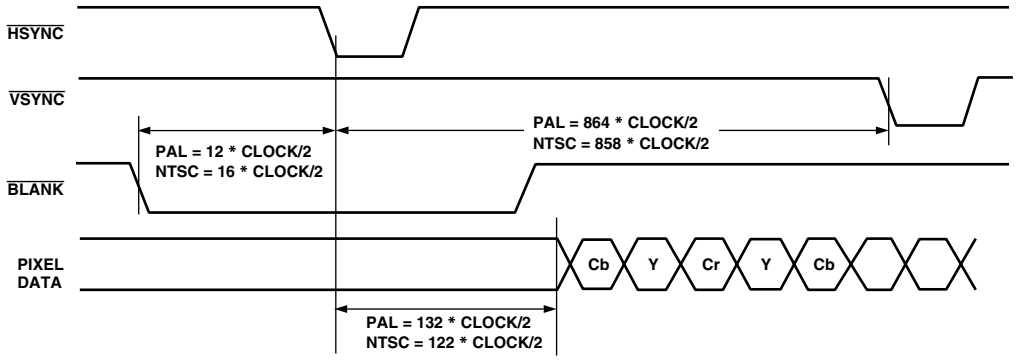


Figure 33. Timing Mode 2 Odd-to-Even Field Transition Master/Slave

Mode 3: Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7172/ADV7173 accepts or generates horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 34 (NTSC) and Figure 35 (PAL).

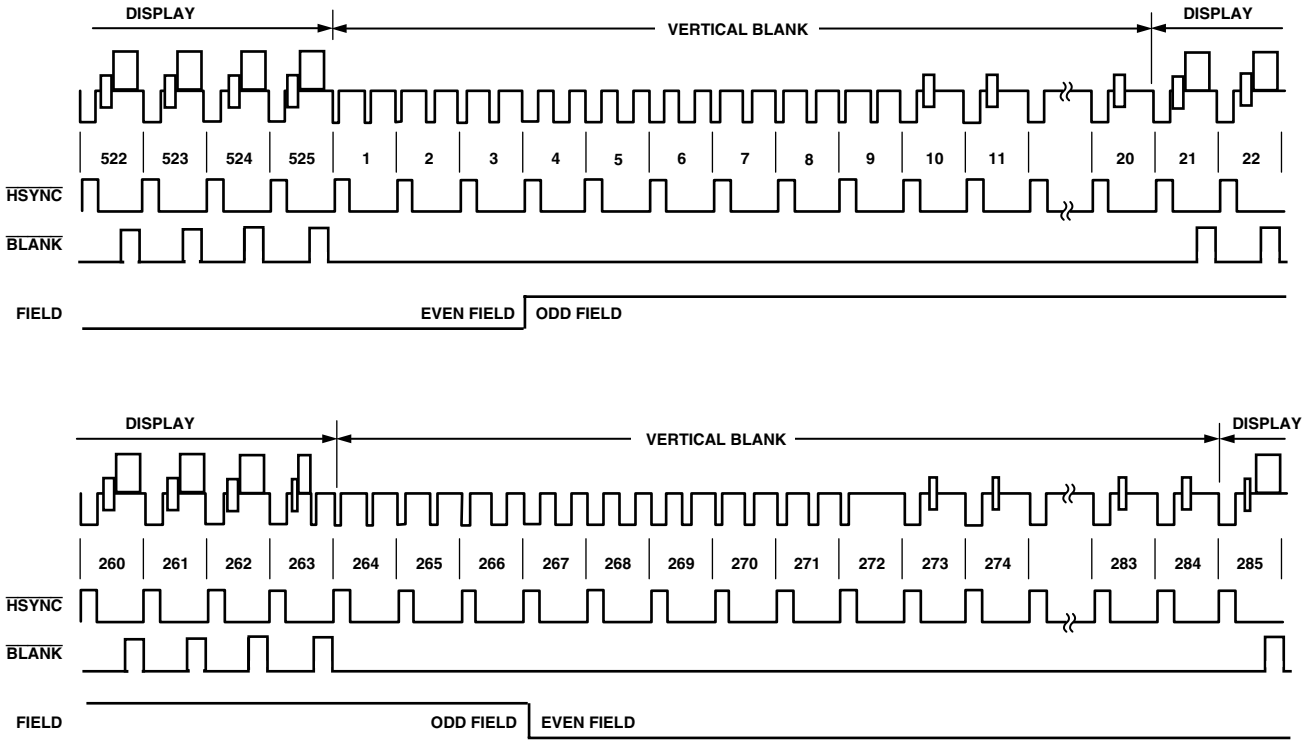


Figure 34. Timing Mode 3 (NTSC)

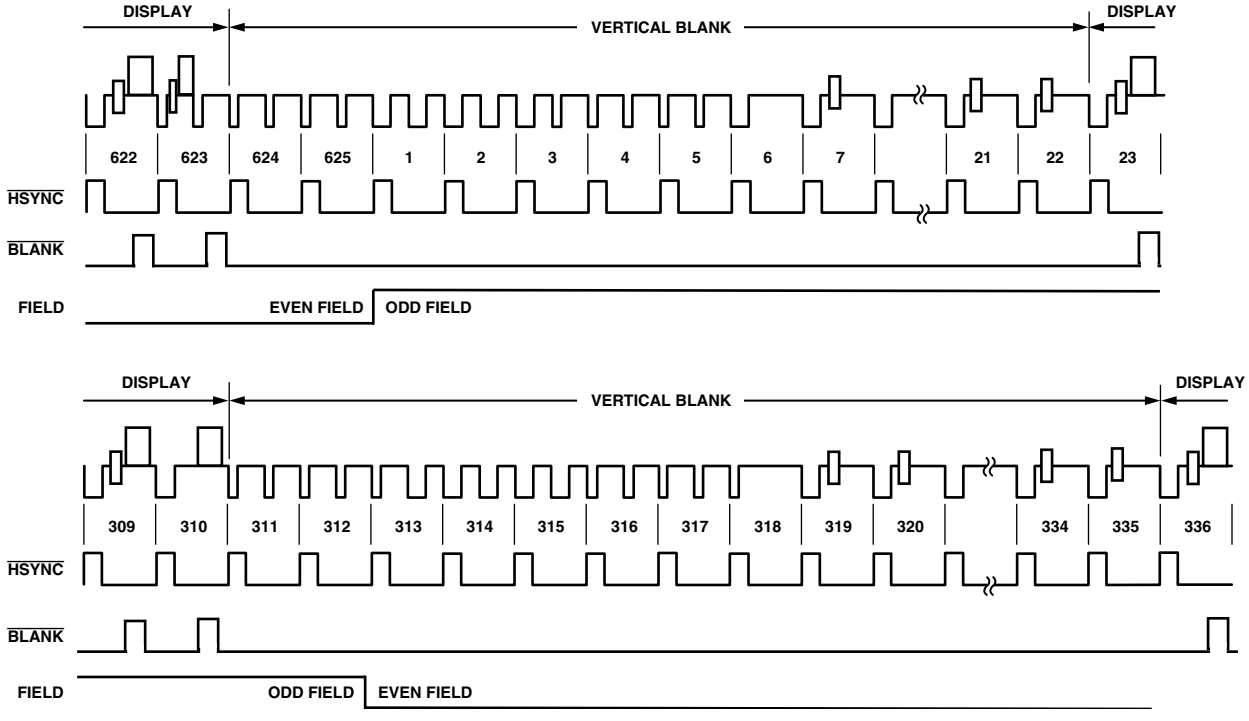


Figure 35. Timing Mode 3 (PAL)

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the pixel inputs P7–P0 are not selected. After reset, the ADV7172/ADV7173 is automatically set up to operate in NTSC/PAL mode, depending on the PAL_NTSC pin. The subcarrier frequency registers are automatically loaded with the correct values for PAL or NTSC. All other registers, with the exception of Mode Registers 1 and 2, are set to 00H. Mode Register 1 is set to 07H. This is to ensure DACs D, E, and F are ON after power-up. All bits of Mode Register 2 are set to "0," with the exception of Bit 3 (i.e., Mode Register 2 reads 08H). Bit MR23 of Mode Register 2 is set to Logic "1." This enables the 7.5 IRE pedestal.

RESET SEQUENCE

When $\overline{\text{RESET}}$ becomes active, the ADV7172/ADV7173 reverts to the default output configuration. DACs A, B, C are off and DACs D, E, F are powered on and output composite, luma and chroma signals respectively. Mode Register 2, Bit 6 (MR26), resets to "0." The ADV7172/ADV7173 internal timing is under the control of the logic level on the NTSC_PAL pin.

When $\overline{\text{RESET}}$ is released Y, Cr, Cb values corresponding to a black screen are input to the ADV7172/ADV7173. Output timing signals are still suppressed at this stage.

When the user requires valid data, MR26 is set to "1" to allow the valid pixel data to pass through the encoder. Digital output timing signals become active and the encoder timing is now under the control of the timing registers. If, at this stage, the user wishes to select a video standard different from that on the NTSC_PAL pin, Mode Register 2, Bit 5 (MR25) is set ("1") and the video standard required is selected by programming Mode Register 0. Figure 36 illustrates the reset sequence timing.

SLEEP MODE

If after reset the SCRESET/RTC and NTSC_PAL pins are both set to high, the part ADV7172/ADV7173 will power-up in sleep mode to facilitate low power consumption before all registers have been initialized. If Mode Register 6, Bit 0 (MR60) is then set to ("1") sleep mode control passes to Mode Register 2, Bit 7 (i.e., control via I^2C).

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four (NTSC) or eight (PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7172/ADV7173 is configured in RTC mode (MR41 = "1" and MR42 = "1"). Under these conditions (unstable video) the subcarrier phase reset should be enabled (MR42 = "0" and MR41 = "1") but no reset applied. In this configuration the SCH phase will never be reset, which that the output video will now track the unstable input video.

The subcarrier phase reset when applied will reset the SCH phase to Field 0 at the start of the next field (e.g., subcarrier phase reset applied in Field 5 (PAL) on the start of the next field SCH phase will be reset to Field 0).

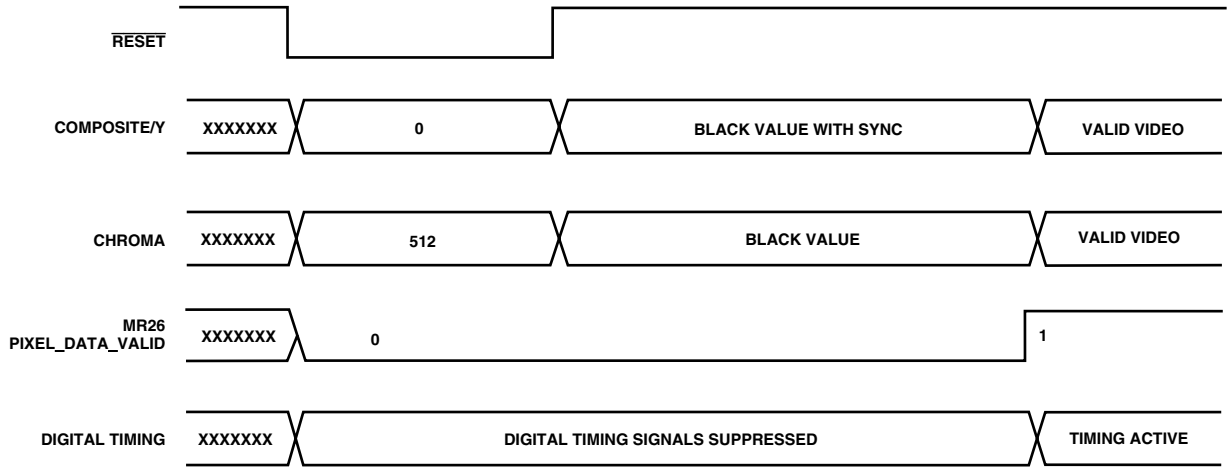


Figure 36. $\overline{\text{RESET}}$ Sequence Timing Diagram

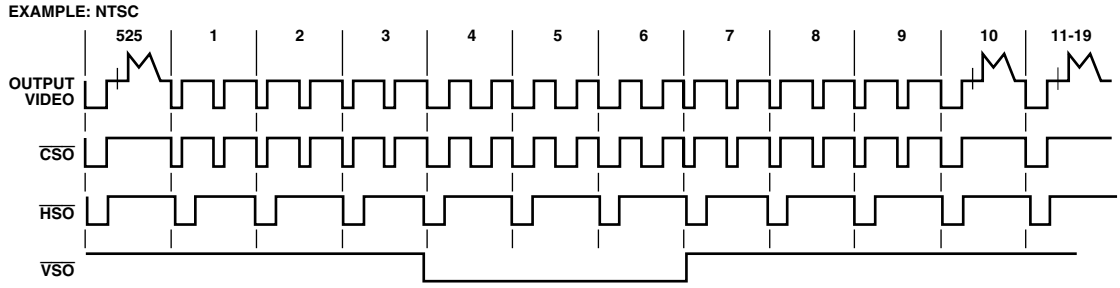


Figure 37. $\overline{CSO}$, $\overline{HSO}$, $\overline{VSO}$ Timing Diagram

$\overline{CSO}$, $\overline{HSO}$, AND $\overline{VSO}$ OUTPUTS

The ADV7172/ADV7173 supports three timing signals, $\overline{CSO}$ (composite sync signal), $\overline{HSO}$ (horizontal sync signal) and $\overline{VSO}$ (vertical sync signal). These output TTL signals are aligned with the analog video outputs. $\overline{HSO}$ and $\overline{CSO}$ are shared on Pin 10. Mode Register 7, Bit MR75 can be used to configure this output pin. See Figure 37 for an example of these waveforms.

CLAMP OUTPUT

The ADV7172/ADV7173 has a programmable clamp TTL output signal. The clamp signal is programmable to the front and back porch. Mode Register 5, Bit MR57 can be used to control the porch position. Also the position of the clamp signal can be varied by 1–3 clock cycles in a positive and negative direction from the default position. Mode Register 5, Bits MR56, MR55, and MR54 control this position.

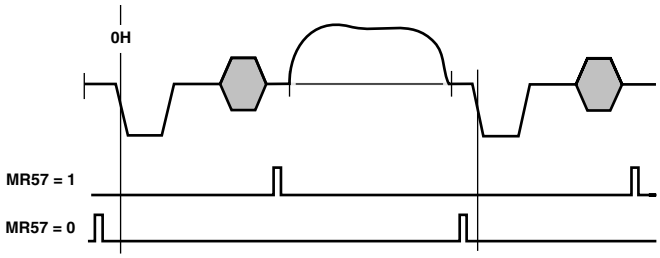


Figure 38. Clamp Output Timing

MPU PORT DESCRIPTION

The ADV7172 and ADV7173 support a 2-wire serial (I^2C-Compatible) microprocessor bus driving multiple peripherals. Two inputs serial data (SDATA) and serial clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7172 and ADV7173 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 39 and Figure 40. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7172/ADV7173 to Logic Level "0" or Logic Level "1." When ALSB is set to "0," there is greater bandwidth on the I^2C lines, which allows high-speed data transfers on this bus. When ALSB is set to "1," there is reduced input bandwidth on the I^2C lines, which means that impulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

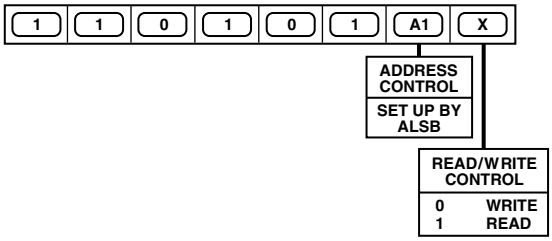


Figure 39. ADV7172 Slave Address

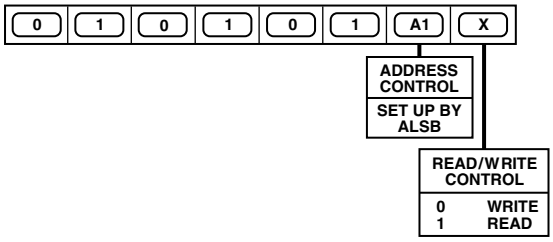


Figure 40. ADV7173 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7172/ADV7173 acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers. There is one exception. The subcarrier frequency registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto increment function should then be used to increment and access Subcarrier Frequency Registers 1, 2 and 3. The subcarrier frequency registers should not be accessed independently.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period, the user should issue only one start condition, one stop condition or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7172/ADV7173 will not issue an acknowledge and will return to the idle condition. If, in autoincrement mode, the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7172/ADV7173 and the part will return to the idle condition.

Figure 41 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

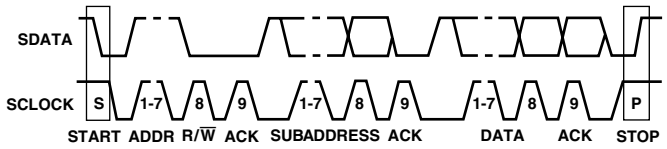


Figure 41. Bus Data Transfer

Figure 42 shows bus write and read sequences.

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7172/ADV7173 except the Subaddress Register, which is a write-only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. A read/write operation is then performed from/to the target address, which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including subaddress register, mode registers, subcarrier frequency registers, subcarrier phase register, timing registers, closed captioning extended data registers, closed captioning data registers, NTSC pedestal Control/PAL teletext control registers, CGMS/WSS registers, contrast register, U- or V-scale registers, hue adjust register, brightness control register and sharpness control register in terms of its configuration. All registers can be read from as well as written to.

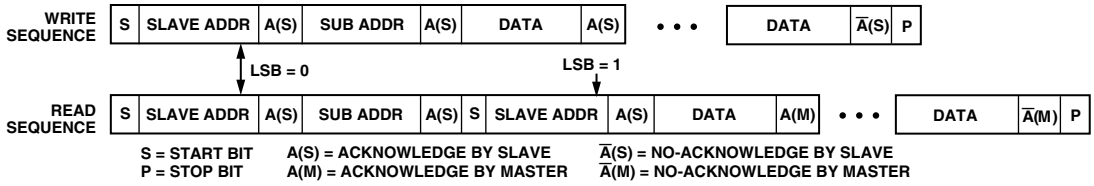


Figure 42. Write and Read Sequences