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Chip Scale PAL/NTSC Video Encoder with Advanced Power Management

Data Sheet

ADV7174/ADV7179

FEATURES

- ITU-R[1] BT601/BT656 YCrCb to PAL/NTSC video encoder
- High quality 10-bit video DACs
- SSAF™ (super sub-alias filter)
- Advanced power management features
- CGMS (copy generation management system)
- WSS (wide screen signaling)
- NTSC M, PAL N[2], PAL B/D/G/H/I, PAL-M[3] , PAL 60
- Single 27 MHz clock required (×2 oversampling)
- Macrovision 7.1 (ADV7174 only)
- 80 dB video SNR
- 32-bit direct digital synthesizer for color subcarrier
- Multistandard video output support:
  - Composite (CVBS)
  - Component S-video (Y/C)
- Video input data port supports:
  - CCIR-656 4:2:2 8-bit parallel input format
- Programmable simultaneous composite and S-video or RGB (SCART)/YPbPr video outputs
- Programmable luma filters low-pass [PAL/NTSC] notch, extended SSAF, CIF, and QCIF
- Programmable chroma filters (low-pass [0.65 MHz, 1.0 MHz, 1.2 MHz, and 2.0 MHz], CIF, and QCIF)
- Programmable VBI (vertical blanking interval)
- Programmable subcarrier frequency and phase
- Programmable LUMA delay
- Individual on/off control of each DAC
- CCIR and square pixel operation
- Integrated subcarrier locking to external video source
- Color signal control/burst signal control
- Interlaced/noninterlaced operation
- Complete on-chip video timing generator
- Programmable multimode master/slave operation
- Closed captioning support
- Teletext insertion port (PAL-WST)
- On-board color bar generation
- On-board voltage reference
- 2-wire serial MPU interface (I²C® compatible and fast I²C)
- Single-supply 2.8 V and 3.3 V operation
- Small 40-lead 6 mm × 6 mm LFCSP package
- −40°C to +85°C at 3.3 V
- −20°C to +85°C at 2.8 V
- Qualified for automotive applications

APPLICATIONS

- Portable video applications
- Mobile phones
- Digital still cameras

FUNCTIONAL BLOCK DIAGRAM

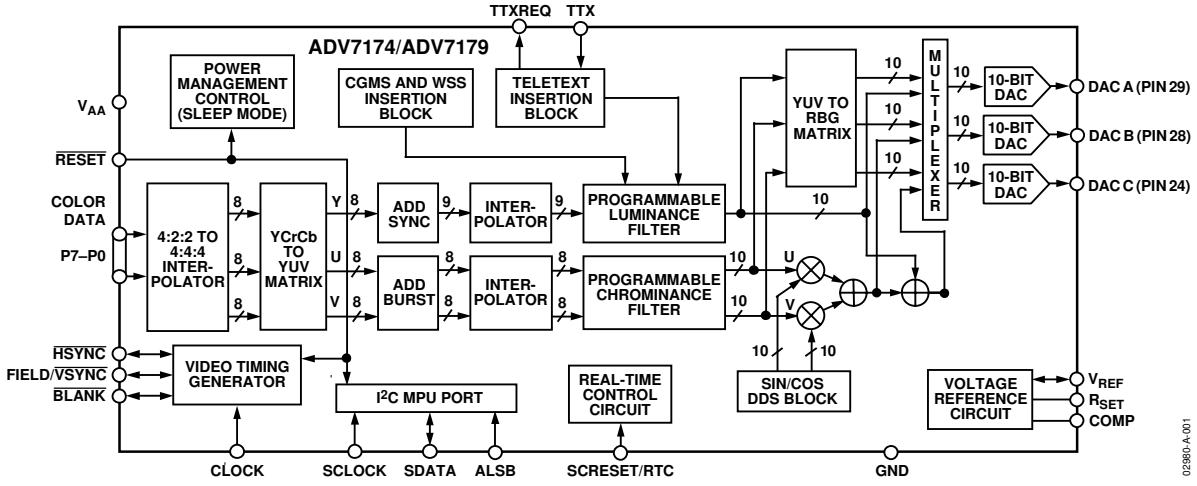

Figure 1.

[1] ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).
[2] Throughout the document, N is referenced to PAL – Combination – N.
[3] ADV7174 only.
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Rev. C Document Feedback

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SPECIFICATIONS

2.8 V SPECIFICATIONS

V_{AA} = 2.8 V, V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.

Table 1.

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[2]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		±3.0		LSB
Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS[2]					
Input High Voltage, V_{INH}		1.6			V
Input Low Voltage, V_{INL}				0.7	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[2]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[2]					
Output Current[3]	R_{SET} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
DAC-to-DAC Matching			2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[2, 4]					
V_{AA}		2.8			V
Normal Power Mode					
I_{DAC} (Max)[5]	R_{SET} = 150 Ω, R_L = 37.5 Ω		115	120	mA
I_{CCT}[6]			30		mA
Low Power Mode					
I_{DAC} (Max)[5]			62		mA
I_{CCT}[6]			30		mA
Sleep Mode					
I_{DAC}[7]			0.1		μA
I_{CCT}[8]			0.001		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] Temperature range T_{MIN} to T_{MAX}: −20°C to +85°C.
[2] Guaranteed by characterization.
[3] DACs can output 35 mA typically at 2.8 V (R_{SET} = 150 Ω and R_L = 37.5 Ω). Full drive into 37.5 Ω load.
[4] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[5] I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 37 mA output per DAC) to drive all three DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[6] I_{CCT} (circuit current) is the continuous current required to drive the device.
[7] Total DAC current in sleep mode.
[8] Total continuous current during sleep mode.

2.8 V TIMING SPECIFICATIONS

V_{AA} = 2.8 V, V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.

Table 2.

Parameter	Conditions[1]	Min	Typ	Max	Unit
MPU PORT[2, 3]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulse Width, t_1		0.6			µs
SCLOCK Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the first clock is generated	0.6			µs
Setup Time (Start Condition), t_4	Relevant for repeated start condition	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 4]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			12		ns
Digital Output Hold Time, t_1[4]			8		ns
Pipeline Delay, t_{PD}[5]			48		Clock Cycles
TELETEXT[3, 4, 6]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
$\overline{\text{RESET}}$ CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

[1] Temperature range T_{MIN} to T_{MAX}: –20°C to +85°C.
[2] TTL input values are 0 V to 2.8 V, with input rise/fall times –3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load –10 pF.
[3] Guaranteed by characterization.
[4] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
[5] See Figure 60.
[6] Teletext Port consists of the following:
Teletext Output: TTXREQ
Teletext Input: TTX

3.3 V SPECIFICATIONS

V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 3.

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		± 0.6		LSB
Differential Nonlinearity	Guaranteed Monotonic			± 1	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}[3, 4]	V_{IN} = 0.4 V or 2.4 V			± 1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current[4, 5]	R_{SET} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current[6]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching			2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 7]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (Max)[8]	R_{SET} = 150 Ω, R_L = 37.5 Ω		115	120	mA
I_{DAC} (Min)[8]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		20		mA
I_{CCT}[9]			35		mA
Low Power Mode					
I_{DAC} (Max)[8]			62		mA
I_{DAC} (Min)[8]			20		mA
I_{CCT}[9]			35		mA
Sleep Mode					
I_{DAC}[10]			0.1		μA
I_{CCT}[11]			0.001		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.
[2] Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C.
[3] Guaranteed by characterization.
[4] Full drive into 37.5 Ω load.
[5] DACs can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 37.5 Ω), optimum performance obtained at 18 mA DAC current (R_{SET} = 300 Ω and R_L = 75 Ω).
[6] Minimum drive current (used with buffered/scaled output load).
[7] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[8] I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 37 mA output per DAC) to drive all three DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[9] I_{CCT} (circuit current) is the continuous current required to drive the device.
[10] Total DAC current in sleep mode.
[11] Total continuous current during sleep mode.

3.3 V TIMING SPECIFICATIONS

V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 4.

Parameter	Conditions[1]	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulse Width, t_1		0.6			µs
SCLOCK Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period, the first clock is generated	0.6			µs
Setup Time (Start Condition), t_4	Relevant for repeated start condition	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			12		ns
Digital Output Hold Time, t_{14}			8		ns
Pipeline Delay, t_{PD}[6]			48		Clock Cycles
TELETEXT[3, 4]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
$\overline{\text{RESET}}$ CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

[1] The maximum/minimum specifications are guaranteed over this range. The maximum/minimum values are typical over 3.0 V to 3.6 V range.
[2] Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C.
[3] TTL input values are 0 V to 3 V, with input rise/fall times –3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load –10 pF.
[4] Guaranteed by characterization.
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
[6] See Figure 60.

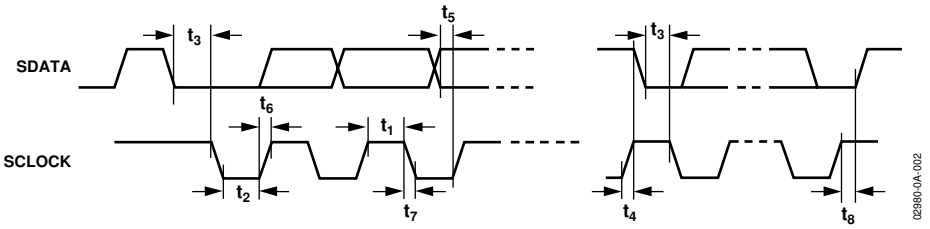


Figure 2. MPU Port Timing Diagram

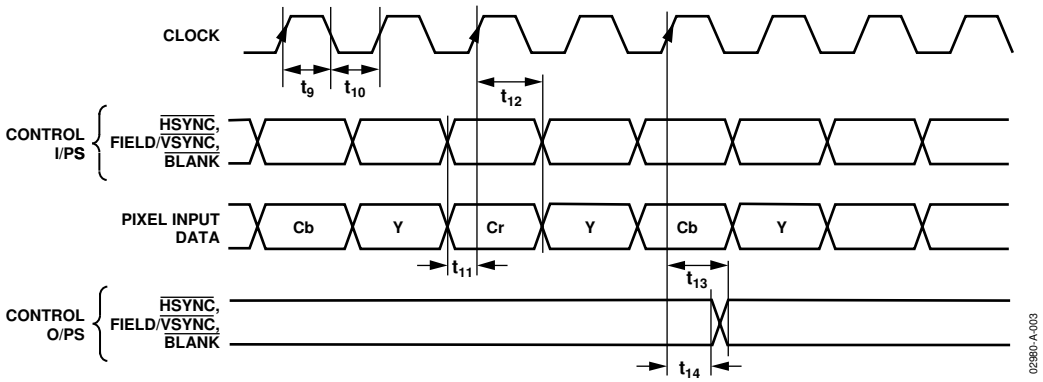


Figure 3. Pixel and Control Data Timing Diagram

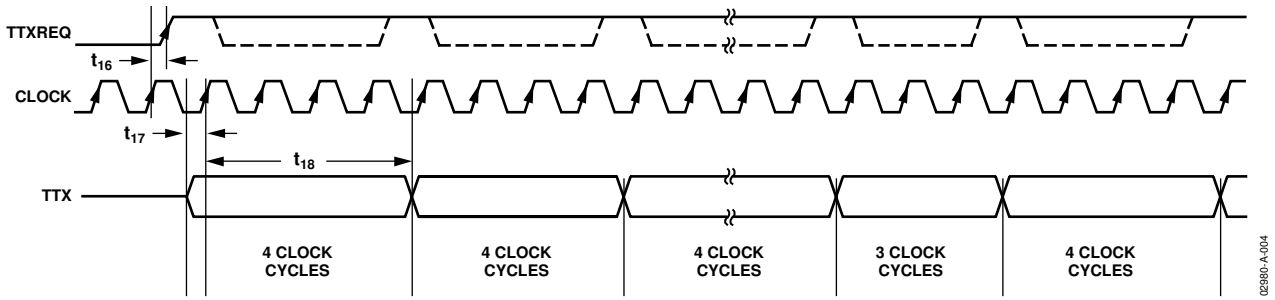


Figure 4. Teletext Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{AA} to GND	4 V
Voltage on Any Digital Input Pin	GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S)	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature Soldering, 10 sec	260°C
Analog Outputs to GND[1]	GND – 0.5 V to V_{AA}
θ_{JA}[2]	30°C/W

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.
[2] With the exposed metal paddle on the underside of LFCSP soldered to GND on the PCB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

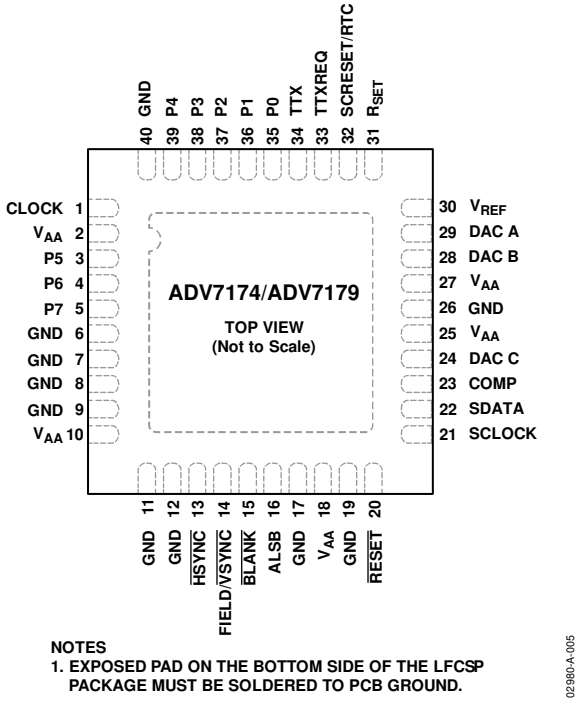


Figure 5. Pin Configurations

Table 6. Pin Function Descriptions

Mnemonic	Input/ Output	Function
P7–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0). P0 is the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (master mode) or accept (slave mode) sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (master mode) or accept (slave mode) these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic 0. This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR22 and MR21 of Mode Register 2. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin resets the subcarrier to Field 0. Alternatively, it can be configured as a real-time control (RTC) input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the video signals.
COMP	O	Compensation Pin. Connect a 0.1 µF capacitor from COMP to V_{AA}. For optimum dynamic performance in low power mode, the value of the COMP capacitor can be lowered to as low as 2.2 nF.
DAC A	O	DAC Output (see Table 13)
DAC B	O	DAC Output (see Table 13).
DAC C	O	DAC Output (see Table 13).
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7174/ADV7179 into default mode. This is NTSC operation, Timing Slave Mode 0, 8-bit operation, 2× composite out signals. DACs A, B, and C are enabled.
TTX	I	Teletext Data.
TTXREQ	O	Teletext Data Request Signal/Defaults to GND when Teletext Not Selected.
V_{AA}	P	Power Supply (2.8 V or 3.3 V).
GND	G	Ground Pin.
EPAD		Exposed Pad. The exposed pad on the bottom side of the LFCSP package must be soldered to PCB ground for proper heat dissipation and also for noise and mechanical strength benefits.

GENERAL DESCRIPTION

The ADV7174/ADV7179 is an integrated digital video encoder that converts digital CCIR-601 4:2:2 8-bit component video data into a standard analog baseband television signal compatible with worldwide standards.

The on-board SSAF (super sub-alias filter) with extended luminance frequency response and sharp stop-band attenuation enables studio quality video playback on modern TVs, giving optimal horizontal line resolution.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes and in power-down or sleep modes.

The ADV7174/ADV7179 supports both PAL and NTSC square pixel operation. The parts incorporate WSS and CGMS-A data control generation.

The output video frames are synchronized with the incoming data timing reference codes. Optionally, the encoder accepts (and can generate) HSYNC, VSYNC, and FIELD timing signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The encoder requires a signal two times the pixel rate (27 MHz) clock for standard operation. Alternatively, the encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

A separate Teletext port enables the user to directly input Teletext data during the vertical blanking interval.

The ADV7174/ADV7179 modes are set up over a 2-wire serial bidirectional port (I^2C compatible) with two slave addresses.

The ADV7174/ADV7179 is packaged in a 40-lead 6 mm × 6 mm LFCSP package.

DATA PATH DESCRIPTION

For PAL B/D/G/H/I/M/N and NTSC M and N modes, YCrCb 4:2:2 data is input via the CCIR-656 compatible pixel port at a 27 MHz data rate. The pixel data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, and Cr and Cb typically have a range of 128 ± 112; however, it is possible to input data from 1 to 254 on both Y, Cb, and Cr. The ADV7174/ADV7179 supports PAL (B/D/G/H/I/M/N) and NTSC (with and without pedestal) standards. The appropriate SYNC, BLANK, and burst levels are added to the YCrCb data. Macrovision Anti-taping (ADV7174 only), closed-captioning, and Teletext levels are also added to Y and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate subcarrier sine/cosine phases and added together to make up the chrominance signal. The luma (Y) signal can be delayed 1–3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate SYNC and BLANK levels. The RGB data is in synchronization with the composite video output. Alternatively, analog YPbPr data can be generated instead of RGB data.

The three l0-bit DACs can be used to output:

- Composite Video + Composite Video
- S-Video + Composite Video
- YPrPb Video
- SCART RGB Video

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in Appendix 6.

INTERNAL FILTER RESPONSE

The Y filter supports several different frequency responses, including two low-pass responses, two notch responses, an extended (SSAF) response, a CIF response, and a QCIF response. The UV filter supports several different frequency responses, including four low-pass responses, a CIF response, and a QCIF response. These can be seen in Table 7 and Table 8 and Figure 6 to Figure 18.

Table 7. Luminance Internal Filter Specifications

Filter Type	Filter Selection			Pass-Band Ripple (dB)	3 dB Bandwidth (MHz)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)
	MR04	MR03	MR02				
Low-Pass (NTSC)	0	0	0	0.091	4.157	7.37	−56
Low-Pass (PAL)	0	0	1	0.15	4.74	7.96	−64
Notch (NTSC)	0	1	0	0.015	6.54	8.3	−68
Notch (PATL)	0	1	1	0.095	6.24	8.0	−66
Extended (SSAF)	1	0	0	0.051	6.217	8.0	−61
CIF	1	0	1	0.018	3.0	7.06	−61
QCIF	1	1	0	Monotonic	1.5	7.15	−50

Table 8. Chrominance Internal Filter Specifications

Filter Type	Filter Selection			Pass-Band Ripple (dB)	3 dB Bandwidth (MHz)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)
	MR07	MR06	MR05				
1.3 MHz Low-Pass	0	0	0	0.084	1.395	3.01	−45
0.65 MHz Low-Pass	0	0	1	Monotonic	0.65	3.64	−58.5
1.0 MHz Low-Pass	0	1	0	Monotonic	1.0	3.73	−49
2.0 MHz Low-Pass	0	1	1	0.0645	2.2	5.0	−40
Reserved	1	0	0				
CIF	1	0	1	0.084	0.7	3.01	−45
QCIF	1	1	0	Monotonic	0.5	4.08	−50

TYPICAL PERFORMANCE CHARACTERISTICS

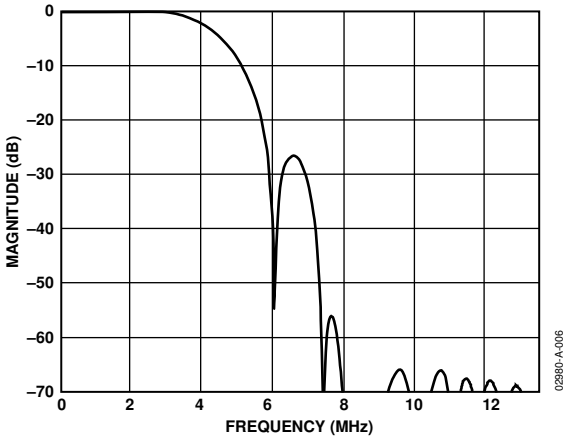


Figure 6. Chrominance Internal Filter Specifications

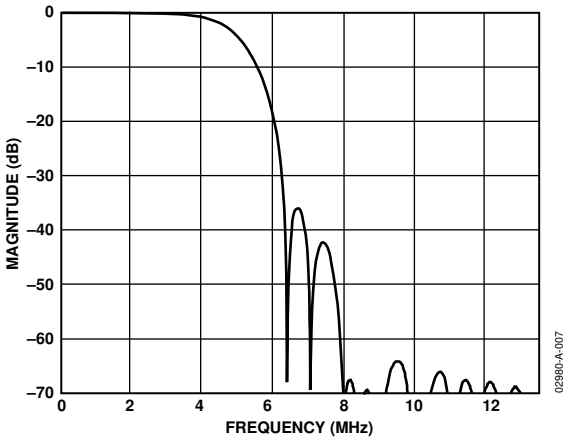


Figure 7. PAL Low-Pass Luma Filter

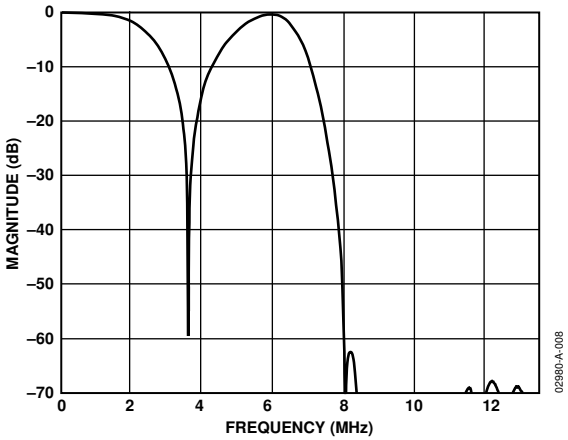


Figure 8. NTSC Notch Luma Filter

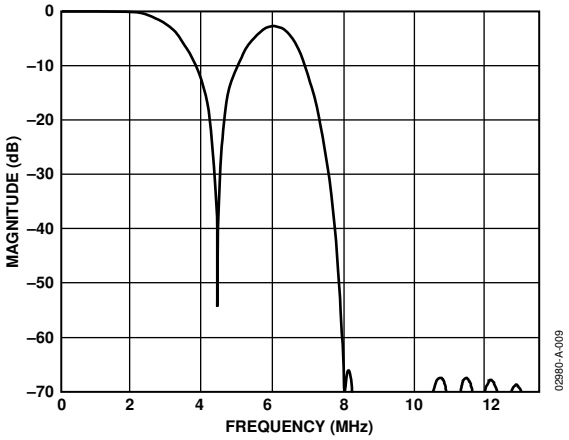


Figure 9. PAL Notch Luma Filter

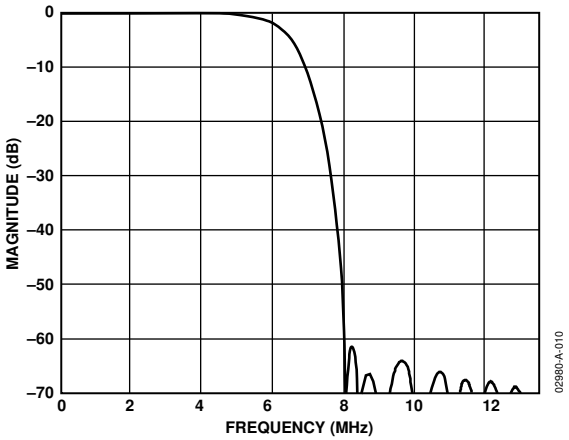


Figure 10. Extended Mode (SSAF) Luma Filter

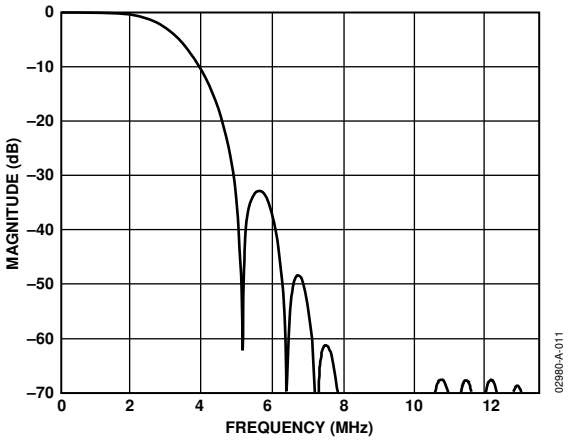


Figure 11. CIF Luma Filter

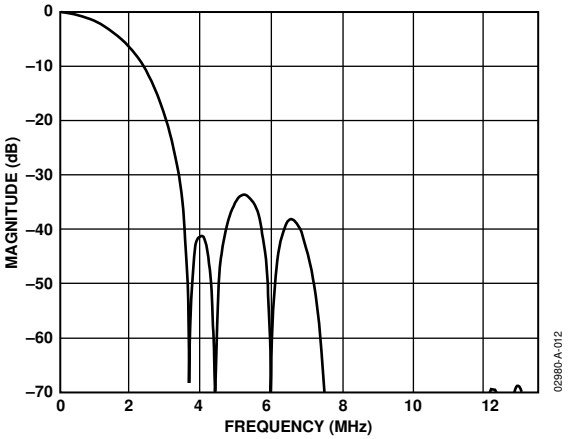


Figure 12. QCIF Luma Filter

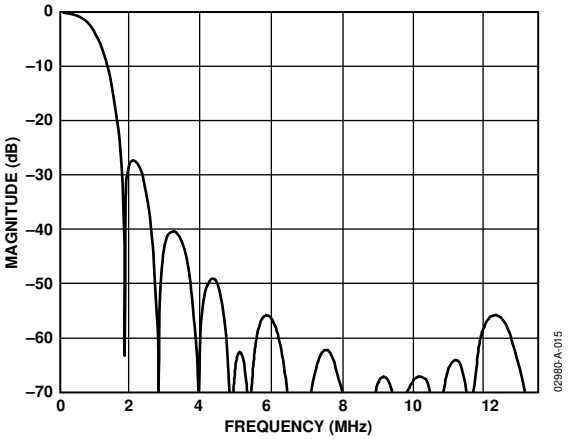


Figure 15. 1.0 MHz Low-Pass Chroma Filter

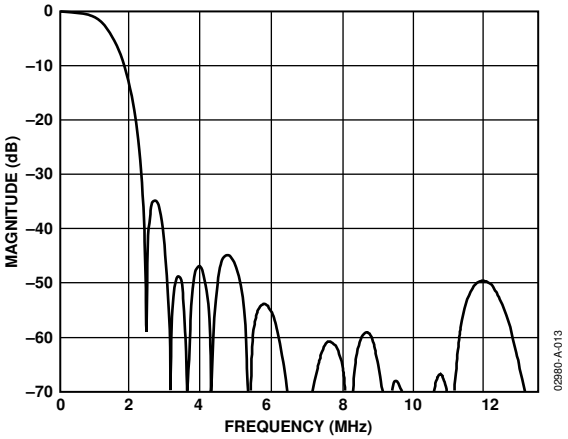


Figure 13. 1.3 MHz Low-Pass Chroma Filter

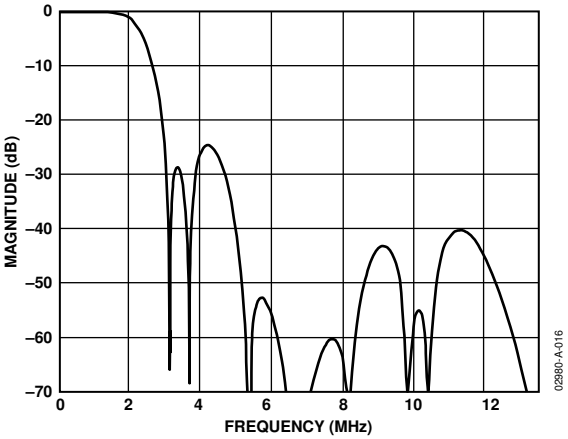


Figure 16. 2.0 MHz Low-Pass Chroma Filter

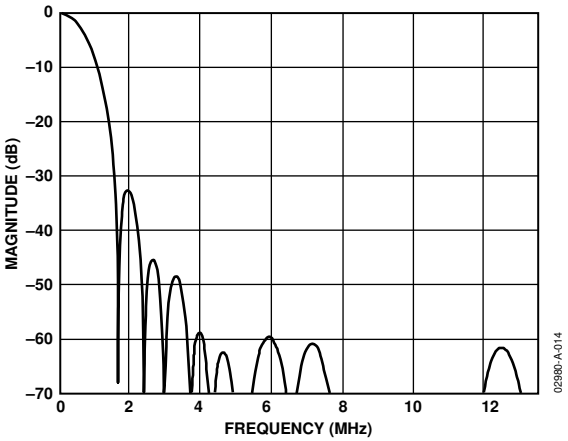


Figure 14. 0.65 MHz Low-Pass Chroma Filter

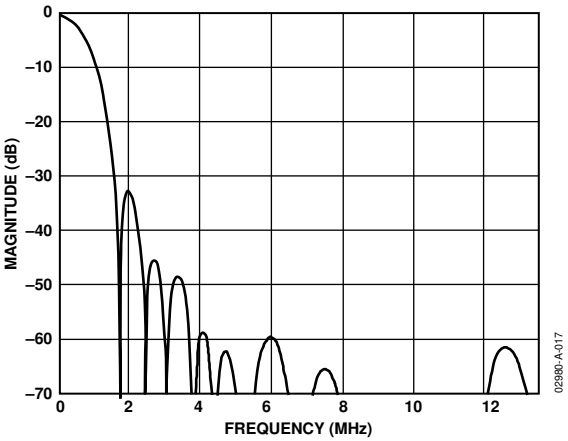


Figure 17. CIF Chroma Filter

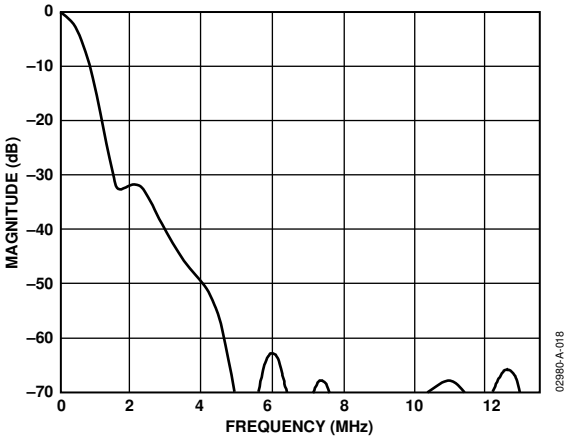


Figure 18. QCIF Chroma Filter

FEATURES

COLOR BAR GENERATION

The ADV7174/ADV7179 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to Logic 1.

SQUARE PIXEL MODE

The ADV7174/ADV7179 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL

The pedestal on both odd and even fields can be controlled on a line-by-line basis using the NTSC pedestal control registers. This allows the pedestals to be controlled during the vertical blanking interval.

PIXEL TIMING DESCRIPTION

The ADV7174/ADV7179 operates in an 8-bit YCrCb mode.

8-Bit YCrCb Mode

This default mode accepts multiplexed YCrCb inputs through the P7–P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1, Cb1, Y2, and so on. The Y, Cb, and Cr data are input on a rising clock edge.

SUBCARRIER RESET

Together with the SCRESET/RTC pin and Bits MR22 and MR21 of Mode Register 2, the ADV7174/ADV7179 can be used in subcarrier reset mode. The subcarrier resets to Field 0 at the start of the following field when a low-to-high transition occurs on this input pin.

REAL-TIME CONTROL

Together with the SCRESET/RTC pin and Bits MR22 and MR21 of Mode Register 2, the ADV7174/ADV7179 can be used to lock to an external video source. The real-time control mode allows the ADV7174/ADV7179 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7183A video decoder; see Figure 19), the part automatically changes to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00H should be written into all four subcarrier frequency registers when using this mode.

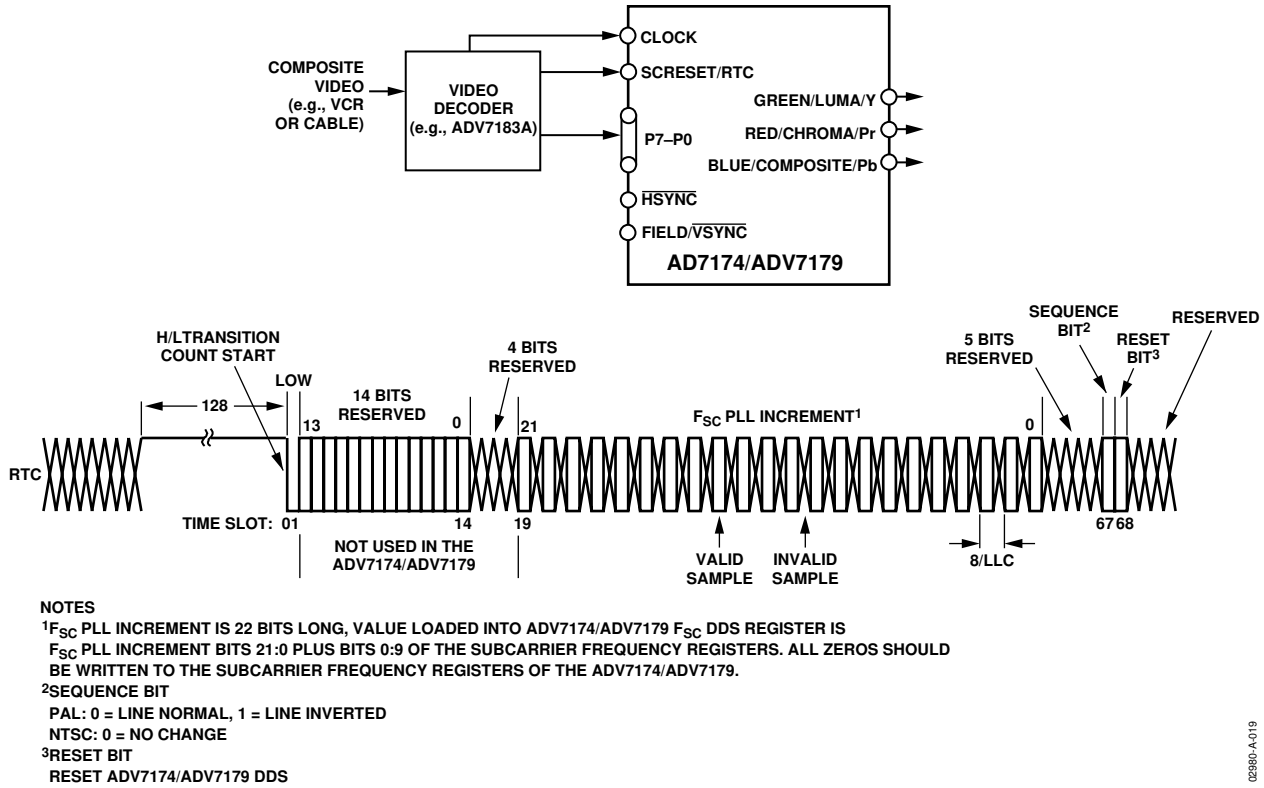
Video Timing Description

The ADV7174/ADV7179 is intended to interface with off-the-shelf MPEG1 and MPEG2 decoders. Consequently, the ADV7174/ADV7179 accepts 4:2:2 YCrCb pixel data via a CCIR-656 pixel port and has several video timing modes of operation that allow it to be configured as either a system master video timing generator or as a slave to the system video timing generator. The ADV7174/ADV7179 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7174/ADV7179 calculates the width and placement of analog sync pulses, blanking levels, and color burst envelopes. Color bursts are disabled on appropriate lines, and serration and equalization pulses are inserted where required.

In addition, the ADV7174/ADV7179 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections into the correct location for the new clock frequencies.

The ADV7174/ADV7179 has four distinct master and four distinct slave timing configurations. Timing control is established with the bidirectional $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths and where they occur in relation to each other.



NOTES
[1]F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7174/ADV7179 F_{SC} DDS REGISTER IS F_{SC} PLL INCREMENT BITS 21:0 PLUS BITS 0:9 OF THE SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7174/ADV7179.
[2]SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
[3]RESET BIT
RESET ADV7174/ADV7179 DDS

Figure 19. RTC Timing and Connections

Vertical Blanking Data Insertion

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not bear line sync or pre-/post-equalization pulses (see Figure 21 to Figure 32). This mode of operation is called partial blanking and is selected by setting MR32 to 1. It allows the insertion of any VBI data (opened VBI) into the encoded output waveform. This data is present in the digitized incoming YCbCr data stream, for example. WSS data, CGMS, VPS, and so on. Alternatively, the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR32 to 0.

Mode 0 (CCIR-656): Slave Option

(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7174/ADV7179 is controlled by the SAV (start active video) and EAV (end active video) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 20. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

Mode 0 (CCIR-656): Master Option

(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7174/ADV7179 generates H, V, and F signals required for the SAV and EAV time codes in the CCIR-656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin, and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 21 (NTSC) and Figure 22 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 23.

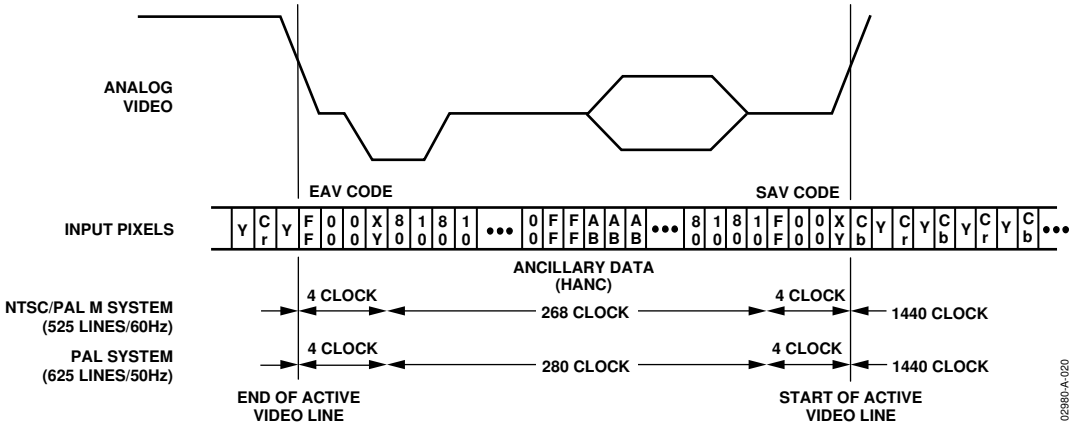


Figure 20. Timing Mode 0 (Slave Mode)

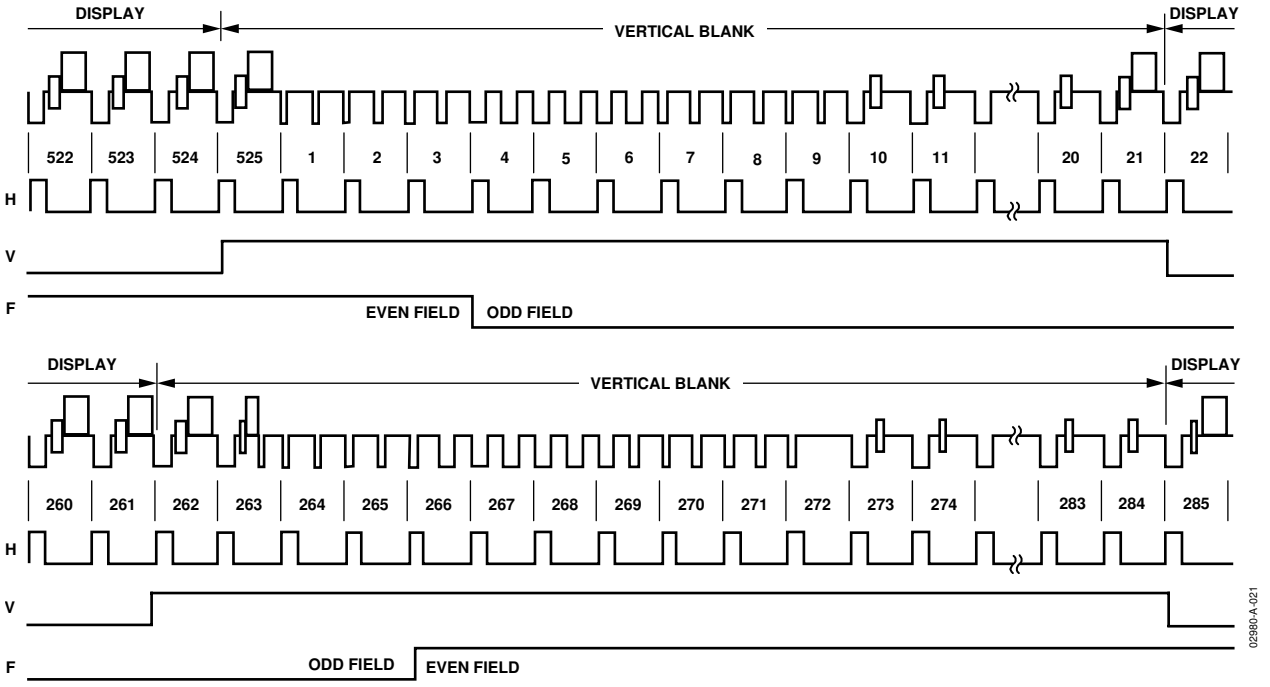


Figure 21. Timing Mode 0 (NTSC Master Mode)

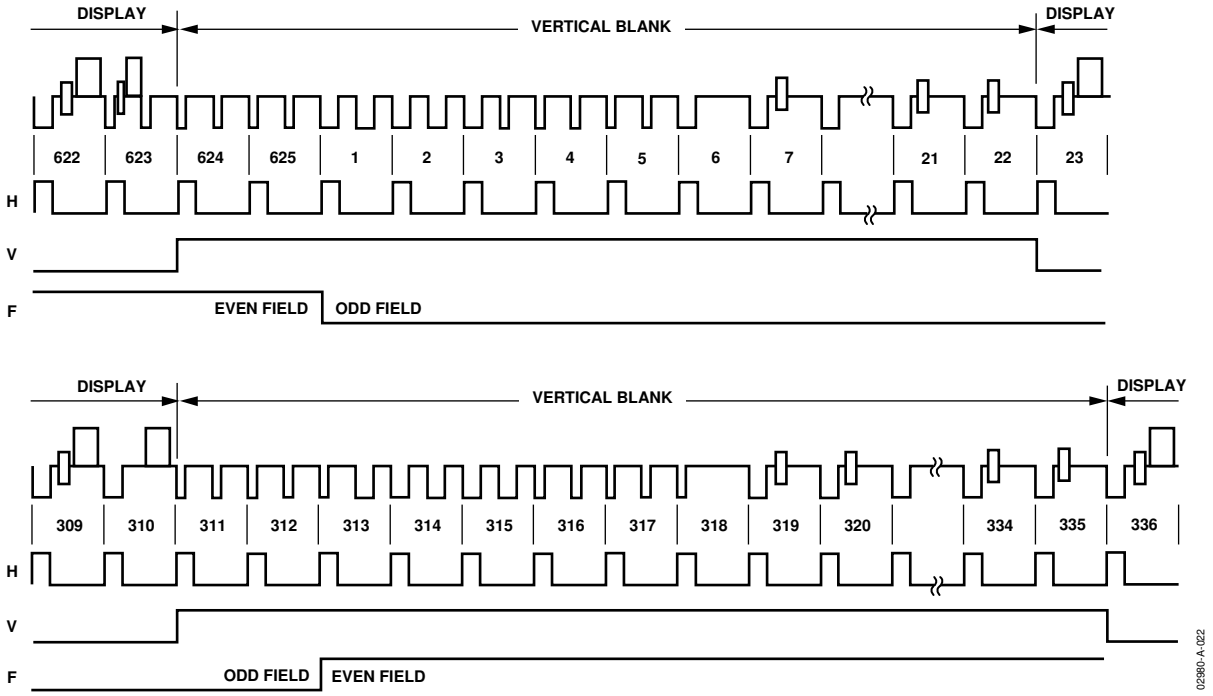


Figure 22. Timing Mode 0 (PAL Master Mode)

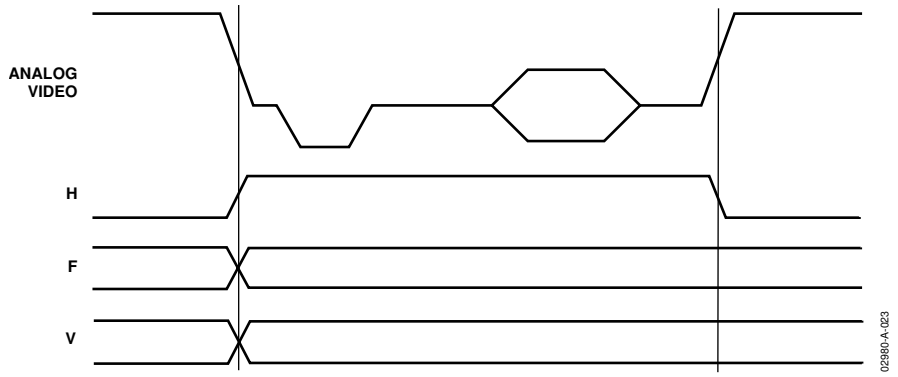


Figure 23. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode, the ADV7174/ADV7179 accepts horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{HSYNC}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7174/ADV7179 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

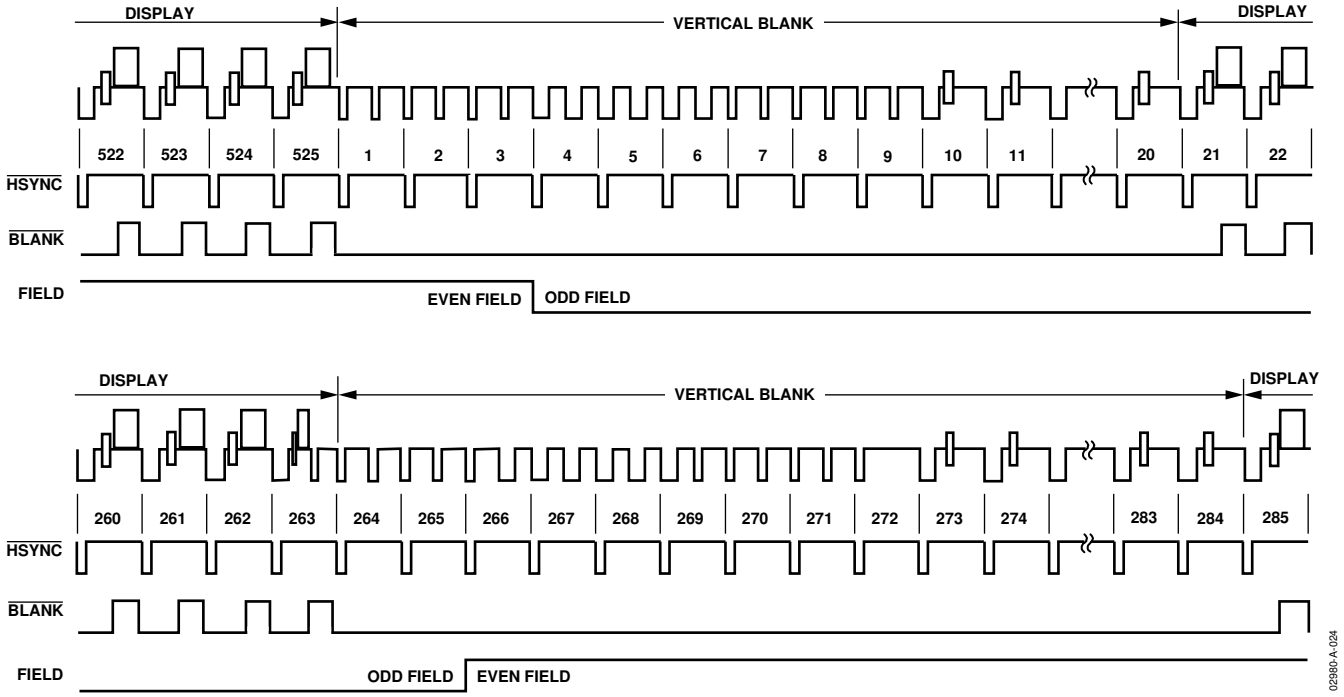


Figure 24. Timing Mode 1 (NTSC)

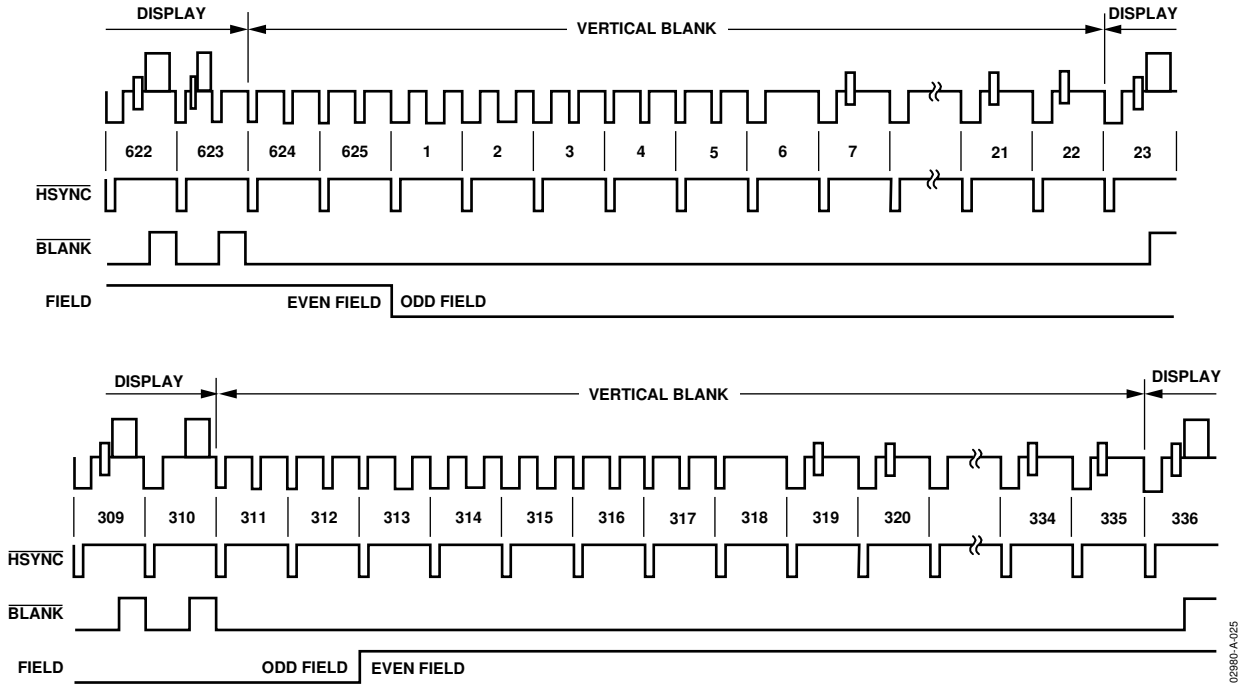


Figure 25. Timing Mode 1 (PAL)

Mode 1: Master Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode, the ADV7174/ADV7179 can generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{HSYNC}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7174/ADV7179 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL). Figure 26 illustrates the $\overline{HSYNC}$, $\overline{BLANK}$, and FIELD for an odd or even field transition relative to the pixel data.

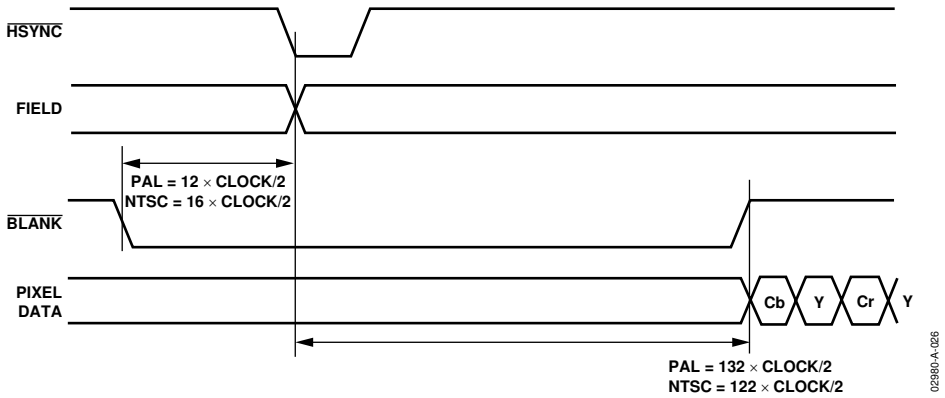


Figure 26. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option HSYNC, VSYNC, BLANK

(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode, the ADV7174/ADV7179 accepts horizontal and vertical SYNC signals. A coincident low transition of both and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7174/ADV7179 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL).

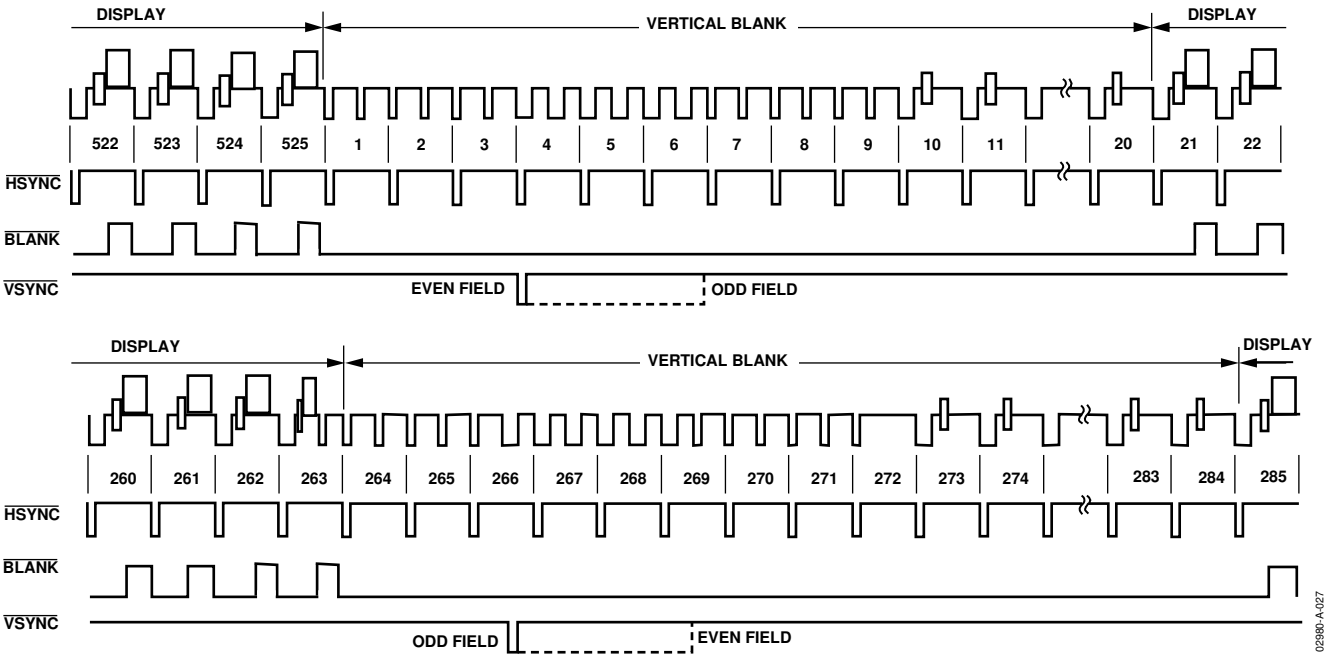


Figure 27. Timing Mode 2 (NTSC)

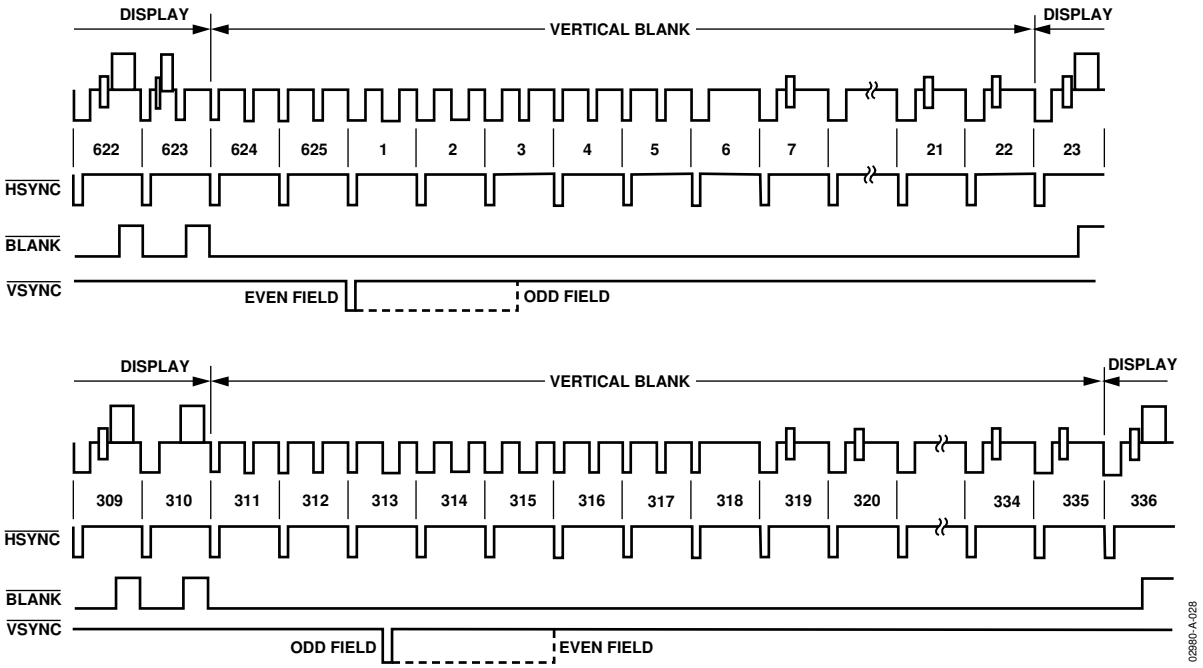


Figure 28. Timing Mode 2 (PAL)

Mode 2: Master Option HSYNC, VSYNC, BLANK

(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode, the ADV7174/ADV7179 can generate horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7174/ADV7179 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL). Figure 29 illustrates the HSYNC, BLANK, and VSYNC for an even-to-odd field transition relative to the pixel data. Figure 30 illustrates the HSYNC, BLANK, and VSYNC for an odd-to-even field transition relative to the pixel data.

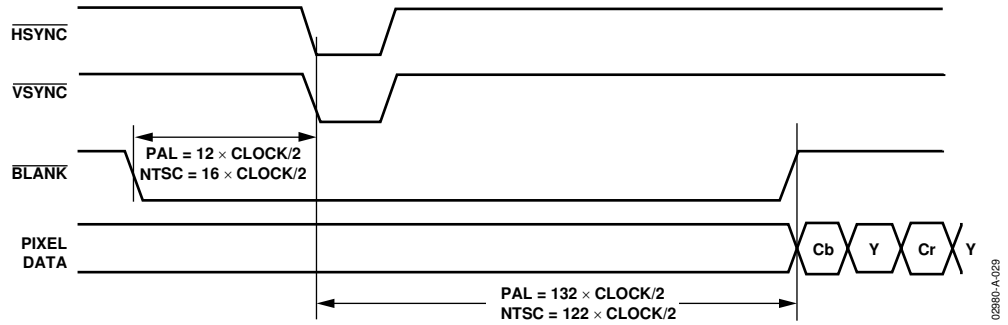


Figure 29. Timing Mode 2 Even-to-Odd Field Transition Master/Slave

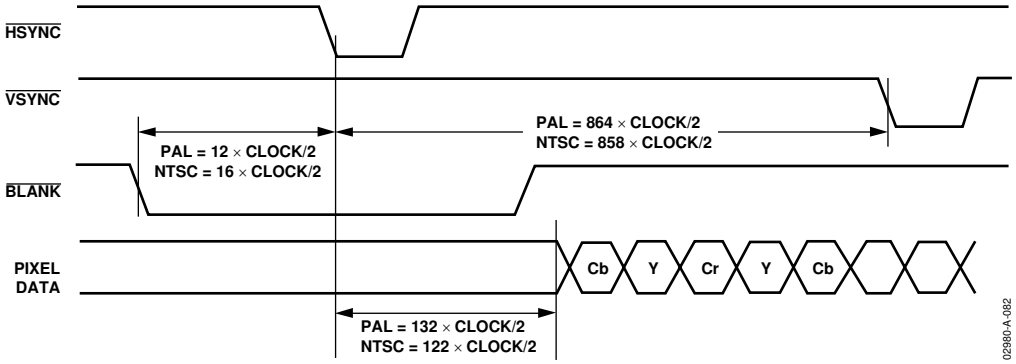


Figure 30. Timing Mode 2 Odd-to-Even Field Transition Master/Slave

Mode 3: Master/Slave Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode, the ADV7174/ADV7179 accepts or generates horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{HSYNC}$ is high indicates a new frame, that is, vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7174/ADV7179 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 31 (NTSC) and Figure 32 (PAL).

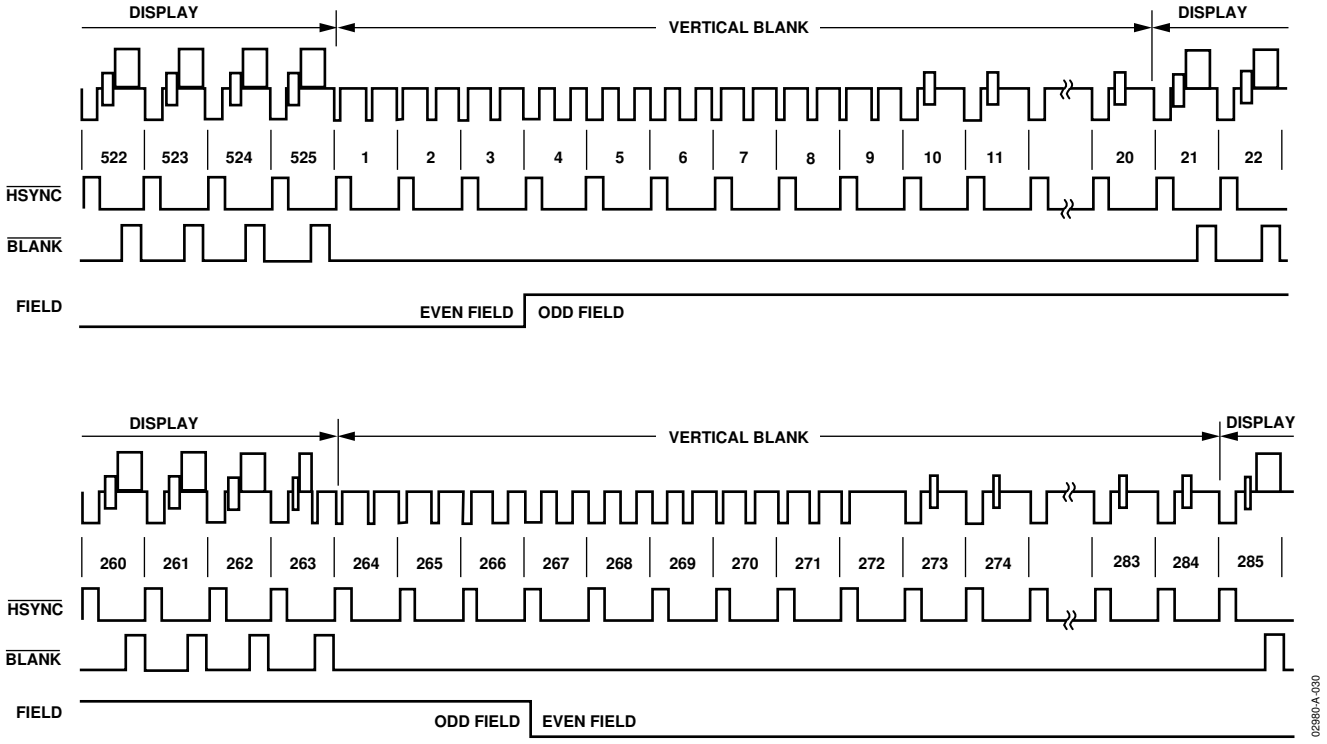


Figure 31. Timing Mode 3 (NTSC)

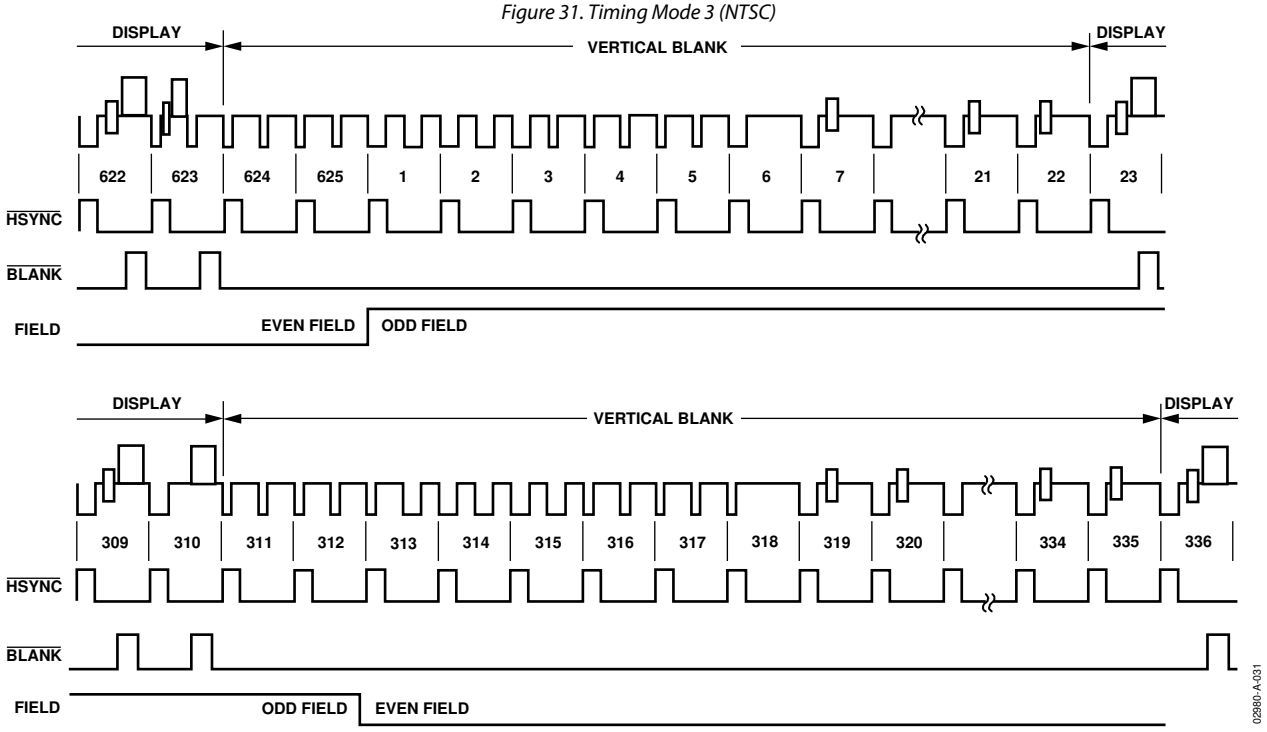


Figure 32. Timing Mode 3 (PAL)

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port so that the pixel inputs, P7–P0, are selected. After reset, the ADV7174/ADV7179 are automatically set up to operate in NTSC mode. Subcarrier frequency code 21F07C16H is loaded into the subcarrier frequency registers. All other registers, with the exceptions of Mode Register 1 and Mode Register 4, are set to 00H. Bit MR44 of Mode Register 4 is set to Logic 1. This enables the 7.5 IRE pedestal. Bit MR13, DAC A, and Bit MR16, DAC C, are powered down by default.

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four (NTSC) or eight (PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, 0 SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error and results in very minor SCH phase jumps at the start of the 4- or 8-field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7174/ADV7179 is configured in RTC mode (MR21 = 1 and MR22 = 1). Under these conditions (unstable video), the subcarrier phase reset should be enabled (MR22 = 0 and MR21 = 1), but no reset applied. In this configuration, the SCH phase can never be reset, which means that the output video can now track the unstable input video. The subcarrier phase reset, when applied, resets the SCH phase to Field 0 at the start of the next field, for example, subcarrier phase reset applied in Field 5 (PAL) on the start of the next field SCH phase is reset to Field 0.

MPU PORT DESCRIPTION

The ADV7174/ADV7179 supports a 2-wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDATA) and serial clock (SCLOCK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7174/ADV7179 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 33 and Figure 34. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A 1 is set by setting the ALSB pin of the ADV7174/ ADV7179 to Logic 0 or Logic 1.

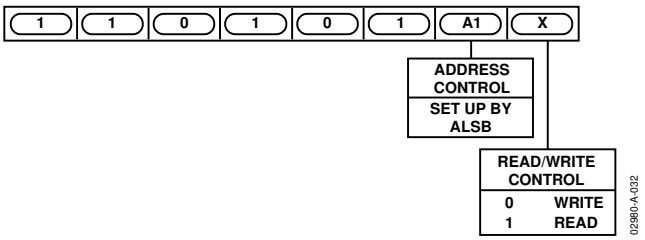


Figure 33. ADV7174 Slave Address

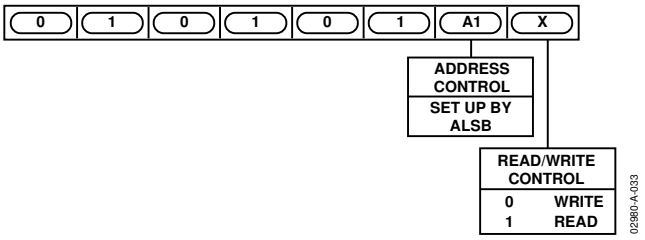


Figure 34. ADV7179 Slave Address

To control the various devices on the bus, the following protocol must be followed: first, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + $R/\overline{W}$ bit). The bits transfer from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the start condition and the correct transmitted address. The $R/\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master will write information to the peripheral. A Logic 1 on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7174/ADV7179 acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit addresses plus the $R/\overline{W}$ bit. The ADV7174/ADV7179 has 26 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses' auto increment allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers. There is one exception. The subcarrier frequency registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto increment function should then be used to increment and access Subcarrier Frequency Registers 1, 2, and 3. The subcarrier frequency registers should not be accessed independently.