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10-Bit, 4× Oversampling SDTV Video Decoder

Data Sheet

ADV7180

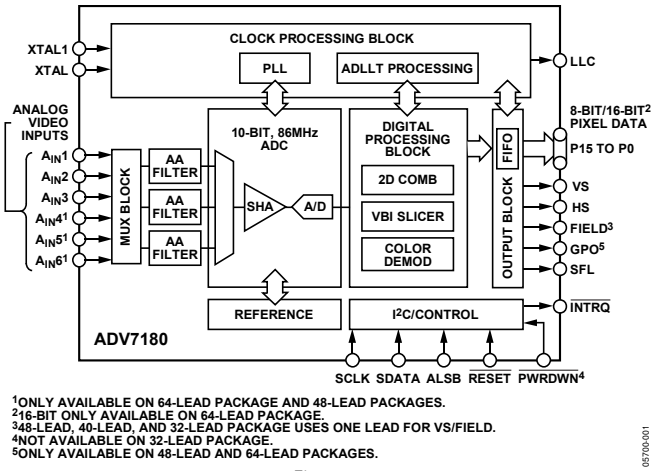
FEATURES

- Qualified for automotive applications
- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit ADC, 4× oversampling for CVBS, 2× oversampling for Y/C mode, and 2× oversampling for YPrPb (per channel)
- 3 video input channels with on-chip antialiasing filter
- CVBS (composite), Y/C (S-Video), and YPrPb (component) video input support
- 5-line adaptive comb filters and CTI/DNR video enhancement
- Mini-TBC functionality provided by adaptive digital line length tracking (ADLLT), signal processing, and enhanced FIFO management
- Integrated AGC with adaptive peak white mode
- Macrovision copy protection detection
- NTSC/PAL/SECAM autodetection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, and FIELD[1]
- 1.0 V analog input signal range
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode and ultralow sleep mode current
- 2-wire serial MPU interface (I²C compatible)
- Single 1.8 V supply possible
- 1.8 V analog, 1.8 V PLL, 1.8 V digital, 1.8 V to 3.3 V I/O supply
- −10°C to +70°C commercial temperature grade
- −40°C to +85°C industrial/automotive qualified temperature grade
- −40°C to +125°C temperature grade for automotive qualified
- 4 package types
  - 64-lead, 10 mm × 10 mm, RoHS compliant LQFP
  - 48-Lead, 7 mm × 7 mm, RoHS compliant LQFP
  - 40-lead, 6 mm × 6 mm, RoHS compliant LFCSP
  - 32-lead, 5 mm × 5 mm, RoHS compliant LFCSP

APPLICATIONS

- Digital camcorders and PDAs
- Low cost SDTV PIP decoders for digital TVs
- Multichannel DVRs for video security
- AV receivers and video transcoding
- PCI-/USB-based video capture and TV tuner cards
- Personal media players and recorders
- Smartphone/multimedia handsets
- In-car/automotive infotainment units
- Rearview camera/vehicle safety systems

FUNCTIONAL BLOCK DIAGRAM



[1]ONLY AVAILABLE ON 64-LEAD PACKAGE AND 48-LEAD PACKAGES.
[2]16-BIT ONLY AVAILABLE ON 64-LEAD PACKAGE.
[3]48-LEAD, 40-LEAD, AND 32-LEAD PACKAGE USES ONE LEAD FOR VS/FIELD.
[4]NOT AVAILABLE ON 32-LEAD PACKAGE.
[5]ONLY AVAILABLE ON 48-LEAD AND 64-LEAD PACKAGES.

05700-001

Figure 1.

GENERAL DESCRIPTION

The ADV7180 automatically detects and converts standard analog baseband television signals compatible with worldwide NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with the 8-bit ITU-R BT.656 interface standard.

The simple digital output interface connects gluelessly to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices, Inc., digital video encoders, such as the ADV7391. External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs, if required. Accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution. Three analog video input channels accept standard composite, S-Video, or component video signals, supporting a wide range of consumer video sources. AGC and clamp-restore circuitry allow an input video signal peak-to-peak range to 1.0 V. Alternatively, these can be bypassed for manual settings.

The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% line length variation. Output control signals allow glueless interface connections in many applications. The ADV7180 is programmed via a 2-wire, serial bidirectional port (I²C-compatible) and is fabricated in a 1.8 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. LFCSP package options make the decoder ideal for space-constrained portable applications. The 64-lead LQFP package is pin compatible with the ADV7181C.

[1] The 48-Lead LQFP, 40-lead LFCSP, and 32-lead LFCSP use one pin to output VS or FIELD.

Rev. J
Document Feedback

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- ADV7180 Evaluation Boards

DOCUMENTATION

Application Notes

- AN-1180: Optimizing Video Platforms for Automated Post-Production Self-Tests
- AN-1240: Low Cost Video Multiplexer for Video Switching Using the ADA4853-2 Op Amp with Disable Function
- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers
- AN-850: Adaptive Digital Line Length Tracking

Data Sheet

- ADV7180: 10-Bit, 4x Oversampling SDTV Video Decoder Data Sheet

TOOLS AND SIMULATIONS

- ADV7180 IBIS Models

REFERENCE DESIGNS

- CN0060
- CN0263

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analog Video Time Base Correction and Processing for Nonstandard TV Signals
- Optimizing standard-definition video on high-definition displays

DESIGN RESOURCES

- ADV7180 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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1/06—Revision 0: Initial Version

INTRODUCTION

The ADV7180 is a versatile one-chip multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format.

The simple digital output interface connects gluelessly to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices digital video encoders, such as the ADV7391. External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs that do not support the ITU-R BT.656 interface standard. The different package options available for the ADV7180 are shown in Table 2.

ANALOG FRONT END

The ADV7180 analog front end comprises a single high speed, 10-bit analog-to-digital converter (ADC) that digitizes the analog video signal before applying it to the standard definition processor. The analog front end employs differential channels to the ADC to ensure high performance in mixed-signal applications.

The front end also includes a 3-channel input mux that enables multiple composite video signals to be applied to the ADV7180. Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter. A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 29). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7180.

Table 1 shows the three ADC clocking rates that are determined by the video input format to be processed—that is, INSEL[3:0]. These clock rates ensure 4× oversampling per channel for CVBS mode and 2× oversampling per channel for Y/C and YPrPb modes.

Table 1. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)[2]	86	2×
YPrPb	86	2×

[1] Based on a 28.6363 MHz crystal between the XTAL and XTAL1 pins.
[2] See INSEL[3:0] in Table 107 for the mandatory write for Y/C (S-Video) mode.

STANDARD DEFINITION PROCESSOR

The ADV7180 is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported by the video processor include PAL B/D/I/G/H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7180 can automatically detect the video standard and process it accordingly.

The ADV7180 has a five-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7180.

The ADV7180 implements a patented ADLLT™ algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7180 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7180 contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The video processor can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar® 1×/2×, and extended data service (XDS). Teletext data slicing for world standard teletext (WST), along with program delivery control (PDC) and video programming service (VPS), are provided. Data is transmitted via the 8-bit video output port as ancillary data packets (ANC). The ADV7180 is fully Macrovision® certified; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

Table 2. ADV7180 Selection Guide

Part Number[1]	Package Type	Analog Inputs	Digital Outputs	Temperature Grade
ADV7180KCP32Z	32-lead LFCSP	3	8-bit	−10°C to +70°C
ADV7180WBCP32Z (Automotive)	32-lead LFCSP	3	8-bit	−40°C to +85°C
ADV7180BCPZ	40-lead LFCSP	3	8-bit	−40°C to +85°C
ADV7180WBCPZ (Automotive)	40-lead LFCSP	3	8-bit	−40°C to +125°C
ADV7180BSTZ	64-lead LQFP	6	8-bit/16-bit	−40°C to +85°C
ADV7180WBSTZ (Automotive)	64-lead LQFP	6	8-bit/16-bit	−40°C to +125°C
ADV7180WBST48Z (Automotive)	48-lead LQFP	6	8-bit	−40°C to +85°C

[1] W = Automotive qualification completed.

FUNCTIONAL BLOCK DIAGRAMS

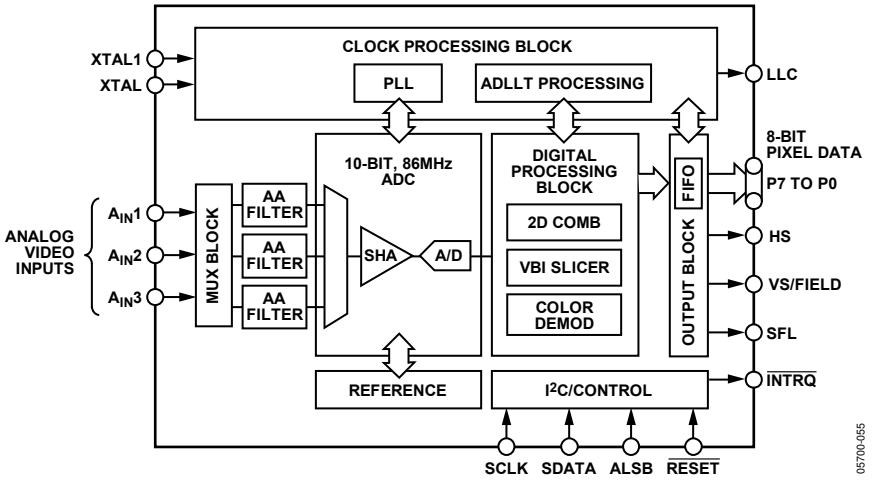


Figure 2. 32-Lead LFCSP Functional Diagram

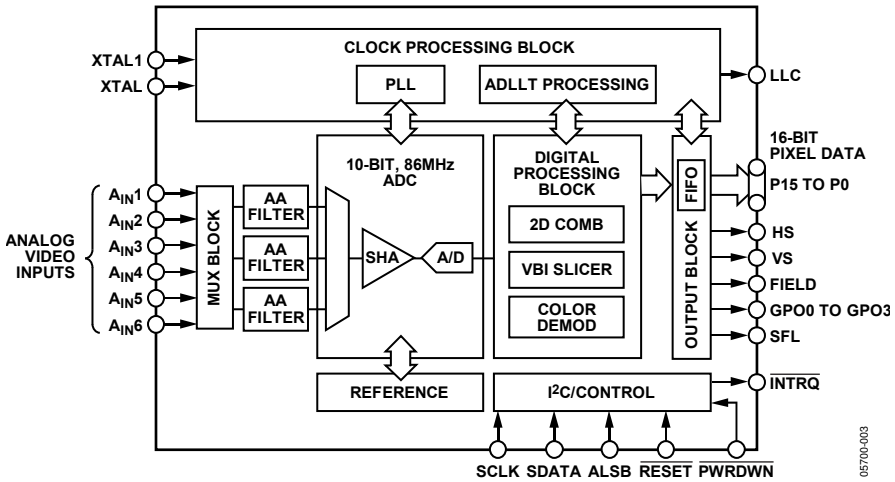


Figure 3. 64-Lead LQFP Functional Block Diagram

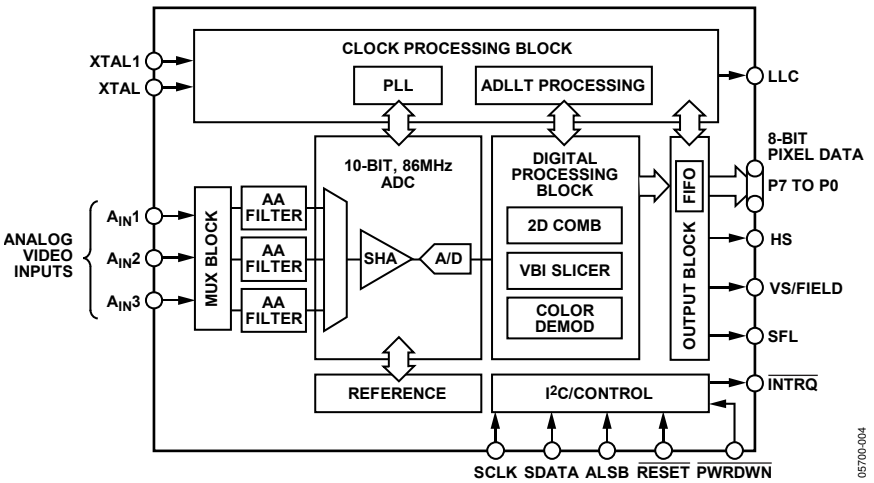


Figure 4. 40-Lead LFCSP Functional Block Diagram

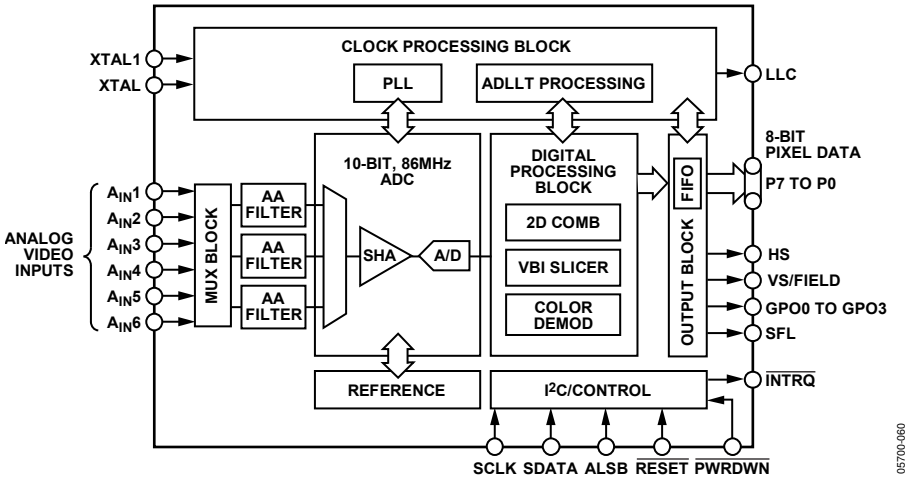


Figure 5. 48-Lead LQFP Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL in CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		−0.6/+0.6		LSB
DIGITAL INPUTS						
Input High Voltage (DVDDIO = 3.3 V)	V_{IH}		2			V
Input High Voltage (DVDDIO = 1.8 V)	V_{IH}		1.2			V
Input Low Voltage (DVDDIO = 3.3 V)	V_{IL}				0.8	V
Input Low Voltage (DVDDIO = 1.8 V)	V_{IL}				0.4	V
Crystal Inputs	V_{IH}		1.2			V
	V_{IL}				0.4	V
Input Current	I_{IN}		−10		+10	µA
Input Current (SDA, SCLK)[1]	I_{IN}		−10		+15	µA
Input Current ($\overline{\text{PWRDWN}}$)[2]	I_{IN}		−10		+48	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage (DVDDIO = 3.3 V)	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output High Voltage (DVDDIO = 1.8 V)	V_{OH}	I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage (DVDDIO = 3.3 V)	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Output Low Voltage (DVDDIO = 1.8 V)	V_{OL}	I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[3, 4, 5]						
Digital Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		1.62	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2.0	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Supply Current	I_{DVDD}			77	85	mA
Digital I/O Supply Current[6]	I_{DVDDIO}			3	5	mA
PLL Supply Current	I_{PVDD}			12	15	mA
Analog Supply Current	I_{AVDD}	CVBS input[7]		33	43	mA
		CVBS input[8]		43	53	mA
		Y/C input		59	75	mA
		YPrPb input		77	94	mA
Power-Down Current	I_{DVDD}			6	10	µA
	I_{DVDDIO}			0.1	1	µA
	I_{PVDD}			1	5	µA
	I_{AVDD}			1	5	µA
Total Power Dissipation in Power-Down Mode[9]				15	44	µW
Power-Up Time	t_{PWRUP}			20		ms

[1] ADV7180KCP32Z, ADV7180WBCP32Z, and ADV7180WBST48Z only.
[2] Applies to ADV7180WBST48Z, ADV7180WBST48Z-RL, ADV7180KST48Z, ADV7180KST48Z-RL, ADV7180BST48Z, ADV7180BST48Z-RL only.
[3] Guaranteed by characterization.
[4] Typical current consumption values are recorded with nominal voltage supply levels and a SMPTEBAR pattern.
[5] Maximum current consumption values are recorded with maximum rated voltage supply levels and a multiburst pattern.
[6] Typical (Typ) number is measured with DVDDIO = 3.3 V and maximum (Max) number is measured with DVDDIO = 3.6 V.
[7] CVBS input when CVBS_IBIAS[3:0] (User Map, Register 0x52, Bits[3:0]) equal 0b'1011.
[8] CVBS input when CVBS_IBIAS[3:0] (User Map, Register 0x52, Bits [3:0]) equal 0b'1101. Recommended setting.
[9] ADV7180 clocked.

VIDEO SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulate five-step [NTSC]		0.6		Degrees
Differential Gain	DG	CVBS input, modulate five-step [NTSC]		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step [NTSC]		2.0		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed				100		Lines
Chroma Luma Gain Delay	CVBS			2.9		ns
	Y/C			5.6		ns
	YPrPb			−3.0		ns
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

TIMING SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.6363		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Times	t_6				300	ns
SCLK and SDA Fall Times	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{SETUP} = t_{10} - t_{11}$)			3.6	ns
Data Output Transitional Time	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 - t_{12}$)			2.4	ns

Timing Diagrams

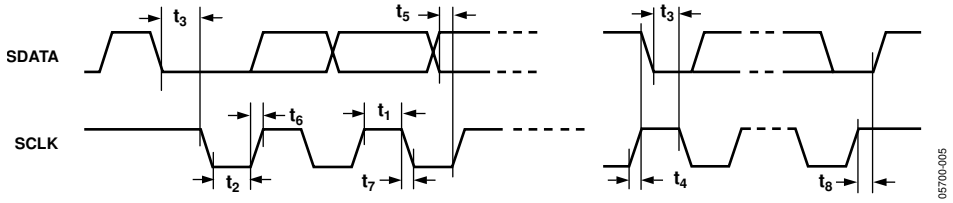


Figure 6. I²C Timing

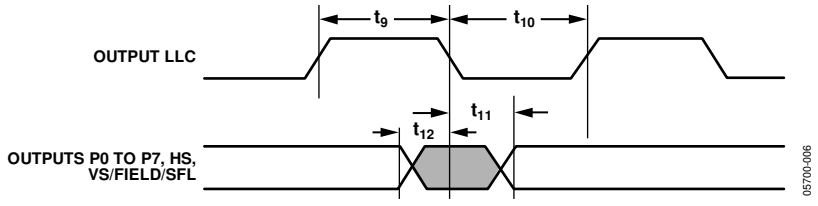


Figure 7. Pixel Port and Control Output Timing

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 6.

Parameter	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large-Clamp Source Current			0.4		mA
Large-Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		µA
Fine Clamp Sink Current			10		µA

THERMAL SPECIFICATIONS

Table 7.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 32-lead LFCSP		32.5		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 32-lead LFCSP		2.3		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 40-lead LFCSP		30		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 40-lead LFCSP		3		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 64-lead LQFP		47		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 64-lead LQFP		11.1		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 48-lead LQFP		50		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 48-lead LQFP		20		°C/W

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
A_{VDD} to AGND	2.2 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to A_{VDD}	−0.3 V to +4 V
P_{VDD} to D_{VDD}	−0.3 V to +0.9 V
D_{VDDIO} to P_{VDD}	−0.3 V to +4 V
D_{VDDIO} to D_{VDD}	−0.3 V to +4 V
A_{VDD} to P_{VDD}	−0.3 V to +0.3 V
A_{VDD} to D_{VDD}	−0.3 V to +0.9 V
Digital Inputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to AGND	AGND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

32-LEAD LFCSP

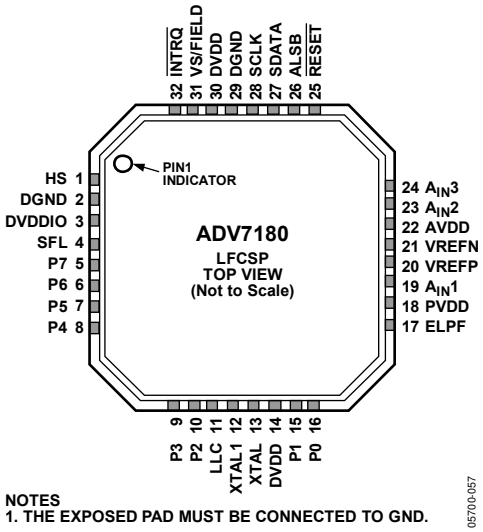


Figure 8. 32-Lead LFCSP Pin Configuration

Table 9. 32-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	HS	O	Horizontal Synchronization Output Signal.
2, 29	DGND	G	Ground for Digital Supply.
3	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
4	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
5 to 10, 15, 16	P7 to P2, P1, P0	O	Video Pixel Output Port.
11	LLC	O	Line-Locked Output Clock for the Output Pixel Data. Nominally 27 MHz but varies up or down according to video line length.
12	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
13	XTAL	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
14, 30	DVDD	P	Digital Supply Voltage (1.8 V).
17	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 60.
18	PVDD	P	PLL Supply Voltage (1.8 V).
19, 23, 24	$A_{IN}1$ to $A_{IN}3$	I	Analog Video Input Channels.
20	VREFP	O	Internal Voltage Reference Output. See Figure 60 for recommended output circuitry.
21	VREFN	O	Internal Voltage Reference Output. See Figure 60 for recommended output circuitry.
22	AVDD	P	Analog Supply Voltage (1.8 V).
25	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
26	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
27	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
28	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
31	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
32	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
	EPAD (EP)		The exposed pad must be connected to GND.

40-LEAD LFCSP

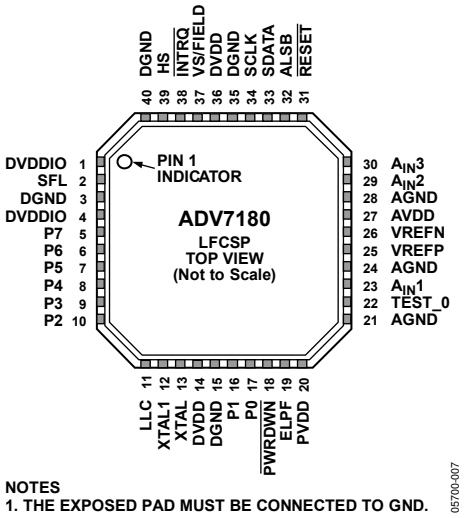


Figure 9. 40-Lead LFCSP Pin Configuration

Table 10. 40-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
2	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
3, 15, 35, 40	DGND	G	Ground for Digital Supply.
5 to 10, 16, 17	P7 to P2, P1, P0	O	Video Pixel Output Port.
11	LLC	O	Line-Locked Output Clock for the Output Pixel Data. Nominally 27 MHz but varies up or down according to video line length.
12	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
13	XTAL	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
14, 36	DVDD	P	Digital Supply Voltage (1.8 V).
18	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 into power-down mode.
19	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 57.
20	PVDD	P	PLL Supply Voltage (1.8 V).
21, 24, 28	AGND	G	Ground for Analog Supply.
22	TEST_0	I	This pin must be tied to DGND.
23, 29, 30	$A_{IN}1$ to $A_{IN}3$	I	Analog Video Input Channels.
25	VREFP	O	Internal Voltage Reference Output. See Figure 57 for recommended output circuitry.
26	VREFN	O	Internal Voltage Reference Output. See Figure 57 for recommended output circuitry.
27	AVDD	P	Analog Supply Voltage (1.8 V).
31	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
32	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
33	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
34	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
37	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
38	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
39	HS	O	Horizontal Synchronization Output Signal.
	EPAD (EP)		The exposed pad must be connected to GND.

64-LEAD LQFP

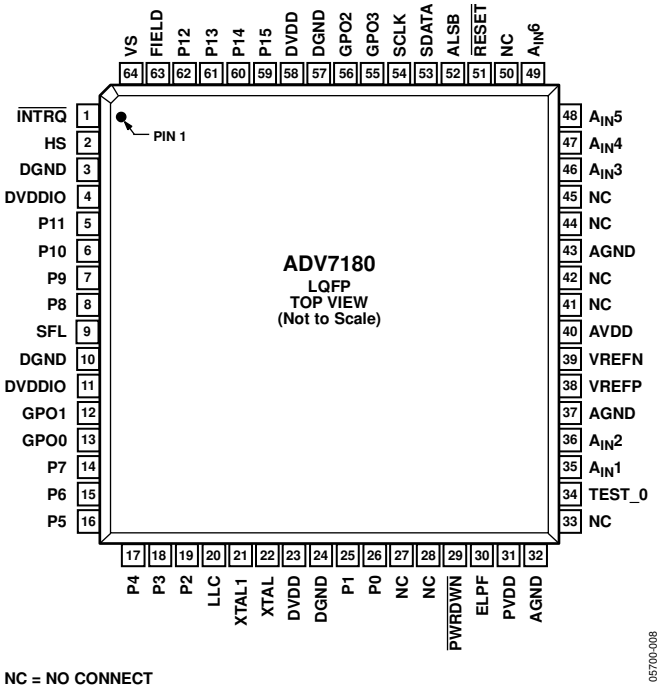


Figure 10. 64-Lead LQFP Pin Configuration

Table 11. 64-Lead LQFP Pin Function Description

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
2	HS	O	Horizontal Synchronization Output Signal.
3, 10, 24, 57	DGND	G	Digital Ground.
4, 11	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
5 to 8, 14 to 19, 25, 26, 59 to 62	P11 to P8, P7 to P2, P1, P0, P15 to P12	O	Video Pixel Output Port. See Table 100 for output configuration for 8-bit and 16-bit modes.
9	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
12, 13, 55, 56	GPO0 to GPO3	O	General-Purpose Outputs. These pins can be configured via I^2C to allow control of external devices.
20	LLC	O	This is a line-locked output clock for the pixel data output by the ADV7180. It is nominally 27 MHz but varies up or down according to video line length.
21	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
22	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or this pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
23, 58	DVDD	P	Digital Supply Voltage (1.8 V).
27, 28, 33, 41, 42, 44, 45, 50	NC		No Connect. These pins are not connected internally.
29	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 in power-down mode.
30	ELPF	I	The recommended external loop filter must be connected to the ELPF pin, as shown in Figure 58.
31	PVDD	P	PLL Supply Voltage (1.8 V).
32, 37, 43	AGND	G	Analog Ground.
34	TEST_0	I	This pin must be tied to DGND.
35, 36, 46 to 49	$A_{IN}1$ to $A_{IN}6$	I	Analog Video Input Channels.
38	VREFP	O	Internal Voltage Reference Output. See Figure 58 for recommended output circuitry.

Pin No.	Mnemonic	Type	Description
39	VREFN	O	Internal Voltage Reference Output. See Figure 58 for recommended output circuitry.
40	AVDD	P	Analog Supply Voltage (1.8 V).
51	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
52	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
53	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
54	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
63	FIELD	O	Field Synchronization Output Signal.
64	VS	O	Vertical Synchronization Output Signal.

48-LEAD LQFP

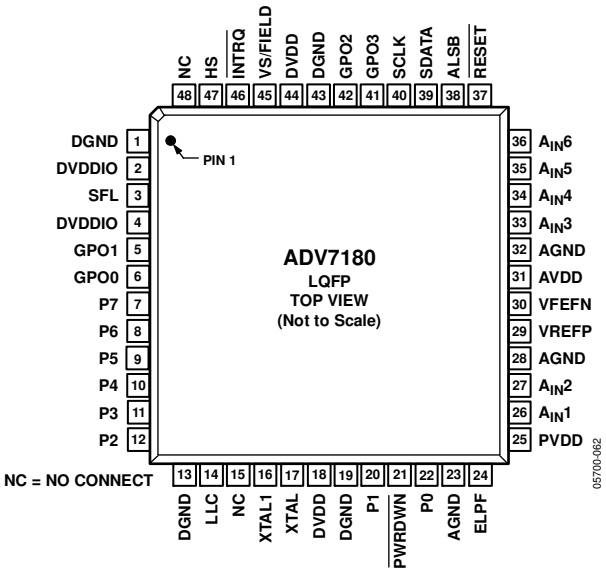


Figure 11. 48-Lead LQFP Pin Configuration

Table 12. 48-Lead LQFP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 13, 19, 43	DGND	G	Digital Ground.
2, 4	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
3	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
5, 6, 41, 42	GPO0 to GPO3	O	General-Purpose Outputs. These pins can be configured via I²C to allow control of external devices.
7 to 12, 20, 22	P7 to P2, P1, P0	O	Video Pixel Output Port. See Table 100 for output configuration for 8-bit and 16-bit modes.
14	LLC	O	This is a line-locked output clock for the pixel data output by the ADV7180. It is nominally 27 MHz but varies up or down according to video line length.
15, 48	NC		No Connect Pins. These pins are not connected internally.
16	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
17	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or this pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
18, 44	DVDD	P	Digital Supply Voltage (1.8 V).
21	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 in power-down mode.
23, 28, 32	AGND	G	Analog Ground.
24	ELPF	I	The recommended external loop filter must be connected to the ELPF pin, as shown in Figure 59.
25	PVDD	P	PLL Supply Voltage (1.8 V).
26, 27, 33 to 36	$A_{IN}1$ to $A_{IN}6$	I	Analog Video Input Channels.
29	VREFP	O	Internal Voltage Reference Output. See Figure 59 for recommended output circuitry.
30	VREFN	O	Internal Voltage Reference Output. See Figure 59 for recommended output circuitry.
31	AVDD	P	Analog Supply Voltage (1.8 V).
37	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
38	ALSB	I	This pin selects the I²C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
39	SDATA	I/O	I²C Port Serial Data Input/Output Pin.
40	SCLK	I	I²C Port Serial Clock Input. The maximum clock rate is 400 kHz.
45	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
46	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
47	HS	O	Horizontal Synchronization Output Signal.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The power-up sequence for the ADV7180 is to power up all power supplies simultaneously. If this is not possible, the 3.3 V supply (D_{VDDIO}) must be established first. When the 3.3 V supply is stable, power up the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}) as quickly as possible. Until the 1.8 V supplies are fully established, all digital pins are in an undefined state.

During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

Take care to ensure that a lower rated supply does not go above a higher rated supply. For example, the 3.3 V D_{VDDIO} supply must never drop below a 1.8 V supply such as the D_{VDD}, P_{VDD}, or A_{VDD}.

To power up the ADV7180, follow these steps.

1. Assert the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin (that is, pull the pins low.)
2. Power up the 3.3 V supply (D_{VDDIO}) and 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}) simultaneously.[1, 2]
3. When all supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high. Note that this step can be ignored on the 32-lead LFCSP, as the $\overline{\text{PWRDWN}}$ pin is not available.
4. Wait 5 ms, then pull the $\overline{\text{RESET}}$ pin high.
5. When all power supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7180.

POWER-DOWN SEQUENCE

The ADV7180 supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY

The ADV7180 can operate with a D_{VDDIO} supply at a nominal value of 1.8 V. Therefore, it is possible to power up all the supplies for the ADV7180 (D_{VDD}, A_{VDD}, P_{VDD}, and D_{VDDIO}) to 1.8 V.

When D_{VDDIO} is at a nominal value of 1.8 V, power up the ADV7180 in the following manner:

1. Follow the power-up sequence described in the Power-Up Sequence section, but power up the D_{VDDIO} supply to 1.8 V instead of 3.3 V. In addition, power up the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin to 1.8 V instead of 3.3 V.
2. Set the drive strengths of the digital outputs of the ADV7180 to their maximum setting. See the Global Pin Control section.
3. Connect any pull-up resistors connected to pins on the ADV7180, such as the SCLK pin and the SDATA pin, to 1.8 V, rather than 3.3 V.

[1] If it is not possible to power up the D_{VDDIO} and 1.8 V supplies simultaneously, the D_{VDDIO} supply must be powered up first. When the D_{VDDIO} is stable, power up the 1.8 V supplies as quickly as possible.
[2] During power-up, take care to ensure that the D_{VDDIO} supply never drops below any of the 1.8 V supplies.

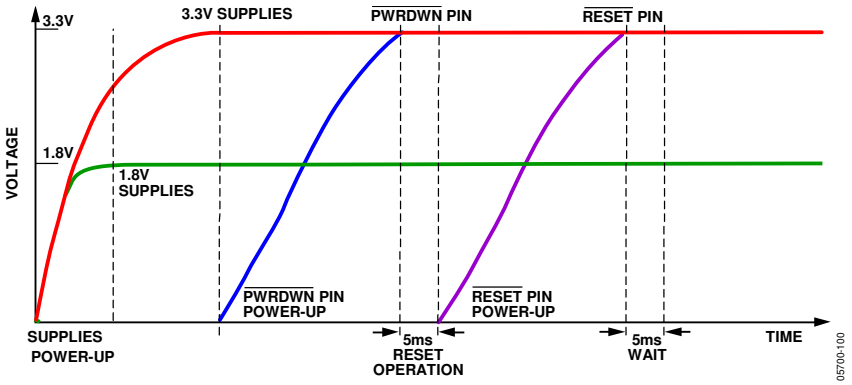


Figure 12. Power-Up Sequence of the 40-Lead LFCSP, 48-Lead LQFP, and 64-Lead LQFP

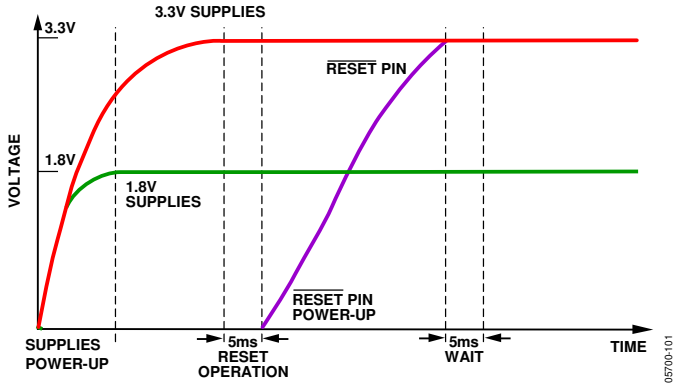


Figure 13. Power-Up Sequence of the 32-Lead LFCSP

ANALOG FRONT END

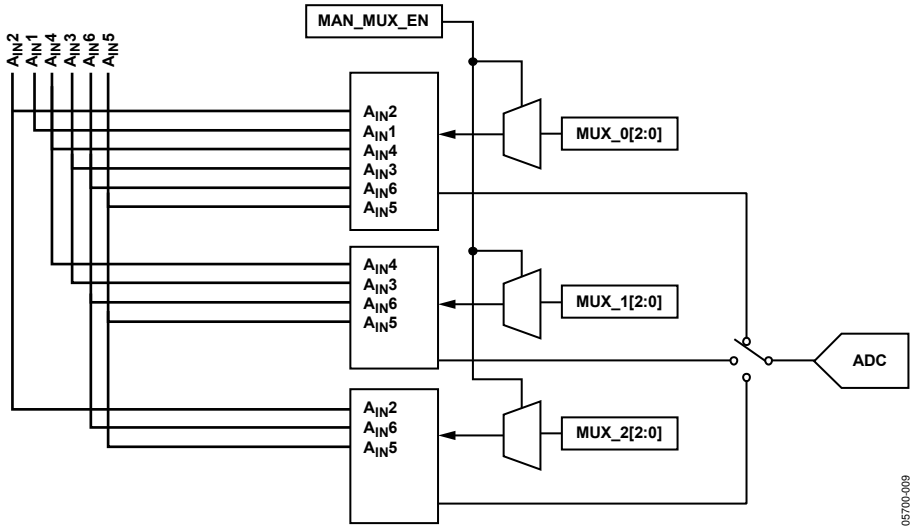


Figure 14. 64-Lead and 48-Lead LQFP Internal Pin Connections

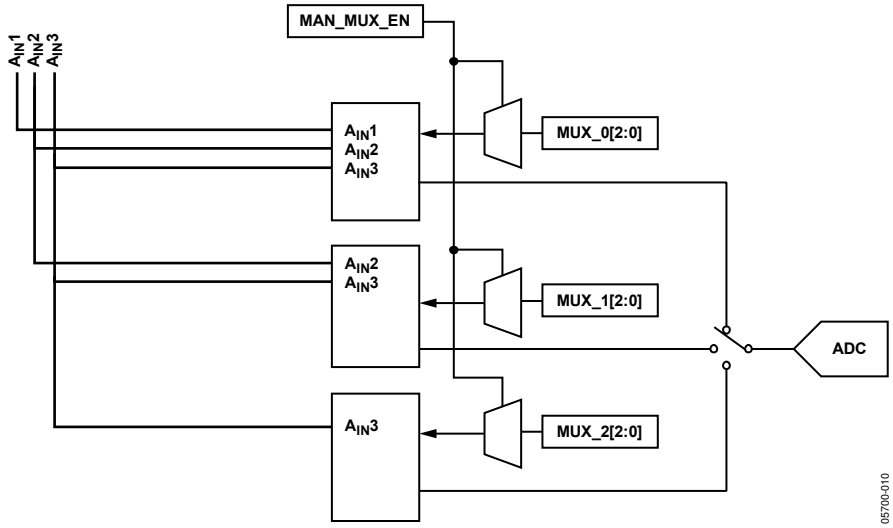


Figure 15. 40-Lead and 32-Lead LFCSP Internal Pin Connections

INPUT CONFIGURATION

The following are the two key steps for configuring the ADV7180 to correctly decode the input video:

1. Use INSEL[3:0] to configure the routing and format decoding (CVBS, Y/C, or YPrPb). For the 64-lead and 48-lead LQFP, see Table 13. For the 40-lead and 32-lead LFCSP, see Table 14.
2. If the input requirements are not met using the INSEL[3:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. The standard definition processor block, which decodes the digital data, must be configured to process the CVBS, Y/C, or YPrPb format. This is performed by INSEL[3:0] selection.

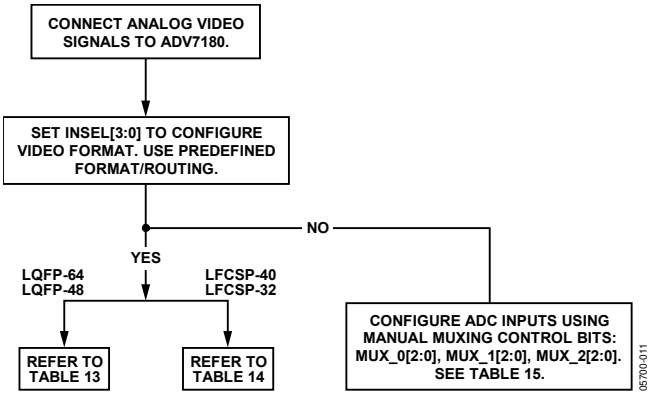


Figure 16. Signal Routing Options

INSEL[3:0], Input Selection, Address 0x00[3:0]

The INSEL bits allow the user to select the input format. They also configure the standard definition processor core to process composite (CVBS), S-Video (Y/C), or component (YPrPb) format.

INSEL[3:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 13 and Table 14). This allows the user to route the various video signal types to the decoder and select them using INSEL[3:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 13. 64-Lead and 48-Lead LQFP INSEL[3:0]

INSEL[3:0]	Video Format	Analog Input
0000	Composite	CVBS input on $A_{IN}1$
0001	Composite	CVBS input on $A_{IN}2$
0010	Composite	CVBS input on $A_{IN}3$
0011	Composite	CVBS input on $A_{IN}4$
0100	Composite	CVBS input on $A_{IN}5$
0101	Composite	CVBS input on $A_{IN}6$
0110	Y/C (S-Video)	Y input on $A_{IN}1$
		C input on $A_{IN}4$
0111	Y/C (S-Video)	Y input on $A_{IN}2$
		C input on $A_{IN}5$
1000	Y/C (S-Video)	Y input on $A_{IN}3$
		C input on $A_{IN}6$
1001	YPrPb	Y input on $A_{IN}1$
		Pb input on $A_{IN}4$
		Pr input on $A_{IN}5$
1010	YPrPb	Y input on $A_{IN}2$
		Pr input on $A_{IN}6$
		Pb input on $A_{IN}3$
1011 to 1111	Reserved	Reserved

Table 14. 40-Lead and 32-Lead LFCSP INSEL[3:0]

INSEL[3:0]	Video Format	Analog Input
0000	Composite	CVBS input on $A_{IN}1$
0001 to 0010	Reserved	Reserved
0011	Composite	CVBS input on $A_{IN}2$
0100	Composite	CVBS input on $A_{IN}3$
0101	Reserved	Reserved
0110	Y/C (S-Video)	Y input on $A_{IN}1$
		C input on $A_{IN}2$
0111 to 1000	Reserved	Reserved
1001	YPrPb	Y input on $A_{IN}1$
		Pr input on $A_{IN}3$
		Pb input on $A_{IN}2$
1010 to 1111	Reserved	Reserved

ANALOG INPUT MUXING

The ADV7180 has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 14 and Figure 15 outline the overall structure of the input muxing provided in the ADV7180.

A maximum of six CVBS inputs can be connected to and decoded by the 64-lead and 48-lead devices, and a maximum of three CVBS inputs can be connected to and decoded by the 40-lead and 32-lead LFCSP devices. As shown in the Pin Configurations and Function Descriptions section, these analog input pins lie in close proximity to one another, which requires careful design of the printed circuit board (PCB) layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended to connect any unused analog input pins to AGND to act as a shield.

MAN_MUX_EN, Manual Input Muxing Enable, Address 0xC4[7]

To configure the ADV7180 analog muxing section, the user must select the analog input ($A_{IN}1$ to $A_{IN}6$ for the 64-lead LQFP and 48-lead devices or $A_{IN}1$ to $A_{IN}3$ for the 40-lead and 32-lead LFCSP devices) that is to be processed by the ADC. MAN_MUX_EN must be set to 1 to enable the following muxing blocks:

- MUX0[2:0], ADC Mux Configuration, Address 0xC3[2:0]
- MUX1[2:0], ADC Mux Configuration, Address 0xC3[6:4]
- MUX2[2:0], ADC Mux Configuration, Address 0xC4[2:0]

The three mux sections are controlled by the signal buses MUX0/MUX1/MUX2[2:0]. Table 15 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX0. For example, in a Y/C input configuration, MUX0 should be connected to the Y channel and MUX1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers should be powered down (see the description of Register 0x3A in Table 107).

Table 15. Manual Mux Settings for the ADC (MAN_MUX_EN Must be Set to 1)

	ADC Connected To			ADC Connected To			ADC Connected To	
MUX0[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32	MUX1[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32	MUX2[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32
000	No connect	No connect	000	No connect	No connect	000	No connect	No connect
001	$A_{IN}1$	$A_{IN}1$	001	No connect	No connect	001	No connect	No connect
010	$A_{IN}2$	No connect	010	No connect	No connect	010	$A_{IN}2$	No connect
011	$A_{IN}3$	No connect	011	$A_{IN}3$	No connect	011	No connect	No connect
100	$A_{IN}4$	$A_{IN}2$	100	$A_{IN}4$	$A_{IN}2$	100	No connect	No connect
101	$A_{IN}5$	$A_{IN}3$	101	$A_{IN}5$	$A_{IN}3$	101	$A_{IN}5$	$A_{IN}3$
110	$A_{IN}6$	No connect	110	$A_{IN}6$	No connect	110	$A_{IN}6$	No connect
111	No connect	No connect	111	No connect	No connect	111	No connect	No connect

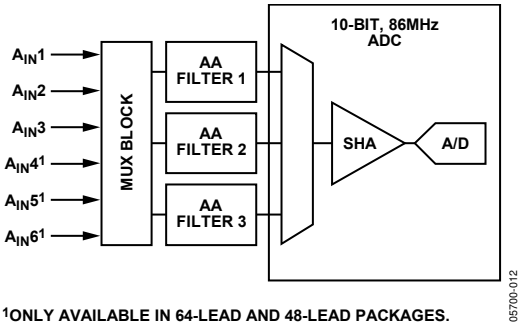
Note the following:

- CVBS can only be processed by MUX0.
- Y/C can only be processed by MUX0 and MUX1.
- YPrPb can only be processed by MUX0, MUX1, and MUX2.

ANTIALIASING FILTERS

The ADV7180 has optional on-chip antialiasing (AA) filters on each of the three channels that are multiplexed to the ADC (see Figure 17). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 18 and Figure 19 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[3:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.



1ONLY AVAILABLE IN 64-LEAD AND 48-LEAD PACKAGES.

Figure 17. Antialias Filter Configuration

AA_FILT_MAN_OVR, Antialiasing Filter Override, Address 0xF3[3]

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[3:0].

AA_FILT_EN, Antialiasing Filter Enable, Address 0xF3[2:0]

These bits allow the user to enable or disable the antialiasing filters on each of the three input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filter and is routed directly to the ADC.

AA_FILT_EN, Address 0xF3[0]

When AA_FILT_EN[0] is 0, AA Filter 1 is bypassed.

When AA_FILT_EN[0] is 1, AA Filter 1 is enabled.

AA_FILT_EN, Address 0xF3[1]

When AA_FILT_EN[1] is 0, AA Filter 2 is bypassed.

When AA_FILT_EN[1] is 1, AA Filter 2 is enabled.

AA_FILT_EN, Address 0xF3[2]

When AA_FILT_EN[2] is 0, AA Filter 3 is bypassed.

When AA_FILT_EN[2] is 1, AA Filter 3 is enabled.

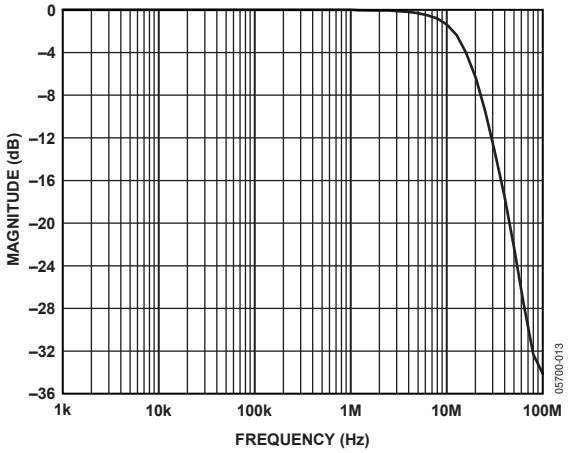


Figure 18. Antialiasing Filter Magnitude Response

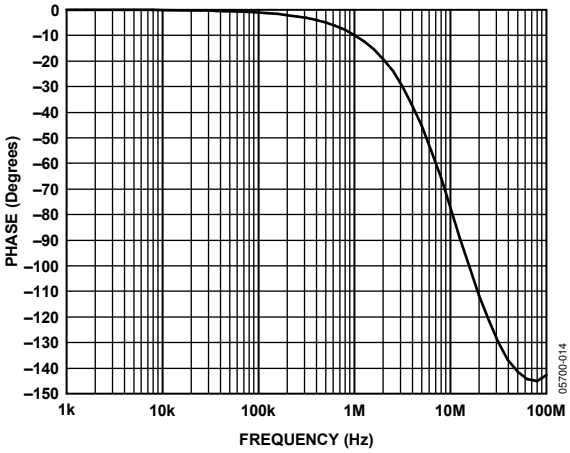


Figure 19. Antialiasing Filter Phase Response

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVING MODES

Power-Down

PDBP, Address 0x0F[2]

The digital supply of the ADV7180 can be shut down by using the $\overline{\text{PWRDWN}}$ pin or via I²C[1] (see the PWRDWN, Address 0x0F[5] section). PDBP controls whether the I²C control or the pin has the higher priority. The default is to give the pin ($\overline{\text{PWRDWN}}$) priority[2]. This allows the user to have the ADV7180 powered down by default at power-up without the need for an I²C write.

When PDBP is 0 (default), the digital supply power is controlled by the $\overline{\text{PWRDWN}}$ pin[2] (the PWRDWN bit, Address 0x0F[5], is disregarded).

When PDBP is 1, the PWRDWN bit has priority (the pin is disregarded).

PWRDWN, Address 0x0F[5]

When PDBP is set to 1, setting the PWRDWN bit switches the ADV7180 to a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No I²C bits are lost during power-down. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I²C interface is unaffected and remains operational in power-down mode.

The ADV7180 leaves the power-down state if the PWRDWN bit is set to 0 (via I²C) or if the ADV7180 is reset using the $\overline{\text{RESET}}$ pin.

PDBP must be set to 1 for the PWRDWN bit to power down the ADV7180.

When PWRDWN is 0 (default), the chip is operational. When PWRDWN is 1, the ADV7180 is in a chip-wide power-down mode.

RESET CONTROL

Reset, Chip Reset, Address 0x0F[7]

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7180, issues a full chip reset. All I²C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register tables (see Table 107 and Table 108). After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the part returns to the default for its primary mode of operation. All I²C bits are loaded with their default values, making this bit self-clearing.

Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I²C writes are performed.

The I²C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the MPU Port Description section).

When the reset bit is 0 (default), operation is normal.

When the reset bit is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Three-State Output Drivers

TOD, Address 0x03[6]

This bit allows the user to three-state the output drivers of the ADV7180.

Upon setting the TOD bit, the P15 to P0 (P7 to P0 for the 48-lead, 40-lead, and 32-lead devices), HS, VS, FIELD (VS/FIELD pin for the 48-lead, 40-lead, and 32-lead LFCSP), and SFL pins are three-stated.

The timing pins (HS, VS, FIELD) can be forced active via the TIM_OE bit. For more information on three-state control, see the Three-State LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TOD is 0 (default), the output drivers are enabled.

When TOD is 1, the output drivers are three-stated.

Three-State LLC Driver

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC pin of the ADV7180 to be three-stated. For more information on three-state control, refer to the Three-State Output Drivers and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TRI_LLC is 0 (default), the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is 1, the LLC pin drivers are three-stated.

[1] For 32-lead, I²C is the only power-down option.
[2] For 64-lead, 48-lead, and 40-lead only.

Timing Signals Output Enable

TIM_OE, Address 0x04[3]

The TIM_OE bit is regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD into the active state (that is, driving state) even if the TOD bit is set. If TIM_OE is set to low, the HS, VS, and FIELD pins are three-stated depending on the TOD bit. This functionality is beneficial if the decoder is only used as a timing generator. This may be the case if only the timing signals are extracted from an incoming signal or if the part is in free-run mode, where a separate chip can output a company logo, for example.

For more information on three-state control, see the Three-State Output Drivers section and the Three-State LLC Driver section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TIM_OE is 0 (default), HS, VS, and FIELD are three-stated according to the TOD bit.

When TIM_OE is 1, HS, VS, and FIELD are forced active all the time.

Drive Strength Selection (Data)

DR_STR[1:0], Address 0xF4[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[15:0] for the 64-lead device or P[7:0] for the 48-lead, 40-lead, and 32-lead devices output drivers.

Note that DR_STR[1:0] also affects the drive strength of the INTRQ interrupt pin on all ADV7180 models.

For more information on three-state control, see the Drive Strength Selection (Clock) and the Drive Strength Selection (Sync) sections.

Table 16. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Drive Strength Selection (Clock)

DR_STR_C[1:0], Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Sync) and the Drive Strength Selection (Data) sections.

Table 17. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Drive Strength Selection (Sync)

DR_STR_S[1:0], Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and FIELD are driven. For more information, see the Drive Strength Selection (Data) section.

Table 18. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN, Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7180 core to an encoder in a decoder/encoder back-to-back arrangement.

When EN_SFL_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

Polarity LLC Pin

PCLK, Address 0x37[0]

The polarity of the clock that leaves the ADV7180 via the LLC pin can be inverted using the PCLK bit.

Changing the polarity of the LLC clock output may be necessary to meet the setup-and-hold time expectations of follow-on chips.

When PCLK is 0, the LLC output polarity is inverted.

When PCLK is 1 (default), the LLC output polarity is normal (see the Timing Specifications section).