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10-Bit, SDTV Video Decoder with Differential Inputs

Data Sheet

ADV7182A

FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit ADC, 4× oversampling per channel for CVBS, S-Video mode, and YPrPb
- 4 analog video input channels with on-chip antialiasing filter
- Video input support for CVBS (composite), S-Video (Y/C), and YPrPb (component)
- Fully differential, pseudo differential, and single-ended CVBS video input support
- NTSC/PAL/SECAM autodetection
- Up to 4 V common-mode input range solution
- Excellent common-mode rejection capability
- 5-line adaptive comb filters and CTI/DNR video enhancement
- Integrated AGC with adaptive peak white mode
- Fast switch capability
- ACE
- Downdither (8 bits to 6 bits)
- Rovi copy protection detection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, or field synchronization
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode available
- 2-wire serial MPU interface (I^2C compatible)
- Single 1.8 V supply possible
- −40°C to +105°C automotive temperature grade
- −40°C to +85°C industrial qualified temperature grade
- 32-lead, 5 mm × 5 mm, RoHS compliant LFCSP
- Qualified for automotive applications

APPLICATIONS

- Advanced driver assistance
- Automotive infotainment
- DVRs for video security
- Media players

GENERAL DESCRIPTION

The ADV7182A[1] has the same pinout and is software compatible with the ADV7182.

The ADV7182A is a versatile, one chip, multiformat video decoder that automatically detects standard analog baseband video signals and converts them into YCbCr 4:2:2 component video data streams.

The analog input of the ADV7182A features a single, 10-bit analog-to-digital converter (ADC) and an on-chip differential to single-ended converter to accommodate direct connection of differential, pseudo differential, or single-ended CVBS without the need for external amplifier circuitry.

The standard definition processor (SDP) on the ADV7182A automatically detects NTSC, PAL, and SECAM standards in the form of CVBS (composite), S-Video (Y/C), and YPrPb (component). The analog video is converted into a 4:2:2 component video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard. External synchronization timing signals are also available.

The ADV7182A is provided in a space-saving, LFCSP, surface-mount, RoHS compliant package. It is offered in an automotive grade rated over the −40°C to +105°C temperature range, as well as a −40°C to +85°C industrial temperature range, making the device ideal for automotive, industrial, and consumer applications.

The ADV7182A must be configured in accordance with the I^2C writes provided in the evaluation board script files available at www.analog.com/ADV7182A.

[1] Protected by U.S. Patent 5,784,120.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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REVISION HISTORY

9/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

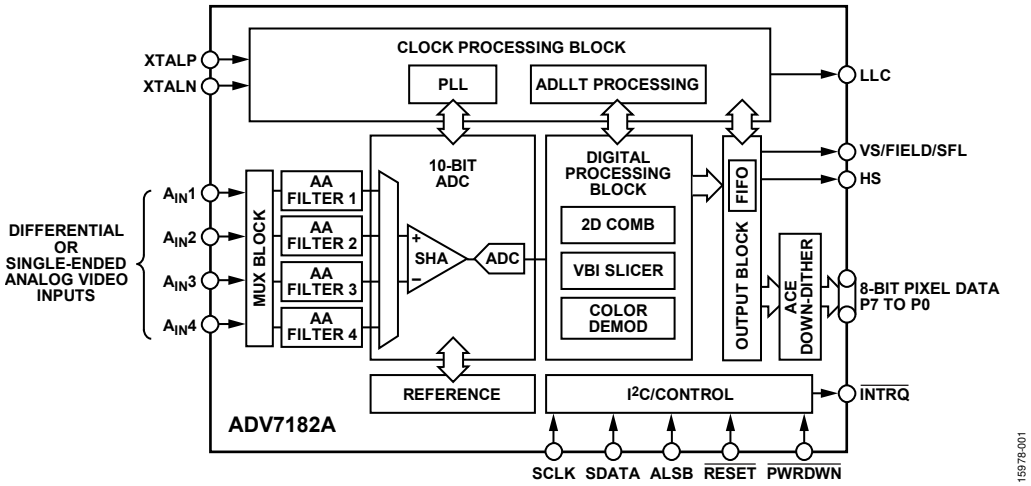

Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}					
D_{VDDIO} = 3.3 V			2			V
D_{VDDIO} = 1.8 V			1.2			V
Input Low Voltage	V_{IL}					
D_{VDDIO} = 3.3 V					0.8	V
D_{VDDIO} = 1.8 V					0.4	V
Crystal Inputs						
V_{IH}			1.2			V
V_{IL}					0.4	V
Input Leakage Current	I_{IN}		−10		+10	µA
SDATA, SCLK			−10		+15	µA
$\overline{PWRDWN}$, ALSB			−10		+48	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}					
D_{VDDIO} = 3.3 V		I_{SOURCE} = 0.4 mA	2.4			V
D_{VDDIO} = 1.8 V		I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage	V_{OL}					
D_{VDDIO} = 3.3 V		I_{SINK} = 3.2 mA			0.4	V
D_{VDDIO} = 1.8 V		I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2]						
Digital Input/Output Power Supply	D_{VDDIO}		1.62	3.3	3.63	V
Phase-Locked Loop (PLL) Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
Digital Input/Output Supply Current	I_{DVDDIO}			3		mA
PLL Supply Current	I_{PVDD}			12		mA
Analog Supply Current	I_{AVDD}	Single-ended CVBS input		47		mA
		Differential CVBS input		69		mA
		Single-ended CVBS fast switch		47		mA
		Differential CVBS fast switch		69		mA
		S-Video input		60		mA
		YPrPb input		75		mA
Digital Supply Current	I_{DVDD}	Single-ended CVBS input		60		mA
		Differential CVBS input		66		mA
		Single-ended CVBS fast switch		60		mA
		Differential CVBS fast switch		66		mA
		S-Video input		60		mA
		YPrPb input		60		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DOWN PERFORMANCE[1]						
Digital Input/Output Supply Power-Down Current						
PLL Supply Power-Down Current	I_{DVDDIO}			73		µA
Analog Supply Power-Down Current	I_{PVDD}			38		µA
Digital Supply Power-Down Current	I_{AVDD}			0.15		µA
Total Power Dissipation in Power-Down Mode	I_{DVDD}			368		µA
				1		mW
CRYSTAL OSCILLATOR[1]						
Transconductance	g_M			30		mA/V

[1] Guaranteed by characterization.
[2] Typical current consumption values are recorded with nominal voltage supply levels and an SMPTEBAR test pattern.

VIDEO SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulate five step		0.9		Degrees
Differential Gain	DG	CVBS input, modulate five step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five step		2.0		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp		57		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection[2]	CMR			75		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±1.3		kHz
Color Lock In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed[3]				100		Lines
Fast Switch Speed[4]				100		ms
LUMA SPECIFICATIONS		CVBS, 1 V input				
Luma Brightness Accuracy				1		%
Luma Contrast Accuracy				1		%

[1] These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.
[2] The CMR of this circuit design is critically dependent on the external resistor matching on its inputs. This measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] Autodetection switch speed is the time it takes the ADV7182A to detect the video format present at its input, for example, PAL I or NTSC M.
[4] Fast switch speed is the time it takes the ADV7182A to switch from one single-ended or differential analog input to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

TIMING SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.63636		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width						
High	t_1		0.6			µs
Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDATA Setup Time	t_5		100			ns
SCLK and SDATA Rise Times	t_6				300	ns
SCLK and SDATA Fall Times	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
$\overline{\text{RESET}}$ FEATURE						
$\overline{\text{RESET}}$ Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{ACCESS} = t_{10} - t_{11}$)			3.8	ns
	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 + t_{12}$)			6.9	ns

Timing Diagrams

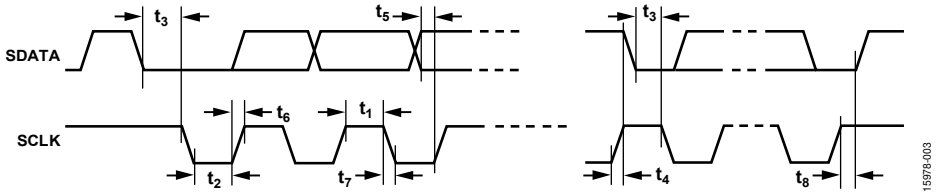

Figure 2. I²C Timing Diagram

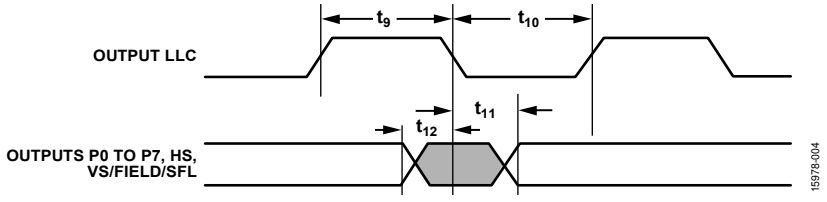

Figure 3. Pixel Port and Control Output Timing Diagram

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp					
Source Current			0.32		mA
Sink Current			0.32		mA
Fine Clamp					
Source Current			7		µA
Sink Current			7		µA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Rating
A_{VDD} to GND	2.2 V
D_{VDD} to GND	2.2 V
P_{VDD} to GND	2.2 V
D_{VDDIO} to GND	4 V
P_{VDD} to D_{VDD}	−0.9 V to +0.9 V
A_{VDD} to D_{VDD}	−0.9 V to +0.9 V
Digital Inputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to Ground	GND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature ($T_{J\,MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	JEDEC J-STD-020

[1] The absolute maximum ratings assume that DGND pins and the exposed pad of the ADV7182A are connected together to a common ground plane (GND); this is part of the recommended layout scheme. See the PCB Layout Recommendations section for more information. The absolute maximum ratings are stated in relation to this common ground plane.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure as per JEDEC JESD51. ψ_{JT} is the junction to top thermal characterization parameter measured on a standard test board, as per JEDEC JESD51, allowing the heat generated in the ADV7182A die to flow normally along preferred thermal conduction paths that more closely represent the thermal flows in a typical application board.

Table 6. Thermal Resistance

Package	θ_{JA}	ψ_{JT}	Unit
CP-32-12[1]	39.6	0.86	°C/W

[1] JEDEC JESD51 2s2p 4-layer PCB with two signal layers and two buried solid ground planes (GND), and with via nine thermal vias connecting the exposed pad to the ground plane (GND).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

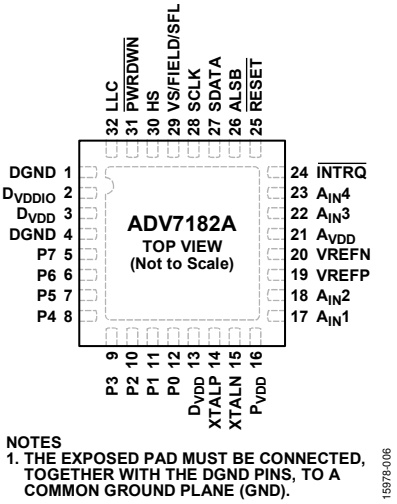

Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital Input/Output Supply Voltage (1.8 V to 3.3 V).
3, 13	D_{VDD}	Power	Digital Supply Voltage (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Port.
14	XTALP	Output	Output Pin for the Crystal Oscillator Amplifier. Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7182A. The crystal used with the ADV7182A must be a fundamental crystal.
15	XTALN	Input	Input Pin for the Crystal Oscillator Amplifier. The crystal used with the ADV7182A must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7182A, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Supply Voltage (1.8 V).
17, 18, 22, 23	$A_{IN}1$ to $A_{IN}4$	Input	Analog Video Input Channels.
19	VREFP	Output	Positive Internal Voltage Reference Output.
20	VREFN	Output	Negative Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Supply Voltage (1.8 V).
24	$\overline{\text{INTRQ}}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
25	$\overline{\text{RESET}}$	Input	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7182A circuitry.
26	ALSB	Input	Address Least Significant Bit. This pin selects the I^2C address for the ADV7182A. For ALSB set to Logic 0, the address selected for a write is 0x40; for ALSB set to Logic 1, the address selected is 0x42.
27	SDATA	Input/ output	I^2C Port Serial Data Input/Output Pin.
28	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
29	VS/FIELD/SFL	Output	Vertical Synchronization Output Signal (VS)/Field Synchronization Output Signal (FIELD)/ Subcarrier Frequency Lock (SFL). This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc., digital video encoder.
30	HS	Output	Horizontal Synchronization Output Signal.
31	$\overline{\text{PWRDWN}}$	Input	Power-Down. A logic low on this pin places the ADV7182A in power-down mode.
32	LLC	Output	Line Locked Clock for Output Pixel Data. This pin is nominally 27 MHz but varies up or down according to the video line length.
	EPAD (EP)		Exposed Ground Pad. The exposed pad must be connected, together with the DGND pins, to a common ground plane (GND).

THEORY OF OPERATION

The ADV7182A is a versatile, multiformat video decoder that automatically detects standard analog baseband video signals and converts them into a YCbCr 4:2:2 component video data stream. The ADV7182A supports video signals compatible with worldwide NTSC, PAL, and SECAM standards.

The analog front end (AFE) of the ADV7182A features a 4-channel input mux, a differential to single-ended converter, and a single 10-bit ADC. The analog video inputs accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources, making the ADV7182A ideal for automotive, industrial, and consumer applications.

The ADV7182A converts these analog video formats into a digital 8-bit ITU-R BT.656 video stream. External HS, VS, and FIELD signals provide timing references for liquid crystal display (LCD) controllers and other video application specific integrated circuits (ASICs).

The digital video output stream of the ADV7182A interfaces easily to a wide range of mobile video processors, MPEG encoders, codecs, and Analog Devices digital video encoders, such as the ADV7391.

The ADV7182A is programmed via a 2-wire, serial bidirectional port (I^2C compatible) and can communicate with other devices using the hardware interrupt pin.

The ADV7182A is fabricated in a low power, 1.8 V CMOS process. The device is provided in a space-saving, LFCSP, surface-mount, RoHS compliant package. The ADV7182A is available in an automotive grade rated over the −40°C to +105°C temperature range, making the ADV7182A ideal for automotive applications. The ADV7182A is also available in a −40°C to +85°C temperature range, making it ideal for consumer or industrial applications.

ANALOG FRONT END (AFE)

The ADV7182A AFE is comprised of a 4-channel input mux, a differential to single-ended converter with clamp circuitry, a set of four antialiasing filters, and a single 10-bit ADC.

The 4-channel input mux enables multiple composite video signals to be applied to the ADV7182A and is software controlled.

The next stage in the AFE features the differential to single-ended converter and the clamp circuitry. The incorporation of a differential front end allows differential video to be connected directly to the ADV7182A. The differential front end enables small and large signal noise rejection, improved electromagnetic interference (EMI), and the ability to absorb ground bounce. The architecture can support true differential, pseudo differential, and single-ended signals.

In conjunction with an external resistor divider, the ADV7182A provides a common-mode input range of 4 V, facilitating in the removal of large signal, common-mode transients present on both video inputs. CMR values of up to 80 dB can be achieved without the need for external amplifier circuitry.

The external resistor divider is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 23). Current and voltage clamps in the circuit attempt to ensure that the video signal remains within the range on the ADC.

The single 10-bit ADC digitizes the analog video before it is applied to the SDP. Table 8 shows the three ADC clocking rates determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, S-Video, and YPrPb modes.

Table 8. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
S-Video (Y/C)[2]	114	4×
YPrPb[2]	172	4×

[1] Based on a 28.63636 MHz clock input to the ADV7182A.
[2] See INSEL[4:0] in Table 96 for writes needed to set S-Video (Y/C) and YPrPb modes.

STANDARD DEFINITION PROCESSOR

The SDP in the ADV7182A is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include PAL B/PAL D/PAL I/PAL G/PAL H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/NTSC J, NTSC 4.43, and SECAM B/SECAM D/SECAM G/SECAM K/SECAM L. The ADV7182A can automatically detect the video standard and process it accordingly.

The ADV7182A features a five-line, superadaptive, 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts the processing mode according to the video standard and signal quality without requiring user intervention. Video user controls, such as brightness, contrast, saturation, and hue, are also available in the ADV7182A.

The ADV7182A implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7182A to track and decode poor quality video sources, such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7182A contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7182A features an automatic gain control (AGC) algorithm to ensure that the optimum luma gain is selected as the input video varies in brightness.

Adaptive contrast enhancement (ACE) is an algorithm that automatically varies the contrast level applied across an image to enhance the picture detail visible. This automatic variation enables the contrast in the dark areas of an image to be increased without saturating the bright areas, which is particularly useful in automotive applications where it can be important to be able to clearly discern objects in shaded areas.

Downdithering from eight bits to six bits enables ease of design for standard LCD panels.

The SDP can handle a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world standard teletext (WST). Data is transmitted via the 8-bit video output port as ancillary data packets (ANC).

The ADV7182A is fully Rovi™ (formerly Macrovision® and now rebranded as TiVo upon acquisition of the same) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The SDP is fully robust to all Rovi signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7182A is guaranteed by production testing.

The optimal power-up sequence for the ADV7182A is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}).

When powering up the ADV7182A, follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7182A.

SIMPLIFIED POWER-UP SEQUENCE

The simplified power-up sequence is guaranteed by characterization.

Alternatively, the ADV7182A can be powered up by asserting all supplies and the $\overline{\text{PWRDWN}}$ pin simultaneously. During this operation, the $\overline{\text{RESET}}$ pin must remain low. After the supplies and $\overline{\text{PWRDWN}}$ are fully asserted, wait at least 5 ms before bringing the $\overline{\text{RESET}}$ pin high. After the $\overline{\text{RESET}}$ pin is fully asserted, wait an additional 5 ms before initiating I^2C communication with the ADV7182A.

While the supplies are being established, take care to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7182A supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY

It is possible to power all the supplies (D_{VDD}, P_{VDD}, A_{VDD}, and D_{VDDIO}) to 1.8 V. In this case, apply the power-up sequences as described in the Optimal Power-Up Sequence section and the Simplified Power-Up Sequence section. The only change is that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V.

In this setup,

- Power up the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin to 1.8 V instead of 3.3 V.
- Set the drive strengths of the digital outputs of the ADV7182A to the maximum setting (see the Global Pin Control section).
- Connect any pull-up resistors connected to pins on the ADV7182A (such as the SCLK pin and the SDATA pin) to 1.8 V and not 3.3 V.

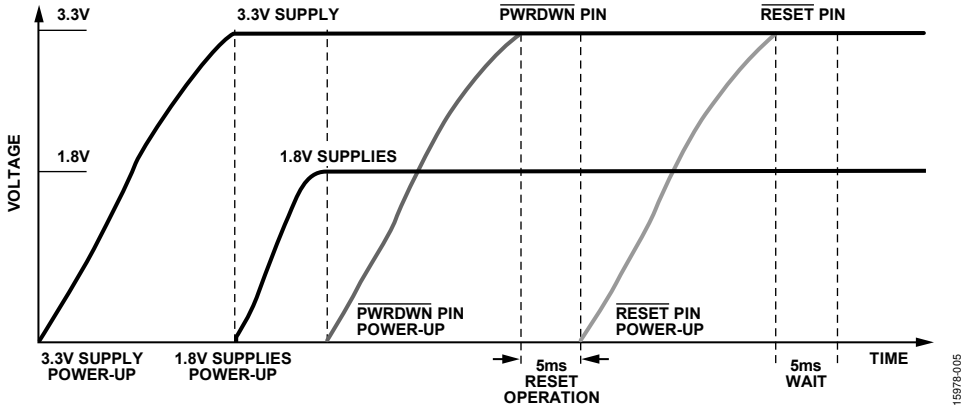

Figure 5. Recommended Power-Up Sequence

CRYSTAL OSCILLATOR DESIGN

The ADV7182A requires a stable and accurate clock source to guarantee operation. This clock is typically provided by a crystal resonator (XTAL), but can also be provided by a clock oscillator.

The required circuitry for an XTAL is shown in Figure 50. A damping resistor (R_{DAMP}) is required on the output of the ADV7182A XTAL amplifier (XTALP). The purpose of this damping resistor is to limit the current flowing through the XTAL and to limit the voltage across the XTAL amplifier. To define the appropriate value of the damping resistor, R_{DAMP} (see the Typical Circuit Connection section), consult the accompanying calculator tool (visit the design resources section at www.analog.com/ADV7182A to download).

The other components in the XTAL circuit must be chosen carefully; for example, incorrectly selected load capacitors may result in an offset to the crystal oscillation frequency. For more information on such considerations, refer to the AN-1260 Application Note, *Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers*. After the XTAL circuit is defined, it is recommended to consult the XTAL vendor to ensure that the design operates with a sufficient margin across all conditions.

The evaluation of the ADV7182A was completed using an XTAL with typical characteristics, as described in Table 9.

Table 9. Reference XTAL Characteristics

Characteristic	Value	Unit
Package	3.2 × 2.5 × 0.8	mm
Nominal Frequency	28.63636	MHz
Mode of Oscillation	Fundamental	Not applicable
Frequency Calibration (at 25°C)	±20	ppm
Frequency Temperature Stability Tolerance	±50	ppm
Operating Temperature Range	−40 to +125	°C
Maximum Equivalent Series Resistance	25	Ω
Load Capacitance	12	pF
Drive Level	200	µW
Maximum Shunt Capacitance	5	pF
Aging per Year	±3	ppm

The values in Table 9 are provided for reference only. It is recommended to characterize the operation of the XTAL circuit thoroughly across the operating temperature range of the application, in conjunction with the XTAL vendor, prior to releasing any new design.

INPUT NETWORKS

This section describes the input networks (external resistor and capacitor circuits) to be placed on the analog video input pins ($A_{IN}x$) of the ADV7182A. Different input networks are required for different analog input video formats.

SINGLE-ENDED INPUT NETWORK

Use the input network described in Figure 6 on each $A_{IN}x$ input pin of the ADV7182A when any of the following video input formats are used: single-ended CVBS, YC (S-Video), or YPrPb.

It is recommended that the input network circuit shown in Figure 6 be placed as close as possible to the $A_{IN}x$ pins of the ADV7182A.

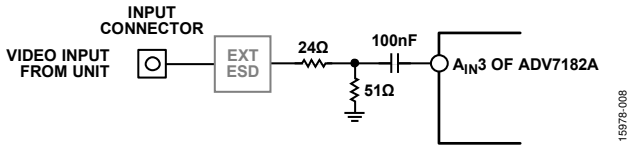

Figure 6. Input Single-Ended Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. In addition, these resistors create a resistor divider with a 0.68 gain that attenuates the amplitude of the inputted analog video and scales the input to the ADC range of the ADV7182A. This allows the ADV7182A to have an input range of up to 1.47 V p-p.

Note that amplifiers within the ADV7182A restore the amplitude of the input signal so that signal-to-noise (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog input pins of the ADV7182A.

The clamping circuitry within the ADV7182A restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7182A. See the Clamp Operation section for more information.

DIFFERENTIAL INPUT NETWORK

Use the input network shown in Figure 7 when differential CVBS video is input on the $A_{IN}x$ input pins of the ADV7182A.

It is recommended that the input network circuit shown in Figure 7 be placed as close as possible to the $A_{IN}x$ pins of the ADV7182A.

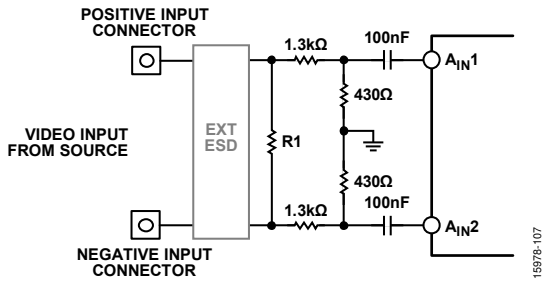

Figure 7. Input Differential Network

Differential video transmission involves transmitting two complementary CVBS signals and has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection.
- Improved EMI performance.
- Ability to absorb ground bounce.

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 kΩ and 430 Ω resistors provide a resistor divider with a 0.25 gain, resulting in an attenuation of the inputted analog video but also an increase in the input common-mode range of the ADV7182A of up to 4 V p-p.

Note that amplifiers within the ADV7182A restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog video input pins of the ADV7182A.

The clamping circuitry within the ADV7182A restores the dc bias of the optimized level before it is fed into the ADC of the ADV7182A. See the Clamp Operation section for further information.

The combination of the 1.3 kΩ and 430 Ω resistors and the 100 nF ac coupling capacitor limits current flow into the ADV7182A during short to battery (STB) events. See the Short to Battery (STB) Protection section.

To achieve optimal performance, closely match the 1.3 kΩ and 430 Ω resistors; that is, all the 1.3 kΩ and 430 Ω resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

SHORT TO BATTERY (STB) PROTECTION

In differential mode, the ADV7182A is protected against STB events by the external 100 nF ac coupling capacitors (see Figure 7). The external input network resistors are sized to be large enough to reduce the current flow during a STB event, but to be small enough not to effect the operation of the ADV7182A.

Choose the power rating of the input network resistors to withstand the high voltages of STB events. Similarly, choose the breakdown voltage of the AC coupling capacitors to be robust to STB events.

The R1 resistor is protected because no current or limited current flows through it during an STB event.

ANALOG FRONT END

INPUT CONFIGURATION

The following two steps are crucial for configuring the ADV7182A to correctly decode the input video.

1. Use INSEL[4:0] to configure the routing and format decoding (CVBS, S-Video, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. Using the INSEL[4:0] selection, configure the SDP block, which decodes the digital data, to process the CVBS, S-Video or YPrPb format.

INSEL[4:0], Input Control—Address 0x00, Bits[4:0]

The INSEL bits allow the user to select the input format. They also configure the SDP core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format.

INSEL[4:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 10). This allows the user to route the various video signal types to the decoder and select them using INSEL[4:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 10. INSEL[4:0]

INSEL[4:0]	Video Format	Analog Input
00000	CVBS	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$
01000	S-Video (Y/C)	Y input on $A_{IN}1$ C input on $A_{IN}2$
01001	S-Video (Y/C)	Y input on $A_{IN}3$ C input on $A_{IN}4$
01100	YPrPb	Y input on $A_{IN}1$ Pb input on $A_{IN}2$ Pr input on $A_{IN}3$
01110	Differential CVBS	Positive on $A_{IN}1$ Negative on $A_{IN}2$
01111	Differential CVBS	Positive on $A_{IN}3$ Negative on $A_{IN}4$

ANALOG INPUT MUXING

The ADV7182A has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder.

A maximum of four CVBS inputs can be connected to and decoded by the ADV7182A. As shown in the Pin Configuration and Function Description section, these analog input pins lie in close proximity to one another, which requires careful design of the PCB layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended that any unused analog input pins be connected to AGND to act as a shield.

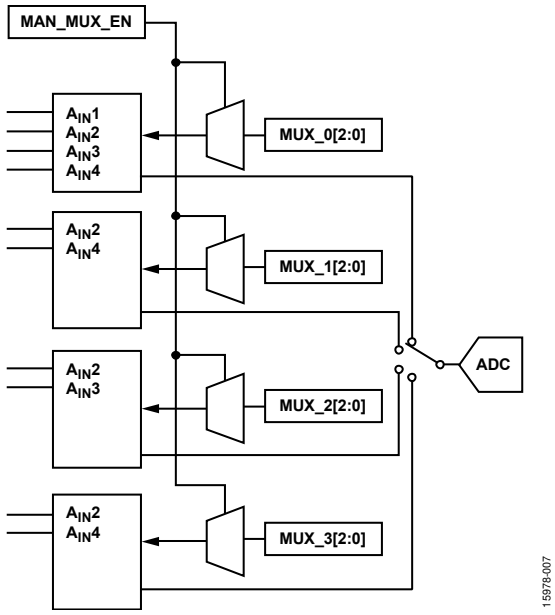

Figure 8. Manual Muxing

MAN_MUX_EN, Manual Input Muxing Enable—Address 0xC4, Bit 7

To configure the ADV7182A analog muxing section, the user must select the analog input $A_{IN}1$ to $A_{IN}8$ that is to be processed by the ADC. MAN_MUX_EN must be set to 1 to enable the following muxing blocks:

- MUX_0[2:0], ADC mux configuration (Address 0xC3, Bits[2:0])
- MUX_1[2:0], ADC mux configuration (Address 0xC3, Bits[6:4])
- MUX_2[2:0], ADC mux configuration (Address 0xC4, Bits[2:0])
- MUX_3[2:0], ADC mux configuration (Address 0x60, Bits[2:0])

The four mux sections are controlled by the signal buses, MUX_0/MUX_1/MUX_2/MUX_3[2:0]. Table 11 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX_0. For example, in an S-Video input configuration, connect MUX_0 to the Y channel and MUX_1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers must be powered down (see the description of Register 0x3A in Table 96).

ANTIALIASING FILTERS

The ADV7182A has optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 9). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 10 and Figure 11 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.

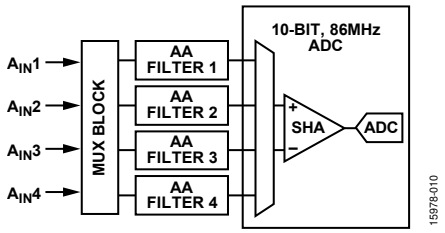

Figure 9. Antialias Filter Configuration

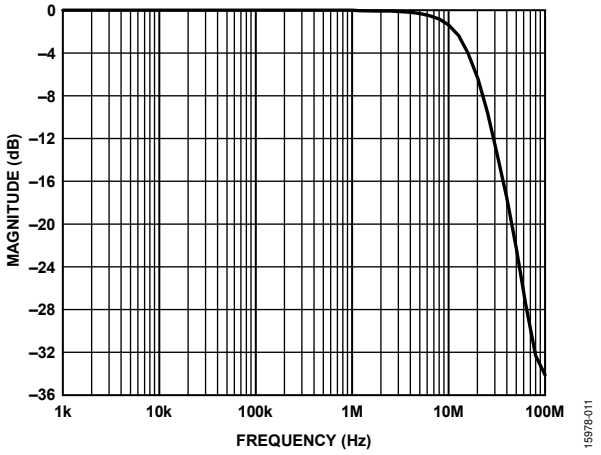

Figure 10. Antialiasing Filter Magnitude Response

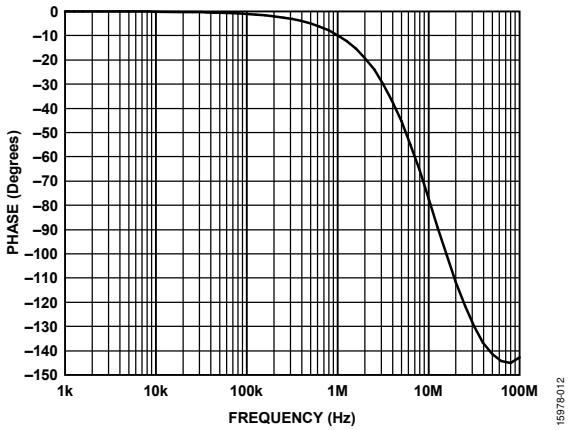

Figure 11. Antialiasing Filter Phase Response

AA_FILT_MAN_OVR, Antialiasing Filter Override—Address 0xF3, Bit 4

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

AA_FILT_EN[3:0], Antialiasing Filter Enable—Address 0xF3, Bits[3:0]

These bits allow the user to enable or disable the antialiasing filters on each of the four input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

AA_FILT_EN[0], Antialiasing Filter Enable—Address 0xF3, Bit 0

When AA_FILT_EN[0] is 0, AA Filter 1 is disabled. When AA_FILT_EN[0] is 1, AA Filter 1 is enabled.

AA_FILT_EN[1], Antialiasing Filter Enable—Address 0xF3, Bit 1

When AA_FILT_EN[1] is 0, AA Filter 2 is disabled. When AA_FILT_EN[1] is 1, AA Filter 2 is enabled.

AA_FILT_EN[2], Antialiasing Filter Enable—Address 0xF3, Bit 2

When AA_FILT_EN[2] is 0, AA Filter 3 is disabled. When AA_FILT_EN[2] is 1, AA Filter 3 is enabled.

AA_FILT_EN[3], Antialiasing Filter Enable—Address 0xF3, Bit 3

When AA_FILT_EN[3] is 0, AA Filter 4 is disabled. When AA_FILT_EN[3] is 1, AA Filter 4 is enabled.

Table 11. Manual Mux Settings for ADC (MAN_MUX_EN Must be Set to 1)[1, 2, 3, 4]

MUX_0[2:0]	ADC Connected To	MUX_1[2:0]	ADC Connected To	MUX_2[2:0]	ADC Connected To	MUX_3[2:0]	ADC Connected To
000	No connect	000	No connect	000	No connect	000	No connect
001	$A_{IN}1$	001	No connect	001	No connect	001	No connect
010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$
011	$A_{IN}3$	011	No connect	011	$A_{IN}3$	011	No connect
100	$A_{IN}4$	100	$A_{IN}4$	100	No connect	100	$A_{IN}4$

[1] CVBS can only be processed by MUX_0.
[2] Differential CVBS can only be processed by MUX_0 (positive channel) and MUX_3 (negative channel).
[3] Y/C can only be processed by MUX_0 and MUX_1.
[4] YPrPb can only be processed by MUX_0, MUX_1, and MUX_2.

GLOBAL CONTROL REGISTERS

Register control bits described in this section affect the entire chip.

POWER SAVING MODES

Power-Down

PWRDWN—Address 0x0F, Bit 5

The ADV7182A can be placed into a chip wide, power-down mode by setting the PWRDWN bit or by using the $\overline{\text{PWRDWN}}$ pin. The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I^2C interface is unaffected and remains operational in power-down mode.

When PWRDWN is 0, the chip is operational. When PWRDWN is 1 (default), the ADV7182A is in a chip-wide, power-down mode.

RESET CONTROL

Reset, Chip Reset—Address 0x0F, Bit 7

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7182A, issues a full chip reset. All I^2C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified and keep the last written value. These bits are marked as having a reset value of x in the register tables (see Table 96 and Table 98). After the reset sequence, the device immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the device returns to the default for its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.

The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the I2C Interface section).

When the reset bit is 0 (default), operation is normal. When the reset bit is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Tristate Output Drivers

TOD—Address 0x03, Bit 6

This bit allows the user to tristate the output drivers of the ADV7182A.

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL) can be forced active via the TIM_OE bit. For more information on tristate control, see the Tristate LLC Driver section and the Timing Signals Output Enable section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TOD is 0, the output drivers are enabled. When TOD is 1 (default), the output drivers are tristated.

Tristate LLC Driver

TRI_LLC—Address 0x1D, Bit 7

This bit allows the output drivers for the LLC pin of the ADV7182A to be tristated. For more information on tristate control, refer to the Tristate Output Drivers section and the Timing Signals Output Enable section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TRI_LLC is 0, the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled). When TRI_LLC is 1 (default), the LLC pin drivers are tristated.

Timing Signals Output Enable

TIM_OE—Address 0x04, Bit 3

Regard the TIM_OE bit as an addition to the TOD bit. Setting this bit high forces the output drivers for HS and VS/FIELD/SFL into the active state (that is, driving state), even if the TOD bit is set. If TIM_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator, which may be the case if only the timing signals are extracted from an incoming signal or if the device is in freerun mode, where a separate chip can output a company logo, for example.

For more information on tristate control, see the Tristate Output Drivers section and the Tristate LLC Driver section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TIM_OE is 0 (default), HS and VS/FIELD/SFL are tristated according to the TOD bit. When TIM_OE is 1, HS and VS/FIELD/SFL are always forced active.

VS/FIELD/SFL Sync Mux Selection

FLD_OUT_SEL[2:0]—Address 0x6B, Bits[2:0]

The FLD_OUT_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the Tristate Output Drivers section and the Tristate LLC Driver section.

Table 12. FLD_OUT_SEL Function

FLD_OUT_SEL[2:0]	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information.
001	The VS/FIELD/SFL pin outputs vertical sync information.
010 (default)	The VS/FIELD/SFL pin outputs field sync information.
011	The VS/FIELD/SFL pin outputs DE information.
100	The VS/FIELD/SFL pin outputs SFL information.

HS Sync Mux Selection

HS_OUT_SEL[2:0]—Address 0x6A, Bits[2:0]

The HS_OUT_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, DE, or SFL information.

Note that the HS pin must be active for this selection to occur (see the Tristate Output Drivers section and the Tristate LLC Driver section).

Table 13. HS_OUT_SEL Function

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs DE information.
100	The HS pin outputs SFL information.

Drive Strength Selection (Data)

DR_STR[1:0]—Address 0xF4, Bits[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the drive strength for the pixel output pins (P[7:0]) and the timing pins (HS and VS/FIELD/SFL).

For more information on tristate control, see the Tristate Output Drivers section and the Tristate LLC Driver section.

Table 14. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

DR_STR_C[1:0]—Address 0xF4, Bits[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Data) section.

Table 15. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (I^2C)

DR_STR_S[1:0]—Address 0xF4, Bits[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the I^2C signal output drivers. This affects the drive strength for the SDA and SCL pins.

Table 16. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN—Address 0x04, Bit 1

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7182A core to an encoder in a decoder/encoder back to back arrangement.

When the EN_SFL_PIN is 0 (default), the SFL output is disabled. When EN_SFL_PIN is 1, the SFL information is presented on the SFL pin.

GLOBAL STATUS REGISTERS

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7182A. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV7182A.

IDENTIFICATION REGISTER

IDENT[7:0]—Address 0x11, Bits[7:0]

This is the register identification of the ADV7182A revision. Table 17 describes the various versions of the ADV7182A.

Table 17. IDENT[7:0] CODE

IDENT[7:0]	Description
0x40	Prerelease silicon
0x41	Released silicon

STATUS 1 REGISTER

Status 1[7:0]—Address 0x10, Bits[7:0]

This read only register provides information about the internal status of the ADV7182A.

See the CIL[2:0], Count in to Lock—Address 0x51, Bits[2:0] section and the COL[2:0], Count Out of Lock (COL)—Address 0x51, Bits[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable—Address 0x51, Bit 7 section.

See the Autodetection of SD Modes section for a description of the AD_RESULT bits.

Table 18. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read)
2	FSC_LOCK	f_{SC} locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2 REGISTER

Status 2[7:0]—Address 0x12, Bits[7:0]

Table 19. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Rovi color striping
1	MVCS T3	Rovi color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV PS DET	Detected Rovi pseudo sync pulses
3	MV AGC DET	Detected Rovi AGC pulses
4	LL NSTD	Line length is nonstandard
5	FSC NSTD	f_{SC} frequency is nonstandard
6	Reserved	Reserved
7	Reserved	Reserved

STATUS 3 REGISTER

Status 3[7:0]—Address 0x13, Bits[7:0]

Table 20. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	Reserved	Reserved
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved
4	FREE_RUN_ACT	Flags if the ADV7182A entered freerun mode (see the Freerun Operation section)
5	STD FLD LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

AUTODETECTION RESULT

AD_RESULT[2:0]—Address 0x10, Bits[6:4]

The AD_RESULT[2:0] bits report back on the findings from the ADV7182A autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure the autodetection block.

Table 21. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

VIDEO PROCESSOR

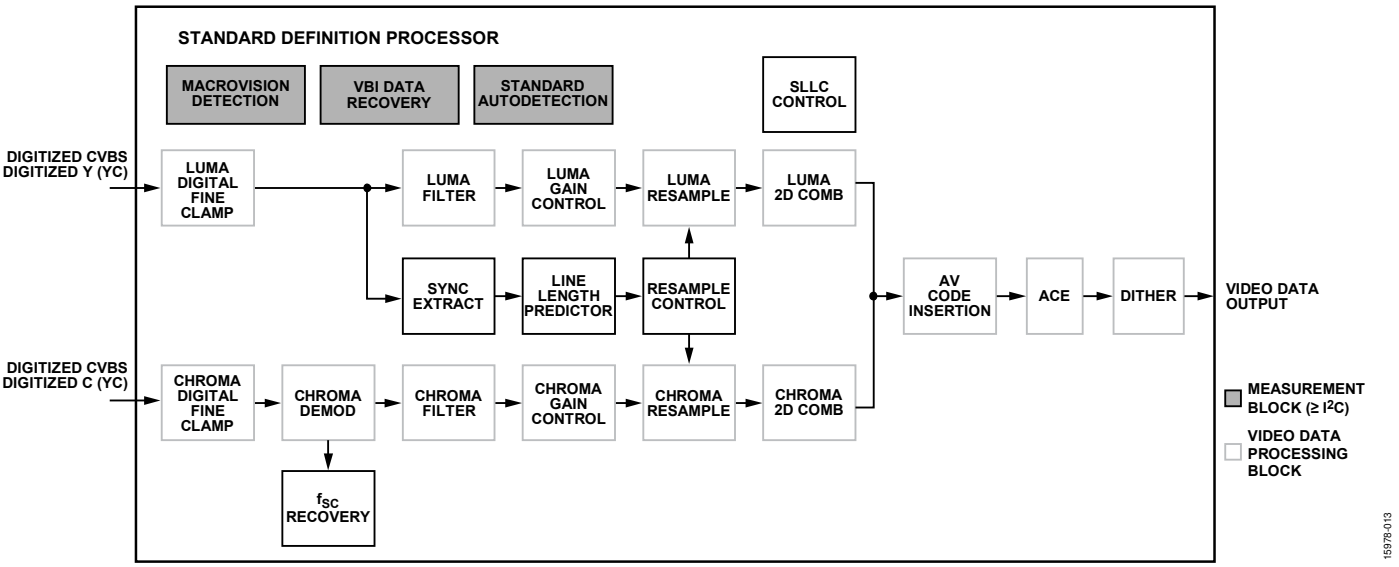

Figure 12. Block Diagram of Video Processor

Figure 12 shows a block diagram of the ADV7182A video processor. The ADV7182A can handle standard definition (SD) video in CVBS, Y/C, and YPrPb formats. The video processor features luminance and chrominance paths. If the input video is a composite type (CVBS), CVBS is supplied to both processing paths.

STANDARD DEFINITION (SD) LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct line length errors and dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted as per ITU-R BT.656.

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is performed to correct static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, superadaptive comb filter provides high quality Y/C separation if the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted as per ITU-R BT.656.

ACE AND DITHER PROCESSING BLOCKS

The ACE block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail (see the Adaptive Contrast Enhancement section).

When enabled, the dither block converts the digital output of the ADV7182A from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV7182A to communicate with some LCD panels (see the Dither Function section).

SYNC PROCESSING

The ADV7182A extracts syncs embedded in the analog input video signal. There is currently no support for external HS/VS inputs. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm uses a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this information then drives the digital resampling section to ensure that the ADV7182A outputs 720 active pixels per line.

The sync processing on the ADV7182A also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSYNC processor. This block provides extra filtering of the detected VSYNC signals to improve vertical lock.
- HSYNC processor. The HSYNC processor filters incoming HSYNCS signals corrupted by noise, providing much improved performance for video signals with a stable time base but poor SNR.

VERTICAL BLANK INTERVAL (VBI) DATA RECOVERY

The ADV7182A can retrieve the following information from the input video:

- Wide screen signaling (WSS).
- Copy generation management system (CGMS).
- Closed captioning (CCAP).
- Rovi protection presence.
- Teletext.

The ADV7182A is also capable of automatically detecting the incoming video standard with respect to color subcarrier frequency, field rate, and line rate.

The ADV7182A can configure itself to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x02, Bits[7:4]) allow the user to force the digital core into a specific video standard; this is not necessary under normal circumstances. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Autodetection of SD Modes

To guide the autodetect system of the ADV7182A, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x02[7:4]

Table 22. VID_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

AD_SEC525_EN, SECAM 525 Autodetect Enable—Address 0x07, Bit 7

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM modulated color component. Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM modulated color component.

AD_SECAM_EN, SECAM Autodetect Enable—Address 0x07, Bit 6

Setting AD_SECAM_EN to 0 (default) disables the autodetection of SECAM. Setting AD_SECAM_EN to 1 enables the detection of SECAM.

AD_N443_EN, NTSC 4.43 Autodetect Enable—Address 0x07, Bit 5

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier. Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, PAL 60 Autodetect Enable—Address 0x07, Bit 4

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate. Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, PAL N Autodetect Enable—Address 0x07, Bit 3

Setting AD_PALN_EN to 0 (default) disables the detection of the PAL N standard. Setting AD_PALN_EN to 1 enables the detection of the PAL N standard.

AD_PALM_EN, PAL M Autodetect Enable—Address 0x07, Bit 2

Setting AD_PALM_EN to 0 (default) disables the autodetection of PAL M. Setting AD_PALM_EN to 1 enables the detection of PAL M.

AD_NTSC_EN, NTSC Autodetect Enable—Address 0x07, Bit 1

Setting AD_NTSC_EN to 0 (default) disables the detection of standard NTSC. Setting AD_NTSC_EN to 1 enables the detection of standard NTSC.

AD_PAL_EN, PAL B/PAL D/PAL I/PAL G/PAL H Autodetect Enable—Address 0x07, Bit 0

Setting AD_PAL_EN to 0 (default) disables the detection of standard PAL. Setting AD_PAL_EN to 1 enables the detection of standard PAL.

SFL_INV, Subcarrier Frequency Lock Inversion—Address 0x41, Bit 6

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. This control solves some compatibility issues with video encoders, as well as solving two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

The second problem is to accommodate a design change using newer Analog Devices encoders, such as the ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179. The older encoders used the SFL (genlock telegram) bit directly, whereas the newer encoders invert the bit prior to using because the inversion compensates for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the newer video encoders (ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179), the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For the older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back to back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL_INV to 0 (default) makes the device SFL compatible with newer video encoders such as the ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179.

Setting SFL_INV to 1 makes the device SFL compatible with the older video encoders.

Lock Related Controls

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1[7:0]—Address 0x10, Bits[7:0] section). Figure 13 shows the signal flow and the controls available to influence the way the lock status information is generated.

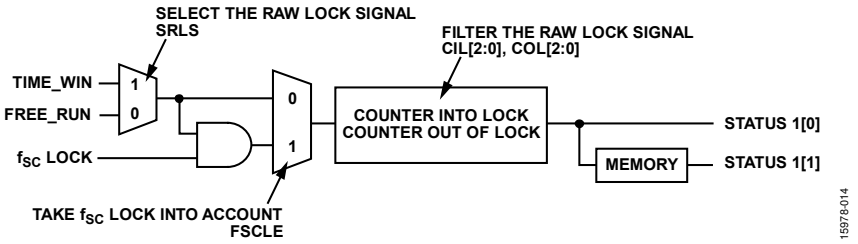

Figure 13. Lock Related Signal Path

SRLS, Select Raw Lock Signal—Address 0x51, Bit 6

Using the SRLS bit, the user can choose between two sources for determining the lock status per Bits[1:0] in the Status 1 register (see Figure 13):

- The TIME_WIN signal is based on a line to line evaluation of the horizontal synchronization pulse of the incoming video and reacts quickly.
- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE_RUN signal; that is, the signal evaluates the properties of the incoming video over several fields.

Setting SRLS to 1 selects the TIME_WIN signal; that is, the signal evaluates the horizontal synchronization pulse of the incoming video on a line to line basis.

FSCLE, f_{SC} Lock Enable—Address 0x51, Bit 7

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7182A in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is 0 (default), the overall lock status is dependent only on horizontal sync lock. When FSCLE is 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

CIL[2:0], Count in to Lock—Address 0x51, Bits[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Bits[1:0] in the Status 1 register. The bit counts the value in lines of video.

Table 23. CIL Function

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COL[2:0], Count Out of Lock (COL)—Address 0x51, Bits[5:3]

COL[2:0] determines the number of consecutive lines for which the out of lock condition must be true before the system switches into the unlocked state and reports this via Bits[1:0] in the Status 1 register. COL[2:0] counts the value in lines of video.

Table 24. COL Function

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROL REGISTERS

The color control registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Contrast Adjust—Address 0x08, Bits[7:0]

This register allows the user to control contrast adjustment of the picture.

Table 25. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2