Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

10-Bit, SDTV Video Decoder with Differential Inputs

Data Sheet **ADV7182**

FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling per channel for CVBS, Y/C mode, and YPrPb
- Four analog video input channels with on-chip antialiasing filter
- CVBS (composite), Y/C (S-Video), and YPrPb (component) video input support
- Fully differential, pseudo differential, and single-ended CVBS video input support
- Up to 4 V common-mode input range solution
- Excellent common-mode rejection capabilities
- Five-line adaptive comb filters and CTI/DNR video enhancement
- TBC functionality provided by adaptive digital line length tracking (ADLLT), signal processing, and enhanced first in, first out (FIFO) management
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Video fast switch capability
- Adaptive contrast enhancement (ACE)
- Down dither (8 bits to 6 bits)
- Rovi™ (Macrovision) copy protection detection
- NTSC/PAL/SECAM autodetection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, or FIELD
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode and ultralow sleep mode current
- Two-wire serial MPU interface (I^2C compatible)
- Single 1.8 V supply possible
- Automotive qualified models available
- −40°C to +105°C automotive temperature grade
- −40°C to +85°C industrial qualified temperature grade
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

APPLICATIONS

- Automotive infotainment
- DVRs for video security
- Media players

FUNCTIONAL BLOCK DIAGRAM

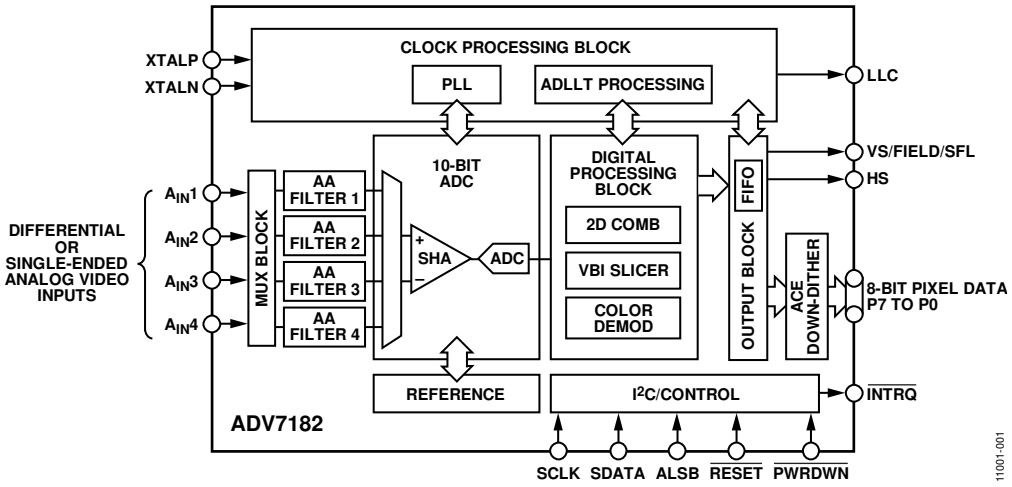

Figure 1.

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADV7182* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADV7182 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1180: Optimizing Video Platforms for Automated Post-Production Self-Tests
- AN-1191: ADV7182 CMRR Measurements Across Frequency Using ADSP-BF527
- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers

Data Sheet

- ADV7182: 10-Bit, SDTV Video Decoder with Differential Inputs Data Sheet

TOOLS AND SIMULATIONS

- ADV7182 IBIS Model

DESIGN RESOURCES

- ADV7182 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADV7182 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

9/14—Rev. B to Rev. C

Changes to Input Networks Section 13
Changes to Analog Interface Inputs Section 94
Changes to Figure 50 95

7/14—Rev. A to Rev. B

Changes to Features Section 1
Moved Revision History 3
Changes to General Description Section 4
Changes to Table 2 and Table Summary Statement 6
Changes to Table 3 Summary Statement 7
Change to Table 4 Summary Statement 8
Change to Table 5 Summary Statement 9
Changes to Table 7 10
Changes to Power Supply Sequencing Section and Figure 5 12
Changes to Input Networks Section and Figure 7 13
Change to Antialiasing Filters Section 16
Changes to Global Pin Control Section 17
Changes to Table 16 19
Changes to Free-Run Operation Section 25
Changes to Clamp Operation Section 26
Changes to Chroma Filter Section 30
Changes to Gain Operation Section 32
Changes to Comb Filters Section 37
Changed Pixel Port Configuration Section to ITU-R BT.565 Tx Configuration Section, Moved Polarity LLC Pin Section, Added Figure 45; Renumbered Sequentially 61
Changes to Table 91 62
Changes to Header Row and Address 0x11, Table 95 68
Change to Header Row, Table 96 83
Changes to Ordering Guide 96

3/13—Rev. 0 to Rev. A

Change to Features Section 1
Changes to General Description Section 4
Changes to Free Run Operation Section and Table 33, Added Luma Ramp Test Pattern Section, VS_COAST_MODE[1:0], Address 0xF9[3:2] Section, and Table 34, Renumbered Sequentially 24
Changes to Register 0x14, Table 94 72
Changes to Register 0xF9, Table 94 82

1/13—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV7182 automatically detects and converts standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards into a 4:2:2 component video data stream. This video data stream is compatible with the 8-bit ITU-R BT.656 interface standard.

External HS, VS, and FIELD signals can provide timing references for LCD controllers and other video ASICs. The accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution. The analog video inputs accept both single-ended, pseudo-differential, and fully differential composite video signals as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources.

The ADV7182 along with an external resistor divider provide a common-mode input range of 4 V, enabling the removal of large signal, common-mode transients present on the video lines. Common-mode rejection (CMR) values of up to 80 dB can be achieved without the need for external amplifier circuitry.

The AGC and clamp restore circuitry allow an input video signal peak-to-peak range to 1.0 V at the analog video input pin of the ADV7182. Alternatively, these can be bypassed for manual settings.

The ADV7182 can be protected from short-to-battery (STB) events with standard ac coupling capacitors.

The ADV7182 is programmed via a two-wire, serial bidirectional port (I²C® compatible) and is fabricated in a 1.8 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7182 is provided in a space-saving LFCSP surface-mount, RoHS compliant package. The ADV7182 is available in an automotive grade that is rated over the −40°C to +105°C temperature range. This makes the ADV7182 ideal for automive applications. The ADV7182 is also available in a −40°C to +85°C temperature range, making it ideal for industrial applications.

The ADV7182 is a versatile one-chip multiformat video decoder that automatically detects PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video. The ADV7182 can receive composite signals in either single-ended or differential modes. This makes the ADV7182 ideal for automotive applications.

The ADV7182 converts these analog video formats into a digital 8-bit ITU-R BT.656 video stream.

The digital video output stream of the ADV7182 interfaces easily to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices, Inc., digital video encoders, such as the ADV7391. External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs.

OVERVIEW OF THE ANALOG FRONT END

The ADV7182 analog front end (AFE) comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor. The AFE employs differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS to be connected directly to the ADV7182.

The front end also includes a 4-channel input mux that enables multiple composite video signals to be applied to the ADV7182. Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter. A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 23). The choice of this resistor divider ratio provides a common-mode range of up to 4 V. Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7182.

Table 1 shows the three ADC clocking rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

The ADV7182 has a fully differential AFE. This allows for inherent small and large signal noise rejection, improved electromagnetic interference (EMI), and the ability to absorb ground bounce. Support is offered for both true differential and pseudo-differential signals.

Table 1. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)[2]	114	4×
YPrPb[2]	172	4×

[1] Based on a 28.63636 MHz clock input to the ADV7182.
[2] See INSEL[4:0] in Table 95 for writes needed to set Y/C (S-Video) and YPrPb modes.

OVERVIEW OF THE STANDARD DEFINITION PROCESSOR

The ADV7182 is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include PAL B/PAL D/PAL I/PAL G/PAL H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/NTSC J, NTSC 4.43, and SECAM B/SECAM D/SECAM G/SECAM K/SECAM L. The ADV7182 can automatically detect the video standard and process it accordingly.

The ADV7182 has a five-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7182.

The ADV7182 implements a patented ADLLT™ algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7182 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7182 contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ACE offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. This enables the contrast in dark areas of an image to be increased without saturating the bright areas of an image. This is particularly useful in automotive applications, where it can be important to be able to discern objects in shaded areas.

Down dithering from eight bits to six bits enables ease of design for standard LCD panels.

The video processor can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world standard teletext (WST). Data is transmitted via the 8-bit video output port as ancillary data packets (ANC). The ADV7182 is fully Macrovision® certified; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		−0.6/+0.6		LSB
DIGITAL INPUTS						
Input High Voltage (DVDDIO = 3.3 V)	V_{IH}		2			V
Input High Voltage (DVDDIO = 1.8 V)	V_{IH}		1.2			V
Input Low Voltage (DVDDIO = 3.3 V)	V_{IL}				0.8	V
Input Low Voltage (DVDDIO = 1.8 V)	V_{IL}				0.4	V
Crystal Inputs	V_{IH}		1.2			V
	V_{IL}				0.4	V
Input Leakage Current	I_{IN}		−10		+10	µA
Input Leakage Current (SDATA, SCLK)	I_{IN}		−10		+15	µA
Input Leakage Current ($\overline{\text{PWRDWN}}$, ALSB)	I_{IN}		−10		+48	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage (DVDDIO = 3.3 V)	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output High Voltage (DVDDIO = 1.8 V)	V_{OH}	I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage (DVDDIO = 3.3 V)	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Output Low Voltage (DVDDIO = 1.8 V)	V_{OL}	I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2]						
Digital I/O Power Supply	D_{VDDIO}		1.62	3.3	3.63	V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
Digital I/O Supply Current	I_{DVDDIO}			3		mA
PLL Supply Current	I_{PVDD}			12		mA
Analog Supply Current	I_{AVDD}	Single-ended CVBS input		47		mA
		Differential CVBS input		69		mA
		Single-ended CVBS fast switch		47		mA
		Differential CVBS fast switch		69		mA
		Y/C input		60		mA
		YPrPb input		75		mA
Digital Supply Current	I_{DVDD}	Single-ended CVBS input		60		mA
		Differential CVBS input		66		mA
		Single-ended CVBS fast switch		60		mA
		Differential CVBS fast switch		66		mA
		Y/C input		60		mA
		YPrPb input		60		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DOWN PERFORMANCE[1]						
Digital I/O Supply Power-Down Current	I_{DVDDIO}			73		µA
PLL Supply Power-Down Current	I_{PVDD}			38		µA
Analog Supply Power-Down Current	I_{AVDD}			0.15		µA
Digital Supply Power-Down Current	I_{DVDD}			368		µA
Total Power Dissipation in Power-Down Mode				1		mW

[1] Guaranteed by characterization.
[2] Typical current consumption values are recorded with nominal voltage supply levels and an SMPTEBAR test pattern.

VIDEO SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulate five-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulate five-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step		2.0		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp		57		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection[2]	CMR			75		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed[3]				100		Lines
Fast Switch Speed[4]				100		ms
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

[1] These specifications apply for all CVBS input types (NTSC, PAL, SECAM) as well as for single-ended and differential CVBS inputs.
[2] The common-mode rejection (CMR) of this circuit design is critically dependent on the external resistor matching on its inputs. This measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] This is the time that it takes the ADV7182 to detect which video format is present at its input, for example, PAL I or NTSC M.
[4] This is the time that it takes the ADV7182 to switch from one (single-ended or differential) analog input to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

TIMING SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.63636		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDATA Setup Time	t_5		100			ns
SCLK and SDATA Rise Times	t_6				300	ns
SCLK and SDATA Fall Times	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
$\overline{\text{RESET}}$ FEATURE						
$\overline{\text{RESET}}$ Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{ACCESS} = t_{10} - t_{11}$)			3.8	ns
	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 + t_{12}$)			6.9	ns

Timing Diagrams

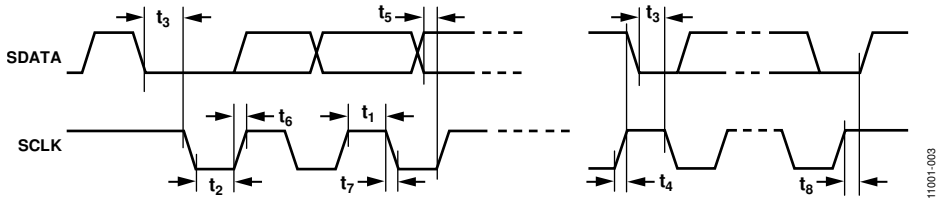

Figure 2. I²C Timing

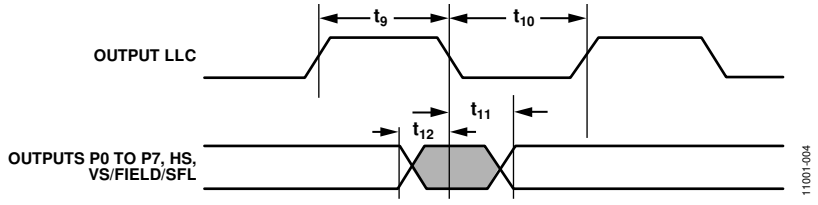

Figure 3. Pixel Port and Control Output Timing

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp Source Current			0.32		mA
Large Clamp Sink Current			0.32		mA
Fine Clamp Source Current			7		µA
Fine Clamp Sink Current			7		µA

THERMAL SPECIFICATIONS

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer printed circuit board (PCB) with solid ground plane, 32-lead LFCSP		32.5		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 32-lead LFCSP		2.3		°C/W

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter[1]	Rating
AVDD to GND	2.2 V
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4 V
PVDD to DVDD	−0.9 V to +0.9 V
AVDD to DVDD	−0.9 V to +0.9 V
Digital Inputs Voltage	GND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage	GND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs to Ground	GND − 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The Absolute Maximum Ratings assume that DGND pins and the exposed pad of the ADV7182 are connected together to a common ground plane (GND). This is part of the recommended layout scheme. See the PCB Layout Recommendations section for more information. The Absolute Maximum Ratings are stated in relation to this common ground plane.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions must be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

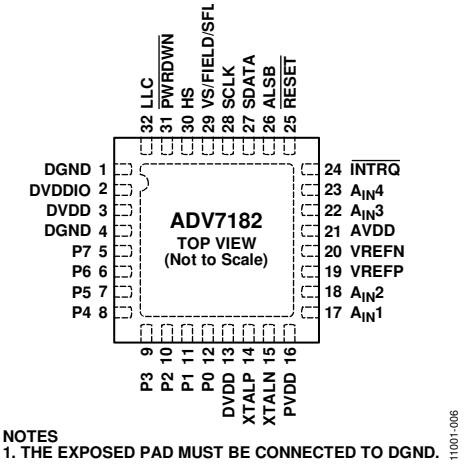

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	G	Ground for Digital Supply.
2	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
3, 13	DVDD	P	Digital Supply Voltage (1.8 V).
5 to 12	P7 to P0	O	Video Pixel Output Port.
14	XTALP	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7182. In crystal mode, the crystal must be a fundamental crystal.
15	XTALN	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
16	PVDD	P	PLL Supply Voltage (1.8 V).
17, 18, 22, 23	$A_{IN}1$ to $A_{IN}4$	I	Analog Video Input Channels.
19	VREFP	O	Internal Voltage Reference Output.
20	VREFN	O	Internal Voltage Reference Output.
21	AVDD	P	Analog Supply Voltage (1.8 V).
24	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video.
25	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7182 circuitry.
26	ALSB	I	This pin selects the I^2C address for the ADV7182. For ALSB set to Logic 0, the address selected for a write is 0x40; for ALSB set to Logic 1, the address selected is 0x42.
27	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
28	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
29	VS/FIELD/SFL	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal/Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
30	$\overline{\text{HS}}$	O	Horizontal Synchronization Output Signal.
31	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7182 is in power-down mode.
32	LLC	O	Line-Locked Output Clock for Output Pixel Data. Nominally 27 MHz but varies up or down according to the video line length.
	EPAD (EP)		The exposed pad must be connected to DGND.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7182 is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}).

When powering up the ADV7182, follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pins (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pin are powerd up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7182.

SIMPLIFIED POWER-UP SEQUENCE

Alternatively, the ADV7182 can be powered up by asserting all supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pins simultaneously. After this operation, perform a software reset, then wait 10 ms before initiating I^2C communication with the ADV7182.

While the supplies are being established, take care to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7182 supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY

It is possible to power all the supplies (D_{VDD}, P_{VDD}, A_{VDD}, and D_{VDDIO}) to 1.8 V. In this case, apply the power-up sequences as described in the Optimal Power-Up Sequence section and the Simplified Power-Up Sequence section. The only change is that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V.

In this setup, note the following:

- Power up the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin to 1.8 V instead of 3.3 V.
- Set the drive strengths of the digital outputs of the ADV7182 to their maximum setting. See the Global Pin Control section.
- Connect any pull-up resistors connected to pins on the ADV7182 (such as the SCLK pin and the SDATA pin) to 1.8 V and not 3.3 V.

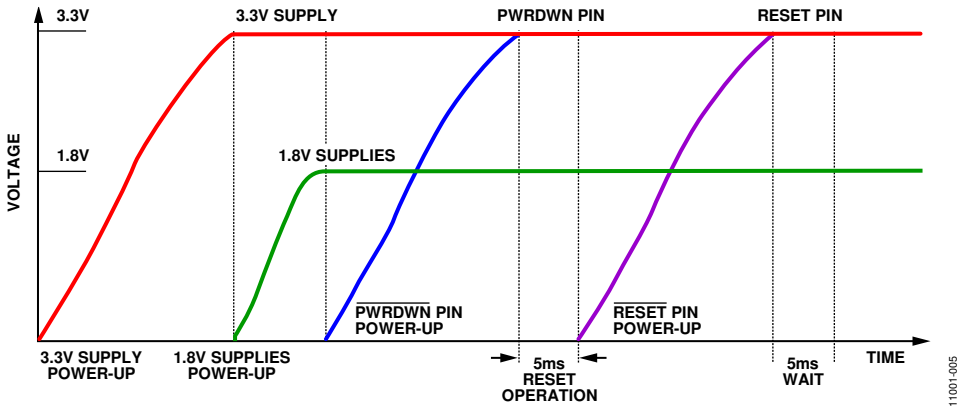

Figure 5. Recommended Power-Up Sequence

INPUT NETWORKS

This section describes the input networks (external resistor and capacitor circuits) that should be placed on the analog video input (A_{IN}) pins of the ADV7182. Different input networks are required for different analog input video formats.

SINGLE-ENDED INPUT NETWORK

Use the input network described in Figure 6 on each A_{IN} input pin of the ADV7182 when any of the following video input formats are used: single-ended CVBS, YC (S-Video), or YPrPb.

It is recommended that the input network circuit shown in Figure 6 be placed as close as possible to the A_{IN} pins of the ADV7182.

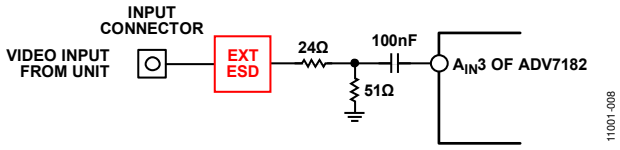

Figure 6. Input Single-Ended Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. In addition, these resistors create a resistor divider with a 0.68 gain that attenuates the amplitude of the inputted analog video and scales the input to the ADC range of the ADV7182. This allows the ADV7182 to have an input range of up to 1.47 V p-p.

Note that amplifiers within the ADV7182 restore the amplitude of the input signal so that signal-to-noise (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog input pins of the ADV7182.

The clamping circuitry within the ADV7182 restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7182. See the Clamp Operation section for more information.

DIFFERENTIAL INPUT NETWORK

Use the input network described in Figure 7 when differential CVBS video is input on the A_{IN} input pins of the ADV7182.

It is recommended that the input network circuit shown in Figure 7 be placed as close as possible to the A_{IN} pins of the ADV7182.

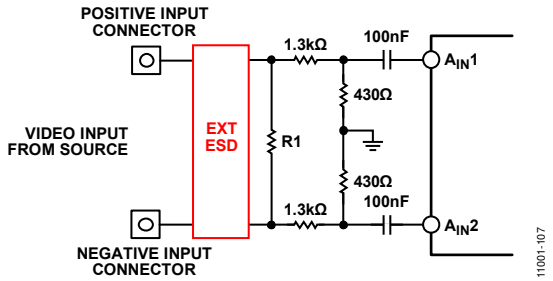

Figure 7. Input Differential Network

Differential video transmission involves transmitting two complementary CVBS signals. It has several key advantages over single-ended transmission, some of which include the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 kΩ and 430 Ω resistors provide a resistor divider with a 0.25 gain. This results in an attenuation of the inputted analog video but also an increase in the input common-mode range of the ADV7182 of up to 4 V p-p.

Note that amplifiers within the ADV7182 restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog video input pins of the ADV7182.

The clamping circuitry within the ADV7182 restores the dc bias of the optimized level before it is fed into the ADC of the ADV7182. See the Clamp Operation section for further information.

The combination of the 1.3 kΩ and 430 Ω resistors and the 100 nF ac coupling capacitor limits current flow into the ADV7182 during short-to-battery (STB) events. See Short-to-Battery Protection section.

To achieve optimal performance, closely match the 1.3 kΩ and 430 Ω resistors; that is, all the 1.3 kΩ and 430 Ω resistors should have the same resistance tolerance, and this tolerance should be as low as possible.

SHORT-TO-BATTERY PROTECTION

In differential mode, the ADV7182 is protected against short-to-battery (STB) events by the external 100 nF ac coupling capacitors (see Figure 7). The external input network resistors are sized to be large enough to reduce the current flow during a STB event, but to be small enough not to effect the operation of the ADV7182.

Choose the power rating of the input network resistors to withstand the high voltages of STB events. Similarly, choose the breakdown voltage of the AC coupling capacitors to be robust to STB events.

The R1 resistor is protected because no current or limited current flows through it during an STB event.

ANALOG FRONT END

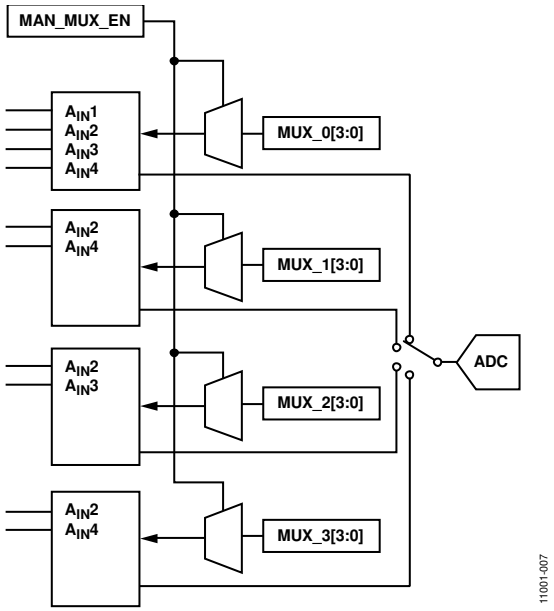

Figure 8. Manual Muxing

INPUT CONFIGURATION

The following two steps are key for configuring the ADV7182 to correctly decode the input video.

1. Use INSEL[4:0] to configure the routing and format decoding (CVBS, Y/C, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. The standard definition processor block, which decodes the digital data, should be configured to process the CVBS, Y/C, or YPrPb format. This is performed by INSEL[4:0] selection.

INSEL[4:0], Input Control, Address 0x00[4:0]

The INSEL bits allow the user to select the input format. They also configure the standard definition processor core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format.

INSEL[4:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 9). This allows the user to route the various video signal types to the decoder and select them using INSEL[4:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 9. INSEL[4:0]

INSEL[4:0]	Video Format	Analog Input
00000	CVBS	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$
01000	Y/C (S-Video)	Y input on $A_{IN}1$
		C input on $A_{IN}2$
01001	Y/C (S-Video)	Y input on $A_{IN}3$
		C input on $A_{IN}4$
01100	YPrPb	Y input on $A_{IN}1$
		Pb input on $A_{IN}2$
		Pr input on $A_{IN}3$
01110	Differential CVBS	Positive on $A_{IN}1$
		Negative on $A_{IN}2$
01111	Differential CVBS	Positive on $A_{IN}3$
		Negative on $A_{IN}4$

ANALOG INPUT MUXING

The ADV7182 has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder.

A maximum of four CVBS inputs can be connected to and decoded by the ADV7182. As shown in the Pin Configuration and Function Description section, these analog input pins lie in close proximity to one another, which requires careful design of the PCB layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended that any unused analog input pins be connected to AGND to act as a shield.

MAN_MUX_EN, Manual Input Muxing Enable, Address 0xC4[7]

To configure the ADV7182 analog muxing section, the user must select the analog input $A_{IN}1$ to $A_{IN}8$ that is to be processed by the ADC. MAN_MUX_EN must be set to 1 to enable the following muxing blocks:

- MUX0[2:0], ADC mux configuration, Address 0xC3[2:0]
- MUX1[2:0], ADC mux configuration, Address 0xC3[6:4]
- MUX2[2:0], ADC mux configuration, Address 0xC4[2:0]
- MUX3[2:0], ADC mux configuration, Address 0x60[2:0]

The four mux sections are controlled by the signal buses, MUX0/MUX1/MUX2/MUX3[2:0]. Table 10 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX0. For example, in a Y/C input configuration, connect MUX0 to the Y channel and MUX1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers should be powered down (see the description of Register 0x3A in Table 95).

Table 10. Manual Mux Settings for ADC (MAN_MUX_EN Must be Set to 1)

MUX0[2:0]	ADC Connected To	MUX1[2:0]	ADC Connected To	MUX2[2:0]	ADC Connected To	MUX3[2:0]	ADC Connected To
000	No connect	000	No connect	000	No connect	000	No connect
001	$A_{IN}1$	001	No connect	001	No connect	001	No connect
010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$
011	$A_{IN}3$	011	No connect	011	$A_{IN}3$	011	No connect
100	$A_{IN}4$	100	$A_{IN}4$	100	No connect	100	$A_{IN}4$

Notes:

- CVBS can only be processed by MUX0.
- Differential CVBS can only be processed by MUX0 (positive channel) and MUX3 (negative channel).
- Y/C can only be processed by MUX0 and MUX1.
- YPrPb can only be processed by MUX0, MUX1, and MUX2.

ANTIALIASING FILTERS

The ADV7182 has optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 9). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 10 and Figure 11 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.

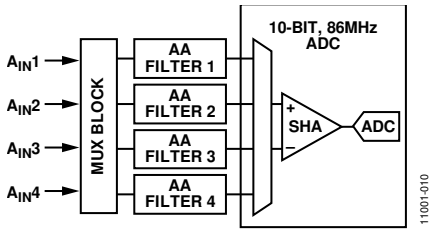

Figure 9. Antialias Filter Configuration

AA_FILT_MAN_OVR, Antialiasing Filter Override, Address 0xF3[4]

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

AA_FILT_EN[3:0], Antialiasing Filter Enable, Address 0xF3[3:0]

These bits allow the user to enable or disable the antialiasing filters on each of the four input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

AA_FILT_EN[0], Antialiasing Filter Enable, Address 0xF3[0]

When AA_FILT_EN[0] is 0, AA Filter 1 is disabled.

When AA_FILT_EN[0] is 1, AA Filter 1 is enabled.

AA_FILT_EN[1], Antialiasing Filter Enable, Address 0xF3[1]

When AA_FILT_EN[1] is 0, AA Filter 2 is disabled.

When AA_FILT_EN[1] is 1, AA Filter 2 is enabled.

AA_FILT_EN[2], Antialiasing Filter Enable, Address 0xF3[2]

When AA_FILT_EN[2] is 0, AA Filter 3 is disabled.

When AA_FILT_EN[2] is 1, AA Filter 3 is enabled.

AA_FILT_EN[3], Antialiasing Filter Enable, Address 0xF3[3]

When AA_FILT_EN[3] is 0, AA Filter 4 is disabled.

When AA_FILT_EN[3] is 1, AA Filter 4 is enabled.

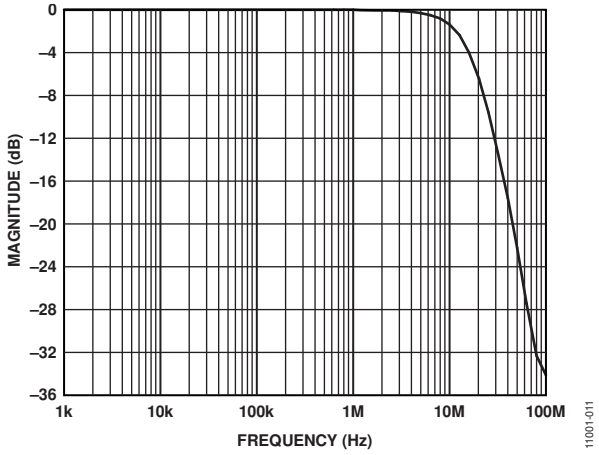

Figure 10. Antialiasing Filter Magnitude Response

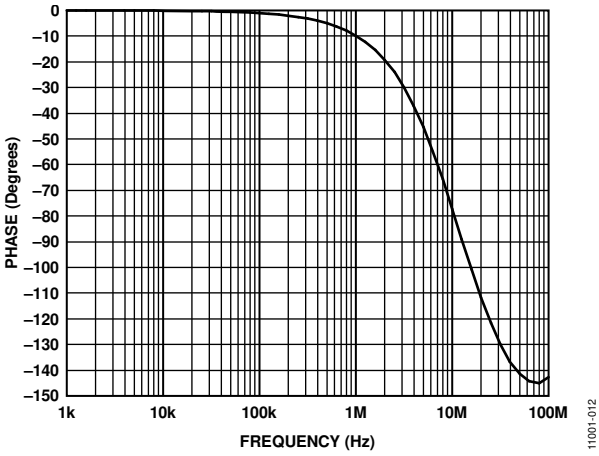

Figure 11. Antialiasing Filter Phase Response

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVING MODES

Power-Down

PWRDWN, Address 0x0F[5]

The ADV7182 can be placed into a chip-wide, power-down mode by setting the PWRDWN bit or by using the $\overline{\text{PWRDWN}}$ pin. The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I^2C interface is unaffected and remains operational in power-down mode.

When PWRDWN is 0, the chip is operational. When PWRDWN is 1 (default), the ADV7182 is in a chip-wide, power-down mode.

RESET CONTROL

Reset, Chip Reset, Address 0x0F[7]

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7182, issues a full chip reset. All I^2C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register tables (see Table 95 and Table 97). After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the part returns to the default for its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self-clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.

The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the MPU Port Description section).

When the reset bit is 0 (default), operation is normal.

When the reset bit is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Tristate Output Drivers

TOD, Address 0x03[6]

This bit allows the user to tristate the output drivers of the ADV7182.

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL pins) can be forced active via the TIM_OE bit. For more information on tristate control, see the Tristate LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TOD is 0, the output drivers are enabled.

When TOD is 1 (default), the output drivers are tristated.

Tristate LLC Driver

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC pin of the ADV7182 to be tristated. For more information on tristate control, refer to the Tristate Output Drivers and Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TRI_LLC is 0, the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is 1 (default), the LLC pin drivers are tristated.

Timing Signals Output Enable

TIM_OE, Address 0x04[3]

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS/FIELD/SFL into the active state (that is, driving state) even if the TOD bit is set. If TIM_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator. This may be the case if only the timing signals are extracted from an incoming signal or if the part is in free-run mode, where a separate chip can output a company logo, for example.

For more information on tristate control, see the Tristate Output Drivers and Tristate LLC Driver sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TIM_OE is 0 (default), HS and VS/FIELD/SFL are tristated according to the TOD bit.

When TIM_OE is 1, HS and VS/FIELD/SFL are forced active all the time.

VS/FIELD/SFL Sync Mux Selection

FLD_OUT_SEL[2:0], Address 0x6B[2:0]

The FLD_OUT_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the Tristate Output Drivers and Tristate LLC Driver sections.

Table 11. FLD_OUT_SEL Function

FLD_OUT_SEL[2:0]	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information.
001	The VS/FIELD/SFL pin outputs vertical sync information.
010 (default)	The VS/FIELD/SFL pin outputs field sync information.
011	The VS/FIELD/SFL pin outputs data enable (DE) information.
100	The VS/FIELD/SFL pin outputs subcarrier frequency lock information.

HS Sync Mux Selection

HS_OUT_SEL[2:0], Address 0x6A[2:0]

The HS_OUT_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) information.

Note that the HS pin must be active for this selection to occur. See the Tristate Output Drivers and Tristate LLC Driver sections.

Table 12. HS_OUT_SEL Function

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs data enable (DE) information.
100	The HS pin outputs subcarrier frequency lock (SFL) information.

Drive Strength Selection (Data)

DR_STR[1:0], Address 0xF4[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the drive strength for the pixel output pins (P[7:0]) and the timing pins (HS and VS/FIELD/SFL).

For more information on tristate control, see the Tristate Output Drivers and Tristate LLC Driver sections.

Table 13. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

DR_STR_C[1:0], Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Data) Section.

Table 14. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (I^2C)

DR_STR_S[1:0], Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the I^2C signal output drivers. This affects the drive strength for the SDA and SCL pins.

Table 15. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN, Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7182 core to an encoder in a decoder/encoder back-to-back arrangement.

When the EN_SFL_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

GLOBAL STATUS REGISTER

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7182. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV7182.

IDENTIFICATION

IDENT[7:0], Address 0x11[7:0]

This is the register identification of the ADV7182 revision. Table 16 describes the various versions of the ADV7182.

Table 16. IDENT CODE

IDENT[7:0]	Description
0x40	Prerelease silicon
0x41	Released silicon

STATUS 1

Status 1[7:0], Address 0x10[7:0]

This read-only register provides information about the internal status of the ADV7182.

See the CIL[2:0], Count into Lock, Address 0x51[2:0] section and the COL[2:0], Count out of Lock, Address 0x51[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable, Address 0x51[7] section.

Table 17. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read)
2	FSC_LOCK	f_{SC} locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2

Status 2[7:0], Address 0x12[7:0]

Table 18. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Macrovision color striping
1	MVCS T3	Macrovision color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV PS DET	Detected Macrovision pseudo-sync pulses
3	MV AGC DET	Detected Macrovision AGC pulses
4	LL NSTD	Line length is nonstandard
5	FSC NSTD	f_{SC} frequency is nonstandard
6	Reserved	
7	Reserved	

STATUS 3

Status 3[7:0], Address 0x13[7:0]

Table 19. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	Reserved	
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved
4	FREE_RUN_ACT	Flags if ADV7182 has entered free-run mode (see Free-Run Operation section)
5	STD FLD LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

AUTODETECTION RESULT

AD_RESULT[2:0], Address 0x10[6:4]

The AD_RESULT[2:0] bits report back on the findings from the ADV7182 autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure it.

Table 20. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

VIDEO PROCESSOR

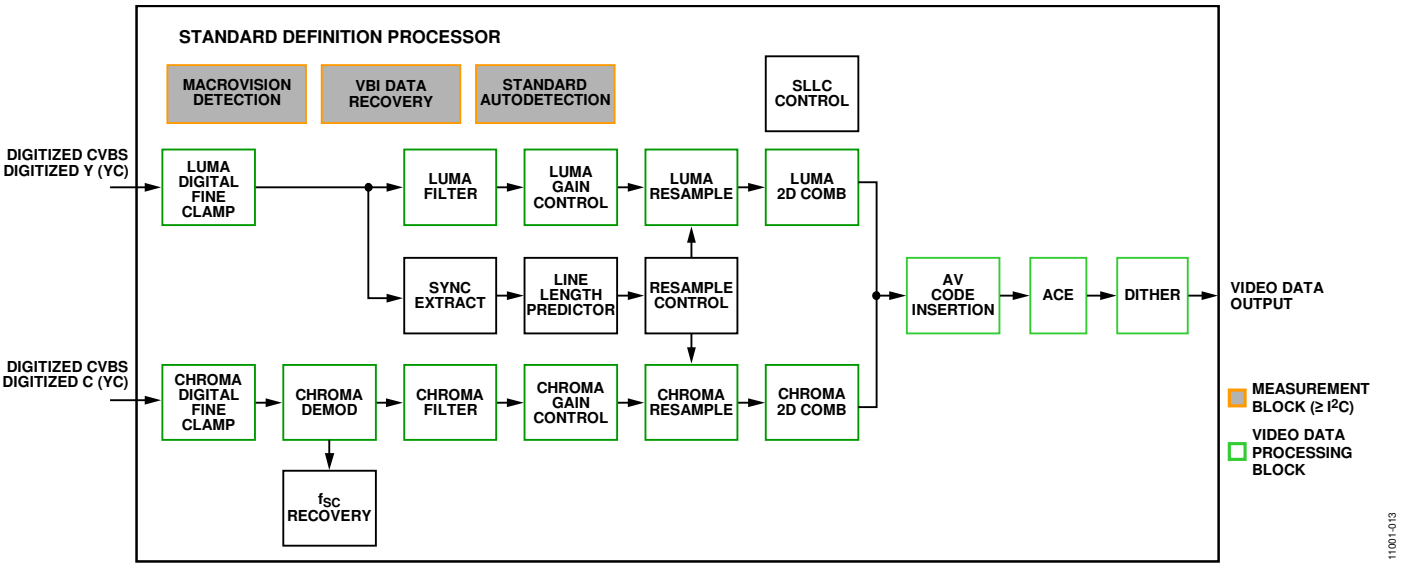

Figure 12. Block Diagram of Video Processor

Figure 12 shows a block diagram of the ADV7182 video processor. The ADV7182 can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

SD LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct for line length errors as well as dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted (as per ITU-R BT.656).

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, superadaptive comb filter provides high quality Y/C separation in case the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted (as per ITU-R BT.656).

ACE AND DITHER PROCESSING BLOCKS

- ACE. This block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail. See the Adaptive Contrast Enhancement section.
- Dither. When enabled, this block converts the digital output of the ADV7182 from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV7182 to communicate with some LCD panels. See the Dither Function section.

SYNC PROCESSING

The ADV7182 extracts syncs embedded in the analog input video signal. There is currently no support for external HS/VS inputs. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure that the ADV7182 outputs 720 active pixels per line.

The sync processing on the ADV7182 also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSync processor. This block provides extra filtering of the detected VSyncs to improve vertical lock.
- HSync processor. The HSync processor is designed to filter incoming HSyncs that were corrupted by noise, providing much improved performance for video signals with a stable time base but poor SNR.

VBI DATA RECOVERY

The ADV7182 can retrieve the following information from the input video:

- Wide screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed captioning (CCAP)
- Macrovision protection presence
- Teletext

The ADV7182 is also capable of automatically detecting the incoming video standard with respect to the following:

- Color subcarrier frequency
- Field rate
- Line rate

The ADV7182 can configure itself to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x02[7:4]) allow the user to force the digital core into a specific video standard. This is not necessary under normal circumstances. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Autodetection of SD Modes

To guide the autodetect system of the ADV7182, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x02[7:4]

Table 21. VID_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

AD_SEC525_EN, SECAM 525 Autodetect Enable, Address 0x07[7]

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM-modulated color component.

AD_SECAM_EN, SECAM Autodetect Enable, Address 0x07[6]

Setting AD_SECAM_EN to 0 (default) disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 enables the detection of SECAM.

AD_N443_EN, NTSC 4.43 Autodetect Enable, Address 0x07[5]

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, PAL 60 Autodetect Enable, Address 0x07[4]

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, PAL N Autodetect Enable, Address 0x07[3]

Setting AD_PALN_EN to 0 (default) disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 enables the detection of the PAL N standard.

AD_PALM_EN, PAL M Autodetect Enable, Address 0x07[2]

Setting AD_PALM_EN to 0 (default) disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 enables the detection of PAL M.

AD_NTSC_EN, NTSC Autodetect Enable, Address 0x07[1]

Setting AD_NTSC_EN to 0 (default) disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 enables the detection of standard NTSC.

AD_PAL_EN, PAL B/PAL D/PAL I/PAL G/PAL H Autodetect Enable, Address 0x07[0]

Setting AD_PAL_EN to 0 (default) disables the detection of standard PAL.

Setting AD_PAL_EN to 1 enables the detection of standard PAL.

SFL_INV, Subcarrier Frequency Lock Inversion, Address 0x41[6]

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

Second, there was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (genlock telegram) bit directly, whereas the newer ones invert the bit prior to using it. The reason for this is that the inversion compensated for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the ADV717x and ADV73xx encoders, the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For the older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL_INV to 0 (default) makes the part SFL compatible with the ADV717x and ADV73xx video encoders.

Setting SFL_INV to 1 makes the part SFL compatible with the older video encoders.

Lock Related Controls

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1[7:0], Address 0x10[7:0] section). Figure 13 outlines the signal flow and the controls that are available to influence the way the lock status information is generated.

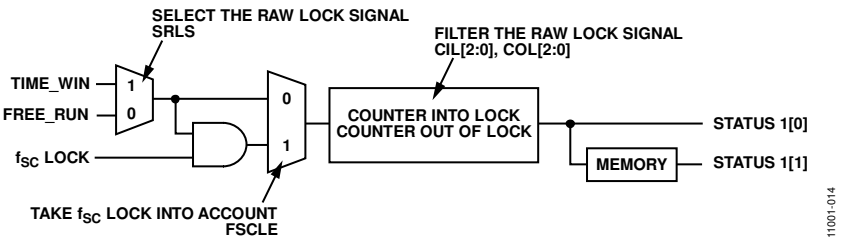

Figure 13. Lock Related Signal Path

SRLS, Select Raw Lock Signal, Address 0x51[6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register). See Figure 13.

- The TIME_WIN signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE_RUN signal (that is, evaluate over several fields).

Setting SRLS to 1 selects the TIME_WIN signal (that is, evaluate on a line-to-line basis) .

FSCLE, f_{SC} Lock Enable, Address 0x51[7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7182 in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is 0 (default), the overall lock status is dependent only on horizontal sync lock.

When FSCLE is 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

CIL[2:0], Count into Lock, Address 0x51[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Status 1[1:0]. The bit counts the value in lines of video.

Table 22. CIL Function

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COL[2:0], Count out of Lock, Address 0x51[5:3]

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into the unlocked state and reports this via Status 1[1:0]. It counts the value in lines of video.

Table 23. COL Function

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROLS

These registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Contrast Adjust, Address 0x08[7:0]

This register allows the user to control contrast adjustment of the picture.

Table 24. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0], SD Saturation Cb Channel, Address 0xE3[7:0]

This register allows the user to control the gain of the Cb channel only, which in turn adjusts the saturation of the picture.

Table 25. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0], SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only, which in turn adjusts the saturation of the picture.

Table 26. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cr channel = −42 dB
0xFF	Gain on Cr channel = +6 dB

SD_OFF_Cb[7:0], SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register (Address 0x0B).

Table 27. SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 mV offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0], SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 28. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 mV offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0], Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 29. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = −30 IRE

HUE[7:0], Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM-modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 30. HUE Function

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0], Default Value Y, Address 0x0C[7:2]

When the ADV7182 loses lock on the incoming video signal or when there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF_VAL_AUTO_EN bit is 1 and the ADV7182 has lost lock to the input video signal, this is the intended mode of operation (automatic mode).
- If the DEF_VAL_EN bit is 1, regardless of the lock status of the video decoder, this is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = {DEF_Y[5:0], 0, 0}.

For DEF_Y[5:0], 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

DEF_C[7:0], Default Value C, Address 0x0D[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if:

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7182 cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7182 for the chroma side is Cr[4:0] = {DEF_C[7:4]} and Cb[4:0] = {DEF_C[3:0]}.

For DEF_C[7:0], 0x7C (blue) is the default value for Cr and Cb.