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Multiformat SDTV Video Decoder

ADV7183B

FEATURES

- Multiformat video decoder supports NTSC-(J, M, 4.43), PAL-(B/D/G/H/I/M/N), SECAM
- Integrates three 54 MHz, 10-bit ADCs
- Clocked from a single 27 MHz crystal
- Line-locked clock-compatible (LLC)
- Adaptive Digital Line Length Tracking (ADLLT™), signal processing, and enhanced FIFO management give mini-TBC functionality
- 5-line adaptive comb filters
- Proprietary architecture for locking to weak, noisy, and unstable video sources such as VCRs and tuners
- Subcarrier frequency lock and status information output
- Integrated AGC with adaptive peak white mode
- Macrovision® copy protection detection
- Chroma transient improvement (CTI)
- Digital noise reduction (DNR)
- Multiple programmable analog input formats
  - Composite video (CVBS)
  - S-Video (Y/C)
  - YPrPb component (VESA, MII, SMPTE, and BetaCam)
- 12 analog video input channels
- Automatic NTSC/PAL/SECAM identification
- Digital output formats (8-bit or 16-bit)
  - ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- 0.5 V to 1.6 V analog signal input range
- Differential gain: 0.5% typ
- Differential phase: 0.5° typ
- Programmable video controls
  - Peak white/hue/brightness/saturation/contrast
- Integrated on-chip video timing generator
- Free-run mode (generates stable video output with no I/P)
- VBI decode support for close captioning, WSS, CGMS, EDTV, Gemstar® 1×/2×
- Power-down mode
- 2-wire serial MPU interface (I²C®-compatible)
- 3.3 V analog, 1.8 V digital core; 3.3 V IO supply
- 2 temperature grades: 0°C to +70°C and –40°C to +85°C
- 80-lead LQFP Pb-free package

APPLICATIONS

- DVD recorders
- Video projectors
- HDD-based PVRs/DVDRs
- LCD TVs
- Set-top boxes
- Security systems
- Digital televisions
- AVR receivers

GENERAL DESCRIPTION

The ADV7183B integrated video decoder automatically detects and converts a standard analog baseband television signal-compatible with worldwide standards NTSC, PAL, and SECAM into 4:2:2 component video data-compatible with 16-/8-bit CCIR601/CCIR656.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape-based sources, broadcast sources, security/surveillance cameras, and professional systems.

The 10-bit accurate A/D conversion provides professional quality video performance and is unmatched. This allows true 8-bit resolution in the 8-bit output mode.

The 12 analog input channels accept standard composite, S-Video, YPrPb video signals in an extensive number of combinations. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 0.5 V up to 1.6 V. Alternatively, these can be bypassed for manual settings.

The fixed 54 MHz clocking of the ADCs and datapath for all modes allows very precise, accurate sampling and digital filtering. The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% line length variation. The output control signals allow glueless interface connections in almost any application. The ADV7183B modes are set up over a 2-wire, serial, bidirectional port (I²C-compatible).

The ADV7183B is fabricated in a 3.3 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7183B is packaged in a small 80-lead LQFP Pb-free package.

Rev. B

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COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers

Data Sheet

- ADV7183B: Multifromat SDTV Video Decoder Data Sheet

REFERENCE MATERIALS

Technical Articles

- Analog Video Time Base Correction and Processing for Nonstandard TV Signals
- Optimizing standard-definition video on high-definition displays

DESIGN RESOURCES

- ADV7183B Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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INTRODUCTION

The ADV7183B is a high quality, single chip, multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked, clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape based sources, broadcast sources, security/surveillance cameras, and professional systems.

ANALOG FRONT END

The ADV7183B analog front end comprises three 10-bit ADCs that digitize the analog video signal before applying it to the standard definition processor. The analog front end uses differential channels to each ADC to ensure high performance in mixed-signal applications.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7183B. Current and voltage clamps are positioned in front of each ADC to ensure the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping within the ADV7183B. The ADCs are configured to run in 4× oversampling mode.

STANDARD DEFINITION PROCESSOR (SDP)

The ADV7183B is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported include PAL B/D/I/G/H, PAL60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7183B can automatically detect the video standard and process it accordingly.

The ADV7183B has a 5-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required. Video user controls such as brightness, contrast, saturation, and hue are also available within the ADV7183B.

The ADV7183B implements a patented adaptive digital line-length tracking (ADLLT) algorithm to track varying video line lengths from sources. ADLLT enables the ADV7183B to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The ADV7183B contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7183B can process a variety of VBI data services, such as closed captioning (CC), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar 1×/2×, and extended data service (XDS). The ADV7183B is fully Macrovision® certified; detection circuitry enables Type I, II, and III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

FUNCTIONAL BLOCK DIAGRAM

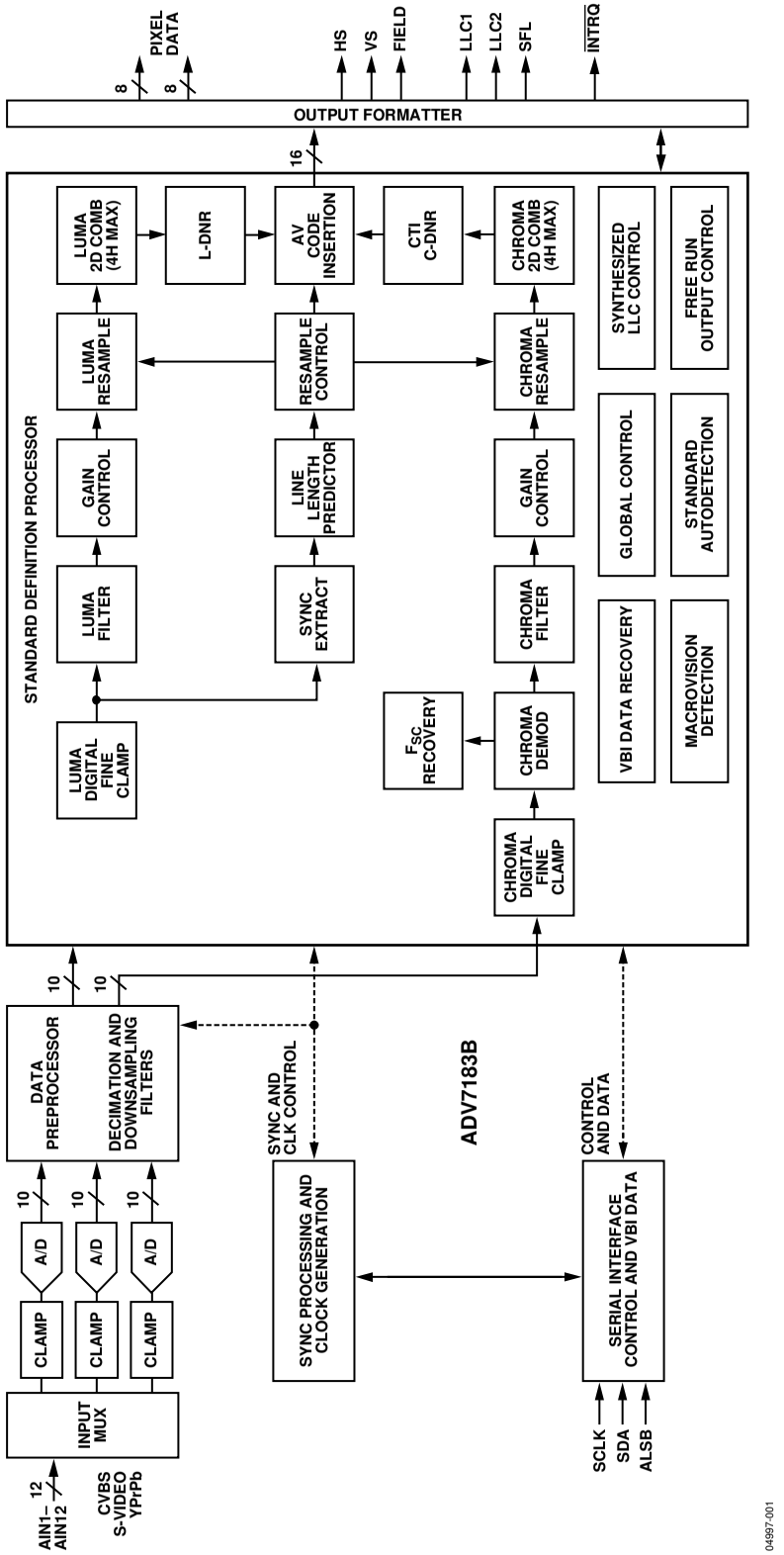

Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 1.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 54 MHz		–0.475/+0.6	±3	LSB
Differential Nonlinearity	DNL	BSL at 54 MHz		–0.25/+0.5	–0.7/+2	LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	Pins listed in Note 3	–50		+50	µA
		All other pins	–10		+10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pins listed in Note 4			50	µA
		All other pins			10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[5]						
Digital Core Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		3.0	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2.0	V
Analog Power Supply	A_{VDD}		3.15	3.3	3.45	V
Digital Core Supply Current	I_{DVDD}			82		mA
Digital I/O Supply Current	I_{DVDDIO}			2		mA
PLL Supply Current	I_{PVDD}			10.5		mA
Analog Supply Current	I_{AVDD}	CVBS input[6]		85		mA
		YPrPb input[7]		180		mA
Power-Down Current	I_{PWRDN}			1.5		mA
Power-Up Time	t_{PWRUP}			20		ms

[1]Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2]The min/max specifications are guaranteed over this range.
[3] Pins 36 and 79.
[4] Pins 1, 2, 5, 6, 8, 12, 17, 18 to 24, 32 to 35, 74 to 76, 80.
[5] Guaranteed by characterization.
[6] ADC1 powered on.
[7] All three ADCs powered on.

VIDEO SPECIFICATIONS

At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 2.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS I/P, modulate 5-step		0.5	0.7	Degrees
Differential Gain	DG	CVBS I/P, modulate 5-step		0.5	0.7	%
Luma Nonlinearity	LNL	CVBS I/P, 5-step		0.5	0.7	%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
		Luma flat field	58	60		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
F_{SC} Subcarrier Lock Range				±1.3		Hz
Color Lock In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		Degrees
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		Degrees
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V I/P		1		%
Luma Contrast Accuracy		CVBS, 1 V I/P		1		%

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

TIMING SPECIFICATIONS

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 3.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.6363		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
LLC1 Rising to LLC2 Rising	t_{11}			0.5		ns
LLC1 Rising to LLC2 Falling	t_{12}			0.5		ns
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{13}	Negative clock edge to start of valid data; ($t_{ACCESS} = t_{10} - t_{13}$)			3.4	ns
Data Output Transitional Time	t_{14}	End of valid data to negative clock edge; ($t_{HOLD} = t_9 + t_{14}$)			2.4	ns
Propagation Delay to Hi-Z	t_{15}			6		ns
Max Output Enable Access Time	t_{16}			7		ns
Min Output Enable Access Time	t_{17}			4		ns

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted). Recommended analog input video signal range: 0.5 V to 1.6 V, typically 1 V p-p.

Table 4.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY						
External Clamp Capacitor				0.1		µF
Input Impedance		Clamps switched off		10		MΩ
Large Clamp Source Current				0.75		mA
Large Clamp Sink Current				0.75		mA
Fine Clamp Source Current				60		µA
Fine Clamp Sink Current				60		µA

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

THERMAL SPECIFICATIONS

Table 5.

Parameter[1,2]	Symbol	Test Conditions	Min	Typ	Max	Unit
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane		7.6		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane		38.1		°C/W

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

TIMING DIAGRAMS

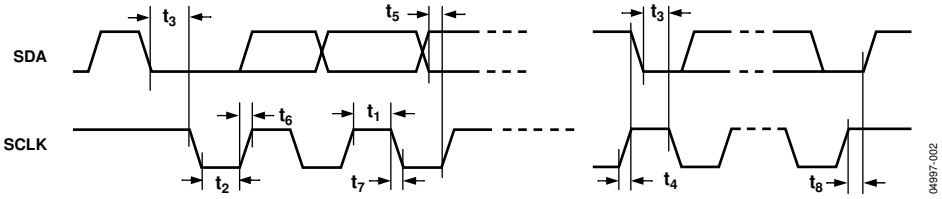

Figure 2. I²C Timing

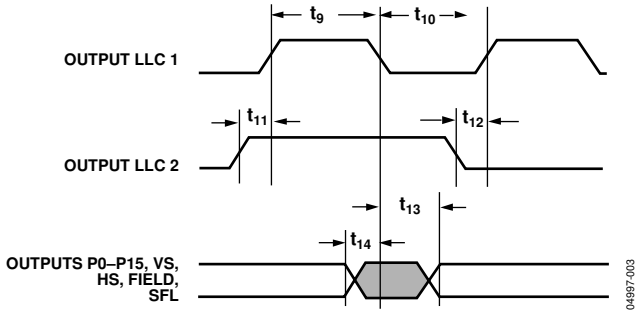

Figure 3. Pixel Port and Control Output Timing

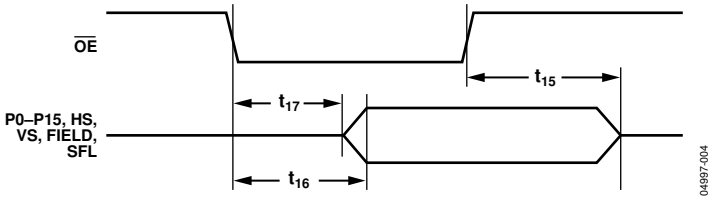

Figure 4. $\overline{OE}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
A_{VDD} to GND	4 V
A_{VDD} to AGND	4 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to A_{VDD}	–0.3 V to +0.3 V
P_{VDD} to D_{VDD}	–0.3 V to +0.3 V
D_{VDDIO} – P_{VDD}	–0.3 V to +2 V
D_{VDDIO} – D_{VDD}	–0.3 V to +2 V
A_{VDD} – P_{VDD}	–0.3 V to +2 V
A_{VDD} – D_{VDD}	–0.3 V to +2 V
Digital Inputs Voltage to DGND	–0.3 V to D_{VDDIO} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to D_{VDDIO} + 0.3 V
Analog Input to AGND	AGND – 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	–65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

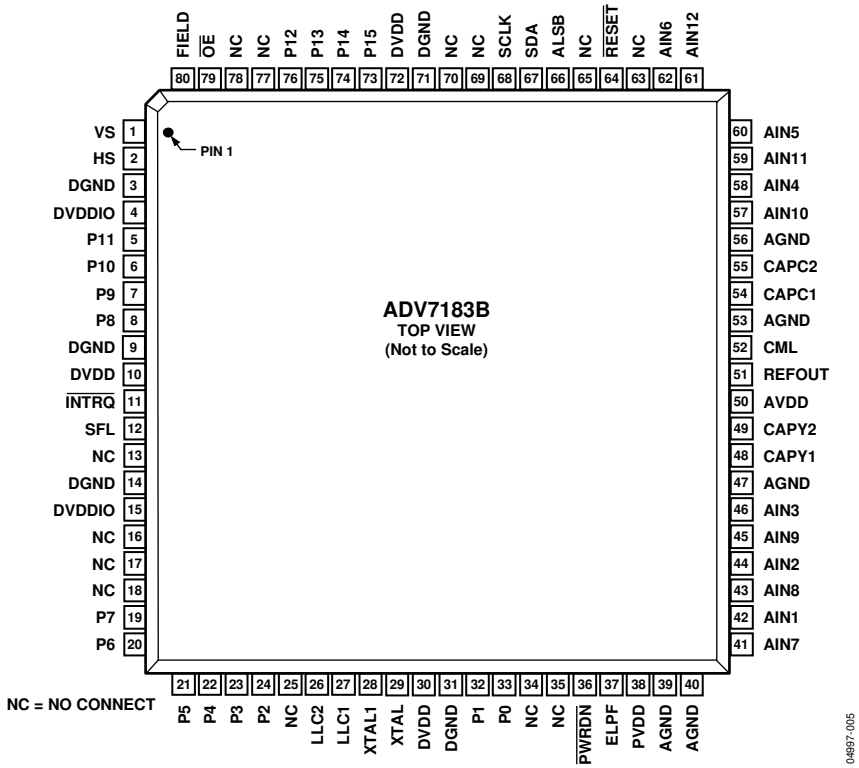

Figure 5. 80-Lead LQFP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
3, 9, 14, 31, 71	DGND	G	Digital Ground.
39, 40, 47, 53, 56	AGND	G	Analog Ground.
4, 15	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
10, 30, 72	DVDD	P	Digital Core Supply Voltage (1.8 V).
50	AVDD	P	Analog Supply Voltage (3.3 V).
38	PVDD	P	PLL Supply Voltage (1.8 V).
42, 44, 46, 58, 60, 62, 41, 43, 45, 57, 59, 61	AIN1 to AIN12	I	Analog Video Input Channels.
11	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video. See the interrupt register map in Table 83.
13, 16 to 18, 25, 34, 35, 63, 65, 69, 70, 77, 78	NC		No Connect Pins.
33, 32, 24, 23, 22, 21, 20, 19, 8, 7, 6, 5, 76, 75, 74, 73	P0 to P15	O	Video Pixel Output Port.
2	HS	O	Horizontal Synchronization Output Signal.
1	VS	O	Vertical Synchronization Output Signal.
80	FIELD	O	Field Synchronization Output Signal.
67	SDA	I/O	I^2C Port Serial Data Input/Output Pin.
68	SCLK	I	I^2C Port Serial Clock Input. Maximum clock rate of 400 kHz.
66	ALSB	I	This pin selects the I^2C address for the ADV7183B. ALSB set to Logic 0 sets the address for a write as 0x40; for ALSB set to logic high, the address selected is 0x42.
64	$\overline{\text{RESET}}$	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7183B circuitry.
27	LLC1	O	This is a line-locked output clock for the pixel data output by the ADV7183B. Nominally 27 MHz, but varies up or down according to video line length.
26	LLC2	O	This is a divide-by-2 version of the LLC1 output clock for the pixel data output by the ADV7183B. Nominally 13.5 MHz, but varies up or down according to video line length.
29	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or can be overdriven by an external 3.3 V, 27 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
28	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 3.3 V, 27 MHz clock oscillator source is used to clock the ADV7183B. In crystal mode, the crystal must be a fundamental crystal.
36	$\overline{\text{PWRDN}}$	I	A logic low on this pin places the ADV7183B in a power-down mode. Refer to the IP2PC Register Maps section for more options on power-down modes for the ADV7183B.
79	$\overline{\text{OE}}$	I	When set to a logic low, $\overline{\text{OE}}$ enables the pixel output bus, P15 to P0 of the ADV7183B. A logic high on the $\overline{\text{OE}}$ pin places Pins P15 to P0, HS, VS, SFL into a high impedance state.
37	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 46.
12	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc. digital video encoder.
51	REFOUT	O	Internal Voltage Reference Output. Refer to Figure 46 for a recommended capacitor network for this pin.
52	CML	O	The CML pin is a common-mode level for the internal ADCs. Refer to Figure 46 for a recommended capacitor network for this pin.
48, 49	CAPY1, CAPY2	I	ADC's Capacitor Network. Refer to Figure 46 for a recommended capacitor network for this pin.
54, 55	CAPC1, CAPC2	I	ADC's Capacitor Network. Refer to Figure 46 for a recommended capacitor network for this pin.

ANALOG FRONT END

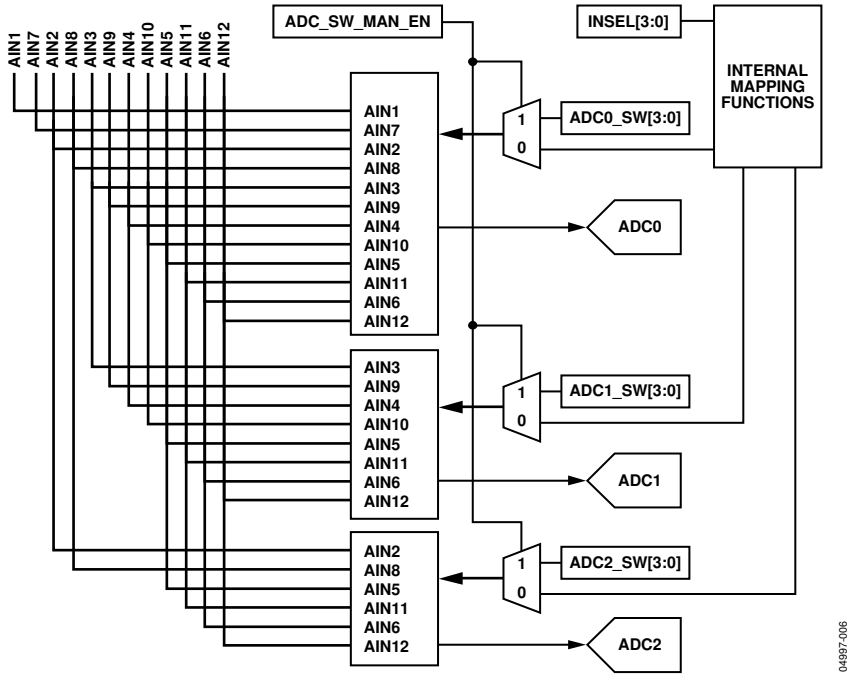

Figure 6. Internal Pin Connections

ANALOG INPUT MUXING

The ADV7183B has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 6 outlines the overall structure of the input muxing provided in the ADV7183B.

As seen in Figure 6, the analog input muxes can be controlled by functional registers (INSEL) or manually. Using INSEL[3:0] simplifies the setup of the muxes and minimizes crosstalk between channels by pre-assigning the input channels. This is referred to as ADI recommended input muxing.

Control via an I²C manual override (ADC_sw_man_en, ADC0_sw, and ADC1_sw, ADC2_sw) is provided for applications with special requirements (for example, number/combinations of signals) that would not be served by the pre-assigned input connections. This is referred to as manual input muxing.

Refer to Figure 7 for an overview of the two methods of controlling the ADV7183B's input muxing.

ADI Recommended Input Muxing

A maximum of 12 CVBS inputs can be connected and decoded by the ADV7183B. As seen in Figure 5, this means the sources will have to be connected to adjacent pins on the IC. This calls for a careful design of the PCB layout, such as ground shielding between all signals routed through tracks that are physically close together.

INSEL[3:0] Input Selection, Address 0x00[3:0]

The INSEL bits allow the user to select an input channel as well as the input format. Depending on the PCB connections, only a subset of the INSEL modes is valid. The INSEL[3:0] not only switches the analog input muxing, it also configures the standard definition processor core to process CVBS (Comp), S-Video (Y/C), or component (YPbPr) format.

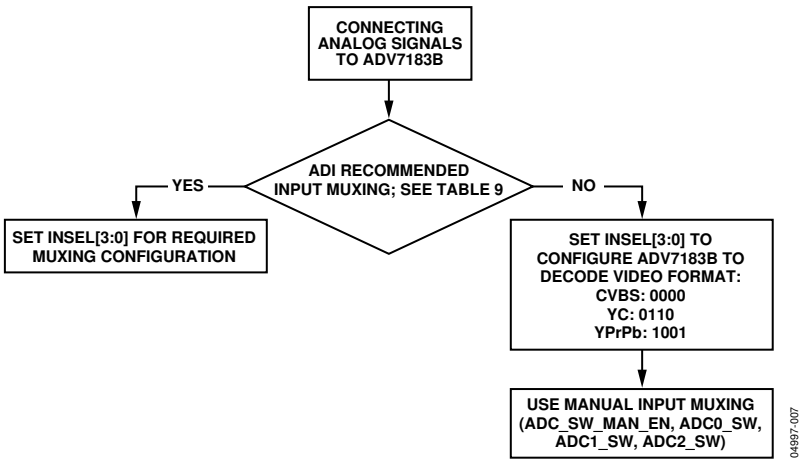

Figure 7. Input Muxing Overview

Table 8. Input Channel Switching Using INSEL[3:0]

	Description	
INSEL[3:0]	**Analog Input Pins**	**Video Format**
0000 (default)	CVBS1 = AIN1	Composite
0001	CVBS2 = AIN2	Composite
0010	CVBS3 = AIN3	Composite
0011	CVBS4 = AIN4	Composite
0100	CVBS5 = AIN5	Composite
0101	CVBS6 = AIN6	Composite
0110	Y1 = AIN1	Y/C
	C1 = AIN4	Y/C
0111	Y2 = AIN2	Y/C
	C2 = AIN5	Y/C
1000	Y3 = AIN3	Y/C
	C3 = AIN6	Y/C
1001	Y1 = AIN1	YPrPb
	PB1 = AIN4	YPrPb
	PR1 = AIN5	YPrPb
1010	Y2 = AIN2	YPrPb
	PB2 = AIN3	YPrPb
	PR2 = AIN6	YPrPb
1011	CVBS7 = AIN7	Composite
1100	CVBS8 = AIN8	Composite
1101	CVBS9 = AIN9	Composite
1110	CVBS10 = AIN10	Composite
1111	CVBS11 = AIN11	Composite

Table 9. Input Channel Assignments

Input Channel	Pin No.	ADI Recommended Input Muxing Control INSEL[3:0]		
AIN7	41	CVBS7		
AIN1	42	CVBS1	Y/C1-Y	YPrPb1-Y
AIN8	43	CVBS8		
AIN2	44	CVBS2	Y/C2-Y	YPrPb2-Y
AIN9	45	CVBS9		
AIN3	46	CVBS3	Y/C3-Y	YPrPb2-Pb
AIN10	57	CVBS10		
AIN4	58	CVBS4	Y/C1-C	YPrPb1-Pb
AIN11	59	CVBS11		
AIN5	60	CVBS5	Y/C2-C	YPrPb1-Pr
AIN12	61	Not available		
AIN6	62	CVBS6	Y/C3-C	YPrPb2-Pr

ADI recommended input muxing is designed to minimize crosstalk between signal channels and to obtain the highest level of signal integrity. Table 9 summarizes how the PCB layout should connect analog video signals to the ADV7183B.

It is strongly recommended to connect any unused analog input pins to AGND to act as a shield.

Inputs AIN7 to AIN11 should be connected to AGND when only six input channels are used. This improves the quality of the sampling due to better isolation between the channels.

AIN12 is not under the control of INSEL[3:0]. It can be routed to ADC0/ADC1/ADC2 only by manual muxing. See Table 10 for details.

MANUAL INPUT MUXING

By accessing a set of manual override muxing registers, the analog input muxes of the ADV7183B can be controlled directly. This is referred to as manual input muxing.

Manual input muxing overrides other input muxing control bits, such as INSEL.

The manual muxing is activated by setting the ADC_SW_MAN_EN bit. It affects only the analog switches in front of the ADCs. This means if the settings of INSEL and the manual input muxing registers (ADC0/ADC1/ADC2_sw) contradict each other, the ADC0/ADC1/ADC2_sw settings apply, and INSEL is ignored.

Manual input muxing controls only the analog input muxes. INSEL[3:0] still has to be set so the follow-on blocks process the video data in the correct format. This means INSEL must still be used to tell the ADV7183B whether the input signal is of component, Y/C, or CVBS format.

Restrictions in the channel routing are imposed by the analog signal routing inside the IC; every input pin cannot be routed to each ADC. Refer to Figure 6 for an overview on the routing capabilities inside the chip. The three mux sections can be controlled by the reserved control signal buses ADC0/ADC1/ADC2_sw[3:0]. Table 10 explains the control words used.

SETADC_sw_man_en, Manual Input Muxing Enable, Address 0xC4[7]

ADC0_sw[3:0], ADC0 mux configuration, Address 0xC3[3:0]
ADC1_sw[3:0], ADC1 mux configuration, Address 0xC3[7:4]
ADC2_sw[3:0], ADC2 mux configuration, Address 0xC4[3:0]

Table 10. Manual Mux Settings for All ADCs (SETADC_sw_man_en = 1)

ADC0_sw[3:0]	ADC0 Connected to	ADC1_sw[3:0]	ADC1 Connected to	ADC2_sw[3:0]	ADC2 Connected to
0000	No connection	0000	No connection	0000	No connection
0001	AIN1	0001	No connection	0001	No connection
0010	AIN2	0010	No connection	0010	AIN2
0011	AIN3	0011	AIN3	0011	No connection
0100	AIN4	0100	AIN4	0100	No connection
0101	AIN5	0101	AIN5	0101	AIN5
0110	AIN6	0110	AIN6	0110	AIN6
0111	No connection	0111	No connection	0111	No connection
1000	No connection	1000	No connection	1000	No connection
1001	AIN7	1001	No connection	1001	No connection
1010	AIN8	1010	No connection	1010	AIN8
1011	AIN9	1011	AIN9	1011	No connection
1100	AIN10	1100	AIN10	1100	No connection
1101	AIN11	1101	AIN11	1101	AIN11
1110	AIN12	1110	AIN12	1110	AIN12
1111	No connection	1111	No connection	1111	No connection

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVE MODES

Power-Down

PDBP, Address 0x0F[2]

The digital core of the ADV7183B can be shut down by using the $\overline{\text{PWRDN}}$ pin and the PWRDN bit (see below). The PDBP controls which of the two pins has the higher priority. The default is to give priority to the $\overline{\text{PWRDN}}$ pin. This allows the user to have the ADV7183B powered down by default.

When PDBD is 0 (default), the digital core power is controlled by the $\overline{\text{PWRDN}}$ pin (the bit is disregarded).

When PDBD is 1, the bit has priority (the pin is disregarded).

PWRDN, Address 0x0F[5]

Setting the PWRDN bit switches the ADV7183B into a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down. The PWRDN bit also affects the analog blocks and switches them into low current modes. The I^2C interface is unaffected and remains operational in power-down mode.

The ADV7183B leaves the power-down state if the PWRDN bit is set to 0 (via I^2C), or if the overall part is reset using the $\overline{\text{RESET}}$ pin.

PDBP must be set to 1 for the PWRDN bit to power down the ADV7183B.

When PWRDN is 0 (default), the chip is operational.

When PWRDN is 1, the ADV7183B is in chip-wide power-down.

ADC Power-Down Control

The ADV7183B contains three 10-bit ADCs (ADC 0, ADC 1, and ADC 2). If required, each ADC can be powered down individually.

The ADCs should be powered down when in:

- CVBS mode. ADC 1 and ADC 2 should be powered down to save on power consumption.
- S-Video mode. ADC 2 should be powered down to save on power consumption.

PWRDN_ADC_0, Address 0x3A[3]

When PWRDN_ADC_0 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_0 is 1, ADC 0 is powered down.

PWRDN_ADC_1, Address 0x3A[2]

When PWRDN_ADC_1 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_1 is 1, ADC 1 is powered down.

PWRDN_ADC_2, Address 0x3A[1]

When PWRDN_ADC_2 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_2 is 1, ADC 2 is powered down.

RESET CONTROL

Chip Reset (RES), Address 0x0F[7]

Setting this bit, equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7183B, issues a full chip reset. All I^2C registers are reset to their default values. (Some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register table.) After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the RES bit (or initiating a reset via the pin), the part returns to the default mode of operation with respect to its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self-clearing.

Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.

The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented. See the MPU Port Description section.

When RES is 0 (default), operation is normal.

When RES is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Three-State Output Drivers

TOD, Address 0x03[6]

This bit allows the user to three-state the output drivers of the ADV7183B.

Upon setting the TOD bit, the P15 to P0, HS, VS, FIELD, and SFL pins are three-stated.

The timing pins (HS/VS/FIELD) can be forced active via the TIM_OE bit. For more information on three-state control, refer to the Three-State LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

The ADV7183B supports three-stating via a dedicated pin. When set high, the $\overline{OE}$ pin three-states the output drivers for the P15 to P0, HS, VS, FIELD, and SFL pins. The output drivers are three-stated if the TOD bit or the $\overline{OE}$ pin is set high.

When TOD is 0 (default), the output drivers are enabled.

When TOD is 1, the output drivers are three-stated.

Three-State LLC Driver

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC1 and LLC2 pins of the ADV7183B to be three-stated. For more information on three-state control, refer to the Three-State Output Drivers and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

When TRI_LLC is 0 (default), the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is 1, the LLC pin drivers are three-stated.

Timing Signals Output Enable

TIM_OE, Address 0x04[3]

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD pins into the active (driving) state even if the TOD bit is set. If set to low, the HS, VS, and FIELD pins are three-stated, dependent on the TOD bit. This functionality is useful if the decoder is used as a timing generator only. This can happen when only the timing signals are to be extracted from an incoming signal, or if the part is in free-run mode where a separate chip can output, for an example, a company logo.

For more information on three-state control, refer to the Three-State Output Drivers and the Three-State LLC Driver sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

When TIM_OE is 0 (default), the HS, VS, and FIELD pins are three-stated according to the TOD bit.

When TIM_OE is 1, HS, VS, and FIELD are forced active all the time.

Drive Strength Selection (Data)

DR_STR[1:0] Address 0xF4[5:4]

For EMC and crosstalk reasons, it can be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[15:0] output drivers.

For more information on three-state control, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Sync) sections.

Table 11. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

DR_STR_C[1:0] Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, refer to the Drive Strength Selection (Sync) and the Drive Strength Selection (Data) sections.

Table 12. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Sync)

DR_STR_S[1:0] Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and F are driven. For more information, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Data) sections.

Table 13. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as GenLock) from the ADV7183B to an encoder in a decoder-encoder back-to-back arrangement.

When EN_SFL_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

Polarity LLC Pin

PCLK Address 0x37[0]

The polarity of the clock that leaves the ADV7183B via the LLC1 and LLC2 pins can be inverted using the PCLK bit.

Changing the polarity of the LLC clock output can be necessary to meet the setup-and-hold time expectations of follow-on chips.

This bit also inverts the polarity of the LLC2 clock.

When PCLK is 0, the LLC output polarity is inverted.

When PCLK is 1 (default), the LLC output polarity is normal (as per the timing diagrams).

GLOBAL STATUS REGISTERS

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7183B. The three other registers contain status bits regarding IC operation.

IDENTIFICATION

IDENT[7:0] Address 0x11[7:0]

This register provides identification of the revision of the ADV7183B.

An identification value of 0x11 indicates the ADV7183, released silicon.

An identification value of 0x13 indicates the ADV7183B silicon.

STATUS 1

STATUS_1[7:0] Address 0x10[7:0]

This read-only register provides information about the internal status of the ADV7183B.

See VS_Coast[1:0] Address 0xF9[3:2], CIL[2:0] Count Into Lock, Address 0x51[2:0], and COL[2:0] Count Out-of-Lock, Address 0x51[5:3] for information on the timing.

Depending on the setting of the FSCLE bit, the Status[0] and Status[1] bits are based solely on horizontal timing information on the horizontal timing and lock status of the color subcarrier. See the FSCLE FSC Lock Enable, Address 0x51[7] section.

AUTODETECTION RESULT

AD_RESULT[2:0] Address 0x10[6:4]

The AD_RESULT[2:0] bits report back on the findings from the autodetection block. For more information on enabling the autodetection block, see the General Setup section. For information on configuring it, see the Autodetection of SD Modes section.

Table 14. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSM-MJ
001	NTSC-443
010	PAL-M
011	PAL-60
100	PAL-BGHID
101	SECAM
110	PAL-Combination N
111	SECAM 525

Table 15. STATUS 1 Function

STATUS 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (right now)
1	LOST_LOCK	Lost lock (since last read of this register)
2	FSC_LOCK	F_{SC} locked (right now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT.0	Result of autodetection
5	AD_RESULT.1	Result of autodetection
6	AD_RESULT.2	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2

STATUS_2[7:0], Address 0x12[7:0]

Table 16. STATUS 2 Function

STATUS 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Macrovision color striping
1	MVCS T3	Macrovision color striping protection. Conforms to Type 3 if high and to Type 2 if low
2	MV_PS DET	Detected Macrovision pseudo sync pulses
3	MV_AGC DET	Detected Macrovision AGC pulses
4	LL_NSTD	Line length is nonstandard
5	FSC_NSTD	F_{SC} frequency is nonstandard
6	Reserved	
7	Reserved	

STATUS 3

STATUS_3[7:0], Address 0x13[7:0]

Table 17. STATUS 3 Function

STATUS 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous).
1	GEMD	Gemstar detect.
2	SD_OP_50HZ	Flags whether 50 Hz or 60 Hz are present at output.
3		Reserved for future use.
4	FREE_RUN_ACT	Outputs a blue screen (see the DEF_VAL_AUTO_EN Default Value Automatic Enable, Address 0x0C[1] section).
5	STD_FLD_LEN	Field length is correct for currently selected video standard.
6	INTERLACED	Interlaced video detected (field sequence found).
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected.

STANDARD DEFINITION PROCESSOR (SDP)

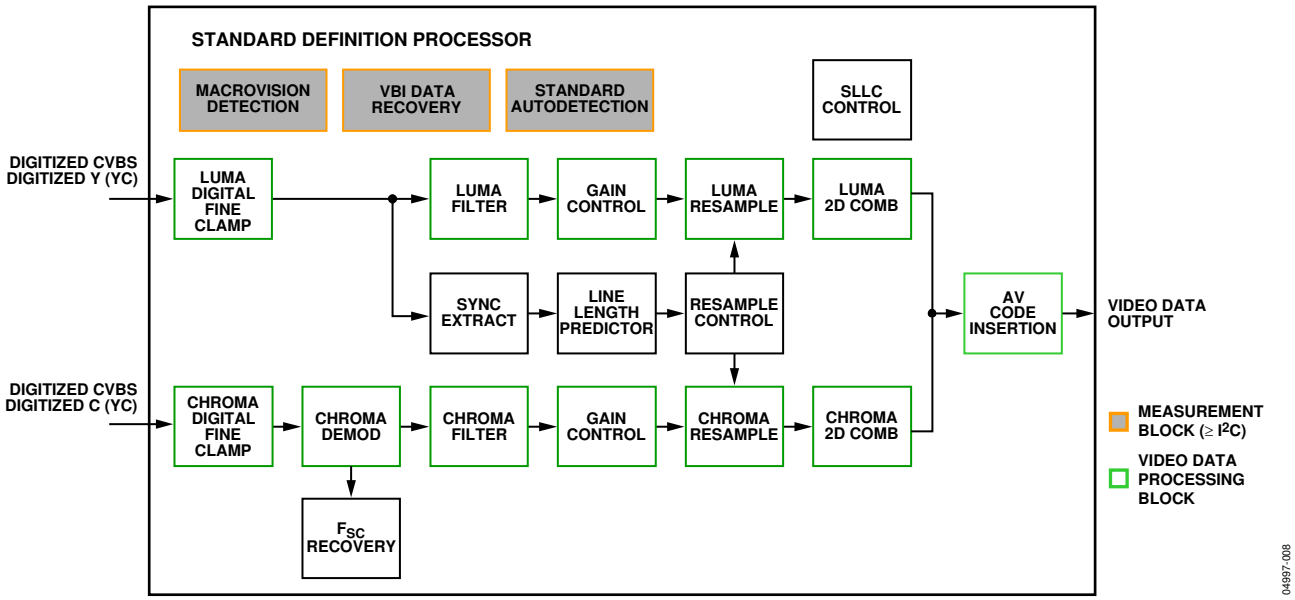

Figure 8. Block Diagram of the Standard Definition Processor

A block diagram of the ADV7183B's standard definition processor (SDP) is shown in Figure 8.

The SDP block can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and a chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

SD LUMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma Filter Block. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma Gain Control. The automatic gain control (AGC) can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma Resample. To correct for line-length errors as well as dynamic line-length changes, the data is digitally resampled.
- Luma 2D Comb. The two-dimensional comb filter provides Y/C separation.
- AV Code Insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes (as per ITU-R. BT-656) can be inserted.

SD CHROMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma Demodulation. This block uses a color subcarrier (F_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma Filter Block. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Gain Control. Automatic gain control (AGC) can operate on several different modes, including gain based on the color subcarrier's amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma Resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line-length errors of the incoming video signal.
- Chroma 2D Comb. The two-dimensional, 5-line, superadaptive comb filter provides high quality Y/C separation when the input signal is CVBS.
- AV Code Insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes (as per ITU-R. BT-656) can be inserted.

SYNC PROCESSING

The ADV7183B extracts syncs embedded in the video data stream. There is currently no support for external HS/VS inputs. The sync extraction has been optimized to support imperfect video sources such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line-length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure the ADV7183B outputs 720 active pixels per line.

The sync processing on the ADV7183B also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video.

- Vsync Processor. This block provides extra filtering of the detected Vsyncs to give improved vertical lock.
- Hsync Processor. The Hsync processor is designed to filter incoming Hsyncs that are corrupted by noise, providing much improved performance for video signals with stable time base but poor SNR.

VBI DATA RECOVERY

The ADV7183B can retrieve the following information from the input video:

- Wide-screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed caption (CC)
- Macrovision protection presence
- EDTV data
- Gemstar-compatible data slicing

The ADV7183B is also capable of automatically detecting the incoming video standard with respect to

- Color subcarrier frequency
- Field rate
- Line rate

The SPD can configure itself to support PAL-B/G/H/I/D, PAL-M/N, PAL-combination N, NTSC-M, NTSC-J, SECAM 50 Hz/60 Hz, NTSC4.43, and PAL60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits allows the user to force the digital core into a specific video standard. Under normal circumstances, this should not be necessary. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof. The following section describes the autodetection system.

Autodetection of SD Modes

To guide the autodetection system, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system picks the closest of the remaining enabled standards. The results of the autodetection can be read back via the status registers. See the Global Status Registers section for more information.

VID_SEL[3:0] Address 0x00[7:4]

Table 18. VID_SEL Function

VID_SEL	Description
0000 (default)	Autodetect (PAL BGHID) <–> NTSC J (no pedestal), SECAM
0001	Autodetect (PAL BGHID) <–> NTSC M (pedestal), SECAM
0010	Autodetect (PAL N) (pedestal) <–> NTSC J (no pedestal), SECAM
0011	Autodetect (PAL N) (pedestal) <–> NTSC M (pedestal), SECAM
0100	NTSC-J (1)
0101	NTSC-M (1)
0110	PAL60
0111	NTSC-.43 (1)
1000	PAL-B/G/H/I/D
1001	PAL-N (= PAL BGHID (with pedestal))
1010	PAL-M (without pedestal)
1011	PAL-M
1100	PAL-Combination N
1101	PAL COMBINATION N (with pedestal)
1110	SECAM
1111	SECAM (with pedestal)

AD_SEC525_EN Enable Autodetection of SECAM 525 Line Video, Address 0x07[7]

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection.

AD_SECAM_EN Enable Autodetection of SECAM, Address 0x07[6]

Setting AD_SECAM_EN to 0 disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 (default) enables the detection.

AD_N443_EN Enable Autodetection of NTSC 443, Address 0x07[5]

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection.

AD_P60_EN Enable Autodetection of PAL60, Address 0x07[4]

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection.

AD_PALN_EN Enable Autodetection of PAL N, Address 0x07[3]

Setting AD_PALN_EN to 0 disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 (default) enables the detection.

AD_PALM_EN Enable Autodetection of PAL M, Address 0x07[2]

Setting AD_PALM_EN to 0 disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 (default) enables the detection.

AD_NTSC_EN Enable Autodetection of NTSC, Address 0x07[1]

Setting AD_NTSC_EN to 0 disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 (default) enables the detection.

AD_PAL_EN Enable Autodetection of PAL, Address 0x07[0]

Setting AD_PAL_EN to 0 disables the detection of standard PAL.

Setting AD_PAL_EN to 1 (default) enables the detection.

SFL_INV Subcarrier Frequency Lock Inversion

This bit controls the behavior of the PAL switch bit in the SFL (GenLock Telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems.

First, the PAL switch bit is only meaningful in PAL. Some encoders (including ADI encoders) also look at the state of this bit in NTSC.

Second, there was a design change in ADI encoders from ADV717x to ADV719x. The older versions used the SFL (Genlock Telegram) bit directly, while the later ones invert the bit prior to using it. The reason for this is that the inversion compensated for the 1-line delay of an SFL (GenLock Telegram) transmission.

As a result, ADV717x encoders need the PAL switch bit in the SFL (Genlock Telegram) to be 1 for NTSC to work, and ADV7190/ADV7191/ADV7194 encoders need the PAL switch bit in the SFL to be 0 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

SFL_INV Address 0x41[6]

Setting SFL_INV to 0 makes the part SFL-compatible with ADV7190/ADV7191/ADV7194 encoders.

Setting SFL_INV to 1 (default), makes the part SFL-compatible with ADV717x/ADV7173x encoders.

Lock-Related Controls

Lock information is presented to the user through Bits[1:0] of the Status 1 register. See the STATUS_1[7:0] Address 0x10[7:0] section. Figure 9 outlines the signal flow and the controls available to influence the way the lock status information is generated.

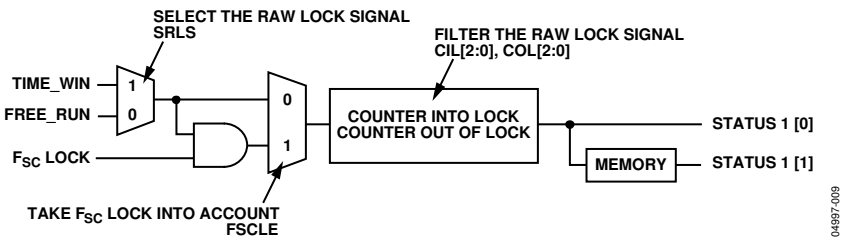

Figure 9. Lock-Related Signal Path

SRLS Select Raw Lock Signal, Address 0x51[6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register).

- The time_win signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The free_run signal evaluates the properties of the incoming video over several fields and takes vertical synchronization information into account.

Setting SRLS to 0 (default) selects the free_run signal.

Setting SRLS to 1 selects the time_win signal.

FSCLE F_{SC} Lock Enable, Address 0x51[7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in Status Register 1. This bit must be set to 0 when operating in YPrPb component mode to generate a reliable HLOCK status bit.

Setting FSCLE to 0 (default) makes the overall lock status dependent on only horizontal sync lock.

Setting FSCLE to 1 makes the overall lock status dependent on horizontal sync lock and F_{SC} lock.

VS_Coast[1:0] Address 0xF9[3:2]

These bits are used to set VS free-run (coast) frequency.

Table 19. VS_COAST[1:0] Function

VS_COAST[1:0]	Description
00 (default)	Auto coast mode—follows VS frequency from last video input
01	Forces 50 Hz coast mode
10	Forces 60 Hz coast mode
11	Reserved

CIL[2:0] Count Into Lock, Address 0x51[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state, and reports this via Status 0[1:0]. It counts the value in lines of video.

Table 20. CIL Function

CIL[2:0]	Description
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100000

COL[2:0] Count Out-of-Lock, Address 0x51[5:3]

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into unlocked state, and reports this via Status 0[1:0]. It counts the value in lines of video.

Table 21. COL Function

COL[2:0]	Description
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100000

COLOR CONTROLS

These registers allow the user to control the picture appearance, including control of the active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent from picture clamping, although both controls affect the signal's dc level.

CON[7:0] Contrast Adjust, Address 0x08[7:0]

This allows the user to adjust the contrast of the picture.

Table 22. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0] SD Saturation Cb Channel, Address 0xE3[7:0]

This register allows the user to control the gain of the Cb channel only. The user can adjust the saturation of the picture.

Table 23. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0] SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only. The user can adjust the saturation of the picture.

Table 24. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_OFF_Cb[7:0] SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for data on the Cb channel only and adjust the hue of the picture. There is a functional overlap with the Hue[7:0] register.

Table 25.SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0] SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for data on the Cr channel only and adjust the hue of the picture. There is a functional overlap with the Hue[7:0] register.

Table 26. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0] Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 27. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0IRE
0x7F	Offset of the luma channel = +100IRE
0xFF	Offset of the luma channel = −100IRE

HUE[7:0] Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 28. HUE Function

HUE[7:0]	Description
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0] Default Value Y, Address 0x0C[7:2]

If the ADV7183B loses lock on the incoming video signal or if there is no input signal, the DEF_Y[5:0] bits allow the user to specify a default luma value to be output. This value is used if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7183B lost lock to the input video signal. This is the intended mode of operation (automatic mode).
- The DEF_VAL_EN bit is set, regardless of the lock status of the video decoder. This is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the 6 MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = {DEF_Y[5:0], 0, 0}.

DEF_Y[5:0] is 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

DEF_C[7:0] Default Value C, Address 0x0D[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the 4 MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7183B cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7183B for the chroma side is Cr[7:0] = {DEF_C[7:4], 0, 0, 0, 0}, Cb[7:0] = {DEF_C[3:0], 0, 0, 0, 0}.

DEF_C[7:0] is 0x7C (blue) is the default value for Cr and Cb.