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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Multiformat SDTV Video Decoder with Fast Switch Overlay Support

# ADV7184

## FEATURES

- Multiformat video decoder supports NTSC (J/M/4.43), PAL (B/D/G/H/I/M/N), SECAM
- Integrates four 54 MHz, 10-bit ADCs
- SCART fast blank support
- Clocked from a single 28.63636 MHz crystal
- Line-locked clock-compatible (LLC)
- Adaptive Digital Line Length Tracking (ADLLT™), signal processing, and enhanced FIFO management give mini-TBC functionality
- 5-line adaptive comb filters
- Proprietary architecture for locking to weak, noisy, and unstable video sources such as VCRs and tuners
- Subcarrier frequency lock and status information output
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Macrovision® copy protection detection
- Chroma transient improvement (CTI)
- Digital noise reduction (DNR)
- Multiple programmable analog input formats
  - CVBS (composite video)
  - Y/C (S-video)
  - YPrPb (component) (VESA, MII, SMPTE, and BETACAM)
- 12 analog video input channels
- Integrated antialiasing filters
- Programmable interrupt request output pin
- Automatic NTSC/PAL/SECAM identification
- Digital output formats (8-bit or 16-bit)
  - ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- 0.5 V to 1.6 V analog signal input range
- Differential gain: 0.5% typical
- Differential phase: 0.5° typical
- Programmable video controls
  - Peak white/hue/brightness/saturation/contrast
- Integrated on-chip video timing generator
- Free-run mode (generates stable video output with no input)
- VBI decode support for close captioning (including Gemstar® 1×/2× (XDS)), WSS, CGMS, teletext, VITC, VPS
- Power-down mode
- 2-wire serial MPU interface (I²C® compatible)
- 3.3 V analog, 1.8 V digital core, 3.3 V input/output supply
- Industrial temperature grade: −40°C to +85°C
- 80-lead, Pb-free LQFP

## APPLICATIONS

- High end DVD recorders
- Video projectors
- HDD-based PVRs/DVDRs
- LCD TVs
- Set-top boxes
- Security systems
- Digital televisions
- AVR receivers

## GENERAL DESCRIPTION

The ADV7184 integrated video decoder automatically detects and converts standard analog baseband television signals compatible with worldwide NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with 16- or 8-bit CCIR 601/CCIR 656.

The advanced, highly flexible digital output interface enables performance video decoding and conversion in line-locked, clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape-based sources, broadcast sources, security and surveillance cameras, and professional systems.

The accurate 10-bit ADC provides professional quality video performance and is unmatched. This allows true 8-bit resolution in the 8-bit output mode.

The 12 analog input channels accept standard composite, S-video, and component video signals in an extensive number of combinations.

AGC and clamp-restore circuitry allow an input video signal peak-to-peak range of 0.5 V to 1.6 V. Alternatively, these can be bypassed for manual settings.

The fixed 54 MHz clocking of the ADCs and datapath for all modes allows very precise, accurate sampling and digital filtering. The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% variation in line length. The output control signals allow glueless interface connections in most applications. The ADV7184 modes are set up over a 2-wire, serial, bidirectional port (I²C compatible).

SCART and overlay functionality are enabled by the ability of the ADV7184 to process CVBS and standard definition RGB signals simultaneously. Signal mixing is controlled by the fast blank pin. The ADV7184 is fabricated in a 3.3 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. It is packaged in a small, Pb-free, 80-lead LQFP.

**Rev. A**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Application Notes**

- AN-1180: Optimizing Video Platforms for Automated Post-Production Self-Tests
- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers
- AN-850: Adaptive Digital Line Length Tracking

**Data Sheet**

- ADV7184: Multiformat SDTV Video Decoder with Fast Switch Overlay Support Data Sheet

**User Guides**

- ADV7184 Design Support Files

## REFERENCE MATERIALS

**Informational**

- Advantiv™ Advanced TV Solutions

**Technical Articles**

- Analog Video Time Base Correction and Processing for Nonstandard TV Signals
- Optimizing standard-definition video on high-definition displays

## DESIGN RESOURCES

- ADV7184 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADV7184 EngineerZone Discussions.

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**7/05—Revision 0: Initial Version**

# INTRODUCTION

The ADV7184 is a high quality, single chip, multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-video, and component video into a digital ITU-R BT.656 format.

The advanced, highly flexible digital output interface enables performance video decoding and conversion in line-locked, clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape-based sources, broadcast sources, security and surveillance cameras, and professional systems.

## ANALOG FRONT END

The ADV7184 analog front end includes four 10-bit ADCs that digitize the analog video signal before applying it to the standard definition processor (SDP). The analog front end uses differential channels for each ADC to ensure high performance in mixed-signal applications.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7184. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping within the ADV7184. The ADCs are configured to run in 4× oversampling mode.

The ADV7184 has optional antialiasing filters on each of the four input channels. The filters are designed for standard definition (SD) video with approximately 6 MHz bandwidth.

SCART and overlay functionality are enabled by the ability of the ADV7184 to process CVBS and standard definition RGB signals simultaneously. Signal mixing is controlled by the fast blank (FB) pin.

## STANDARD DEFINITION PROCESSOR (SDP)

The ADV7184 is capable of decoding a large selection of baseband video signals in composite, S-video, and component formats. The video standards that are supported include PAL B/D/I/G/H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7184 can automatically detect the video standard and process it accordingly.

The ADV7184 has a 5-line, superadaptive, 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available within the ADV7184.

The ADV7184 implements the patented ADLLT algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7184 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7184 contains a CTI processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7184 can process a variety of VBI data services, such as closed captioning (CC), wide-screen signaling (WSS), copy generation management system (CGMS), Gemstar® 1×/2×, extended data service (XDS), and teletext. The ADV7184 is fully Macrovision certified; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

## FUNCTIONAL BLOCK DIAGRAM

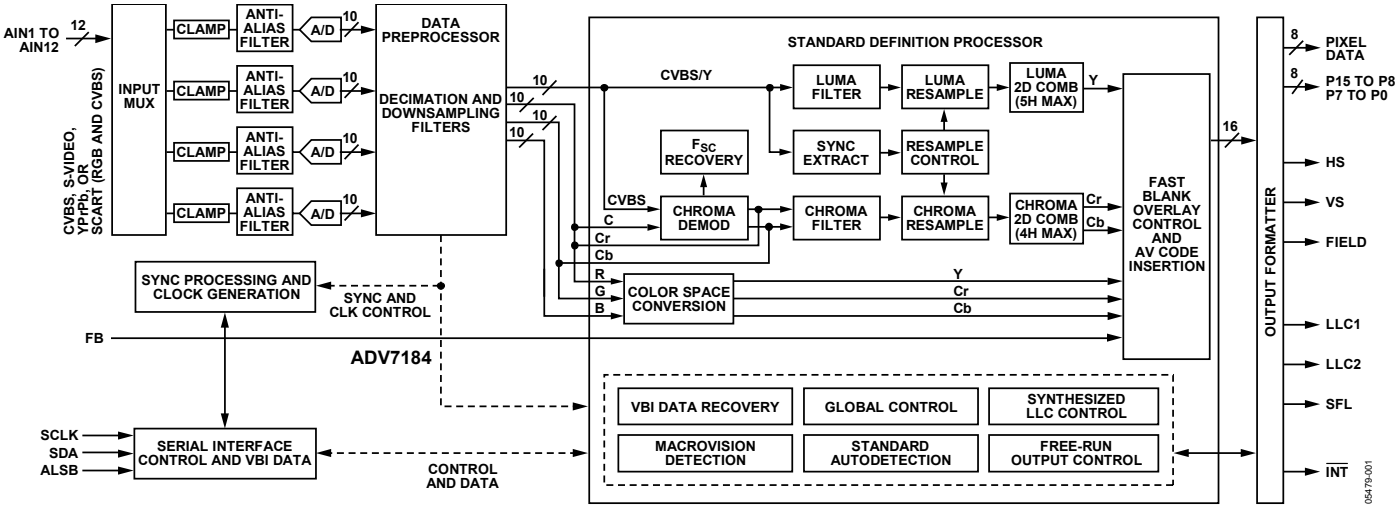


*Figure 1.*

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$A_{VDD}$ = 3.15 V to 3.45 V, $D_{VDD}$ = 1.65 V to 2.0 V, $D_{VDDIO}$ = 3.0 V to 3.6 V, $P_{VDD}$ = 1.71 V to 1.89 V, nominal input range 1.6 V. Operating temperature range, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| STATIC PERFORMANCE[1, 2, 3] | | | | | | |
| Resolution (Each ADC) | N | | | | 10 | Bits |
| Integral Nonlinearity | INL | BSL at 54 MHz | | −0.6/+0.7 | ±3 | LSB |
| Differential Nonlinearity | DNL | BSL at 54 MHz | | −0.5/+0.5 | −0.99/+2.5 | LSB |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage[4] | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage[5] | $V_{IL}$ | | | | 0.8 | V |
| Input Current[6, 7] | $I_{IN}$ | | −50 | | +50 | µA |
| | | | −10 | | +10 | µA |
| Input Capacitance[8] | $C_{IN}$ | | | | 10 | pF |
| DIGITAL OUTPUTS | | | | | | |
| Output High Voltage[9] | $V_{OH}$ | $I_{SOURCE}$ = 0.4 mA | 2.4 | | | V |
| Output Low Voltage[9] | $V_{OL}$ | $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| High Impedance Leakage Current | $I_{LEAK}$ | | | | 10 | µA |
| Output Capacitance[8] | $C_{OUT}$ | | | | 20 | pF |
| POWER REQUIREMENTS[8] | | | | | | |
| Digital Core Power Supply | $D_{VDD}$ | | 1.65 | 1.8 | 2 | V |
| Digital Input/Output Power Supply | $D_{VDDIO}$ | | 3.0 | 3.3 | 3.6 | V |
| PLL Power Supply | $P_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| Analog Power Supply | $A_{VDD}$ | | 3.15 | 3.3 | 3.45 | V |
| Digital Core Supply Current | $I_{DVDD}$ | | | 105 | | mA |
| Digital Input/Output Supply Current | $I_{DVDDIO}$ | | | 4 | | mA |
| PLL Supply Current | $I_{PVDD}$ | | | 11 | | mA |
| Analog Supply Current | $I_{AVDD}$ | CVBS input[10] | | 99 | | mA |
| | | YPrPb input[11] | | 269 | | mA |
| Power-Down Current | $I_{PWRDN}$ | | | 0.65 | | mA |
| Power-Up Time | $t_{PWRUP}$ | | | 20 | | ms |

[1] All ADC linearity tests performed with the input range at full scale − 12.5% and at zero scale + 12.5%.
[2] Maximum INL and DNL specifications obtained with the part configured for component video input.
[3] Temperature range $T_{MIN}$ to $T_{MAX}$, −40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.
[4] To obtain specified $V_{IH}$ level on Pin 29, Register 0x13 (write only) must be programmed with Value 0x04. If Register 0x13 is programmed with Value 0x00, then $V_{IH}$ on Pin 29 is 1.2 V.
[5] To obtain specified $V_{IL}$ level on Pin 29, Register 0x13 (write only) must be programmed with Value 0x04. If Register 0x13 is programmed with Value 0x00, then $V_{IL}$ on Pin 29 is 0.4 V.
[6] Pins 36 and 79.
[7] Excluding all TEST pins (TEST0 to TEST12)
[8] $V_{OH}$ and $V_{OL}$ levels obtained using default drive strength value (0xD5) in Register 0xF4.
[9] Guaranteed by characterization.
[10] Only ADC0 is powered on.
[11] All four ADCs powered on.

## VIDEO SPECIFICATIONS

At $A_{VDD}$ = 3.15 V to 3.45 V, $D_{VDD}$ = 1.65 V to 2.0 V, $D_{VDDIO}$ = 3.0 V to 3.6 V, $P_{VDD}$ = 1.71 V to 1.89 V (operating temperature range, unless otherwise noted).

**Table 2.**

| Parameter[1, 2] | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| NONLINEAR SPECIFICATIONS | | | | | | |
| Differential Phase | DP | CVBS input, modulate five steps | | 0.5 | 0.7 | Degree |
| Differential Gain | DG | CVBS input, modulate five steps | | 0.5 | 0.7 | % |
| Luma Nonlinearity | LNL | CVBS input, five steps | | 0.5 | 0.7 | % |
| NOISE SPECIFICATIONS | | | | | | |
| SNR Unweighted | | Luma ramp | 54 | 56 | | dB |
| | | Luma flat field | 56 | 58 | | dB |
| Analog Front End Crosstalk | | | | 60 | | dB |
| LOCK TIME SPECIFICATIONS | | | | | | |
| Horizontal Lock Range | | | −5 | | +5 | % |
| Vertical Lock Range | | | 40 | | 70 | Hz |
| $F_{SC}$ Subcarrier Lock Range | | | | ±1.3 | | Hz |
| Color Lock-In Time | | | | 60 | | Lines |
| Sync Depth Range[3] | | | 20 | | 200 | % |
| Color Burst Range | | | 5 | | 200 | % |
| Vertical Lock Time | | | | 2 | | Fields |
| Autodetection Switch Speed | | | | 100 | | Lines |
| CHROMA SPECIFICATIONS | | | | | | |
| Hue Accuracy | HUE | | | 1 | | Degree |
| Color Saturation Accuracy | CL_AC | | | 1 | | % |
| Color AGC Range | | | 5 | | 400 | % |
| Chroma Amplitude Error | | | | 0.5 | | % |
| Chroma Phase Error | | | | 0.4 | | Degree |
| Chroma Luma Intermodulation | | | | 0.2 | | % |
| LUMA SPECIFICATIONS | | | | | | |
| Luma Brightness Accuracy | | CVBS, 1 V input | | 1 | | % |
| Luma Contrast Accuracy | | CVBS, 1 V input | | 1 | | % |

[1] Temperature range $T_{MIN}$ to $T_{MAX}$ is −40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.
[3] Nominal sync depth is 300 mV at 100% sync depth range.

## ANALOG SPECIFICATIONS

At $A_{VDD}$ = 3.15 V to 3.45 V, $D_{VDD}$ = 1.65 V to 2.0 V, $D_{VDDIO}$ = 3.0 V to 3.6 V, $P_{VDD}$ = 1.71 V to 1.89 V (operating temperature range, unless otherwise noted). Recommended analog input video signal range is 0.5 V to 1.6 V, typically 1 V p-p.

**Table 3.**

| Parameter[1, 2] | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLAMP CIRCUITRY | | | | | | |
| External Clamp Capacitor | | | | 0.1 | | µF |
| Input Impedance[3] | | Clamps switched off | | 10 | | MΩ |
| Input Impedance of Pin 40 (FB) | | | | 20 | | kΩ |
| Large-Clamp Source Current | | | | 0.75 | | mA |
| Large-Clamp Sink Current | | | | 0.75 | | mA |
| Fine-Clamp Source Current | | | | 17 | | µA |
| Fine-Clamp Sink Current | | | | 17 | | µA |

[1] Temperature range $T_{MIN}$ to $T_{MAX}$ is −40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.
[3] Except Pin 40 (FB).

## THERMAL SPECIFICATIONS

**Table 4.**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Junction-to-Case Thermal Resistance | $\theta_{JC}$ | 4-layer PCB with solid ground plane | | 7.6 | | °C/W |
| Junction-to-Ambient Thermal Resistance (Still Air) | $\theta_{JA}$ | 4-layer PCB with solid ground plane | | 38.1 | | °C/W |

## TIMING SPECIFICATIONS

$A_{VDD}$ = 3.15 V to 3.45 V, $D_{VDD}$ = 1.65 V to 2.0 V, $D_{VDDIO}$ = 3.0 V to 3.6 V, $P_{VDD}$ = 1.71 V to 1.89 V (operating temperature range, unless otherwise noted).

**Table 5.**

| Parameter[1, 2] | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SYSTEM CLOCK AND CRYSTAL | | | | | | |
| Nominal Frequency | | | | 28.63636 | | MHz |
| Frequency Stability | | | | | ±50 | ppm |
| I²C PORT[3] | | | | | | |
| SCLK Frequency | | | | | 400 | kHz |
| SCLK Minimum Pulse Width High | $t_1$ | | 0.6 | | | µs |
| SCLK Minimum Pulse Width Low | $t_2$ | | 1.3 | | | µs |
| Hold Time (Start Condition) | $t_3$ | | 0.6 | | | µs |
| Setup Time (Start Condition) | $t_4$ | | 0.6 | | | µs |
| SDA Setup Time | $t_5$ | | 100 | | | ns |
| SCLK and SDA Rise Time | $t_6$ | | | | 300 | ns |
| SCLK and SDA Fall Time | $t_7$ | | | | 300 | ns |
| Setup Time for Stop Condition | $t_8$ | | | 0.6 | | µs |
| RESET FEATURE | | | | | | |
| Reset Pulse Width | | | 5 | | | ms |
| CLOCK OUTPUTS | | | | | | |
| LLC1 Mark-Space Ratio | $t_9$:$t_{10}$ | | 45:55 | | 55:45 | % duty cycle |
| LLC1 Rising to LLC2 Rising | $t_{11}$ | | | 1 | | ns |
| LLC1 Rising to LLC2 Falling | $t_{12}$ | | | 1 | | ns |
| DATA AND CONTROL OUTPUTS | | | | | | |
| Data Output Transitional Time[4] | $t_{13}$ | Negative clock edge to start of valid data ($t_{ACCESS} = t_{10} - t_{13}$) | | | 3.6 | ns |
| Data Output Transitional Time[4] | $t_{14}$ | End of valid data to negative clock edge ($t_{HOLD} = t_9 + t_{14}$) | | | 2.4 | ns |
| Propagation Delay to High-Z | $t_{15}$ | | | 6 | | ns |
| Max Output Enable Access Time | $t_{16}$ | | | 7 | | ns |
| Min Output Enable Access Time | $t_{17}$ | | | 4 | | ns |

[1] Temperature range $T_{MIN}$ to $T_{MAX}$ is −40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.
[3] TTL input values are 0 V to 3 V, with rise/fall times of ≤3 ns, measured between the 10% and 90% points.
[4] SDP timing figures obtained using default drive strength value (0xD5) in Register 0xF4.

## TIMING DIAGRAMS

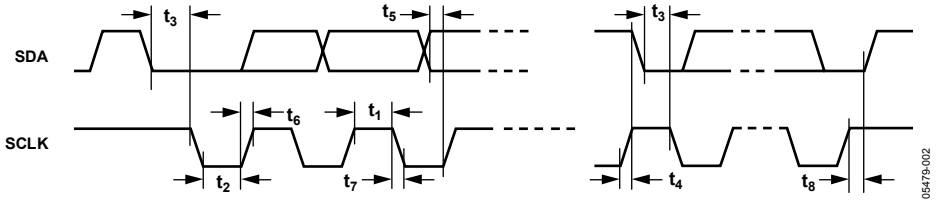


*Figure 2. I²C Timing*

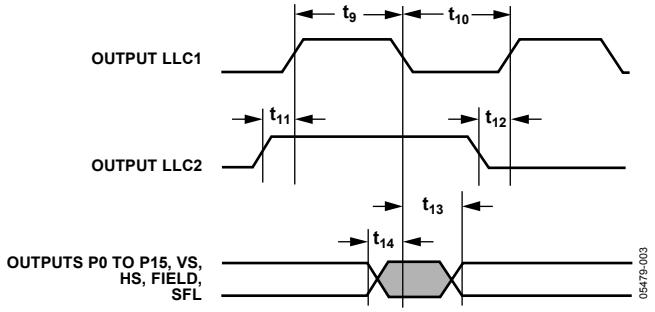


*Figure 3. Pixel Port and Control Output Timing*

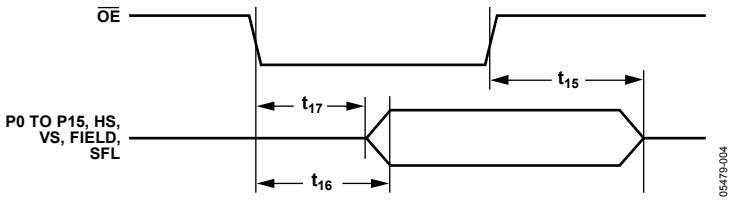


*Figure 4. $\overline{OE}$ Timing*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| $A_{VDD}$ to AGND | 4 V |
| $D_{VDD}$ to DGND | 2.2 V |
| $P_{VDD}$ to AGND | 2.2 V |
| $D_{VDDIO}$ to DGND | 4 V |
| $D_{VDDIO}$ to $A_{VDD}$ | −0.3 V to +0.3 V |
| $P_{VDD}$ to $D_{VDD}$ | −0.3 V to +0.3 V |
| $D_{VDDIO}$ to $P_{VDD}$ | −0.3 V to +2 V |
| $D_{VDDIO}$ to $D_{VDD}$ | −0.3 V to +2 V |
| $A_{VDD}$ to $P_{VDD}$ | −0.3 V to +2 V |
| $A_{VDD}$ to $D_{VDD}$ | −0.3 V to +2 V |
| Digital Inputs Voltage to DGND | −0.3 V to $D_{VDDIO}$ + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to $D_{VDDIO}$ + 0.3 V |
| Analog Inputs to AGND | AGND − 0.3 V to $A_{VDD}$ + 0.3 V |
| Maximum Junction Temperature ($T_{J\,max}$) | 125°C |
| Storage Temperature Range | −65°C to +150°C |
| Infrared Reflow Soldering (20 sec) | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL PERFORMANCE

To reduce power consumption the user is advised to turn off any unused ADCs when using the part.

The junction temperature must always stay below the maximum junction temperature ($T_J$ max) of 125°C. Use the following equation to calculate the junction temperature:

$$T_J = T_{A\,max} + (\theta_{JA} \times W_{max})$$

where:
$T_{A\,max}$ = 85°C.
$\theta_{JA}$ = 30°C/W.
$W_{max} = ((A_{VDD} \times I_{AVDD}) + (D_{VDD} \times I_{DVDD}) + (D_{VDDIO} \times I_{DVDDIO}) + (P_{VDD} \times I_{PVDD}))$.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

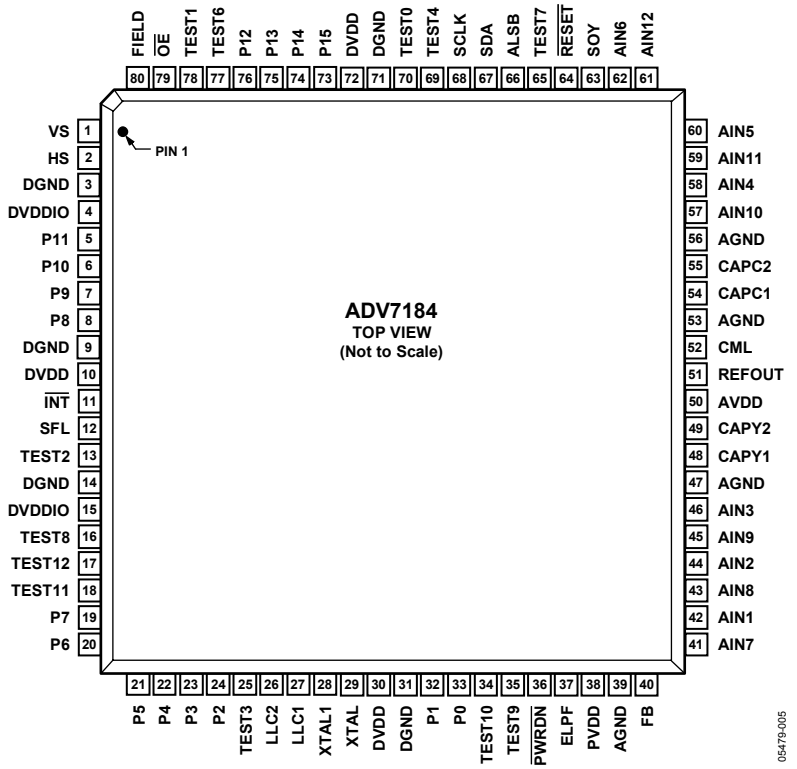


*Figure 5. 80-Lead LQFP Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 3, 9, 14, 31, 71 | DGND | G | Digital Ground. |
| 39, 47, 53, 56 | AGND | G | Analog Ground. |
| 4, 15 | DVDDIO | P | Digital I/O Supply Voltage (3.3 V). |
| 10, 30, 72 | DVDD | P | Digital Core Supply Voltage (1.8 V). |
| 50 | AVDD | P | Analog Supply Voltage (3.3 V). |
| 38 | PVDD | P | PLL Supply Voltage (1.8 V). |
| 42, 44, 46, 58, 60, 62, 41, 43, 45, 57, 59, 61 | AIN1 to AIN12 | I | Analog Video Input Channels. |
| 11 | $\overline{\text{INT}}$ | O | Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video. See the User Sub Map register details in Table 107. |
| 40 | FB | I | Fast Blank. FB is a fast switch overlay input that switches between CVBS and RGB analog input signals. |
| 70, 78, 13, 25, 69, 35, 34, 18, 17 | TEST0 to TEST4, TEST9 to TEST12 | | Leave these pins unconnected. |
| 77, 65 | TEST6, TEST7 | | Tie to AGND. |
| 16 | TEST8 | | Tie to DVDDIO. |
| 33, 32, 24 to 19, 8 to 5, 76 to 73 | P0 to P15 | O | Video Pixel Output Ports. |
| 2 | HS | O | Horizontal Synchronization Output Signal. |
| 1 | VS | O | Vertical Synchronization Output Signal. |
| 80 | FIELD | O | Field Synchronization Output Signal. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 67 | SDA | I/O | $I^2C$ Port Serial Data Input/Output. |
| 68 | SCLK | I | $I^2C$ Port Serial Clock Input. Maximum clock rate of 400 kHz. |
| 66 | ALSB | I | This pin selects the $I^2C$ address for the ADV7184. ALSB set to Logic 0 sets the address for a write to 0x40; set to Logic 1 sets the address to 0x42. |
| 64 | $\overline{\text{RESET}}$ | I | System Reset Input (active low). A minimum low reset pulse width of 5 ms is required to reset the ADV7184 circuitry. |
| 27 | LLC1 | O | Line-Locked Clock 1. This is a line-locked output clock for the pixel data output by the ADV7184. Nominally 27 MHz, but varies according to video line length. |
| 26 | LLC2 | O | Line-Locked Clock 2. This is a divide-by-2 version of the LLC1 output clock for the pixel data output by the ADV7184. Nominally 13.5 MHz, but varies according to video line length. |
| 29 | XTAL | I | Crystal Input. This is the input pin for the 28.63636 MHz crystal, or it can be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal. |
| 28 | XTAL1 | O | This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the ADV7184. In crystal mode, the crystal must be a fundamental crystal. |
| 36 | $\overline{\text{PWRDN}}$ | I | Logic 0 on this pin places the ADV7184 in a power-down mode. Refer to the $I^2C$ Register Maps section for more options on power-down modes for the ADV7184. |
| 79 | $\overline{\text{OE}}$ | I | When set to Logic 0, $\overline{\text{OE}}$ enables the pixel output bus, P15 to P0 of the ADV7184. Logic 1 on the $\overline{\text{OE}}$ pin places P15 to P0, HS, VS, and SFL into a high impedance state. |
| 37 | ELPF | I | The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 52. |
| 12 | SFL | O | Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc., digital video encoder. |
| 63 | SOY | I | SYNC on Y. This input pin should only be used with the standard detection and identification function (see the Standard Detection and Identification section). This pin should be connected to the Y signal of a component input for standard identification function. |
| 51 | REFOUT | O | Internal Voltage Reference Output. Refer to Figure 52 for a recommended capacitor network for this pin. |
| 52 | CML | O | Common-Mode Level. The CML pin is a common-mode level for the internal ADCs. Refer to Figure 52 for a recommended capacitor network for this pin. |
| 48, 49 | CAPY1, CAPY2 | I | ADC Capacitor Network. Refer to Figure 52 for a recommended capacitor network for this pin. |
| 54, 55 | CAPC1, CAPC2 | I | ADC Capacitor Network. Refer to Figure 52 for a recommended capacitor network for this pin. |

# ANALOG FRONT END

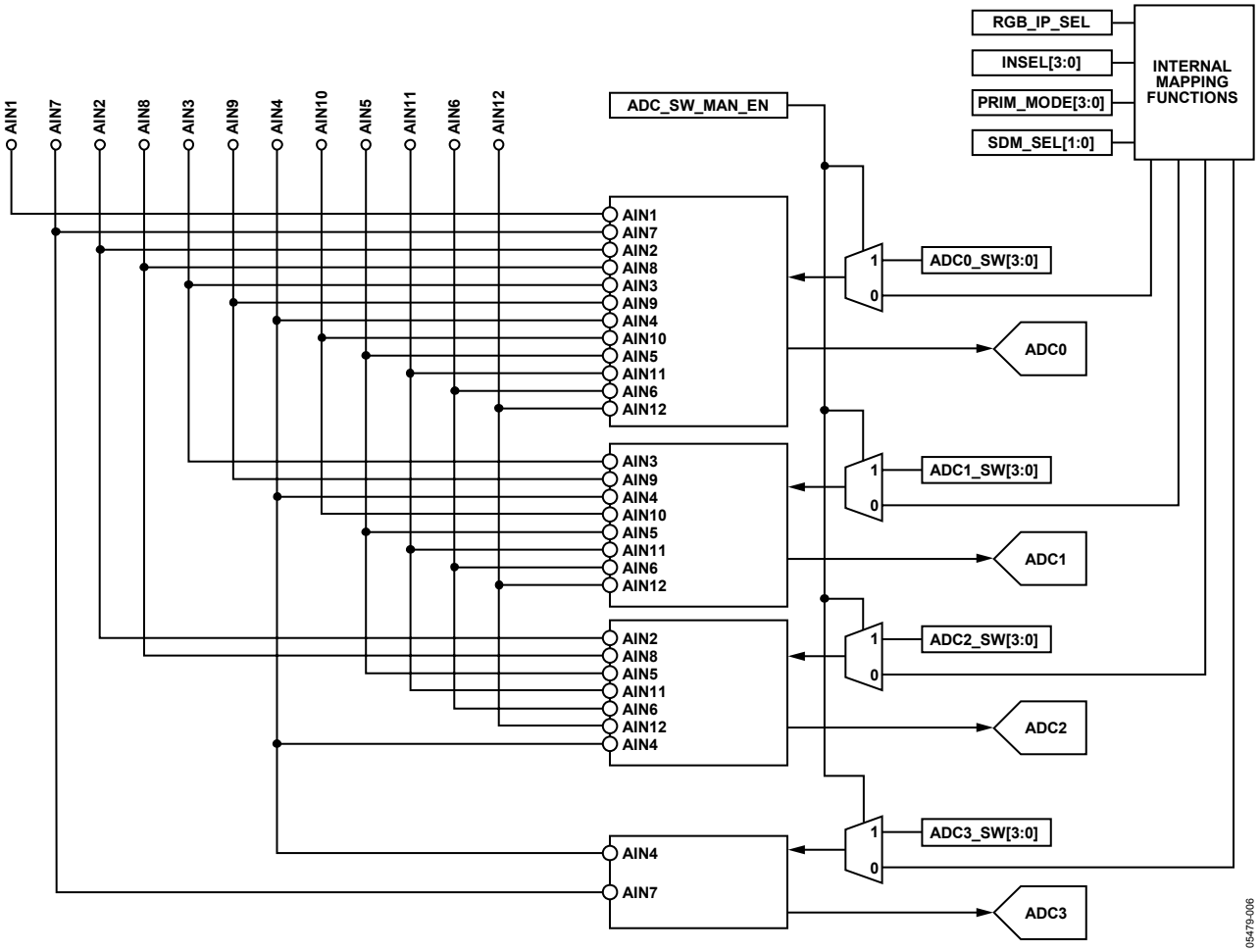


*Figure 6. Internal Pin Connections*

## ANALOG INPUT MUXING

The ADV7184 has an integrated analog muxing section that allows connecting more than one source of video signal to the decoder. Figure 6 outlines the overall structure of the input muxing provided in the ADV7184.

As can be seen in Figure 6, the analog input muxes can be controlled in two ways:

- By the functional register (INSEL). Using INSEL [3:0] simplifies the setup of the muxes and minimizes crosstalk between channels by preassigning the input channels. This is referred to as the recommended input muxing.
- By an I²C manual override (ADC_SW_MAN_EN, ADC0_SW, ADC1_SW, ADC2_SW, and ADC3_SW). This is provided for applications with special requirements, such as number/combinations of signals that are not served by the preassigned input connections. This is referred to as manual input muxing.

Figure 7 shows an overview of the two methods of controlling input muxing.

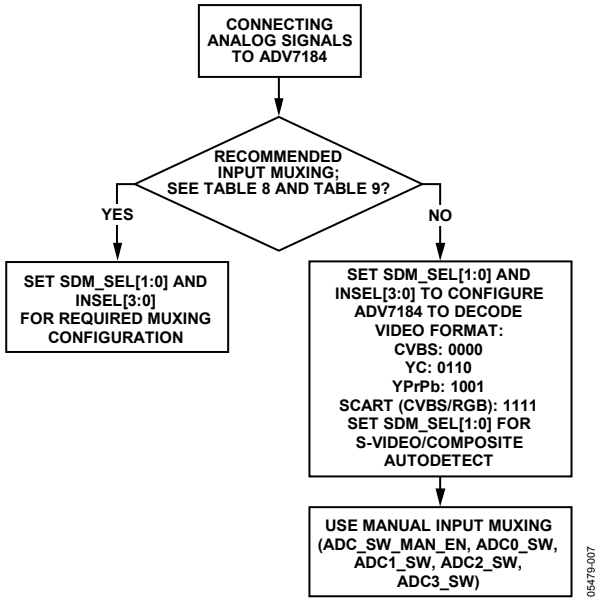


*Figure 7. Input Muxing Overview*

### *Recommended Input Muxing*

A maximum of 12 CVBS inputs can be connected and decoded by the ADV7184, meaning that the sources must be connected to adjacent pins on the IC, as seen in Figure 5. This calls for a careful design of the PCB layout, for example, placing ground shielding between all signals routed through tracks that are physically close together.

### *SDM_SEL [1:0], Y/C and CVBS Autodetect Mode Select, Address 0x69 [1:0]*

The SDM_SEL bits decide on input routing and whether INSEL [3:0] is used to govern input routing decisions.

The S-video/composite autodetection feature is enabled using SDM_SEL = 11.

**Table 8. SDM_SEL [1:0]**

| SDM_SEL [1:0] | Mode | Analog Video Inputs |
|---|---|---|
| 00 | As per INSEL [3:0] | As per INSEL [3:0] |
| 01 | CVBS | AIN11 |
| 10 | Y/C | Y = AIN10<br>C = AIN12 |
| 11 | S-video/composite autodetection | CVBS = AIN11<br>Y = AIN11<br>C = AIN12 |

### *INSEL [3:0], Input Selection, Address 0x00 [3:0]*

The INSEL bits allow the user to select the input channel and format. Depending on the PCB connections, only a subset of the INSEL modes is valid. INSEL [3:0] not only switches the analog input muxing, but also configures ADV7184 to process composite (CVBS), S-video (Y/C), or component (YPbPr/RGB) format signals.

The recommended input muxing is designed to minimize crosstalk between signal channels and to obtain the highest level of signal integrity. Table 10 summarizes how the PCB layout should connect analog video signals to the ADV7184.

It is strongly recommended that users connect any unused analog input pins to AGND to act as a shield.

Connect the AIN7 to AIN11 inputs to AGND when only six input channels are used. This improves the quality of the sampling due to better isolation between the channels.

AIN12 is not controlled by INSEL [3:0]. It can be routed to ADC0/ADC1/ADC2 only by manual muxing. See Table 11 for details.

**Table 9. Input Channel Switching Using INSEL [3:0]**

| INSEL [3:0] | Description | |
|---|---|---|
| | **Analog Input Pins** | **Video Format** |
| 0000 (default) | CVBS1 = AIN1<br>B = AIN4 or AIN7[1]<br>R = AIN5 or AIN8[1]<br>G = AIN6 or AIN9[1] | SCART (CVBS and R, G, B) |
| 0001 | CVBS2 = AIN2<br>B = AIN4 or AIN7[1]<br>R = AIN5 or AIN8[1]<br>G = AIN6 or AIN9[1] | SCART (CVBS and R, G, B) |
| 0010 | CVBS3 = AIN3<br>B = AIN4 or AIN7[1]<br>R = AIN5 or AIN8[1]<br>G = AIN6 or AIN9[1] | SCART (CVBS and R, G, B) |
| 0011 | CVBS4 = AIN4<br>B = AIN7<br>R = AIN8<br>G = AIN9 | SCART (CVBS and R, G, B) |
| 0100 | CVBS1 = AIN5<br>B = AIN7<br>R = AIN8<br>G = AIN9 | SCART (CVBS and R, G, B) |
| 0101 | CVBS1 = AIN6<br>B = AIN7<br>R = AIN8<br>G = AIN9 | SCART (CVBS and R, G, B) |
| 0110 | Y1 = AIN1<br>C1 = AIN4 | Y/C |
| 0111 | Y2 = AIN2<br>C2 = AIN5 | Y/C |
| 1000 | Y3 = AIN3<br>C3 = AIN6 | Y/C |
| 1001 | Y1 = AIN1<br>PB1 = AIN4<br>PR1 = AIN5 | YPrPb |
| 1010 | Y2 = AIN2<br>PB2 = AIN3<br>PR2 = AIN6 | YPrPb |
| 1011 | CVBS7 = AIN7<br>B = AIN4<br>R = AIN5<br>G = AIN6 | SCART (CVBS and R, G, B) |
| 1100 | CVBS8 = AIN8<br>B = AIN4<br>R = AIN5<br>G = AIN6 | SCART (CVBS and R, G, B) |
| 1101 | CVBS9 = AIN9<br>B = AIN4<br>R = AIN5<br>G = AIN6 | SCART (CVBS and R, G, B) |
| 1110 | CVBS10 = AIN10<br>B = AIN4 or AIN7[1]<br>R = AIN5 or AIN8[1]<br>G = AIN6 or AIN9[1] | SCART (CVBS and R, G, B) |
| 1111 | CVBS11 = AIN11<br>B = AIN4 or AIN7[1]<br>R = AIN5 or AIN8[1]<br>G = AIN6 or AIN9[1] | SCART (CVBS and R, G, B) |

[1] Selectable via RGB_IP_SEL.

**Table 10. Input Channel Assignments**

| Input Channel | Pin No. | Recommended Input Muxing Control—INSEL [3:0] | | | |
|---|---|---|---|---|---|
| AIN7 | 41 | CVBS7 | | | SCART1-B |
| AIN1 | 42 | CVBS1 | YC1-Y | YPrPb1-Y | SCART2-CVBS |
| AIN8 | 43 | CVBS8 | | | SCART1-R |
| AIN2 | 44 | CVBS2 | YC2-Y | YPrPb2-Y | |
| AIN9 | 45 | CVBS9 | | | SCART1-G |
| AIN3 | 46 | CVBS3 | YC3-Y | YPrPb2-Pb | |
| AIN10 | 57 | CVBS10 | | | |
| AIN4 | 58 | CVBS4 | YC1-C | YPrPb1-Pb | SCART2-B |
| AIN11 | 59 | CVBS11 | | | SCART1-CVBS |
| AIN5 | 60 | CVBS5 | YC2-C | YPrPb1-Pr | SCART2-R |
| AIN12 | 61 | Not available | | | |
| AIN6 | 62 | CVBS6 | YC3-C | YPrPb2-Pr | SCART2-G |

**Table 11. Manual Mux Settings for All ADCs (Set ADC_SW_MAN_EN to 1)**

| ADC0_SW [3:0] | ADC0 Connected To | ADC1_SW [3:0] | ADC1 Connected To | ADC2_SW [3:0] | ADC2 Connected To | ADC3_SW [3:0] | ADC3 Connected To |
|---|---|---|---|---|---|---|---|
| 0000 | No connection | 0000 | No connection | 0000 | No connection | 0000 | No connection |
| 0001 | AIN1 | 0001 | No connection | 0001 | No connection | 0001 | No connection |
| 0010 | AIN2 | 0010 | No connection | 0010 | AIN2 | 0010 | No connection |
| 0011 | AIN3 | 0011 | AIN3 | 0011 | No connection | 0011 | No connection |
| 0100 | AIN4 | 0100 | AIN4 | 0100 | No connection | 0100 | AIN4 |
| 0101 | AIN5 | 0101 | AIN5 | 0101 | AIN5 | 0101 | No connection |
| 0110 | AIN6 | 0110 | AIN6 | 0110 | AIN6 | 0110 | No connection |
| 0111 | No connection | 0111 | No connection | 0111 | No connection | 0111 | No connection |
| 1000 | No connection | 1000 | No connection | 1000 | No connection | 1000 | No connection |
| 1001 | AIN7 | 1001 | No connection | 1001 | No connection | 1001 | AIN7 |
| 1010 | AIN8 | 1010 | No connection | 1010 | AIN8 | 1010 | No connection |
| 1011 | AIN9 | 1011 | AIN9 | 1011 | No connection | 1011 | No connection |
| 1100 | AIN10 | 1100 | AIN10 | 1100 | No connection | 1100 | No connection |
| 1101 | AIN11 | 1101 | AIN11 | 1101 | AIN11 | 1101 | No connection |
| 1110 | AIN12 | 1110 | AIN12 | 1110 | AIN12 | 1110 | No connection |
| 1111 | No connection | 1111 | No connection | 1111 | No connection | 1111 | No connection |

### *RGB_IP_SEL, Address 0xF1 [0]*

For SCART input, R, G, and B signals can be input either on AIN4, AIN5, and AIN6 or on AIN7, AIN8, and AIN9.

0 (default)—B is input on AIN4, R is input on AIN5, and G is input on AIN6.

1—B is input on AIN7, R is input on AIN8, and G is input on AIN9.

## MANUAL INPUT MUXING

By accessing a set of manual override muxing registers, the analog input muxes of the ADV7184 can be controlled directly. This is referred to as manual input muxing. Manual input muxing overrides other input muxing control bits, including INSEL.

Manual muxing is activated by setting the ADC_SW_MAN_EN bit. It only affects the analog switches in front of the ADCs. Therefore, if the settings of INSEL and the manual input muxing bits (ADC0_SW/ADC1_SW/ADC2_SW/ADC3_SW) contradict each other, the ADC0_SW/ADC1_SW/ADC2_SW/ADC3_SW settings apply and INSEL is ignored.

Manual input muxing controls only the analog input muxes. For the follow-on blocks to process video data in the correct format, however, INSEL must still be used to indicate whether the input signal is of YPbPr, Y/C, or CVBS format.

Restrictions in the channel routing are imposed by the analog signal routing inside the IC; each input pin cannot be routed to each ADC. Refer to Figure 6 for an overview on the routing capabilities inside the chip. The four mux sections can be controlled by the reserved control signal buses, ADC0_SW [3:0], ADC1_SW [3:0], ADC2_SW [3:0], and ADC3_SW [3:0]. Table 11 explains the control words used.

***ADC_SW_MAN_EN, Manual Input Muxing Enable, Address 0xC4 [7]***

***ADC0_SW [3:0], ADC0 Mux Configuration, Address 0xC3 [3:0]***

***ADC1_SW [3:0], ADC1 Mux Configuration, Address 0xC3 [7:4]***

***ADC2_SW [3:0], ADC2 Mux Configuration, Address 0xC4 [3:0]***

***ADC3_SW [3:0], ADC3 Mux Configuration, Address 0xF3 [7:4]***

See Table 11.

## XTAL CLOCK INPUT PIN FUNCTIONALITY

### *XTAL_TTL_SEL, Address 0x13 [2]*

The crystal pad is normally part of the crystal oscillator circuit, powered from a 1.8 V supply. For optimal clock generation, the slice level of the input buffer of this circuit is at approximately half the supply voltage, making it incompatible with TLL level signals.

0 (default)—A crystal is used to generate the ADV7184 clock.

1—An external TTL level clock is supplied. A different input buffer can be selected that slices at TTL-compatible levels. This inhibits operation of the crystal oscillator and therefore can only be used when a clock signal is applied.

## 28.63636 MHz CRYSTAL OPERATION

### *EN28XTAL, Address 0x1D [6]*

The ADV7184 can operate on two different base crystal frequencies. Selecting one over the other may be desirable in systems in which board crosstalk between different components leads to undesirable interference between video signals. It is recommended to use a crystal of frequency 28.63636 MHz to clock the ADV7184.

0 (default)—The crystal frequency is 27 MHz.

1—The crystal frequency is 28.63636 MHz.

## ANTIALIASING FILTERS

The ADV7184 has optional antialiasing filters on each of the four input channels. The filters are designed for SD video with approximately 6 MHz bandwidth.

A plot of the filter response is shown in Figure 8. The filters can be individually enabled via I²C under the control of AA_FILT_EN [3:0].

### *AA_FILT_EN [0], Address 0xF3 [0]*

0 (default)—The filter on Channel 0 is disabled.

1—The filter on Channel 0 is enabled.

### *AA_FILT_EN [1], Address 0xF3 [1]*

0 (default)—The filter on Channel 1 is disabled.

1—The filter on Channel 1 is enabled.

### *AA_FILT_EN [2], Address 0xF3 [2]*

0 (default)—The filter on Channel 2 is disabled.

1—The filter on Channel 2 is enabled.

### *AA_FILT_EN [3], Address 0xF3 [3]*

0 (default)—The filter on Channel 3 is disabled.

1—The filter on Channel 3 is enabled.

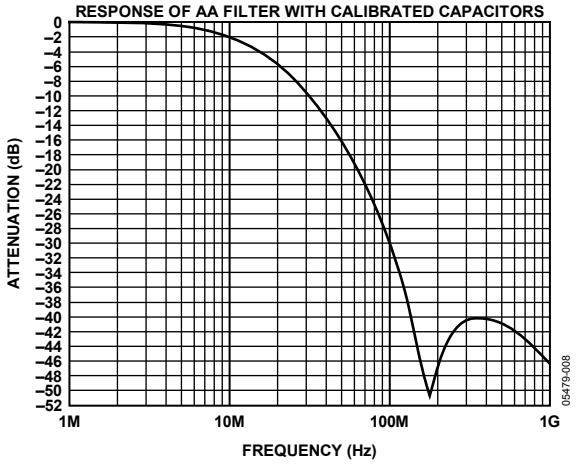


*Figure 8. Frequency Response of Internal ADV7184 Antialiasing Filters*

## SCART AND FAST BLANKING

The ADV7184 can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality.

This function is available when INSEL [3:0] is set appropriately (see Table 9). Timing extraction is always performed by the ADV7184 on the CVBS signal. However, a combination of the CVBS and RGB inputs can be mixed and output under the control of the I²C registers and the FB pin.

Four basic modes are supported:

- Static Switch Mode. The FB pin is not used. The timing is extracted from the CVBS signal, and either the CVBS content or RGB content can be output under the control of CVBS_RGB_SEL. This mode allows the selection of a full-screen picture from either source. Overlay is not possible in static switch mode.
- Fixed Alpha Blending. The FB pin is not used. The timing is extracted from the CVBS signal, and an alpha blended combination of the video from the CVBS and RGB sources is output. This alpha blending is applied to the full screen.

The alpha blend factor is selected with the I²C signal MAN_ALPHA_VAL [6:0]**.** Overlay is not possible in fixed alpha blending mode.

- Dynamic Switching (Fast Mux). The FB pin can be used to select the source. This enables dynamic multiplexing between the CVBS and RGB sources. With default settings, when Logic 1 is applied to the FB pin, the RGB source is selected; when Logic 0 is applied to the FB pin, the CVBS source is selected. This mode is suitable for the overlay of subtitles, teletext, or other material. Typically, the CVBS source carries the main picture, and the RGB source has the overlay data.

- Dynamic Switching with Edge Enhancement**.** This provides the same functionality as the dynamic switching mode, but with the benefit of Analog Devices proprietary edge-enhancement algorithms, which improve the visual appearance of transitions for signals from a wide variety of sources.

### *System Diagram*

A block diagram of the ADV7184 fast blanking configuration is shown in Figure 9.

The CVBS signal is processed by the ADV7184 and converted to YPrPb. The RGB signals are processed by a color space converter (CSC), and samples are converted to YPrPb. Both sets of YPrPb signals are input to the subpixel blender, which can be configured to operate in any of the four modes previously outlined in this section.

The fast blank position resolver determines the time position of the FB pin accurately (<1 ns). This position information is then used by the subpixel blender in dynamic switching modes, enabling the ADV7184 to implement high performance multiplexing between the CVBS and RGB sources even when the RGB data source is completely asynchronous to the sampling crystal reference.

An antialiasing filter is required on all four data channels (R, G, B, and CVBS). The order of this filter is reduced because all signals are sampled at 54 MHz.

The switched or blended data is output from the ADV7184 in the standard output formats (see Table 102).

## FAST BLANK CONTROL

### *FB_MODE [1:0], Address 0xED [1:0]*

FB_MODE controls which fast blank mode is selected.

**Table 12. FB_MODE [1:0] Function**

| FB_MODE [1:0] | Description |
|---|---|
| 00 (default) | Static switch mode |
| 01 | Fixed alpha blending |
| 10 | Dynamic switching (fast mux) |
| 11 | Dynamic switching with edge enhancement |

### *Static Mux Selection Control*

**CVBS_RGB_SEL, Address 0xED [2]**

CVBS_RGB_SEL controls whether the video from the CVBS or RGB source is selected for output from the ADV7184.

0 (default)—Data from the CVBS source is selected for output.

1—Data from the RGB source is selected for output.

### *Alpha Blend Coefficient*

**MAN_ALPHA_VAL [6:0], Address 0xEE [6:0]**

When fixed alpha blending is selected (FB_MODE [1:0] = 01), MAN_ALPHA_VAL [6:0] determines the proportion in which the video from the CVBS and RGB sources are blended. Equation 1 shows how these bits affect the video output.

$$Video_{out} = Video_{CVBS} \times \left(1 - \frac{MAN\_ALPHA\_VAL\,[6:0]}{64}\right) + Video_{RGB} \times \frac{MAN\_ALPHA\_VAL\,[6:0]}{64} \quad (1)$$

The maximum valid value for MAN_ALPHA_VAL [6:0] is 1000000, such that the alpha blender coefficients remain between 0 and 1. The default value for MAN_ALPHA_VAL [6:0] is 0000000.

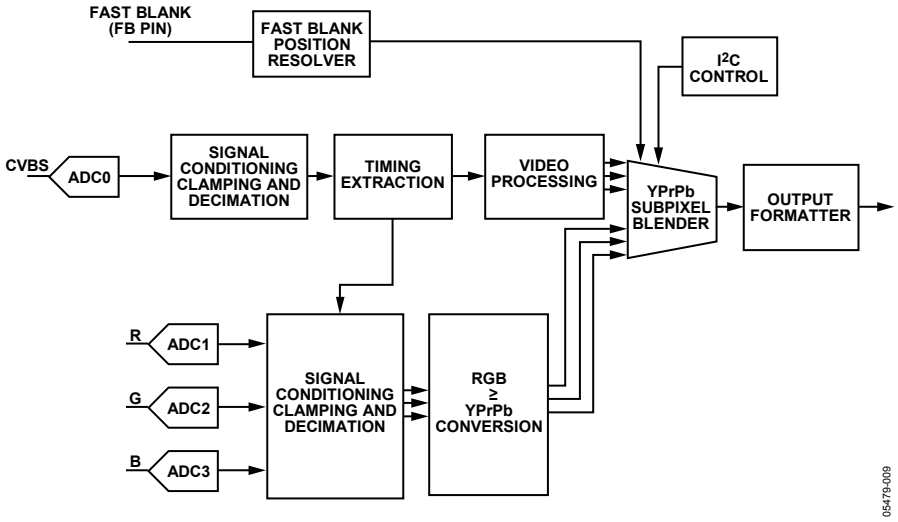


*Figure 9. Fast Blanking Configuration*

### *Fast Blank Edge Shaping*

**FB_EDGE_SHAPE [2:0], Address 0xEF [2:0]**

To improve the picture transition for high speed fast blank switching, an edge-shaping mode is available on the ADV7184. Depending on the format of the RGB inputs, it may be advantageous to apply different levels of edge shaping. The levels are selected via the FB_EDGE_SHAPE [2:0] bits. Users are advised to try each of the settings and select the setting that is most visually pleasing on their system.

**Table 13. FB_EDGE_SHAPE [2:0] Function**

| FB_EDGE_SHAPE [2:0] | Description |
|---|---|
| 000 | No edge shaping |
| 001 | Level 1 edge shaping |
| 010 (default) | Level 2 edge shaping |
| 011 | Level 3 edge shaping |
| 100 | Level 4 edge shaping |
| 101 to 111 | Not valid |

### *Contrast Reduction*

For overlay applications, text can be more readable if the contrast of the video directly behind the text is reduced. To enable the definition of a window of reduced contrast behind inserted text, the signal applied to the FB pin can be interpreted as a trilevel signal, as shown in Figure 10.

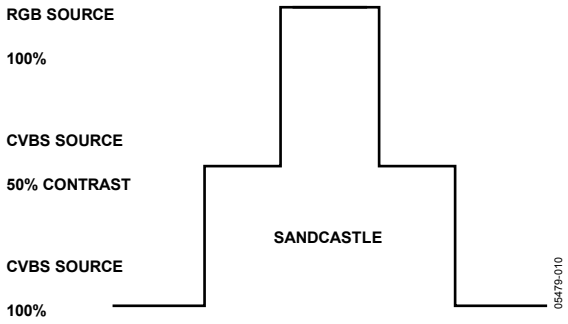


*Figure 10. Fast Blank Signal Representation with Contrast Reduction Enabled*

### *Contrast Reduction Enable*

**CNTR_ENABLE, Address 0xEF [3]**

This bit enables the contrast reduction feature and changes the meaning of the signal applied to the FB pin.

0 (default)—The contrast reduction feature is disabled, and the fast blank signal is interpreted as a bilevel signal.

1—The contrast reduction feature is enabled, and the fast blank signal is interpreted as a trilevel signal.

### *Contrast Mode*

**CNTR_MODE [1:0], Address 0xF1 [3:2]**

The contrast level in the selected contrast reduction box is selected using the CNTR_MODE [1:0] bits.

**Table 14. CNTR_MODE [1:0] Function**

| CNTR_MODE [1:0] | Description |
|---|---|
| 00 (default) | 25% |
| 01 | 50% |
| 10 | 75% |
| 11 | 100% |

### *Fast Blank and Contrast Reduction Programmable Thresholds*

The internal fast blank and contrast reduction signals are resolved from the trilevel FB signal using two comparators, as shown in Figure 11. To facilitate compliance with different input level standards, the reference level to these comparators is programmable via FB_LEVEL [1:0] and CNTR_LEVEL [1:0]. The resulting thresholds are given in Table 15.

#### FB_LEVEL [1:0], Address 0xF1 [5:4]

These bits control the reference level for the fast blank comparator.

#### CNTR_LEVEL [1:0], Address 0xF1 [7:6]

These bits control the reference level for the contrast reduction comparator.

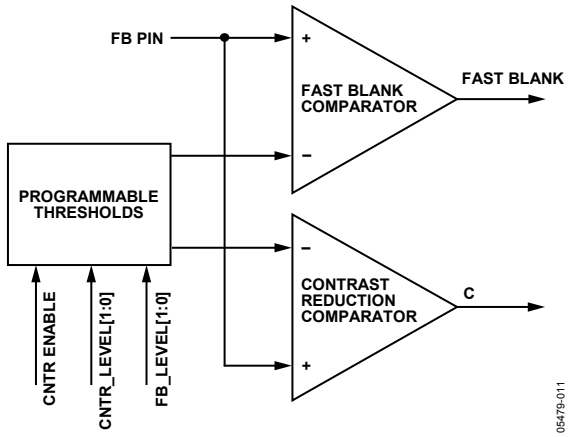


*Figure 11. Fast Blank and Contrast Reduction Programmable Threshold*

**Table 15. Fast Blank and Contrast Reduction Programmable Threshold I²C Controls**

| CNTR_ENABLE | FB_LEVEL [1:0] | CNTR_LEVEL [1:0] | Fast Blanking Threshold (V) | Contrast Reduction Threshold (V) |
|---|---|---|---|---|
| 0 | 00 (default) | XX | 1.4 | n/a |
| 0 | 01 | XX | 1.6 | n/a |
| 0 | 10 | XX | 1.8 | n/a |
| 0 | 11 | XX | 2.0 | n/a |
| 1 | 00 (default) | 00 | 1.6 | 0.4 |
| 1 | 01 | 01 | 1.8 | 0.6 |
| 1 | 10 | 10 | 2.0 | 0.8 |
| 1 | 11 | 11 | 2.2 | 2.0 |

### *FB_INV, Address 0xED [3], Write Only*

The interpretation of the polarity of the signal applied to the FB pin can be changed using FB_INV.

0 (default)—The fast blank pin is active high.

1—The fast blank pin is active low.

### *Readback of FB Pin Status*

**FB_STATUS [3:0], Address 0xED [7:4]**

FB_STATUS [3:0] is a readback value that provides the system information on the status of the FB pins, as shown in Table 16.

### *FB Timing*

**FB_SP_ADJUST [3:0], Address 0xEF [7:4]**

The critical information extracted from the FB signal is the time at which it switches relative to the input video. Due to small timing inequalities either on the IC or on the PCB, it may be necessary to adjust the result by a fraction of one clock cycle. This is controlled by FB_SP_ADJUST [3:0].

Each LSB of FB_SP_ADJUST [3:0] corresponds to ⅛$^{th}$ of an ADC clock cycle. Increasing the value is equivalent to adding delay to the FB signal. The reset value is chosen to produce equalized channels when the ADV7184 internal antialiasing filters are enabled and there are only intentional delays on the PCB.

The default value of FB_SP_ADJUST [3:0] is 0100.

### *Alignment of FB Signal*

**FB_DELAY [3:0], Address 0xF0 [3:0]**

In the event of misalignment between the FB input signal and the other input signals (CVBS and RGB) or unequalized delays in their processing, it is possible to alter the delay of the FB signal in 28.63636 MHz clock cycles. (For a finer granularity delay of the FB signal, refer to the FB_SP_ADJUST [3:0], Address 0xEF [7:4] section.)

The default value of FB_DELAY [3:0] is 0100.

### *Color Space Converter Manual Adjust*

**FB_CSC_MAN, Address 0xEE [7]**

As shown in Figure 9, the data from the CVBS and RGB sources are converted to YPbPr before being combined. For the RGB source, CSC must be used to perform this conversion. When SCART support is enabled, the parameters for CSC are automatically configured for this operation.

If the user wishes to use a different conversion matrix, this autoconfiguration can be disabled and the CSC can be manually programmed. For details on this manual configuration, contact an Analog Devices representative.

0 (default)—The CSC is configured automatically for the RGB-to-YPrPb conversion.

1—The CSC can be configured manually (not recommended).

**Table 16. FB_STATUS Functions**

| FB_STATUS [3:0] | Bit Name | Description |
|---|---|---|
| 0 | FB_STATUS.0 | FB_RISE. A high value indicates that there has been a rising edge on FB since the last I²C read. The value is cleared by an I²C read (this is a self-clearing bit). |
| 1 | FB_STATUS.1 | FB_FALL. A high value indicates that there has been a falling edge on FB since the last I²C read. The value is cleared by an I²C read (this is a self-clearing bit). |
| 2 | FB_STATUS.2 | FB_STAT. The value of the FB input pin at the time of the read. |
| 3 | FB_STATUS.3 | FB_HIGH. A high value indicates that there has been a rising edge on FB since the last I²C read. The value is cleared by an I²C read (this is a self-clearing bit). |

# GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

## POWER-SAVING MODES

### *Power-Down*

**PDBP, Address 0x0F [2]**

The digital core of the ADV7184 can be shut down by using the $\overline{\text{PWRDN}}$ pin or the PWRDN bit. The PDBP bit determines which of the two controls has the higher priority. The default is to give the pin ($\overline{\text{PWRDN}}$) priority. This allows the user to have the ADV7184 powered down by default.

0 (default)—The digital core power is controlled by the $\overline{\text{PWRDN}}$ pin (the bit is disregarded).

1—The bit has priority (the pin is disregarded).

**PWRDN, Address 0x0F [5]**

Setting the PWRDN bit switches the ADV7184 into a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No $I^2C$ bits are lost during power-down. The PWRDN bit also affects the analog blocks and switches them into low current modes. The $I^2C$ interface itself is unaffected and remains operational in power-down mode.

The ADV7184 leaves the power-down state if the PWRDN bit is set to 0 (via $I^2C$) or if the overall part is reset using the $\overline{\text{RESET}}$ pin. Note that PDBP must be set to 1 for the PWRDN bit to power down the ADV7184.

0 (default)—The chip is operational.

1—The ADV7184 is in chip-wide power-down mode.

### *ADC Power-Down Control*

The ADV7184 contains four 10-bit ADCs (ADC0, ADC1, ADC2, and ADC3). If required, it is possible to power down each ADC individually.

- In CVBS mode, ADC1 and ADC2 should be powered down to reduce power consumption.
- In S-video mode, ADC2 should be powered down to reduce power consumption.

**PWRDN_ADC_0, Address 0x3A [3]**

0 (default)—The ADC is in normal operation.

1—ADC0 is powered down.

**PWRDN_ADC_1, Address 0x3A [2]**

0 (default)—The ADC is in normal operation.

1—ADC1 is powered down.

**PWRDN_ADC_2, Address 0x3A [1]**

0 (default)—The ADC is in normal operation.

1—ADC2 is powered down.

**PWRDN_ADC_3, Address 0x3A [0]**

0 (default)—The ADC is in normal operation.

1—ADC3 is powered down.

**FB_PWRDN, Address 0x0F [1]**

To achieve a very low power-down current, it is necessary to prevent activity on toggling input pins from reaching circuitry, where it could consume current. FB_PWRDN gates signals from the FB input pin.

0 (default)—The FB input is in normal operation.

1—The FB input is in the power-saving mode.

## RESET CONTROL

### *RES, Chip Reset, Address 0x0F [7]*

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7184, issues a chip reset. All $I^2C$ registers are reset to their default values, making these bits self-clearing. Some register bits do not have a reset value specified and instead keep the last value written to them. These bits are marked as having a reset value of x in the register tables. After the reset sequence, the part immediately starts to acquire the incoming video signal.

Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before performing subsequent $I^2C$ writes.

The $I^2C$ master controller receives a no acknowledge condition on the ninth clock cycle when a chip reset is implemented. See the MPU Port Description section for a full description.

0 (default)—Operation is normal.

1—The reset sequence starts.

## GLOBAL PIN CONTROL

### *Three-State Output Drivers*

**TOD, Address 0x03 [6]**

This bit allows the user to three-state the output drivers of the ADV7184. Upon setting the TOD bit, the P15 to P0, HS, VS, FIELD, and SFL pins are three-stated. The ADV7184 also supports three-stating via a dedicated pin, $\overline{\text{OE}}$. The output drivers are three-stated if the TOD bit or the $\overline{\text{OE}}$ pin is set high.

The timing pins (HS, VS, and FIELD) can be forced active via the TIM_OE bit of Register 0x04. For more information on three-state control, refer to the Three-State LLC Drivers and the Timing Signals Output Enable sections. Individual drive

strength controls are provided by the DR_STR_S, DR_STR_C, and DR_STR bits of Register 0xF4.

0 (default)—The output drivers are enabled.

1—The output drivers are three-stated.

### *Three-State LLC Drivers*

**TRI_LLC, Address 0x1D [7]**

This bit allows the output drivers for the LLC1 and LLC2 pins of the ADV7184 to be three-stated. For more information on three-state control, refer to the Three-State Output Drivers and the Timing Signals Output Enable sections. Individual drive strength controls are provided via the DR_STR_S, DR_STR_C, and DR_STR bits.

0 (default)—The LLC pin drivers work according to the DR_STR_C [1:0] setting (pin enabled).

1—The LLC pin drivers are three-stated.

### *Timing Signals Output Enable*

**TIM_OE, Address 0x04 [3]**

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD into the active (that is, driving) state even if the TOD bit is set. If the TIM_OE bit is set to low, the HS, VS, and FIELD pins are three-stated depending on the TOD bit. This functionality is useful if the decoder is to be used only as a timing generator. This may be the case if only the timing signals are to be extracted from an incoming signal or if the part is in free-run mode, where, for example, a separate chip can output a company logo. For more information on three-state control, refer to the Three-State Output Drivers and the Three-State LLC Drivers sections. Individual drive strength controls are provided via the DR_STR_S, DR_STR_C, and DR_STR bits.

0 (default)—HS, VS, and FIELD are three-stated according to the TOD bit.

1—HS, VS, and FIELD are forced active.

### *Drive Strength Selection (Data)*

**DR_STR [1:0], Address 0xF4 [5:4]**

Because of EMC and crosstalk factors, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR [1:0] bits affect the P [15:0] output drivers.

For more information on three-state control, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Sync) sections.

**Table 17. DR_STR Function**

| DR_STR [1:0] | Description |
|---|---|
| 01 (default) | Medium-low drive strength (2×) |
| 10 | Medium-high drive strength (3×) |
| 11 | High drive strength (4×) |

### *Drive Strength Selection (Clock)*

**DR_STR_C [1:0], Address 0xF4 [3:2]**

The DR_STR_C [1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, refer to the Drive Strength Selection (Sync) and the Drive Strength Selection (Data) sections.

**Table 18. DR_STR_C Function**

| DR_STR_C [1:0] | Description |
|---|---|
| 01 (default) | Medium-low drive strength (2×) |
| 10 | Medium-high drive strength (3×) |
| 11 | High drive strength (4×) |

### *Drive Strength Selection (Sync)*

**DR_STR_S [1:0], Address 0xF4 [1:0]**

The DR_STR_S [1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and FIELD are driven. For more information, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Data) sections.

**Table 19. DR_STR_S Function**

| DR_STR_S [1:0] | Description |
|---|---|
| 01 (default) | Medium-low drive strength (2×) |
| 10 | Medium-high drive strength (3×) |
| 11 | High drive strength (4×) |

### *Enable Subcarrier Frequency Lock Pin*

**EN_SFL_PIN, Address 0x04 [1]**

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7184 core to an encoder in a decoder/encoder back-to-back arrangement.

0 (default)—The subcarrier frequency lock output is disabled.

1—The subcarrier frequency lock information is presented on the SFL pin.

### *Polarity LLC Pin*

**PCLK, Address 0x37 [0]**

The polarity of the clock that leaves the ADV7184 via the LLC1 and LLC2 pins can be inverted using the PCLK bit. Changing the polarity of the LLC clock output may be necessary to meet the setup time and hold time expectations of follow-on chips. This bit also inverts the polarity of the LLC2 clock.

0—The LLC output polarity is inverted.

1 (default)—The LLC output polarity is normal, as per the timing diagrams (see Figure 2 to Figure 4).

## GLOBAL STATUS REGISTERS

Three registers provide summary information about the video decoder: Status Register 1, Status Register 2, and Status Register 3. These registers contain status bits that report operational information to the user.

### *Status Register 1 [7:0], Address 0x10 [7:0]*

This read-only register provides information about the internal status of the ADV7184. See the CIL [2:0], Count-Into-Lock, Address 0x51 [2:0] and the COL [2:0], Count-Out-of-Lock, Address 0x51 [5:3] sections for information on the timing.

Depending on the setting of the FSCLE bit, the IN_LOCK [0] and LOST_LOCK [1] bits of Status Register 1 are based solely on the horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, $F_{SC}$ Lock Enable, Address 0x51 [7] section.

#### AD_RESULT [2:0], Autodetection Result, Address 0x10 [6:4]

These bits report the findings from the autodetection block. For more information on enabling the autodetection block, see the General Setup section. For information on configuring this block, see the Autodetection of SD Modes section.

**Table 20. AD_RESULT Function**

| AD_RESULT [2:0] | Description |
|---|---|
| 000 | NTSC M/J |
| 001 | NTSC 443 |
| 010 | PAL M |
| 011 | PAL 60 |
| 100 | PAL B/G/H/I/D |
| 101 | SECAM |
| 110 | PAL Combination N |
| 111 | SECAM 525 |

### *Status Register 2 [7:0], Address 0x12 [7:0]*

See Table 22.

### *Status Register 3 [7:0], Address 0x13 [7:0]*

See Table 23.

**Table 21. Status Register 1 Function**

| Status Register 1 [7:0] | Bit Name | Description |
|---|---|---|
| 0 | IN_LOCK | In lock (now). |
| 1 | LOST_LOCK | Lost lock (since last read of this register). |
| 2 | FSC_LOCK | $F_{SC}$ locked (now). |
| 3 | FOLLOW_PW | AGC follows peak white algorithm. |
| 4 | AD_RESULT.0 | Result of autodetection. |
| 5 | AD_RESULT.1 | Result of autodetection. |
| 6 | AD_RESULT.2 | Result of autodetection. |
| 7 | COL_KILL | Color kill is active. |

**Table 22. Status Register 2 Function**

| Status Register 2 [7:0] | Bit Name | Description |
|---|---|---|
| 0 | MVCS DET | Detected Macrovision color striping. |
| 1 | MVCS T3 | Macrovision color striping protection. Conforms to Type 3 if high, Type 2 if low. |
| 2 | MV_PS DET | Detected Macrovision pseudosync pulses. |
| 3 | MV_AGC DET | Detected Macrovision AGC pulses. |
| 4 | LL_NSTD | Line length is nonstandard. |
| 5 | FSC_NSTD | $F_{SC}$ frequency is nonstandard. |
| 6 | Reserved | |
| 7 | Reserved | |

**Table 23. Status Register 3 Function**

| Status Register 3 [7:0] | Bit Name | Description |
|---|---|---|
| 0 | INST_HLOCK | Horizontal lock indicator (instantaneous). |
| 1 | GEMD | Gemstar detect. |
| 2 | SD_OP_50HZ | Flags whether 50 Hz or 60 Hz is present at output. |
| 3 | CVBS | Indicates if a CVBS signal is detected in composite/S-video autodetection configuration. |
| 4 | FREE_RUN_ACT | Indicates if the ADV7184 is in free-run mode. Outputs a blue screen by default. See the DEF_VAL_AUTO_EN, Default Value Automatic Enable, Address 0x0C [1] section for details about disabling this function. |
| 5 | STD_FLD_LEN | Field length is correct for currently selected video standard. |
| 6 | INTERLACED | Interlaced video detected (field sequence found). |
| 7 | PAL_SW_LOCK | Reliable sequence of swinging bursts detected. |

# STANDARD DEFINITION PROCESSOR (SDP)

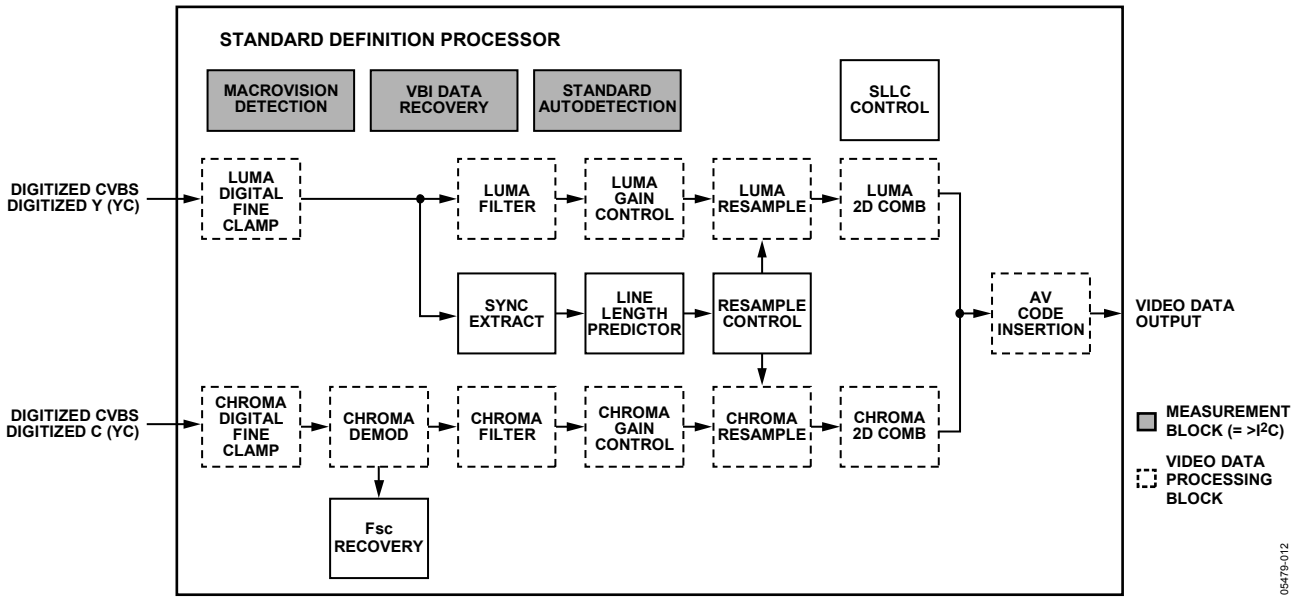


*Figure 12. Block Diagram of the Standard Definition Processor*

A block diagram of the ADV7184 standard definition processor (SDP) is shown in Figure 12.

The SDP can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance path and a chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

## SD LUMA PATH

The input signal is processed by the following blocks:

- Luma Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma Filter. This block contains a luma decimation filter (YAA) with a fixed response and some luma-shaping filters (YSH) that have selectable responses.
- Luma Gain Control. The automatic gain control (AGC) can operate on a variety of modes, including a mode based on the depth of the horizontal sync pulse, a mode based on the peak white mode, and a mode that uses a fixed manual gain.
- Luma Resample. To correct for errors and dynamic changes in line lengths, the data is digitally resampled.
- Luma 2D Comb. The two-dimensional comb filter provides Y/C separation.
- AV Code Insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes (as per ITU-R. BT-656) can be inserted.

## SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma Demodulation. This block uses a color subcarrier ($F_{SC}$) recovery unit to regenerate the color subcarrier for any modulated chroma scheme and then performs an AM demodulation for PAL and NTSC and an FM demodulation for SECAM.
- Chroma Filter. This block contains a chroma decimation filter (CAA) with a fixed response and some chroma-shaping filters (CSH) that have selectable responses.
- Chroma Gain Control. Automatic gain control (AGC) can operate on several modes, including a mode based on the color subcarrier's amplitude, a mode based on the depth of the horizontal sync pulse on the luma channel, and a mode that uses a fixed manual gain.
- Chroma Resample. The chroma data is digitally resampled to keep it aligned with the luma data. The resampling is done to correct for static and dynamic errors in the line lengths of the incoming video signal.
- Chroma 2D Comb. The two-dimensional, 5-line, super-adaptive comb filter provides high quality Y/C separation in case the input signal is CVBS.
- AV Code Insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes (as per ITU-R. BT-656) can be inserted.