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Professional *Extended-10*™ Video Encoder with 54 MHz Oversampling

ADV7194

FEATURES

- 10-Bit Extended CCIR-656 Input Data Port
- Six High-Quality 10-Bit Video DACs
- 10-Bit Internal Digital Video Processing
- Multistandard Video Input
- Multistandard Video Output
- 4× Oversampling with Internal 54 MHz PLL
- Programmable Video Control Includes:
  - Digital Noise Reduction
  - Gamma Correction
  - Black Burst
  - LUMA Delay
  - CHROMA Delay
  - Multiple Luma and Chroma Filters
  - Luma SSAF™ (Super Sub-Alias Filter)
  - Average Brightness Detection
  - Field Counter
- CGMS (Copy Generation Management System)
- WSS (Wide Screen Signaling)
- Closed Captioning Support
- Teletext Insertion Port (PAL-WST)
- 2-Wire Serial MPU Interface (I^2C Compatible and Fast I^2C)
- Supply Voltage 5 V and 3.3 V Operation
- 80-Lead LQFP Package

APPLICATIONS

- Professional DVD Playback Systems
- PC Video/Multimedia Playback Systems
- Progressive Scan Playback Systems
- Professional Studio Equipment

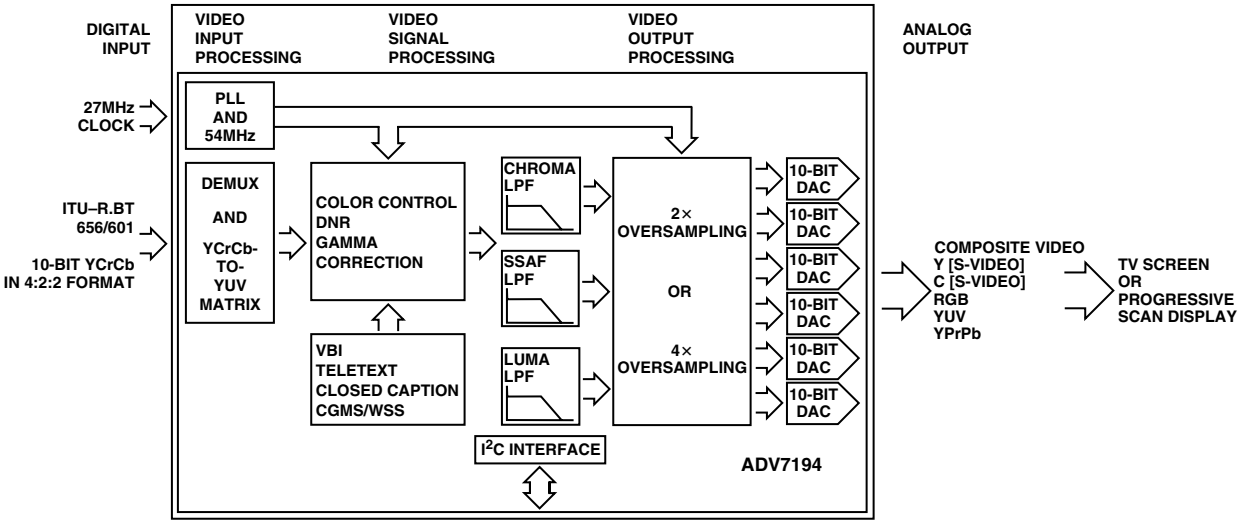
GENERAL DESCRIPTION

The ADV7194 is part of the new generation of video encoders from Analog Devices. The device builds on the performance of previous video encoders and provides new features like interfacing progressive scan devices, digital noise reduction, gamma correction, 4× oversampling and 54 MHz operation, average brightness detection, black burst signal generation, chroma delay, an additional Chroma Filter, etc.

The ADV7194 supports NTSC-M, NTSC-N (Japan), PAL N, PAL-B/D/G/H/I and PAL-60 standards. Input standards supported include ITU-R.BT656 4:2:2 YCrCb in 8-, 10-, 16- or 20-bit format and 3× 10-bit YCrCb progressive scan format. The ADV7194 can output composite video (CVBS), S-Video (Y/C), Component YUV or RGB and analog progressive scan in YPrPb format. The analog component output is also compatible with Betacam, MII and SMPTE/EBU N10 levels, SMPTE 170M NTSC and ITU-R.BT 470 PAL.

For more information about the ADV7194's features refer to Detailed Description of Features section.

SIMPLIFIED BLOCK DIAGRAM



Extended-10 is a trademark of Analog Devices, Inc. This technology combines 10-bit conversion, 10-bit digital video data processing, and 10-bit external interfacing.
SSAF is a trademark of Analog Devices Inc.
ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).
I^2C is a registered trademark of Philips Corporation.

REV. A

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ADV7194* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-205: Video Formats and Required Load Terminations
- AN-213: Low Cost, Two-Chip, Voltage -Controlled Amplifier and Video Switch
- AN-562: Filter specification for the Internal Filters of the ADV719x Video Encoders

Data Sheet

- ADV7194: Professional Extended-10™ Video Encoder With 54 MHz Oversampling Data Sheet

DESIGN RESOURCES

- ADV7194 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADV7194 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

CONTENTS

SPECIFICATIONS

5 V SPECIFICATIONS[1] (V_{AA} = 5 V, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)			10	Bits	
Accuracy (Each DAC)					
Integral Nonlinearity[3]			±1.0	LSB	
Differential Nonlinearity[3]			±1.0	LSB	Guaranteed Monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		0	±1	μA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		6	10	pF	
Input Leakage Current[4]		1		μA	
Input Leakage Current[5]		200		μA	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}		0.8	0.4	V	I_{SINK} = 3.2 mA
Three-State Leakage Current[6]		10		μA	
Three-State Leakage Current[7]		200		μA	
Three-State Output Capacitance		6	10	pF	
ANALOG OUTPUTS					
Output Current (Max)	4.125	4.33	4.625	mA	R_L = 300 Ω
Output Current (Min)		2.16		mA	R_L = 600 Ω, $R_{SET1,2}$ = 2400 Ω
DAC-to-DAC Matching[3]		0.4	2.5	%	
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		6		pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE[8]					
Reference Range, V_{REF}	1.112	1.235	1.359	V	
POWER REQUIREMENTS					
V_{AA}	4.75	5.0	5.25	V	
Normal Power Mode					
I_{DAC}[9]		29	35	mA	
I_{CCT} (2× Oversampling)[10, 11]		80	120	mA	
I_{CCT} (4× Oversampling)[10, 11]		120	170	mA	
I_{PLL}		6	10	mA	
Sleep Mode					
I_{DAC}		0.01		μA	
I_{CCT}		85		μA	

NOTES
[1]All measurements are made in 4× Oversampling Mode unless otherwise specified.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Guaranteed by characterization.
[4]For all inputs but PAL_NTSC and ALSB.
[5]For PAL_NTSC and ALSB inputs.
[6]For all outputs but $\overline{VSO}$/TTX/CLAMP.
[7]For $\overline{VSO}$/TTX/CLAMP outputs.
[8]Measurement made in 2× Oversampling Mode.
[9]I_{DAC} is the total current required to supply all DACs including the V_{REF} circuitry.
[10]All six DACs on.
[11]I_{CCT} or the circuit current, is the continuous current required to drive the digital core without I_{PLL}.

Specifications subject to change without notice.

ADV7194–SPECIFICATIONS

3.3 V SPECIFICATIONS[1] (V_{AA} = 3.0 V, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)			10	Bits	
Accuracy (Each DAC)					
Integral Nonlinearity			±1.0	LSB	
Differential Nonlinearity			±1.0	LSB	Guaranteed Monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2		V	
Input Low Voltage, V_{INL}		0.8		V	
Input Current, I_{IN}			±1	μA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		6	10	pF	
Input Leakage Current[3]		1		μA	
Input Leakage Current[4]		200		μA	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}		2.4		V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}		0.4		V	I_{SINK} = 3.2 mA
Three-State Leakage Current[5]		10		μA	
Three-State Leakage Current[6]		200		μA	
Three-State Output Capacitance		6	10	pF	
ANALOG OUTPUTS					
Output Current (Max)	4.125	4.33	4.625	mA	R_L = 300 Ω
Output Current (Min)		2.16		mA	R_L = 600 Ω, $R_{SET1,2}$ = 2400 Ω
DAC-to-DAC Matching		0.4	2.5	%	
Output Compliance, V_{OC}			1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		6		pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE					
Reference Range[7]		1.235		V	
POWER REQUIREMENTS					
V_{AA}	3.15	3.3	3.6	V	
Normal Power Mode					
I_{DAC}[8]		29		mA	
I_{CCT} (2× Oversampling)[9, 10]		42	54	mA	
I_{CCT} (4× Oversampling)[9, 10]		68	86	mA	
I_{PLL}		6		mA	
Sleep Mode					
I_{DAC}		0.01		μA	
I_{CCT}		85		μA	

NOTES

[1]All measurements are made in 4× Oversampling Mode unless otherwise specified and are guaranteed by characterization. For 2× Oversampling Mode, the power requirements for the ADV7194 are typically 3.0 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]For all inputs but PAL_NTSC and ALSB.

[4]For PAL_NTSC and ALSB inputs.

[5]For all outputs but $\overline{VSO}$/TTX/CLAMP.

[6]For $\overline{VSO}$/TTX/CLAMP outputs.

[7]Measurement made in 2× Oversampling Mode.

[8]I_{DAC} is the total current required to supply all DACs including the V_{REF} circuitry.

[9]All six DACs on.

[10]I_{CCT} or the circuit current, is the continuous current required to drive the digital core without I_{PLL}.

Specifications subject to change without notice.

5 V DYNAMIC SPECIFICATIONS[1]

(V_{AA} = 5 V ± 250 mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
Hue Accuracy		0.5		Degrees	
Color Saturation Accuracy		0.7		%	
Chroma Nonlinear Gain		0.7	0.9	±%	Referenced to 40 IRE
Chroma Nonlinear Phase		0.5		±Degrees	
Chroma/Luma Intermod		0.1		±%	
Chroma/Luma Gain Ineq		1.7		±%	
Chroma/Luma Delay Ineq		2.2		ns	
Luminance Nonlinearity		0.6	0.7	±%	
Chroma AM Noise		82		dB	
Chroma PM Noise		72		dB	
Differential Gain[3]		0.1 (0.4)	0.3 (0.5)	%	
Differential Phase[3]		0.4 (0.15)	0.5 (0.3)	Degrees	
SNR (Pedestal)[3]		78.5 (78)		dB rms	RMS
		78 (78)		dB p-p	Peak Periodic
SNR (Ramp)[3]		61.7 (61.7)		dB rms	RMS
		62 (63)		dB p-p	Peak Periodic

NOTES
[1]All measurements are made in 4× Oversampling Mode unless otherwise specified.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Values in parentheses apply to 2× Oversampling Mode.

Specifications subject to change without notice.

3.3 V DYNAMIC SPECIFICATIONS[1]

(V_{AA} = 3.3 V ± 150 mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
Hue Accuracy		0.5		Degrees	
Color Saturation Accuracy		0.8		%	
Luminance Nonlinearity		0.6		±%	
Chroma AM Noise		83		dB	
Chroma PM Noise		71		dB	
Chroma Nonlinear Gain		0.7		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		0.5		±Degrees	
Chroma/Luma Intermod		0.1		±%	
Differential Gain[3]		0.2 (0.5)		%	
Differential Phase[3]		0.5 (0.2)		Degrees	
SNR (Pedestal)[3]		78.5 (78)		dB rms	RMS
		78 (78)		dB p-p	Peak Periodic
SNR (Ramp)[3]		62.3 (62)		dB rms	RMS
		61 (62.5)		dB p-p	Peak Periodic

NOTES
[1]All measurements are made in 4× Oversampling Mode unless otherwise specified.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Values in brackets apply to 2× Oversampling Mode.

Specifications subject to change without notice.

5 V TIMING CHARACTERISTICS

(V_{AA} = 5 V ± 250 mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[2]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After This Period the First Clock Is Generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
ANALOG OUTPUTS[2]					
Analog Output Delay		8		ns	
DAC Analog Output Skew		0.1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLOCK}		27		MHz	
Clock High Time, t_9	8			ns	
Clock Low Time, t_{10}	8			ns	
Data Setup Time, t_{11}	6			ns	
Data Hold Time, t_{12}	5			ns	
Control Setup Time, t_{11}	6			ns	
Control Hold Time, t_{12}	4			ns	
Digital Output Access Time, t_{13}		13	24	ns	
Digital Output Hold Time, t_{14}		12		ns	
Pipeline Delay, t_{15} (2× Oversampling)		57		Clock Cycles	
Pipeline Delay, t_{15} (4× Oversampling)		67		Clock Cycles	
TELETEXT PORT[4]					
Digital Output Access Time, t_{16}		11		ns	
Data Setup Time, t_{17}		3		ns	
Data Hold Time, t_{18}		6		ns	
$\overline{\text{RESET}}$ CONTROL					
$\overline{\text{Reset}}$ Low Time		3	20	ns	
PLL[2]					
PLL Output Frequency		54		MHz	

NOTES
[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[2]Guaranteed by characterization.
[3]Pixel Port consists of the following:
Data: P0–P9, *Y*0/P10–*Y*9/P19,
Control: $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock: CLKIN Input.
[4]Teletext Port consists of:
Digital Output: TTXRQ,
Data: TTX.

Specifications subject to change without notice.

3.3 V TIMING CHARACTERISTICS

(V_{AA} = 3.3 V ± 150 mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)[2]

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After This Period the First Clock Is Generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6	2		µs	
ANALOG OUTPUTS					
Analog Output Delay		8		ns	
DAC Analog Output Skew		0.1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLOCK}		27		MHz	
Clock High Time, t_9	8			ns	
Clock Low Time, t_{10}	8			ns	
Data Setup Time, t_{11}	6			ns	
Data Hold Time, t_{12}	4			ns	
Control Setup Time, t_{11}	2.5			ns	
Control Hold Time, t_{12}	3			ns	
Digital Output Access Time, t_{13}		13		ns	
Digital Output Hold Time, t_{14}		12		ns	
Pipeline Delay, t_{15}, 2× Oversampling		37		Clock Cycles	
TELETEXT PORT[4]					
Digital Output Access Time, t_{16}		11		ns	
Data Setup Time, t_{17}		3		ns	
Data Hold Time, t_{18}		6		ns	
$\overline{\text{RESET}}$ CONTROL					
$\overline{\text{RESET}}$ Low Time		3	20	ns	
PLL					
PLL Output Frequency		54		MHz	

NOTES
[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[2]Guaranteed by characterization.
[3]Pixel Port consists of the following:
Data: P0–P9, *Y*0/P10–*Y*9/P19,
Control: $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock: CLKIN Input.
[4]Teletext Port consists of:
Digital Output: TTXRQ,
Data: TTX.

Specifications subject to change without notice.

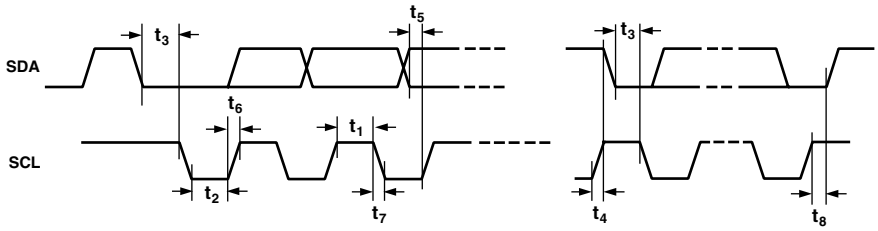


Figure 1. MPU Port Timing Diagram

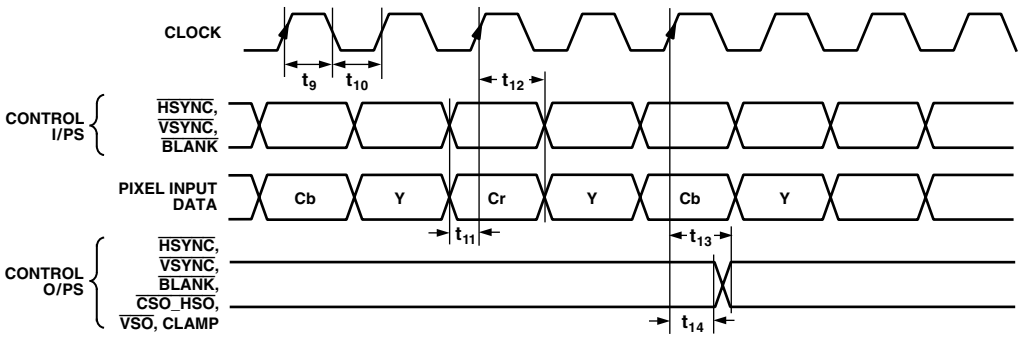


Figure 2. Pixel and Control Data Timing Diagram

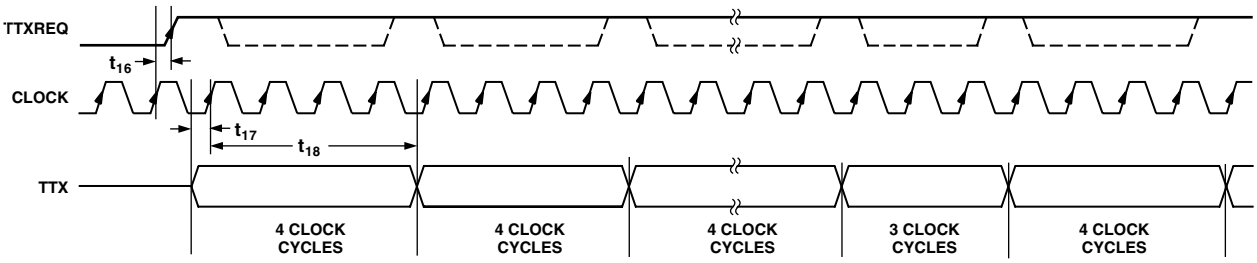


Figure 3. Teletext Timing Diagram

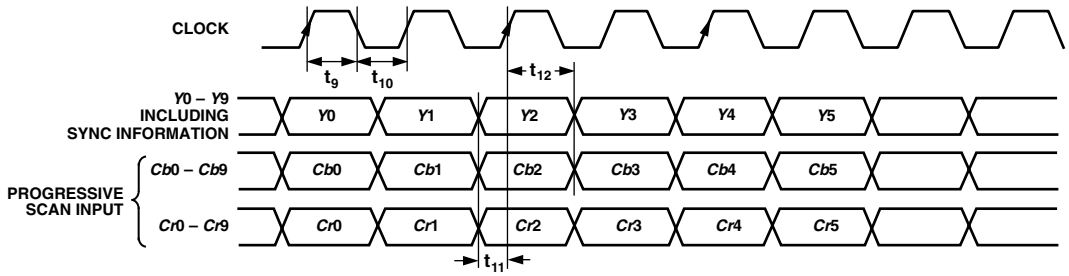


Figure 4. Progressive Scan Input Timing

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Input Pin . . . . GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Body Temperature (Soldering, 10 secs) . . . . . 220°C
Analog Outputs to GND[2] . . . . . GND – 0.5 to V_{AA}

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PACKAGE THERMAL PERFORMANCE

The 80-lead package is used for this device. The junction-to-ambient (θ_{JA}) thermal resistance in still air on a four-layer PCB is 24.7°C.

To reduce power consumption when using this part the user can run the part on a 3.3 V supply, turn off any unused DACs.

The user must at all times stay below the maximum junction temperature of 110°C. The following equation shows how to calculate this junction temperature:

$$\textit{Junction Temperature} = (V_{AA} \times (I_{DAC} + I_{CCT})) \times \theta_{JA} + 70°C\ (T_{AMB})$$

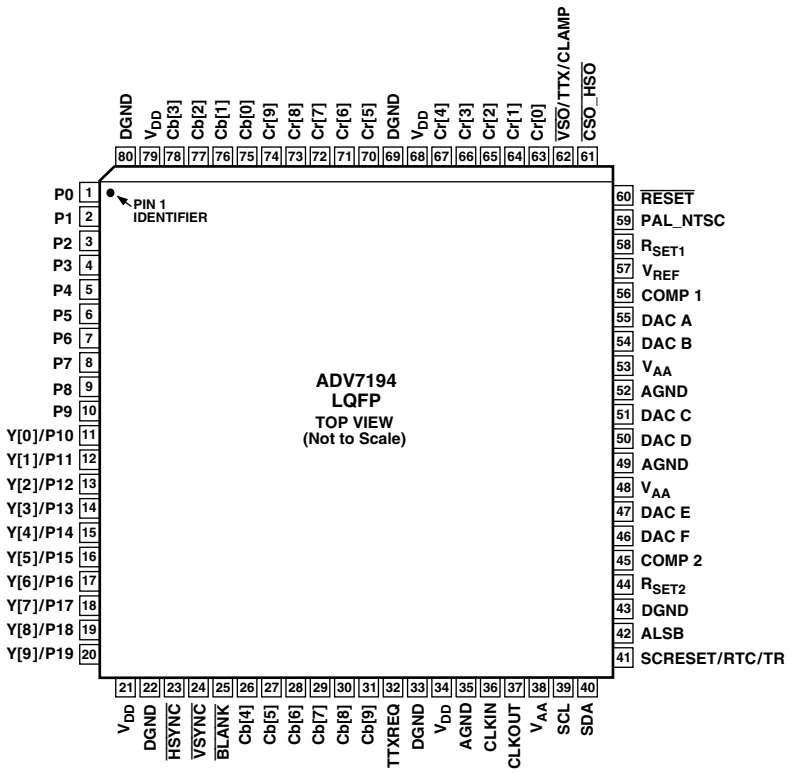
$$I_{DAC} = 10\ mA + (\textit{sum of the average currents consumed by each powered-on DAC})$$

$$\textit{Average current consumed by each powered-on DAC} = (V_{REF} \times K)/R_{SET}$$

$$V_{REF} = 1.235\ V$$

$$K = 4.2146$$

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7194KST	0°C to 70°C	80-Lead Quad Flatpack	ST-80

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7194 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/ Output	Function
1–10	P0–P9	I	10-Bit or 8-Bit 4:2:2 Multiplexed YCrCb Pixel Port. The LSB of the input data is set up on Pin P0 (Pin Number 1) in 10-bit input mode.
11–20	Y0/P10–Y9/P19	I	20-Bit or 16-Bit Multiplexed YCrCb Pixel Port or 1× 10-bit progressive scan input for Y data.
21, 34, 68, 79	V_{DD}	P	Digital Power Supply (3.3 V to 5 V).
22, 33, 43, 69, 80	DGND	G	Digital Ground.
23	$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1, 2, and 3) Control Signal. This pin may be configured to be an output (Master Mode) or an input (Slave Mode) and accept Sync Signals.
24	$\overline{\text{VSYNC}}$	I/O	$\overline{\text{VSYNC}}$ Control Signal. This pin may be configured as an output (Master Mode) or as an input (Slave Mode) and accept $\overline{\text{VSYNC}}$ as a Control Signal.
25	$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. This signal is optional. For further information see Vertical Blanking and Data Insertion Blanking Input section.
26–31, 75–78	Cb0–Cb9	I	1 × 10-Bit Progressive Scan Input Port for Cb Data.
32	TTXREQ	O	Teletext Data Request Output Signal, used to control teletext data transfer.
35, 49, 52	AGND	G	Analog Ground.
36	CLKIN	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
37	CLKOUT	O	Clock Output Pin.
38, 48, 53	V_{AA}	P	Analog Power Supply (3.3 V to 5 V).
39	SCL	I	MPU Port Serial Interface Clock Input.
40	SDA	I/O	MPU Port Serial Data Input/Output.
41	SCRESET/RTC/TR	I	Multifunctional Input: Real-Time Control (RTC) input, Timing Reset input, Subcarrier Reset input.
42	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
44	R_{SET2}	I	A 1200 Ω resistor connected from this pin to AGND is used to control full-scale amplitudes of the Video Signals from the DAC D, E, F.
45	COMP 2	O	Compensation Pin for DACs D, E, and F. Connect a 0.1 µF Capacitor from COMP 2 to V_{AA}.
46	DAC F	O	S-Video C/Pr/V/RED Analog Output. This DAC is capable of providing 4.33 mA output.
47	DAC E	O	S-Video Y/Pb/U/BLUE Analog Output. This DAC is capable of providing 4.33 mA output.
50	DAC D	O	Composite/Y/Y/GREEN Analog Output. This DAC is capable of providing 4.33 mA output.
51	DAC C	O	S-Video C/Pr/V/RED Analog Output. This DAC is capable of providing 4.33 mA output.
54	DAC B	O	S-Video Y/Pb/U/BLUE Analog Output. This DAC is capable of providing 4.33 mA output.
55	DAC A	O	Composite/Y/Y/GREEN Analog Output. This DAC is capable of providing 4.33 mA output.
56	COMP 1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 µF Capacitor from COMP 1 to V_{AA}.
57	V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V). An external V_{REF} can not be used in 4× oversampling mode.
58	R_{SET1}	I	A 1200 Ω resistor connected from this pin to AGND is used to control full-scale amplitudes of the Video Signals from the DAC A, B, C.
59	PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic 1 selects PAL.
60	$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7194 into default mode See Appendix 8 for Default Register settings.
61	$\overline{\text{CSO\_HSO}}$	O	Dual function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ output Sync Signal at TTL level.
62	$\overline{\text{VSO}}$/TTX/CLAMP	I/O	Multifunctional Pin. $\overline{\text{VSO}}$ Output Sync Signal at TTL level. Teletext Data Input pin. CLAMP TTL Output Signals can be used to drive external circuitry to enable clamping of all Video Signals.
63–67, 70–74	Cr0–Cr9	I	1 × 10-Bit Progressive Scan Input Port for Cr Data.

DETAILED DESCRIPTION OF FEATURES

Clocking
- **Single 27 MHz Clock Required to Run the Device**
- **4× Oversampling with Internal 54 MHz PLL**
- **Square Pixel Operation**

Advanced Power Management

Programmable Video Control Features
- **Digital Noise Reduction**
- **Black Burst Signal Generation**
- **Pedestal Level**
- **Hue, Brightness, Contrast and Saturation**
- **Clamping Output signal**
- **VBI (Vertical Blanking Interval)**
- **Subcarrier Frequency and Phase**
- **LUMA Delay**
- **CHROMA Delay**
- **Gamma Correction**
- **Luma and Chroma Filters**
- **Luma SSAF (Super Subalias Filter)**

Average Brightness Detection

Field Counter

Interlaced/Noninterlaced Operation

Complete On-Chip Video Timing Generator

Programmable Multimode Master/Slave Operation

CGMS (Copy Generation Management System)

WSS (Wide Screen Signaling)

Closed Captioning Support

Teletext Insertion Port (PAL-WST)

2-Wire Serial MPU Interface
(I²C Compatible and Fast I²C)

I²C Registers Synchronized to VSYNC

GENERAL DESCRIPTION

The ADV7194 is an integrated Digital Video Encoder that converts digital CCIR-601/656 4:2:2 10-bit (or 20-bit or 8-/16-bit) component video data into a standard analog baseband television signal compatible with worldwide standards. Additionally there is the possibility to input video data in 3× 10-bit YCrCb progressive scan format to facilitate interfacing devices such as progressive scan systems.

There are six DACs available on the ADV7194, each of which is capable of providing 4.33 mA of current. In addition to the composite output signal there is the facility to output S-Video (Y/C Video), RGB Video, and YUV Video. All YUV formats (SMPTE/EBU N10, MII, or Betacam) are supported.

The on-board SSAF (Super Subalias Filter) with extended luminance frequency response and sharp stopband attenuation enables studio quality video playback on modern TVs, giving optimal horizontal line resolution. An additional sharpness control feature allows high-frequency enhancement on the luminance signal.

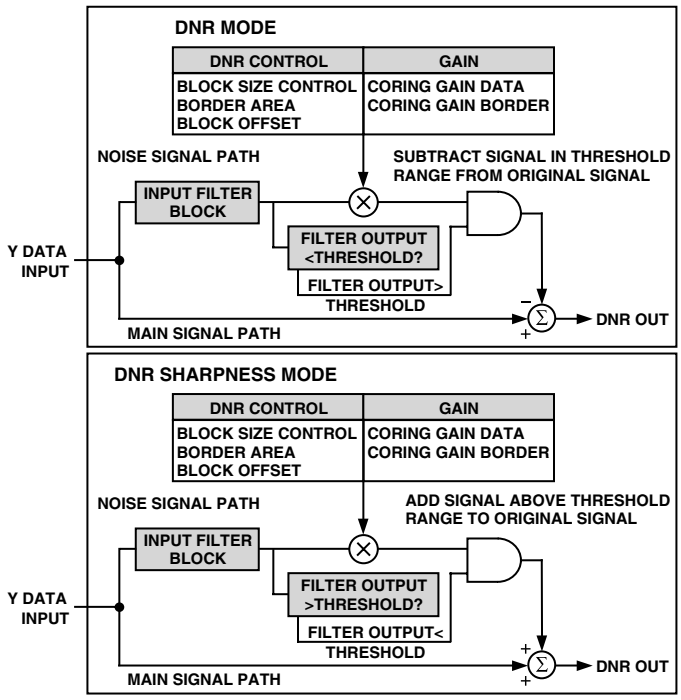


Figure 6. Block Diagram for DNR Mode and DNR Sharpness Mode

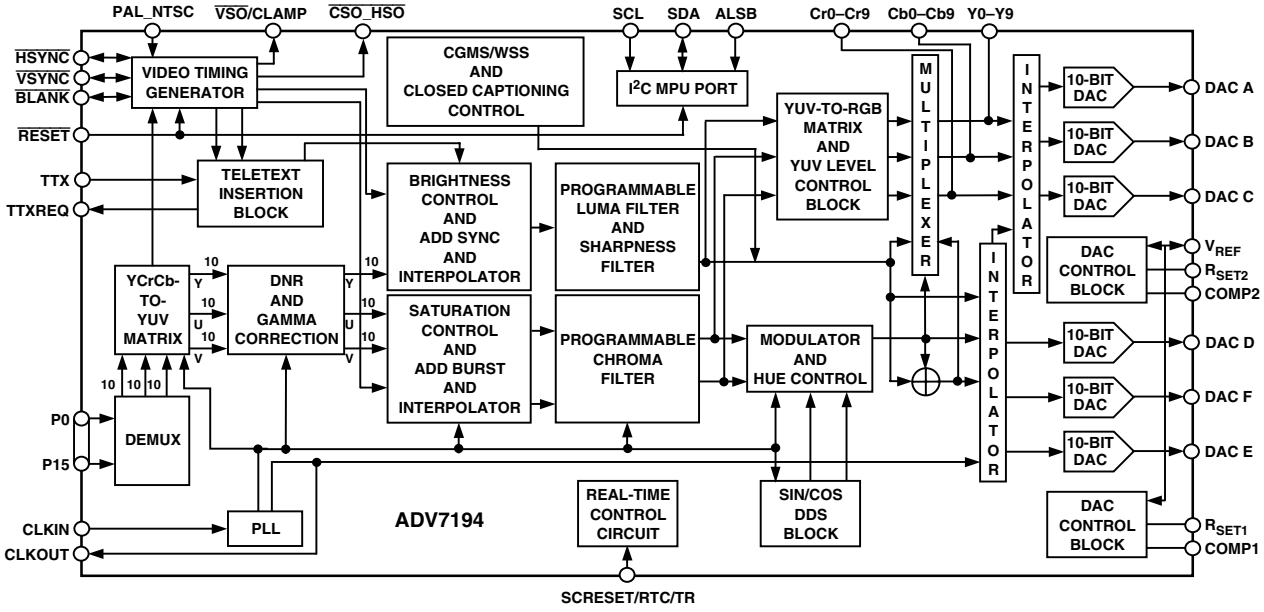


Figure 5. Detailed Functional Block Diagram

Digital noise reduction allows improved picture quality in removing low-amplitude, high-frequency noise. Figure 6 shows the DNR functionality in the two modes available.

Programmable gamma correction is also available. The figure below shows the response of different gamma values to a ramp input signal.

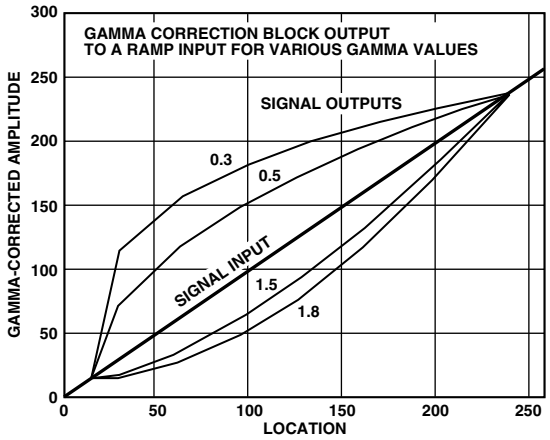


Figure 7. Signal Input (Ramp) and Selectable Gamma Output Curves

The device is driven by a 27 MHz clock. Data can be output at 27 MHz or 54 MHz (on-board PLL) when 4× oversampling is enabled. Also, the filter requirements in 4× oversampling and 2× oversampling differ, as can be seen in the figure below.

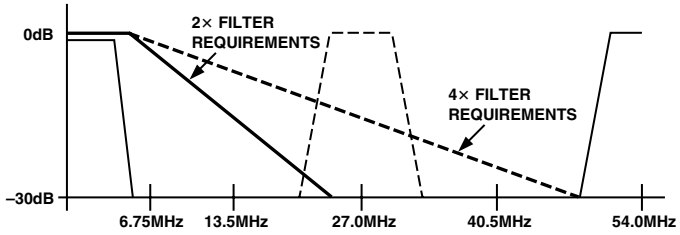


Figure 8. Output Filter Requirements in 2× and 4× Oversampling Mode

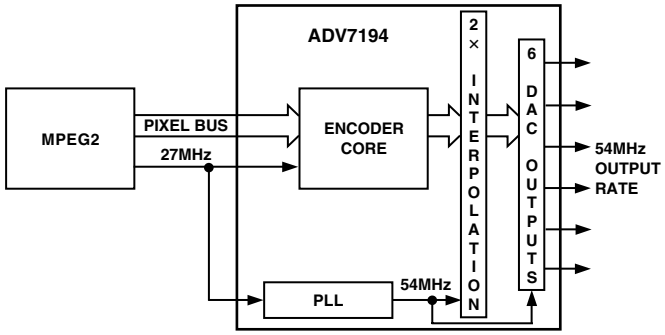


Figure 9. PLL and 4x Oversampling Block Diagram

The ADV7194 also supports both PAL and NTSC square pixel operation. In this case, the encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes or sleep modes.

The output video frames are synchronized with the incoming data timing reference codes. Optionally the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ and FIELD timing signals. These timing signals can be adjusted to change pulsewidth and position while the part is in master mode.

$\overline{\text{HSO/CSO}}$ and $\overline{\text{VSO}}$ TTL outputs are also available and are timed to the analog output video.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7194 also incorporates WSS and CGMS-A data control generation.

The ADV7194 modes are set up over a 2-wire serial bidirectional port (I^2C-compatible) with two slave addresses and the device is register-compatible with the ADV7172/ADV7173.

The ADV7194 is packaged in an 80-lead LQFP package.

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, N, and NTSC M, N modes, YCrCb 4:2:2 Data is input via the CCIR-656/601-compatible Pixel Port at a 27 MHz Data Rate. The Pixel Data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, Cr and Cb typically have a range of 128+/–112; however, it is possible to input data from 1 to 254 on both Y, Cb, and Cr. The ADV7194 supports PAL (B, D, G, H, I, N) and NTSC M, N (with and without Pedestal) and PAL60 standards.

Digital Noise Reduction can be applied to the Y signal. Programmable gamma correction can also be applied to the Y signal if required.

The Y data can be manipulated for contrast control and a setup level can be added for brightness control. The Cr, Cb data can be scaled to achieve color saturation control. All settings become effective at the start of the next field when double buffering is enabled.

The appropriate sync, blank and burst levels are added to the YCrCb data. Closed-Captioning and Teletext levels are also added to Y and the resultant data is interpolated to 54 MHz (4× Oversampling Mode). The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate Subcarrier Sine/Cosine waveforms and a phase offset may be added onto the color subcarrier during active video to allow hue adjustment. The resulting U and V signals are added together to make up the Chrominance Signal. The Luma (Y) signal can be delayed by up to six clock cycles (at 27 MHz) and the Chroma signal can be delayed by up to eight clock cycles (at 27 MHz).

The Luma and Chroma signals are added together to make up the Composite Video Signal. All timing signals are controlled.

The YCrCb data is also used to generate RGB data with appropriate sync and blank levels. The YUV levels are scaled to output the suitable SMPTE/EBU N10, MII, or Betacam levels.

Each DAC can be individually powered off if not required. A complete description of DAC output configurations is given in the Mode Register 2 section.

Video output levels are illustrated in Appendix 9.

When used to interface progressive scan systems, the ADV7194 allows input to YCrCb signals in Progressive Scan format (3 × 10 bit) before these signals are routed to the interpolation filters and the DACs.

INTERNAL FILTER RESPONSE

The Y Filter supports several different frequency responses including two low-pass responses, two notch responses, an Extended (SSAF) response with or without gain boost/attenuation, a CIF response and a QCIF response. The UV Filter supports several different frequency responses including five low-pass responses, a CIF response and a QCIF response, as can be seen in the following figures.

In Extended Mode there is the option of 12 responses in the range from –4 dB to +4 dB. The desired response can be chosen by the user by programming the correct value via the I^2C. The variation of frequency responses can be seen in the tables on the following pages.

For a more detailed filter specification, refer to Analog Devices' application note AN-562.

Table I. Luminance Internal Filter Specifications (4× Oversampling)

Filter Type	Filter Selection			Passband Ripple[1] (dB)	3 dB Bandwidth[2] (MHz)
	MR04	MR03	MR02		
Low-Pass (NTSC)	0	0	0	0.16	4.24
Low-Pass (PAL)	0	0	1	0.1	4.81
Notch (NTSC)	0	1	0	0.09	2.3/4.9/6.6
Notch (PAL)	0	1	1	0.1	3.1/5.6/6.4
Extended (SSAF)	1	0	0	0.04	6.45
CIF	1	0	1	0.127	3.02
QCIF	1	1	0	Monotonic	1.5

NOTES
[1]Passband Ripple is defined to be fluctuations from the 0 dB response in the passband, measured in (dB). The passband is defined to have 0–fc frequency limits for a low-pass filter, 0–f1 and f2–infinity for a notch filter, where fc, f1, f2 are the –3 dB points.
[2]3 dB bandwidth refers to the –3 dB cutoff frequency.

Table II. Chrominance Internal Filter Specifications (4× Oversampling)

Filter Type	Filter Selection			Passband Ripple[1] (dB)	3 dB Bandwidth[2] (MHz)
	MR07	MR06	MR05		
1.3 MHz Low-Pass	0	0	0	0.09	1.395
0.65 MHz Low-Pass	0	0	1	Monotonic	0.65
1.0 MHz Low-Pass	0	1	0	Monotonic	1.0
2.0 MHz Low-Pass	0	1	1	0.048	2.2
3.0 MHz Low-Pass	1	1	1	Monotonic	3.2
CIF	1	0	1	Monotonic	0.65
QCIF	1	1	0	Monotonic	0.5

NOTES
[1]Passband Ripple is defined to be fluctuations from the 0 dB response in the passband, measured in (dB). The passband is defined to have 0–fc frequency limits for a low-pass filter, 0–f1 and f2–infinity for a notch filter, where fc, f1, f2 are the –3 dB points.
[2]3 dB bandwidth refers to the –3 dB cutoff frequency.

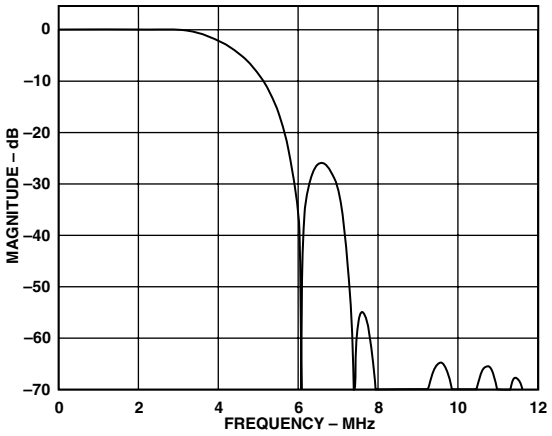


Figure 10. NTSC Low-Pass Luma Filter

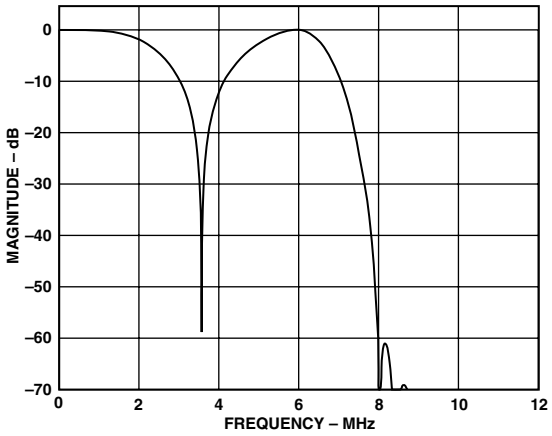


Figure 13. NTSC Notch Luma Filter

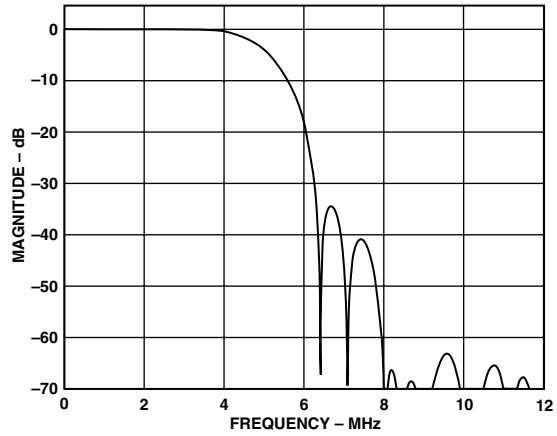


Figure 11. PAL Low-Pass Luma Filter

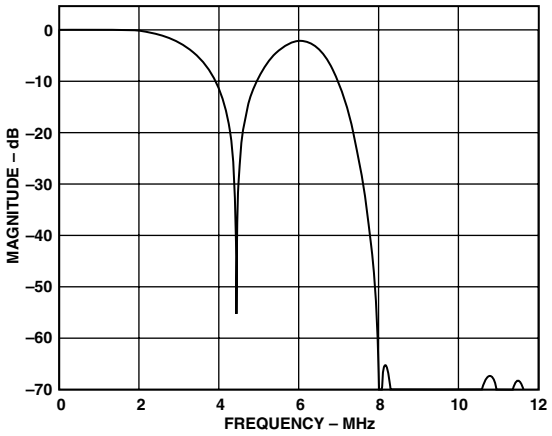


Figure 14. PAL Notch Luma Filter

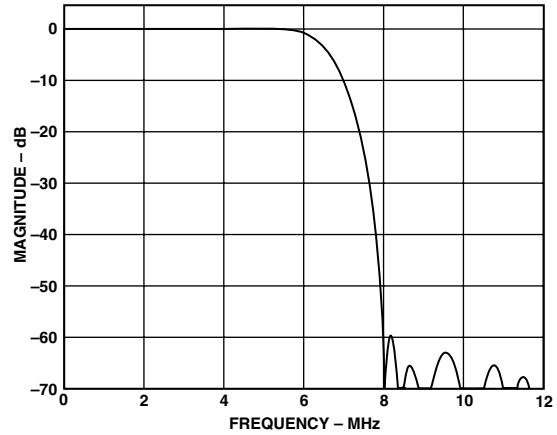


Figure 12. Extended Mode (SSAF) Luma Filter

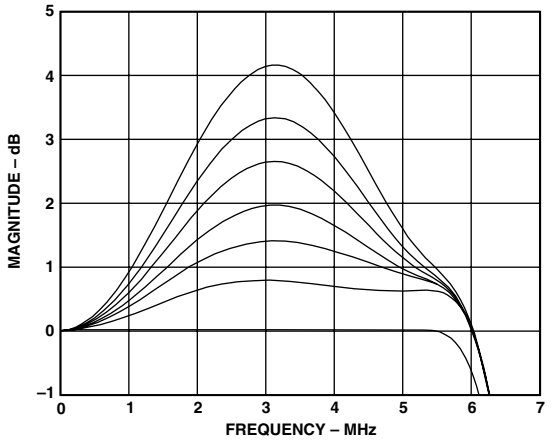


Figure 15. Extended SSAF and Programmable Gain, Showing Range 0 dB/4 dB

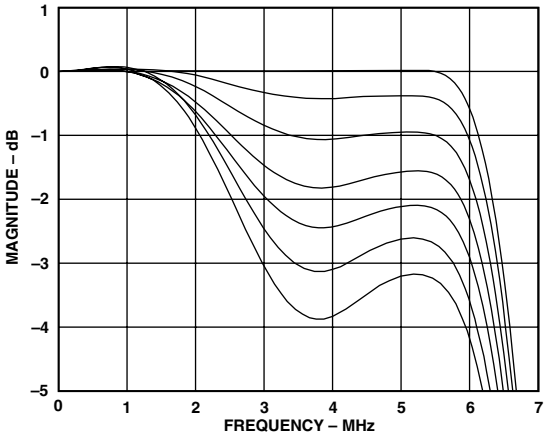


Figure 16. Extended SSAF and Programmable Attenuation, Showing Range 0 dB/–4 dB

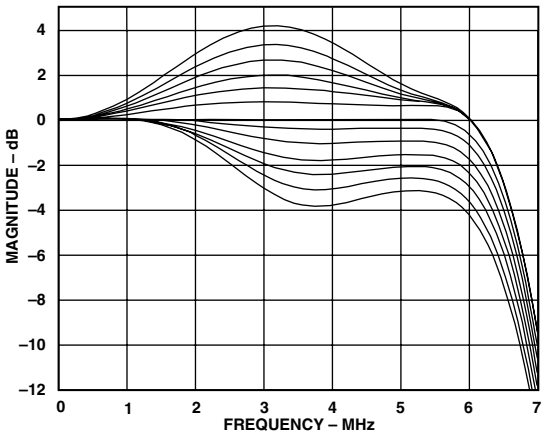


Figure 19. Extended SSAF and Programmable Gain/ Attenuation, Showing Range +4 dB/–12 dB

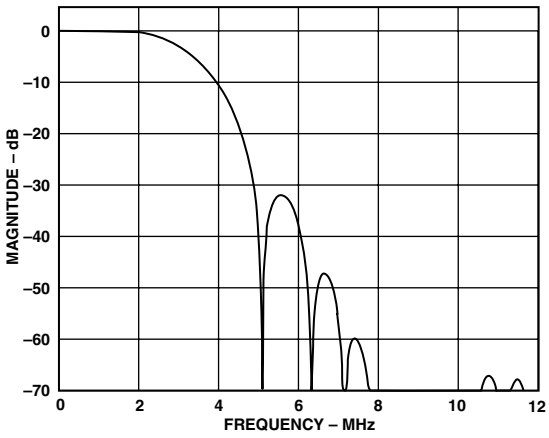


Figure 17. Luma CIF Filter

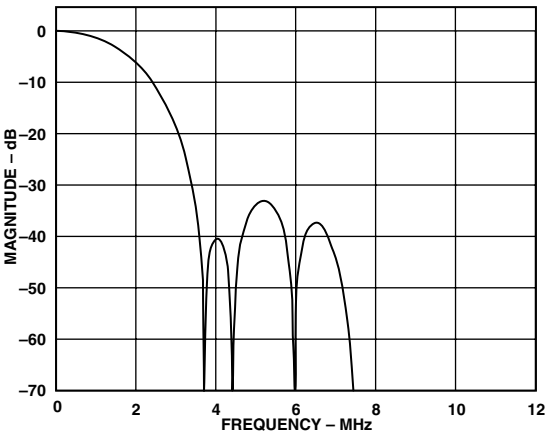


Figure 20. Luma QCIF Filter

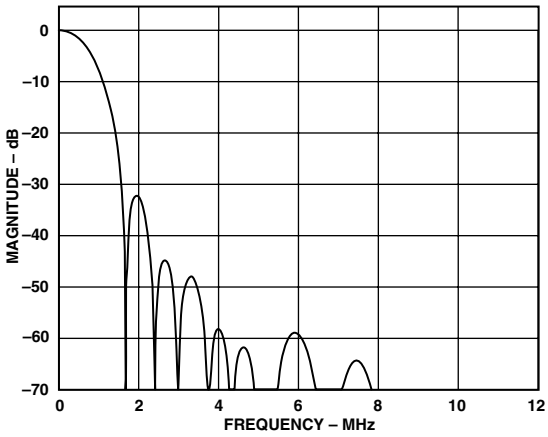


Figure 18. Chroma 0.65 MHz Low-Pass Filter

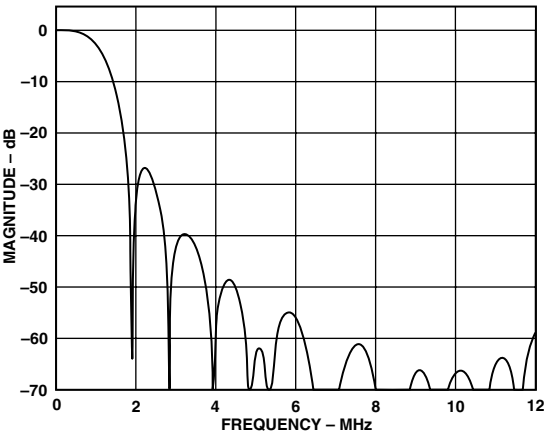


Figure 21. Chroma 1 MHz Low-Pass Filter

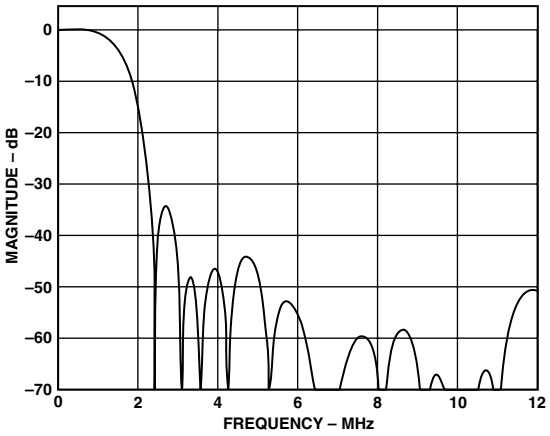


Figure 22. Chroma 1.3 MHz Low-Pass Filter

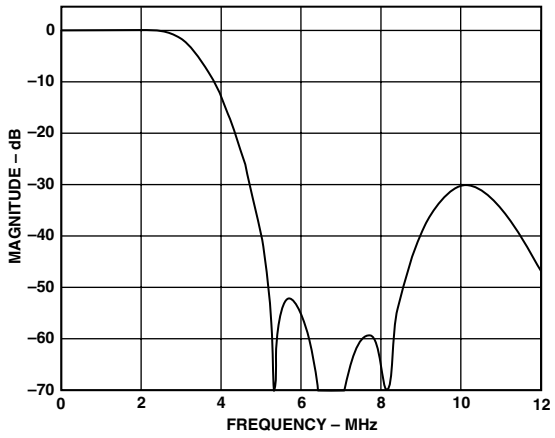


Figure 23. Chroma 3 MHz Low-Pass Filter

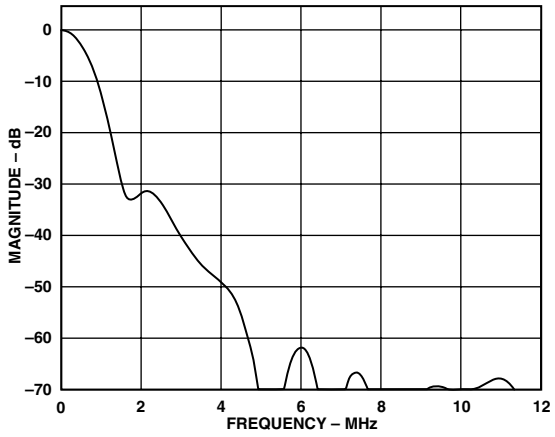


Figure 24. Chroma QCIF Filter

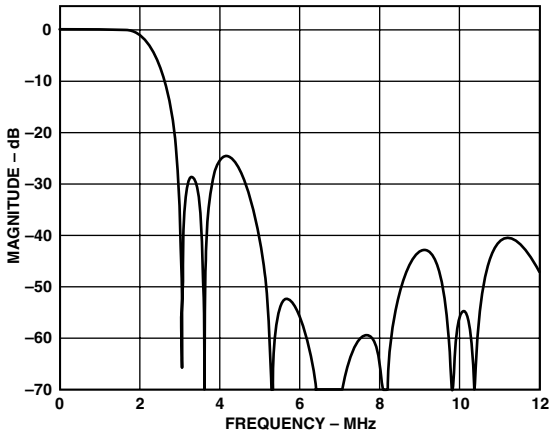


Figure 25. Chroma 2 MHz Low-Pass Filter

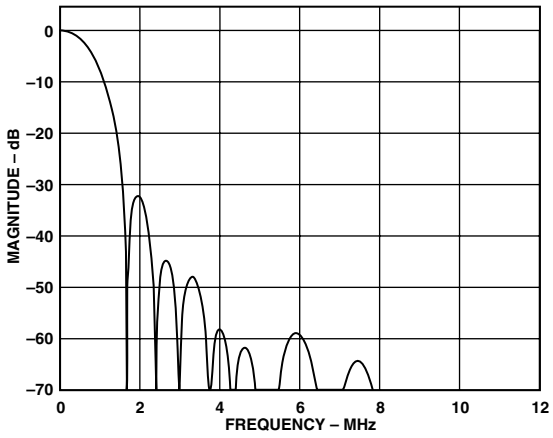


Figure 26. Chroma CIF Filter

FEATURES—FUNCTIONAL DESCRIPTION

BLACK BURST OUTPUT

It is possible to output a black burst signal from two DACs. This signal output is very useful for professional video equipment since it enables two video sources to be locked together. (Mode Register 9.)

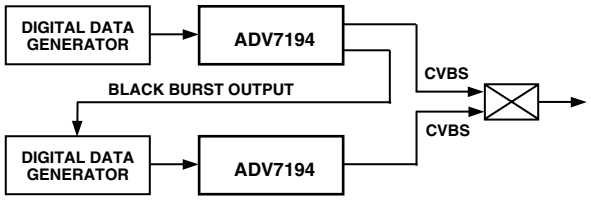


Figure 27. Possible Application for the Black Burst Output Signal

BRIGHTNESS DETECT

This feature is used to monitor the average brightness of the incoming Y video signal on a field by field basis. The information is read from the I^2C and based on this information the color saturation, contrast and brightness controls can be adjusted (for example to compensate for very dark pictures). (Brightness Detect Register.)

CHROMA/LUMA DELAY

The luminance data can be delayed by maximum of six clock cycles. Additionally the Chroma can be delayed by a maximum of eight clock cycles (one clock cycle at 27 MHz). (Timing Register 0 and Mode Register 9.)

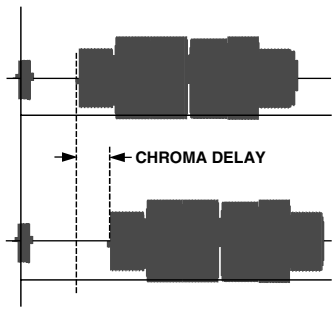


Figure 28. Chroma Delay

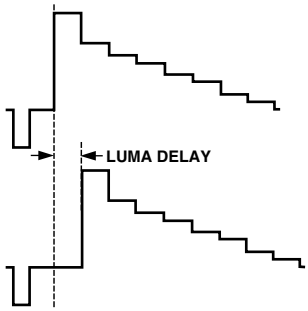


Figure 29. Luma Delay

CLAMP OUTPUT

The ADV7194 has a programmable clamp TTL output signal. This clamp signal is programmable to the front and back porch. The clamp signal can be varied by one to three clock cycles in a positive and negative direction from the default position. (Mode Register 5, Mode Register 7.)

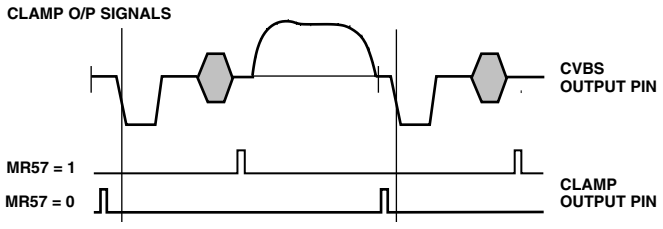


Figure 30. Clamp Output Timing

$\overline{CSO}$, $\overline{HSO}$, AND $\overline{VSO}$ OUTPUTS

The ADV7194 supports three output timing signals, $\overline{CSO}$ (composite sync signal), $\overline{HSO}$ (Horizontal Sync Signal) and $\overline{VSO}$ (Vertical Sync Signal). These output TTL signals are aligned with the analog video outputs. See Figure 31 for an example of these waveforms. (Mode Register 7.)

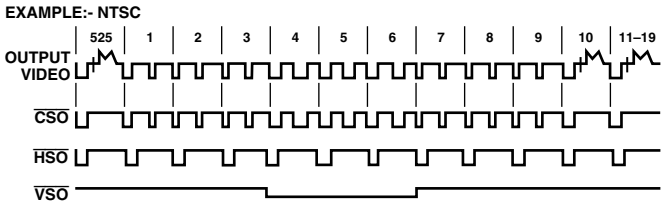


Figure 31. $\overline{CSO}$, $\overline{HSO}$, $\overline{VSO}$ Timing Diagram

COLOR BAR GENERATION

The ADV7194 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 color bars for PAL. (Mode Register 4.)

COLOR BURST SIGNAL CONTROL

The burst information can be switched on and off the composite and chroma video output. (Mode Register 4.)

COLOR CONTROLS

The ADV7194 allows the user to control the brightness, contrast, hue and saturation of the color. The control registers may be double-buffered, meaning that any modification to the registers will be done outside the active video region and, therefore, changes made will not be visible during active video.

Contrast Control

Contrast adjustment is achieved by scaling the Y input data by a factor programmed by the user. This factor allows the data to be scaled between 0% and 150%. (Contrast Control Register.)

Brightness Control

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the Y data. For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and PAL, the setup can vary from –7.5 IRE to +15 IRE. (Brightness Control Register.)

Color Saturation

Color adjustment is achieved by scaling the Cr and Cb input data by a factor programmed by the user. This factor allows the data to be scaled between 0% and 200%. (U Scale Register and V Scale Register.)

Hue Adjust Control

The hue adjustment is achieved on the composite and chroma outputs by adding a phase offset onto the color subcarrier in the active video but leaving the color burst unmodified, i.e., only the phase between the video and the colorburst is modified and hence the hue is shifted. The ADV7194 provides a range of ±22° in increments of 0.17578125°. (Hue Adjust Register.)

CHROMINANCE CONTROL

The color information can be switched on and off the composite, chroma and color component video outputs. (Mode Register 4.)

UNDERSHOOT LIMITER
A limiter is placed after the digital filters. This prevents any synchronization problems for TVs. The level of undershoot is programmable between –1.5 IRE, –6 IRE, –11 IRE when operating in 4× Oversampling Mode. In 2× Oversampling Mode the limits are –7.5 IRE and 0 IRE. (Mode Register 9 and Timing Register 0.)

DIGITAL NOISE REDUCTION
DNR is applied to the Y data only. A filter block selects the high frequency, low-amplitude components of the incoming signal (DNR Input Select). The absolute value of the filter output is compared to a programmable threshold value (DNR Threshold Control). There are two DNR modes available: DNR Mode and DNR Sharpness Mode.

In DNR Mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount (Coring Gain Control) of this noise signal will be subtracted from the original signal.

In DNR Sharpness Mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise, as before. Otherwise, if the level exceeds the threshold, now being identified as a valid signal, a fraction of the signal (Coring Gain Control) will be added to the original signal in order to boost high frequency components and to sharpen the video image.

In MPEG systems it is common to process the video information in blocks of 8 × 8 pixels for MPEG2 systems, or 16 × 16 pixels for MPEG1 systems (Block Size Control). DNR can be applied to the resulting block transition areas that are known to contain noise. Generally the block transition area contains two pixels. It is possible to define this area to contain four pixels (Border Area Control).

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the Block Offset Control. (Mode Register 8, DNR Registers 0–2.)

DOUBLE BUFFERING
Double buffering can be enabled or disabled on the following registers: Closed Captioning Registers, Brightness Control Register, V-Scale Register, U-Scale Register, Contrast Control Register, Hue Adjust Register, and the Gamma Curve Select bit. These registers are updated once per field on the falling edge of the $\overline{\text{VSYNC}}$ signal. Double Buffering improves the overall performance of the ADV7194, since modifications to register settings will not be made during active video, but take effect on the start of the active video. (Mode Register 8.)

GAMMA CORRECTION CONTROL
Gamma correction may be performed on the luma data. The user has the choice to use either of two different gamma curves, A or B. At any one time one of these curves is operational if gamma correction is enabled. Gamma correction allows the mapping of the luma data to a user-defined function. (Mode Register 8, Gamma Correction Registers 0–13.)

NTSC PEDESTAL CONTROL
In NTSC mode it is possible to have the pedestal signal generated on the output video signal. (Mode Register 2.)

POWER-ON $\overline{\text{RESET}}$
After power-up, it is necessary to execute a $\overline{\text{RESET}}$ operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the data on the pixel inputs pins is ignored. See Appendix 8 for the register settings after $\overline{\text{RESET}}$ is applied.

PROGRESSIVE SCAN INPUT
It is possible to input data to the ADV7194 in progressive scan format. For this purpose the input pins Y0/P10–Y9/P19, Cr0–Cr9, Cb0–Cb9 accept 10-bit Y data, 10-bit Cb data and 10-bit Cr data. The data is clocked into the part at 27 MHz. The data is then filtered and sinc corrected in an 2× Interpolation filter and then output to three video DACs at 54 MHz (to interface to a progressive scan monitor).

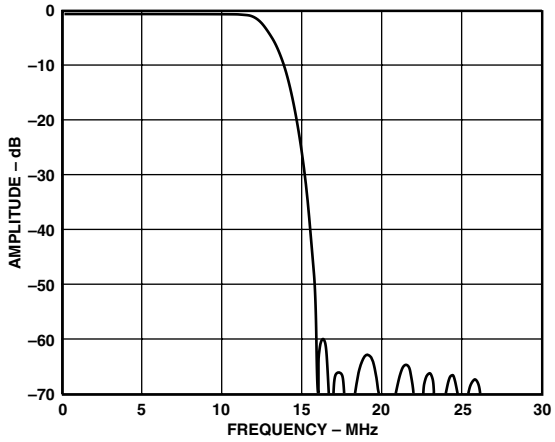


Figure 32. Plot of the Interpolation Filter for the Y Data

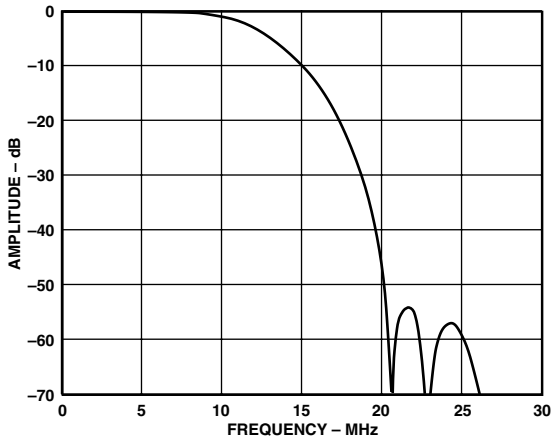


Figure 33. Plot of the Interpolation Filter for the CrCb Data

It is assumed that there is no color space conversion or any other such operation to be performed on the incoming data. Thus if these DAC outputs are to drive a TV, all relevant timing and synchronization data should be contained in the incoming digital Y data. An FPGA can be used to achieve this.

The block diagram below shows a possible configuration for progressive scan mode using the ADV7194.

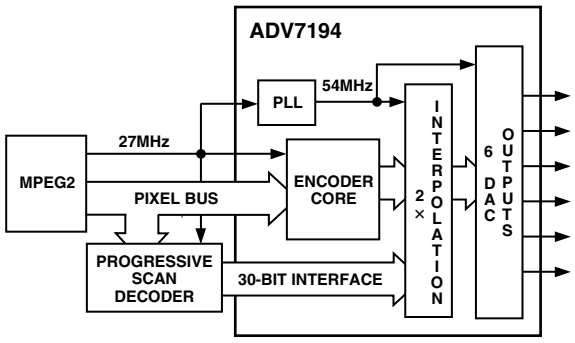


Figure 34. Block Diagram Using the ADV7194 in Progressive Scan Mode

The progressive scan decoder deinterlaces the data from the MPEG2 decoder. This now means that there are 525 video lines per field in NTSC mode and 625 video lines per field in PAL mode. The duration of the video line is now 32 µs.

It is important to note that the data from the MPEG2 decoder is in 4:2:2 format. The data output from the progressive scan decoder is in 4:4:4 format. Thus it is assumed that some form of interpolation on the color component data is performed in the progressive scan decoder IC. (Mode Register 8.)

REAL-TIME CONTROL, SUBCARRIER RESET AND TIMING RESET

Together with the SCRESET/RTC/TR pin and of Mode Register 4 (Genlock Control), the ADV7194 can be used in (a) Timing Reset Mode, (b) Subcarrier Phase Reset Mode or (c) RTC Mode.

(a) A TIMING RESET is achieved in holding this pin high. In this state the horizontal and vertical counters will remain reset. On releasing this pin (set to low), the internal counters will commence counting again. The minimum time the pin has to be held high is 37 ns (1 clock cycle at 27 MHz), otherwise the reset signal might not be recognized.

(b) The SUBCARRIER PHASE will reset to that of Field 0 at the start of the following field when a low to high transition occurs on this input pin.

(c) In RTC MODE, the ADV7194 can be used to lock to an external video source.

The real-time control mode allows the ADV7194 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device that outputs a digital datastream in the RTC format (such as an ADV7185 video decoder, see Figure 37), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital datastream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00Hex should be written into all four Subcarrier Frequency registers when using this mode. It is recommended to use the ADV7185 in this mode (Mode Register 4.)

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four (NTSC) or eight (PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but, in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7194 is configured in RTC mode. Under these conditions (unstable video) the Subcarrier Phase Reset should be enabled but no reset applied. In this configuration the SCH Phase will never be reset; this means that the output video will now track the unstable input video. The Subcarrier Phase Reset when applied will reset the SCH phase to Field 0 at the start of the next field (e.g., Subcarrier Phase Reset applied in Field 5 (PAL) on the start of the next field SCH phase will be reset to Field 0). (Mode Register 4.)

SLEEP MODE

If, after $\overline{\text{RESET}}$, the SCRESET/RTC/TR and NTSC_PAL pins are both set high, the ADV7194 will power-up in Sleep Mode to facilitate low-power consumption before all registers have been initialized.

If Power-up in Sleep Mode is disabled, Sleep Mode control passes to the Sleep Mode control in Mode Register 2 (i.e., control via I^2C). (Mode Register 2 and Mode Register 6.)

SQUARE PIXEL MODE

The ADV7194 can be used to operate in square pixel mode. For NTSC operation an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation. Square pixel mode is not available in 4× Oversampling mode. (Mode Register 2.)

VERTICAL BLANKING DATA INSERTION AND $\overline{\text{BLANK}}$ INPUT

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not have line sync or pre-/post-equalization pulses. This mode of operation is called *Partial Blanking*. It allows the insertion of any VBI data (Opened VBI) into the encoded output waveform, this data is present in digitized incoming YCbCr data stream (e.g., WSS data, CGMS, VPS etc.). Alternatively the entire VBI may be blanked (no VBI data inserted) on these lines. VBI is available in all timing modes.

It is possible to allow control over the $\overline{\text{BLANK}}$ signal using Timing Register 0. When the $\overline{\text{BLANK}}$ input is enabled (TR03 = 0 and input pin tied low), the $\overline{\text{BLANK}}$ input can be used to input externally generated blank signals in Slave Mode 1, 2, or 3. When the $\overline{\text{BLANK}}$ input is disabled (TR03 = 1 and input pin tied low or tied high) the $\overline{\text{BLANK}}$ input is not used and the ADV7194 automatically blanks all normally blank lines as per CCIR-624. (Timing Register 0.)

YUV LEVELS

This functionality allows the ADV7194 to output SMPTE levels or Betacam levels on the Y output when configured in PAL or NTSC mode.

	Sync	Video
Betacam	286 mV	714 mV
SMPTE	300 mV	700 mV
MII	300 mV	700 mV

As the data path is branched at the output of the filters the luma signal relating to the CVBS or S-Video Y/C output is unaltered. It is only the Y output of the YCrCb outputs that is scaled. This control allows color component levels to have a peak-peak amplitude of 700 mV, 1000 mV or the default values of 934 mV in NTSC and 700 mV in PAL. (Mode Register 5.)

20-/16-BIT INTERFACE

It is possible to input data in 20-bit or 16-bit format. In this case, the interface only operates if the data is accompanied by separate $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$/$\overline{\text{BLANK}}$ signals. Twenty-bit or 16-bit mode is not available in Slave Mode 0 since EAV/SAV timing codes are used. (Mode Register 8.)

4× OVERSAMPLING AND INTERNAL PLL

It is possible to operate all six DACs at 27 MHz (2× Oversampling) or 54 MHz (4× Oversampling).

The ADV7194 is supplied with a 27 MHz clock synced with the incoming data. Two options are available: to run the device throughout at 27 MHz or to enable the PLL. In the latter case, even if the incoming data runs at 27 MHz, 4× Oversampling and the internal PLL will output the data at 54 MHz.

NOTE

In 4× Oversampling Mode the requirements for the optional output filters are different than from those in 2× Oversampling. (Mode Register 1, Mode Register 6.)

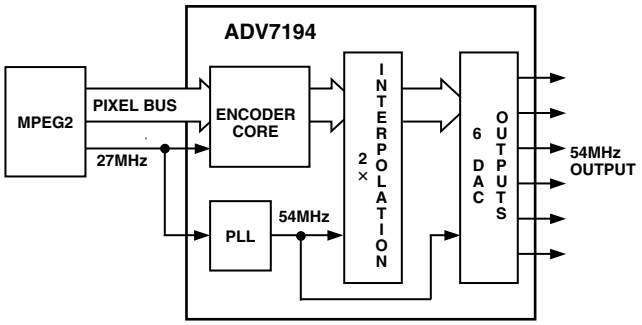


Figure 35a. PLL and 4× Oversampling Block Diagram

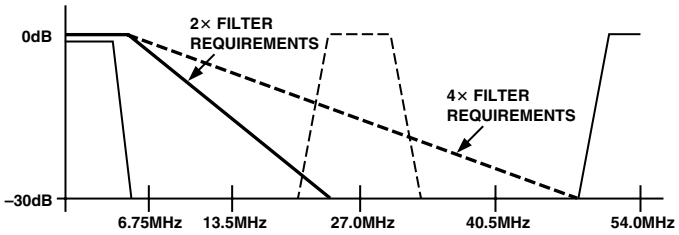


Figure 35b. Output Filter Requirements in 4× Oversampling Mode

VIDEO TIMING DESCRIPTION

The ADV7194 is intended to interface to off-the-shelf MPEG1 and MPEG2 Decoders. As a consequence, the ADV7194 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 Pixel Port and has several Video Timing Modes of operation that allow it to be configured as either System Master Video Timing Generator or a Slave to the System Video Timing Generator. The ADV7194 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7194 calculates the width and placement of analog sync pulses, blanking levels, and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalization pulses are inserted where required.

In addition, the ADV7194 supports a PAL or NTSC square pixel operation. The part requires an input pixel clock of 24.5454 MHz for NTSC square pixel operation and an input pixel clock of 29.5 MHz for PAL square pixel operation. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7194 has four distinct Master and four distinct Slave timing configurations. Timing Control is established with the bidirectional $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and $\overline{\text{VSYNC}}$ pins. Timing Register 1 can also be used to vary the timing pulsewidths and where they occur in relation to each other. (Mode Register 2, Timing Register 0, 1.)

$\overline{\text{RESET}}$ SEQUENCE

When $\overline{\text{RESET}}$ becomes active the ADV7194 reverts to the default output configuration (see Appendix for register settings). The ADV7194 internal timing is under the control of the logic level on the NTSC_PAL pin.

When $\overline{\text{RESET}}$ is released Y, Cr, Cb values corresponding to a black screen are input to the ADV7194. Output timing signals are still suppressed at this stage. DACs A, B, C are switched off and DACs D, E, F are switched on.

When the user requires valid data, Pixel Data Valid Control is enabled (MR26 = 1) to allow the valid pixel data to pass through the encoder. Digital output timing signals become active and the encoder timing is now under the control of the Timing Registers. If at this stage, the user wishes to select a different video standard to that on the NTSC_PAL pin, Standard I^2C Control should be enabled (MR25 = 1) and the video standard required is selected by programming Mode Register 0 (Output Video Standard Selection). Figure 36 illustrates the $\overline{\text{RESET}}$ sequence timing.

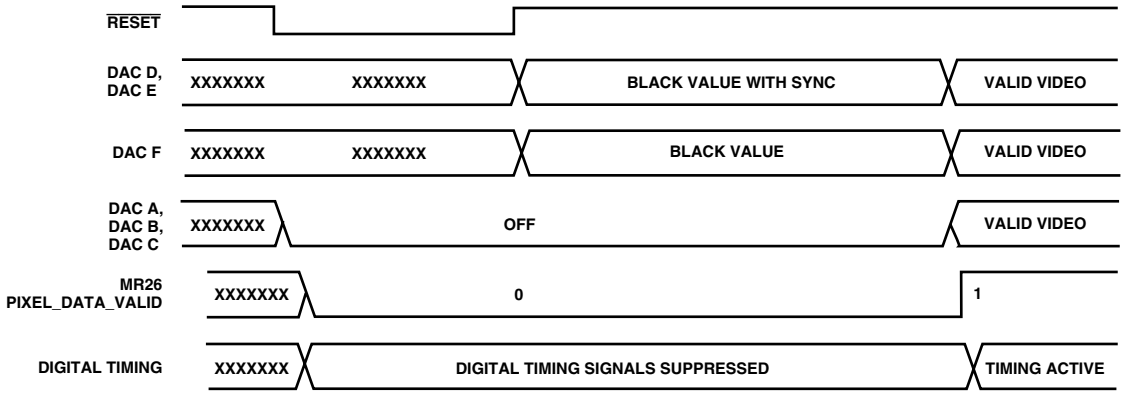
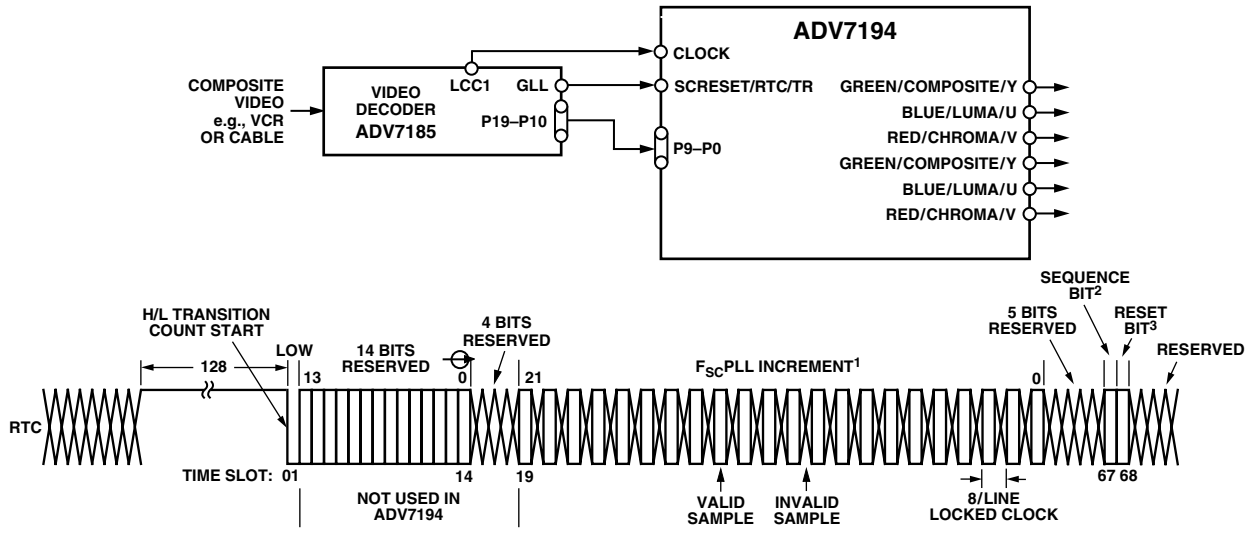


Figure 36. $\overline{RESET}$ Sequence Timing Diagram



NOTES:
[1]F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7194 FSC DDS REGISTER IS FSC PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7194.
[2]SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
[3]RESET BIT
RESET ADV7194's DDS

Figure 37. RTC Timing and Connections

Mode 0 (CCIR–656): Slave Option
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7194 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 38. The $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode. Blank output is available.

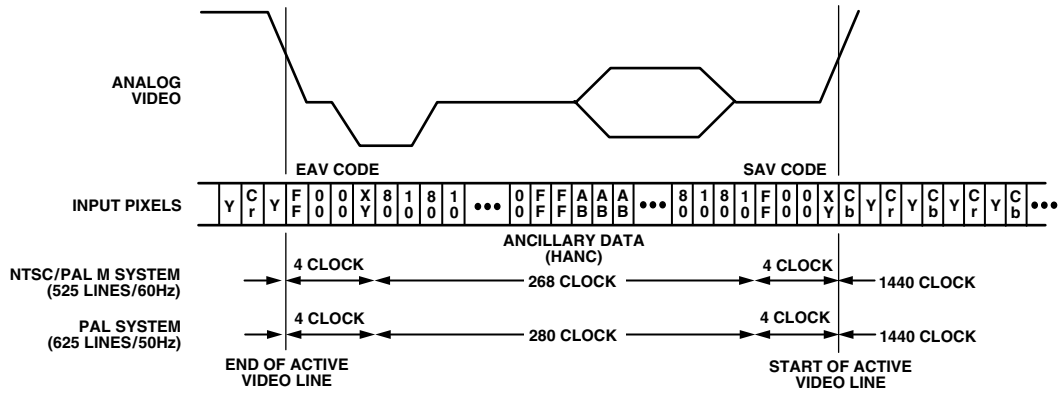


Figure 38. Timing Mode 0, Slave Mode

Mode 0 (CCIR–656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7194 generates H, V, and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the $\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 39 (NTSC) and Figure 40 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 41.

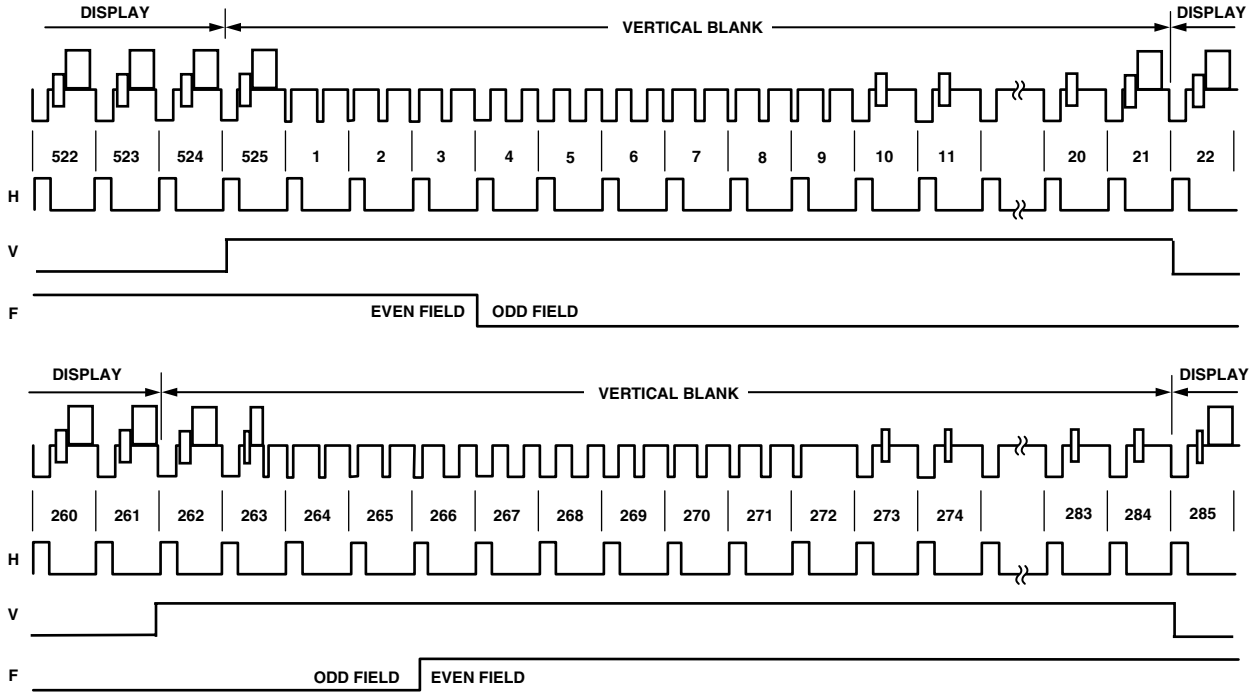


Figure 39. Timing Mode 0, NTSC Master Mode

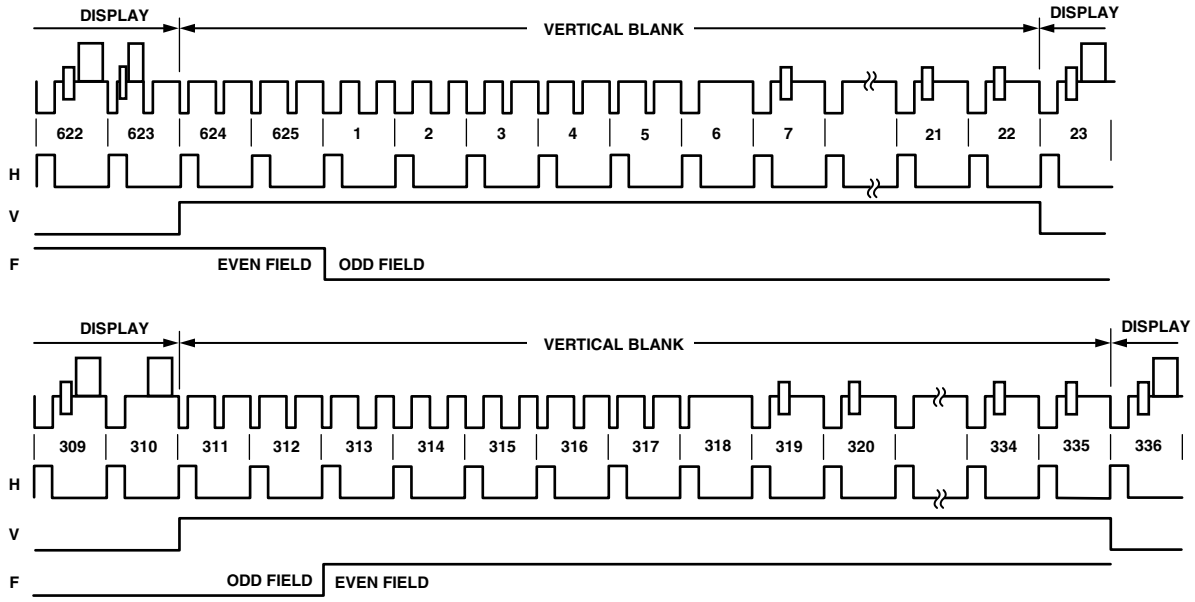


Figure 40. Timing Mode 0, PAL Master Mode

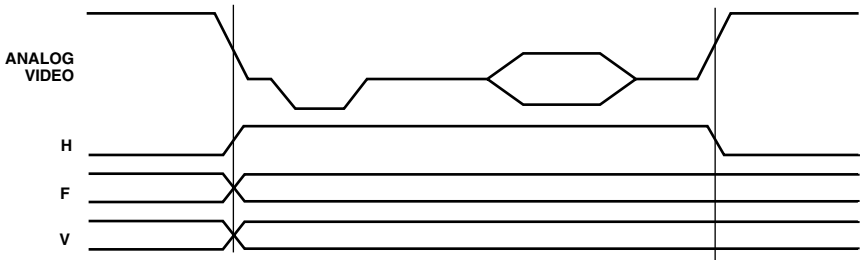


Figure 41. Timing Mode 0 Data Transitions, Master Mode

Mode 1: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7194 accepts Horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7194 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 42 (NTSC) and Figure 43 (PAL).

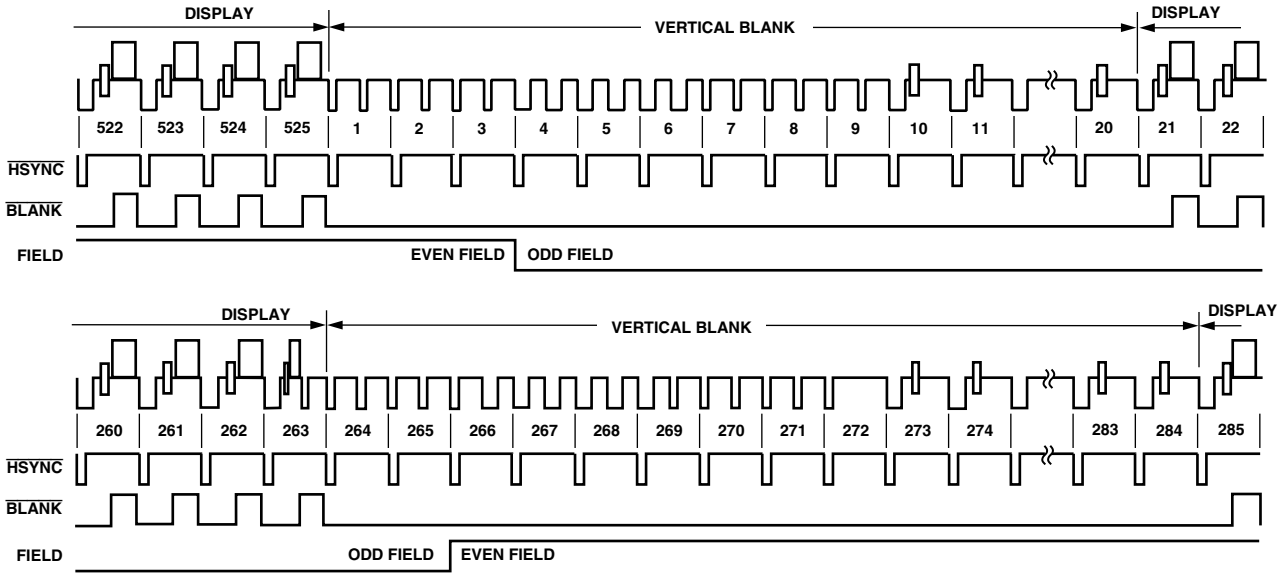


Figure 42. Timing Mode 1, NTSC

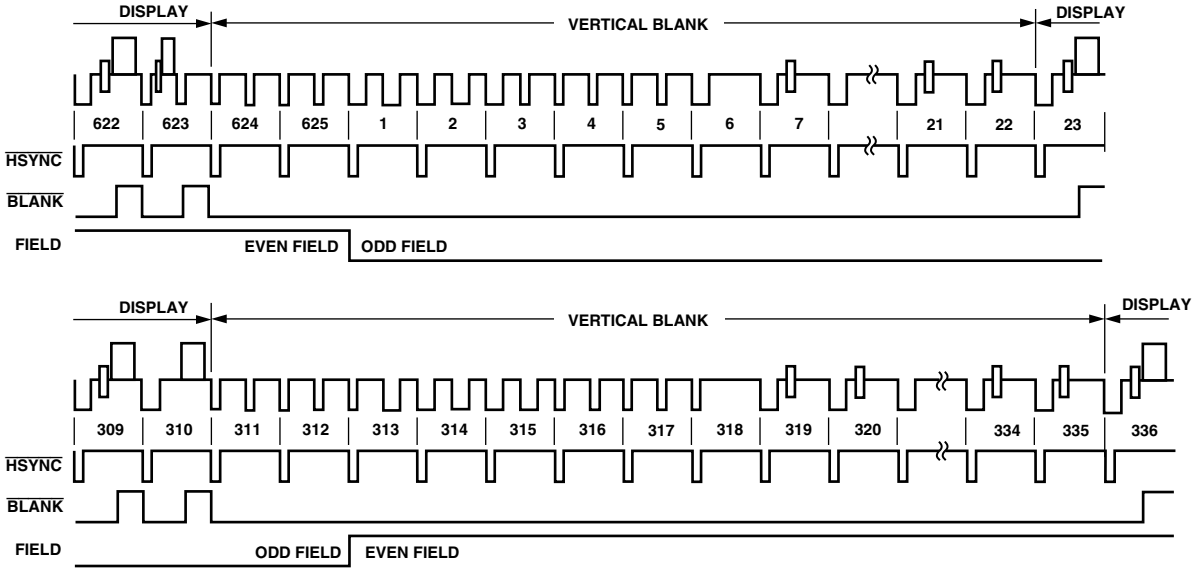


Figure 43. Timing Mode 1, PAL