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FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling per channel for CVBS, Y/C, and YPrPb modes
- ADV7282:** 4 analog video input channels with on-chip antialiasing filter
- ADV7282-M:** 6 analog video input channels with on-chip antialiasing filter
- Video input support for CVBS (composite), Y/C (S-Video), and YPrPb (component)
- Fully differential, pseudo differential, and single-ended CVBS video input support
- NTSC/PAL/SECAM autodetection
- Short-to-battery (STB) diagnostics on 2 video inputs
- Up to 4 V common-mode input range solution
- Excellent common-mode noise rejection capabilities
- 5-line adaptive 2D comb filter and CTI video enhancement
- Adaptive Digital Line Length Tracking (ADLLT), signal processing, and enhanced FIFO management provide mini-time base correction (TBC) functionality
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Fast switching capability
- Integrated interlaced-to-progressive (I2P) video output converter (deinterlacer)
- Adaptive contrast enhancement (ACE)
- Down dither (8-bit to 6-bit)
- Rovi (Macrovision) copy protection detection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output (**ADV7282**)
- MIPI CSI-2 output interface (**ADV7282-M** only)
- Full featured vertical blanking interval (VBI) data slicer with world system teletext (WST) support
- Power-down mode available
- 2-wire, I²C-compatible serial interface
- Qualified for automotive applications
- −40°C to +105°C temperature grade
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

APPLICATIONS

- Smartphone/multimedia handsets
- Automotive infotainment
- DVRs for video security
- Media players

GENERAL DESCRIPTION

The **ADV7282/ADV7282-M** are versatile one-chip, multiformat video decoders. The **ADV7282/ADV7282-M** automatically detects standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The **ADV7282** converts the analog video signals into a YCrCb 4:2:2 video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The **ADV7282-M** converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a mobile industry processor interface (MIPI®) CSI-2 interface.

The analog video inputs of the **ADV7282/ADV7282-M** accept single-ended, pseudo differential, and fully differential signals.

The **ADV7282/ADV7282-M** contain a deinterlacer (I2P converter) and short to battery detection capability with two STB diagnostic pins. The **ADV7282** provides four analog inputs. The **ADV7282-M** provides six analog inputs and three general-purpose outputs.

The **ADV7282/ADV7282-M** are programmed via a 2-wire, serial bidirectional port (I²C compatible) and is fabricated in a 1.8 V CMOS process. The **ADV7282/ADV7282-M** are provided in space-saving, RoHS compliant LFCSP surface-mount packages.

The **ADV7282/ADV7282-M** are rated over the −40°C to +105°C temperature range. This makes the **ADV7282/ADV7282-M** ideal for automotive applications.

ADV7282* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADV7282EBZ Evaluation Board
- ADV7282MEBZ Evaluation Board

DOCUMENTATION

Application Notes

- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers
- AN-1337: Design Considerations for Connecting Analog Devices Video Decoders to MIPI CSI-2 Receivers

Data Sheet

- ADV7282: 10-Bit, 4× Oversampled SDTV Video Decoder with Differential Inputs and Deinterlacer Data Sheet

User Guides

- UG-637: ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features

TOOLS AND SIMULATIONS

- ADV7282 IBIS Model
- ADV7282M IBIS Model

DESIGN RESOURCES

- ADV7282 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

3/14—Rev. A to Rev. B

Changes to General Description	1
Change to Single CVBS Input, Analog Supply Current, Power Requirements Parameter, Table 1	4
Changes to Table 7	10
Changes to Theory of Operation Section	13
Changes to D _{VDDIO} Supply Voltage Section	15
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11/13—Rev. 0 to Rev. A

Changes to Features Section and General Description Section ..	1
Added Figure 1; Renumbered Sequentially	3
Changes to Table 1	4
Added Pixel Port Timing Specifications (ADV7282 Only) Section	9

Added Endnote 1; Table 7	10
Added Figure 6 and Table 9	11
Changes to Theory of Operation Section	13
Changes to D _{VDDIO} Supply Voltage Section	15
Changes to Table 12	17
Changes to Programming the STB Diagnostic Function Section	18
Added ITU-R BT.656 Tx Configuration (ADV7282 Only) Section	22
Changes to Register Maps Section	25
Changes to Power Supply Decoupling Section and Digital Outputs Section	27
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Changes to Ordering Guide	30

8/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

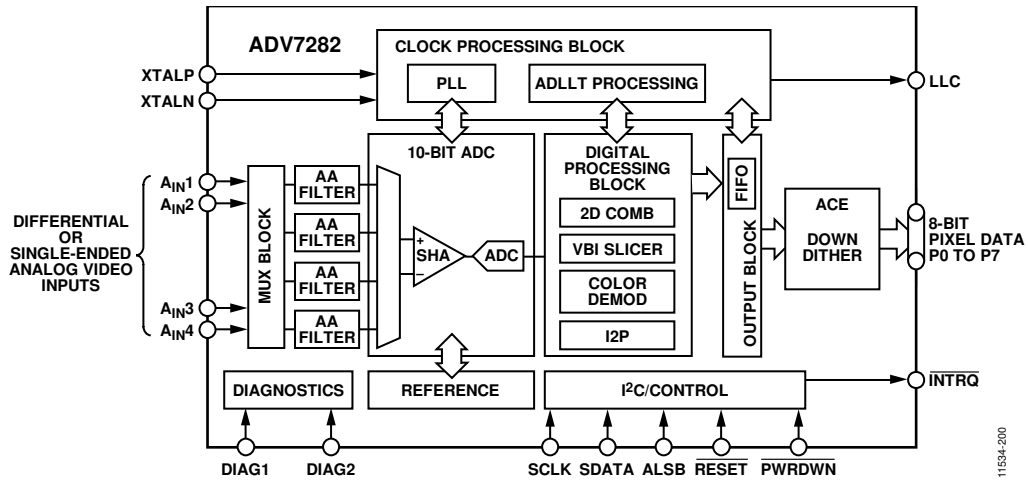


Figure 1. ADV7282 Functional Block Diagram

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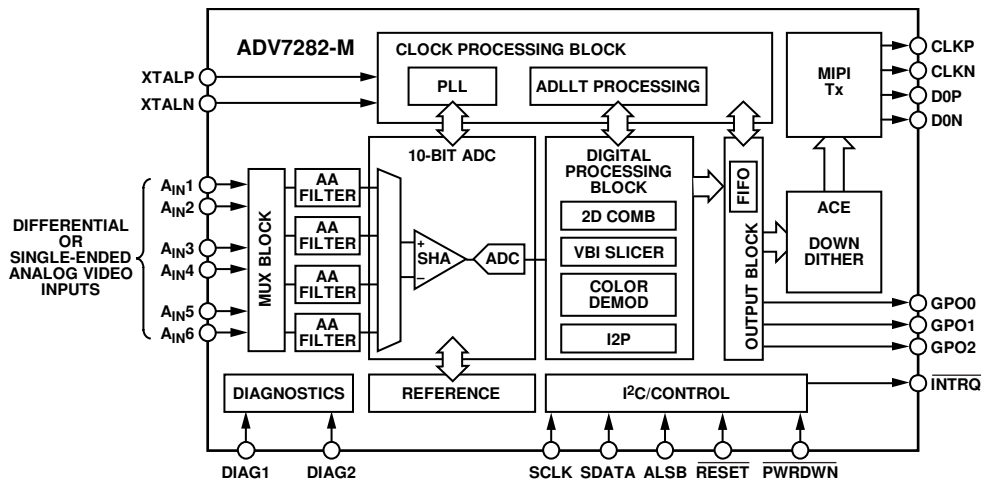


Figure 2. ADV7282-M Functional Block Diagram

11534-001

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

A_{VDD} , D_{VDD} , P_{VDD} , and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Note that M_{VDD} only applies to the [ADV7282-M](#).

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
ADC Resolution	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	$D_{VDDIO} = 3.3\text{ V}$ $D_{VDDIO} = 1.8\text{ V}$, ADV7282 only	2 1.2			V V
Input Low Voltage	V_{IL}	$D_{VDDIO} = 3.3\text{ V}$ $D_{VDDIO} = 1.8\text{ V}$, ADV7282 only			0.8 0.4	V V
Input Leakage Current	I_{IN}	RESET pin SDATA, SCLK pins PWRDWN, ALSB pins	-10 -10 -10		+10 +15 +50	μA μA μA
Input Capacitance	C_{IN}				10	pF
CRYSTAL INPUT						
Input High Voltage	V_{IH}	XTALN pin	1.2			V
Input Low Voltage	V_{IL}	XTALN pin			0.4	V
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	$D_{VDDIO} = 3.3\text{ V}$, $I_{SOURCE} = 0.4\text{ mA}$ $D_{VDDIO} = 1.8\text{ V}$, $I_{SOURCE} = 0.4\text{ mA}$, ADV7282 only	2.4 1.4			V V
Output Low Voltage	V_{OL}	$D_{VDDIO} = 3.3\text{ V}$, $I_{SINK} = 3.2\text{ mA}$ $D_{VDDIO} = 1.8\text{ V}$, $I_{SINK} = 1.6\text{ mA}$, ADV7282 only			0.4 0.2	V V
High Impedance Leakage Current	I_{LEAK}				10	μA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS ^{1, 2, 3}						
Digital I/O Power Supply	D_{VDDIO}	ADV7282-M ADV7282	2.97 1.62	3.3 3.3	3.63 3.63	V V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
MIPI Tx Power Supply	M_{VDD}	ADV7282-M only	1.71	1.8	1.89	V
Digital I/O Supply Current	I_{DVDDIO}	ADV7282-M ADV7282		1.5 5		mA mA
PLL Supply Current	I_{PVDD}			12		mA
MIPI Tx Supply Current	I_{MVDD}	ADV7282-M only		14		mA
Analog Supply Current	I_{AVDD}					
Single-Ended CVBS Input				47		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		69		mA
Y/C Input				60		mA
YPrPb Input				75		mA
Digital Supply Current	I_{DVDD}					
Single-Ended CVBS Input				70		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		70		mA
Y/C Input				70		mA
YPrPb Input				70		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN CURRENTS ¹						
Digital I/O Supply Power-Down Current	I _{DVDDIO_PD}			73		μA
PLL Supply Power-Down Current	I _{PVDD_PD}			46		μA
Analog Supply Power-Down Current	I _{AVDD_PD}			0.2		μA
Digital Supply Power-Down Current	I _{DVDD_PD}			420		μA
MIPI Tx Supply Power-Down Current	I _{MVDD_PD}			4.5		μA
Total Power Dissipation in Power-Down Mode				1		mW

¹ Guaranteed by characterization.

² Typical current consumption values are measured with nominal voltage supply levels and an SMPTE bar test pattern.

³ All specifications apply when the I2P core is activated, unless otherwise stated.

VIDEO SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. Note that M_{VDD} only applies to the [ADV7282-M](#).

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS ¹						
Differential Phase	DP	CVBS input, modulated 5-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulated 5-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5-step		2.0		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio, Unweighted	SNR	Luma ramp Luma flat field		57.1		dB
Analog Front-End Crosstalk				58		dB
Common-Mode Rejection Ratio ²	CMRR			60		dB
				73		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			-5		+5	%
Vertical Lock Range			40		70	Hz
f _{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Synchronization Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed ³				100		Lines
Fast Switch Speed ⁴				100		ms
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy				1		%

¹ These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.

² The CMRR of this circuit design is critically dependent on the external resistor matching on the circuit inputs (see the Input Networks section). The CMRR measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.

³ Autodetection switch speed is the time required for the [ADV7282/ADV7282-M](#) to detect which video format is present at its input, for example, PAL I or NTSC M.

⁴ Fast switch speed is the time required for the [ADV7282/ADV7282-M](#) to switch from one analog input (single-ended or differential) to another, for example, switching from A_{IN1} to A_{IN2}.

ANALOG SPECIFICATIONS

A_{VDD} , D_{VDD} , P_{VDD} , and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. Note that M_{VDD} only applies to the [ADV7282-M](#).

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor	Clamps switched off		0.1		μ F
Input Impedance			10		M Ω
Large Clamp Source Current			0.4		mA
Large Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		μ A
Fine Clamp Sink Current			10		μ A

CLOCK AND I²C TIMING SPECIFICATIONS

A_{VDD} , D_{VDD} , P_{VDD} , and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. Note that M_{VDD} only applies to the [ADV7282-M](#).

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency			28.63636		MHz
Frequency Stability				\pm 50	ppm
I ² C PORT					
SCLK Frequency				400	kHz
SCLK Minimum Pulse Width High	t_1	0.6			μ s
SCLK Minimum Pulse Width Low	t_2	1.3			μ s
Hold Time (Start Condition)	t_3	0.6			μ s
Setup Time (Start Condition)	t_4	0.6			μ s
SDATA Setup Time	t_5	100			ns
SCLK and SDATA Rise Times	t_6			300	ns
SCLK and SDATA Fall Times	t_7			300	ns
Setup Time (Stop Condition)	t_8		0.6		μ s
RESET INPUT					
$\overline{\text{RESET}}$ Pulse Width		5			ms

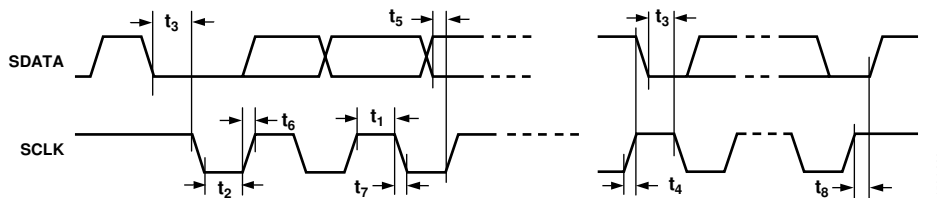


Figure 3. I²C Timing Diagram

11534-002

MIPI VIDEO OUTPUT SPECIFICATIONS (ADV7282-M ONLY)

A_{VDD} , D_{VDD} , P_{VDD} , and $M_{VDD} = 1.71\text{ V to }1.89\text{ V}$, $D_{VDDIO} = 2.97\text{ V to }3.63\text{ V}$, specified at operating temperature range, unless otherwise noted. The CSI-2 clock lane of the **ADV7282-M** remains in high speed (HS) mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the **ADV7282-M** operating in progressive mode and with a nominal 432 Mbps output data rate. Specifications guaranteed by characterization.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNIT INTERVAL	UI					
Interlaced Output				4.63		ns
Progressive Output				2.31		ns
DATA LANE LP TX DC SPECIFICATIONS¹						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		-50	0	+50	mV
DATA LANE LP TX AC SPECIFICATIONS¹						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Rise Time, 30% to 85%					35	ns
Data Lane LP Slew Rate vs. C_{LOAD}						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV $\leq V_{OUT} \leq 930\text{ mV}$		Falling edge	30			mV/ns
400 mV $\leq V_{OUT} \leq 700\text{ mV}$		Rising edge	30			mV/ns
700 mV $\leq V_{OUT} \leq 930\text{ mV}$		Rising edge	>0			mV/ns
Pulse Width of LP Exclusive-OR Clock		First clock pulse after stop state or last pulse before stop state	40			ns
		All other clock pulses	20			ns
Period of LP Exclusive-OR Clock			90			ns
CLOCK LANE LP TX DC SPECIFICATIONS¹						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		-50	0	+50	mV
CLOCK LANE LP TX AC SPECIFICATIONS¹						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Clock Lane LP Slew Rate						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV $\leq V_{OUT} \leq 930\text{ mV}$		Falling edge	30			mV/ns
400 mV $\leq V_{OUT} \leq 700\text{ mV}$		Rising edge	30			mV/ns
700 mV $\leq V_{OUT} \leq 930\text{ mV}$		Rising edge	>0			mV/ns
DATA LANE HS TX SIGNALING REQUIREMENTS						
Low Power to High Speed Transition Stage	t_9	See Figure 4	50			ns
	t_{10}	Time that the D0P pin is at V_{OL} and the D0N pin is at V_{OH}				
	t_{11}	Time that the D0P and D0N pins are at V_{OL}	$40 + (4 \times UI)$		$85 + (6 \times UI)$	ns
	$ V_1 $	t_{10} plus the HS-zero period	$145 + (10 \times UI)$			ns
High Speed Differential Voltage Swing			140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations						
50 MHz to 450 MHz					25	mV
Above 450 MHz					15	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
Rise Time, 20% to 80%	t ₁₂	Time that the ADV7282-M drives the flipped last data bit after sending the last payload data bit of an HS transmission burst	0.15		0.3 × UI	ns	
Fall Time, 80% to 20%			0.15		0.3 × UI	ns	
High Speed to Low Power Transition Stage			60 + (4 × UI)			ns	
	t ₁₃	Post-end-of-transmission rise time (30% to 85%)			35	ns	
	t ₁₄	Time from start of t ₁₂ to start of low power state following an HS transmission burst			105 + (12 × UI)	ns	
	t ₁₅	Time that a low power state is transmitted after an HS transmission burst			100	ns	
CLOCK LANE HS TX SIGNALING REQUIREMENTS		See Figure 4					
Low Power to High Speed Transition Stage ²	V ₂	Time that the CLKP pin is at V _{OL} and the CLKN pin is at V _{OH}	50			ns	
		Time that the CLKP and CLKN pins are at V _{OL}	38		95	ns	
		Clock HS-zero period	300	500		ns	
High Speed Differential Voltage Swing		140	200	270		mV p-p	
Differential Voltage Mismatch				10		mV	
Single-Ended Output High Voltages				360		mV	
Static Common-Mode Voltage Level			150	200	250	mV	
Static Common-Mode Voltage Mismatch							5
Dynamic Common Level Variations							
50 MHz to 450 MHz							25
Above 450 MHz							15
Rise Time, 20% to 80%							0.15
Fall Time, 80% to 20%	0.15						
HS TX CLOCK TO DATA LANE TIMING REQUIREMENTS							
Data to Clock Skew			0.35 × UI		0.65 × UI	ns	

¹ These measurements were performed with C_{LOAD} = 50 pF.

² The clock lane remains in high speed mode throughout normal operation. These results apply only to the ADV7282-M during startup.

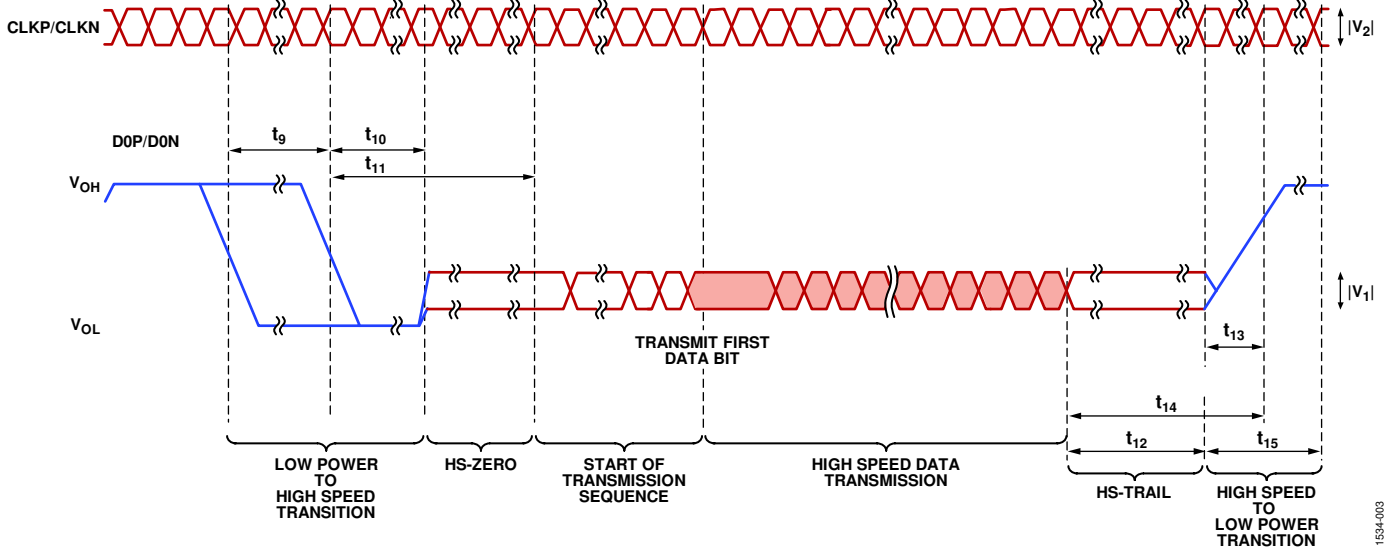


Figure 4. ADV7282-M Output Timing Diagram (Conforms with MIPI CSI-2 Specification)

11534-003

PIXEL PORT TIMING SPECIFICATIONS (ADV7282 ONLY)

A_{VDD} , D_{VDD} , and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK OUTPUTS LLC Mark Space Ratio	$t_{16}:t_{17}$		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS Data Output Transitional Time	t_{18}	Negative clock edge to start of valid data ($t_{SETUP} = t_{17} - t_{18}$)			3.8	ns
	t_{19}	End of valid data to negative clock edge ($t_{HOLD} = t_{16} - t_{19}$)			6.9	ns

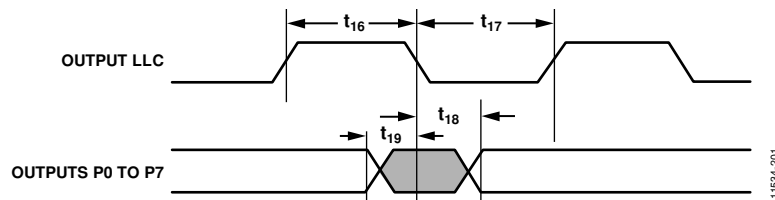


Figure 5. ADV7282 Pixel Port and Control Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter ¹	Rating
A_{VDD} to GND	2.2 V
D_{VDD} to GND	2.2 V
P_{VDD} to GND	2.2 V
M_{VDD} to GND ²	2.2 V
D_{VDDIO} to GND	4 V
P_{VDD} to D_{VDD}	-0.9 V to +0.9 V
M_{VDD} to D_{VDD} ²	-0.9 V to +0.9 V
A_{VDD} to D_{VDD}	-0.9 V to +0.9 V
Digital Inputs Voltage	GND - 0.3 V to $D_{VDDIO} + 0.3$ V
Digital Outputs Voltage	GND - 0.3 V to $D_{VDDIO} + 0.3$ V
Analog Inputs to Ground	GND - 0.3 V to $A_{VDD} + 0.3$ V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	-65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

¹ The Absolute Maximum Ratings assumes that DGND pins and the exposed pad of the [ADV7282/ADV7282-M](#) are connected together to a common ground plane (GND). This is part of the recommended layout scheme. See PCB Layout Recommendations section for more information. The Absolute Maximum Ratings are stated in relation to this common ground plane.

² M_{VDD} applies to the [ADV7282-M](#) only.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions must be taken for handling and assembly.

THERMAL RESISTANCE

The thermal resistance values in Table 8 are specified for the device soldered onto a 4-layer printed circuit board (PCB) with a common ground plane and with the exposed pad of the device connected to DGND. The values in Table 8 are maximum values.

Table 8. Thermal Resistance for the 32-Lead LFCSP

Thermal Characteristic	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	32.5	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	2.3	°C/W

REFLOW SOLDER

The [ADV7282/ADV7282-M](#) is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C ($\pm 5^\circ\text{C}$).

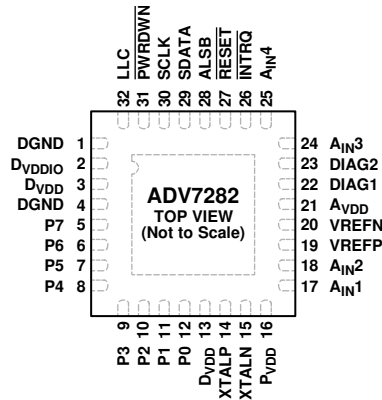
In addition, the [ADV7282/ADV7282-M](#) is backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



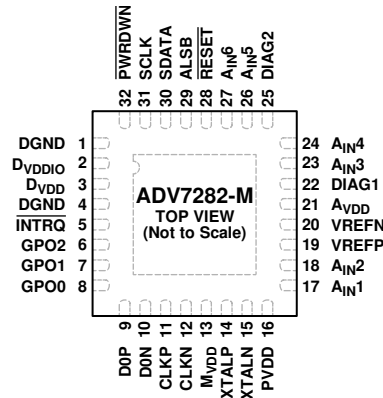
NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO DGND.

11534-202

Figure 6. Pin Configuration, [ADV7282](#)

Table 9. Pin Function Descriptions, [ADV7282](#)

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D _{VDDIO}	Power	Digital I/O Power Supply (1.8 V or 3.3 V).
3, 13	D _{VDD}	Power	Digital Power Supply (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Ports.
14	XTALP	Output	Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282 . The crystal used with the ADV7282 must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the ADV7282 must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282 , the output of the oscillator is fed into the XTALN pin.
16	P _{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 24, 25	A _{IN1} to A _{IN4}	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	A _{VDD}	Power	Analog Power Supply (1.8 V).
22	DIAG1	Input	Diagnostic Input 1.
23	DIAG2	Input	Diagnostic Input 2.
26	INTRQ	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
27	RESET	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7282 circuitry.
28	ALSB	Input	This pin selects the I ² C write address for the ADV7282 . When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
29	SDATA	Input/output	I ² C Port Serial Data Input/Output.
30	SCLK	Input	I ² C Port Serial Clock Input. The maximum clock rate is 400 kHz.
31	PWRDWN	Input	Power-Down Pin. A logic low on this pin places the ADV7282 in power-down mode.
32	LLC	Output	Line-Locked Output Clock for Output Pixel Data. The clock output is nominally 27 MHz, but it increases or decreases according to the video line length.
	EPAD (EP)		Exposed Pad. The exposed pad must be connected to DGND.



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO DGND.

11534-004

Figure 7. Pin Configuration, *ADV7282-M*

Table 10. Pin Function Descriptions, *ADV7282-M*

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D _{VDDIO}	Power	Digital I/O Power Supply (3.3 V).
3	D _{VDD}	Power	Digital Power Supply (1.8 V).
5	INTRQ	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
6 to 8	GPO2 to GPO0	Output	General-Purpose Outputs. These pins can be configured via I ² C to allow control of external devices.
9	D0P	Output	Positive MIPI Differential Data Output.
10	D0N	Output	Negative MIPI Differential Data Output.
11	CLKP	Output	Positive MIPI Differential Clock Output.
12	CLKN	Output	Negative MIPI Differential Clock Output.
13	M _{VDD}	Power	MIPI Digital Power Supply (1.8 V).
14	XTALP	Output	Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the <i>ADV7282-M</i> . The crystal used with the <i>ADV7282-M</i> must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the <i>ADV7282-M</i> must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the <i>ADV7282-M</i> , the output of the oscillator is fed into the XTALN pin.
16	P _{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 23, 24, 26, 27	A _{IN1} to A _{IN6}	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	A _{VDD}	Power	Analog Power Supply (1.8 V).
22	DIAG1	Input	Diagnostic Input 1.
25	DIAG2	Input	Diagnostic Input 2.
28	RESET	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the <i>ADV7282-M</i> circuitry.
29	ALSB	Input	This pin selects the I ² C write address for the <i>ADV7282-M</i> . When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
30	SDATA	Input/output	I ² C Port Serial Data Input/Output.
31	SCLK	Input	I ² C Port Serial Clock Input. The maximum clock rate is 400 kHz.
32	PWRDWN	Input	Power-Down Pin. A logic low on this pin places the <i>ADV7282-M</i> in power-down mode.
	EPAD (EP)		Exposed Pad. The exposed pad must be connected to DGND.

THEORY OF OPERATION

The [ADV7282/ADV7282-M](#) are versatile one-chip, multiformat video decoders. The [ADV7282/ADV7282-M](#) automatically detect standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The [ADV7282](#) converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The [ADV7282-M](#) converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a MIPI CSI-2 interface.

The MIPI CSI-2 output interface connects to a wide range of video processors and FPGAs. The accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution.

The analog video inputs of the [ADV7282/ADV7282-M](#) accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPrPb video signals, supporting a wide range of consumer and automotive video sources.

In differential CVBS mode, the [ADV7282/ADV7282-M](#), along with an external resistor divider, provides a common-mode input range of up to 4 V, enabling the removal of large signal, common-mode transients present on the video lines.

The advanced interlaced-to-progressive (I2P) function allows the [ADV7282/ADV7282-M](#) to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The [ADV7282/ADV7282-M](#) uses edge adaptive technology to minimize video defects on low angle lines.

The automatic gain control (AGC) and clamp restore circuitry allows an input video signal peak-to-peak range of 0 V to 1.0 V at the analog video input pins of the [ADV7282/ADV7282-M](#). Alternatively, the AGC and clamp restore circuitry can be bypassed for manual settings.

AC coupling of the input video signals provides short-to-battery (STB) protection. STB diagnostics can be performed on two input video signals.

The [ADV7282/ADV7282-M](#) support a number of other functions, including 8-bit to 6-bit down dither mode and adaptive contrast enhancement (ACE).

The [ADV7282/ADV7282-M](#) are programmed via a 2-wire, serial bidirectional port (I²C compatible) and is fabricated in a 1.8 V CMOS process. The monolithic CMOS construction of the [ADV7282/ADV7282-M](#) ensures greater functionality with lower power dissipation. The [ADV7282/ADV7282-M](#) are rated over the -40°C to +105°C temperature range. This makes the [ADV7282/ADV7282-M](#) ideal for automotive applications.

ANALOG FRONT END (AFE)

The analog front end (AFE) of the [ADV7282/ADV7282-M](#) comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor (SDP). The AFE uses differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS inputs to be connected directly to the [ADV7282/ADV7282-M](#).

The AFE also includes an input mux that enables multiple video signals to be applied to the [ADV7282/ADV7282-M](#). The input mux allows up to four composite video signals to be applied to the [ADV7282](#) and up to six composite video signals to be applied to the [ADV7282-M](#).

Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter.

A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see the Input Networks section). Fine clamping of the video signal is performed downstream by digital fine clamping within the [ADV7282/ADV7282-M](#).

Table 11 lists the three ADC clock rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

Table 11. ADC Clock Rates

Input Format	ADC Clock Rate (MHz) ¹	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)	114	4×
YPrPb	172	4×

¹ Based on a 28.63636 MHz crystal between the XTALP and XTALN pins.

The fully differential AFE of the [ADV7282/ADV7282-M](#) provides inherent small and large signal noise rejection, improved electromagnetic interference (EMI) protection, and the ability to absorb ground bounce. Support is provided for both true differential and pseudo differential signals.

STANDARD DEFINITION PROCESSOR (SDP)

The [ADV7282/ADV7282-M](#) is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, PAL 60
- NTSC J, NTSC M, NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, SECAM L

Using the standard definition processor (SDP), the [ADV7282/ADV7282-M](#) can automatically detect the video standard and process it accordingly.

The [ADV7282/ADV7282-M](#) has a five-line adaptive 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the [ADV7282/ADV7282-M](#).

The [ADV7282/ADV7282-M](#) implements the patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as VCRs. ADLLT enables the [ADV7282/ADV7282-M](#) to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs and camcorders. The [ADV7282/ADV7282-M](#)

contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

Adaptive contrast enhancement (ACE) offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. ACE increases the contrast in dark areas of an image without saturating the bright areas of the image. This feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

Down dithering converts the output of the [ADV7282/ADV7282-M](#) from an 8-bit to a 6-bit output, enabling ease of design for standard LCD panels.

The I2P block converts the interlaced video input into a progressive video output without the need for external memory.

The SDP can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world system teletext (WST). VBI data is transmitted via the MIPI CSI-2 link as ancillary data packets.

The [ADV7282/ADV7282-M](#) is fully Rovi® (Macrovision®) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the [ADV7282/ADV7282-M](#) is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies (D_{VDD} , P_{VDD} , A_{VDD} , and M_{VDD}). Note that M_{VDD} only applies to the [ADV7282-M](#).

When powering up the [ADV7282/ADV7282-M](#), follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the \overline{PWRDWN} and \overline{RESET} pins (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the \overline{PWRDWN} pin high.
5. Wait 5 ms and then pull the \overline{RESET} pin high.
6. After all power supplies and the \overline{PWRDWN} and \overline{RESET} pins are powered up and stable, wait an additional 5 ms before initiating I²C communication with the [ADV7282-M](#).

SIMPLIFIED POWER-UP SEQUENCE

Alternatively, the [ADV7282/ADV7282-M](#) can be powered up by asserting all supplies and the \overline{PWRDWN} and \overline{RESET} pins simultaneously. After this operation, perform a software reset, then wait 10 ms before initiating I²C communication with the [ADV7282/ADV7282-M](#).

While the supplies are being established, take care to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The [ADV7282/ADV7282-M](#) supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

D_{VDDIO} SUPPLY VOLTAGE

For correct operation of the [ADV7282-M](#), the D_{VDDIO} supply must be from 2.97 V to 3.63 V.

The [ADV7282](#) however, can operate with a nominal D_{VDDIO} voltage of 1.8 V. In this case, apply the power-up sequences described previously. The only change is that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V, and the \overline{PWRDWN} and \overline{RESET} pins of the [ADV7282](#) are powered up to 1.8 V instead of 3.3 V.

Note that when the [ADV7282](#) operates with a nominal D_{VDDIO} voltage of 1.8 V, then set the drive strength of all digital outputs to a maximum.

Note that when D_{VDDIO} is 1.8 V, no pin of the [ADV7282](#) is to be pulled up to 3.3 V. For example, the I²C pins of the [ADV7282](#) (SCLK and SDATA) must also be pulled up to 1.8 V instead of 3.3 V.

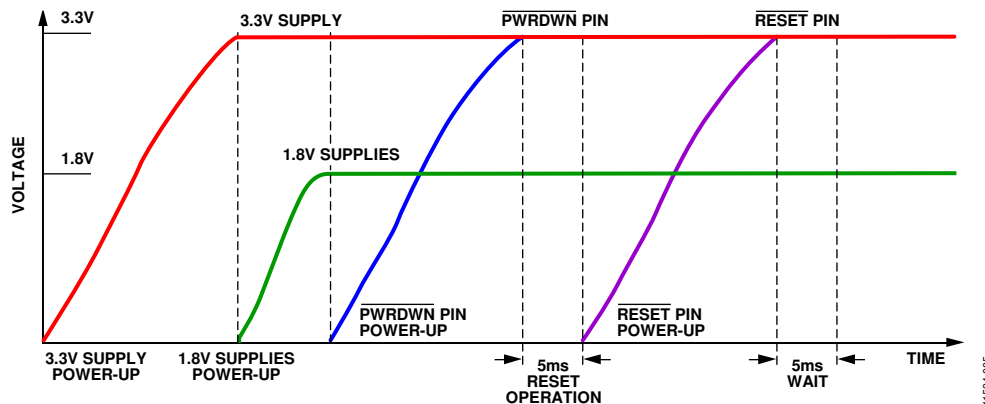


Figure 8. Optimal Power-Up Sequence

INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the A_{INX} input pins of the [ADV7282/ADV7282-M](#). The components of the input network depend on the video format selected for the analog input.

SINGLE-ENDED INPUT NETWORK

Figure 9 shows the input network to use on each A_{INX} input pin of the [ADV7282/ADV7282-M](#) when any of the following video input formats is used:

- Single-ended CVBS
- YC (S-Video)
- YPrPb

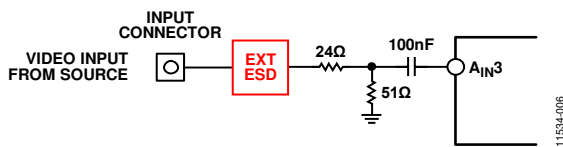


Figure 9. Single-Ended Input Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the [ADV7282/ADV7282-M](#). This allows an input range to the [ADV7282/ADV7282-M](#) of up to 1.47 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that signal-to-noise ratio (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the A_{INX} pin of the [ADV7282/ADV7282-M](#). The clamping circuitry within the [ADV7282/ADV7282-M](#) restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the [ADV7282/ADV7282-M](#).

DIFFERENTIAL INPUT NETWORK

Figure 10 shows the input network to use when differential CVBS video is input on the A_{INX} input pins of the [ADV7282/ADV7282-M](#).

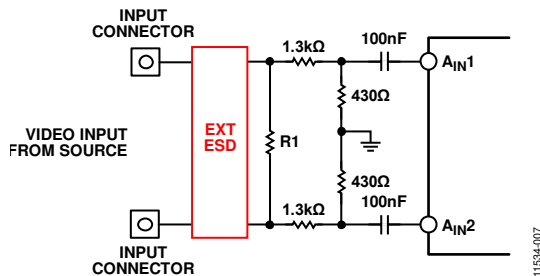


Figure 10. Differential Input Network

Fully differential video transmission involves transmitting two complementary CVBS signals. Pseudo differential video

transmission involves transmitting a CVBS signal and a source ground signal.

Differential video transmission has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 k Ω and 430 Ω resistors create a resistor divider with a gain of 0.25. The resistor divider attenuates the amplitude of the input analog video, but increases the input common-mode range of the [ADV7282/ADV7282-M](#) to 4 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the A_{INX} pin of the [ADV7282/ADV7282-M](#). The clamping circuitry within the [ADV7282/ADV7282-M](#) restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the [ADV7282/ADV7282-M](#).

The combination of the 1.3 k Ω and 430 Ω resistors and the 100 nF ac coupling capacitors limits the current flow into the [ADV7282/ADV7282-M](#) during short-to-battery (STB) events (see the Short-to-Battery Protection section).

To achieve optimal performance, the 1.3 k Ω and 430 Ω resistors must be closely matched; that is, all 1.3 k Ω and 430 Ω resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

SHORT-TO-BATTERY PROTECTION

In differential mode, the [ADV7282/ADV7282-M](#) is protected against short-to-battery (STB) events by the external 100 nF ac coupling capacitors (see Figure 10). The external input network resistors are sized to be large enough to reduce the current flow during an STB event, but to be small enough not to affect the operation of the [ADV7282/ADV7282-M](#).

The power rating of the input network resistors must be chosen in order to withstand the high voltages of STB events. Similarly, the breakdown voltage of the ac coupling capacitors must be chosen to be robust to STB events. The R1 resistor is protected because no current or limited current flows through it during an STB event.

The [ADV7282/ADV7282-M](#) provides two STB diagnostic pins that can be used to generate an interrupt when an STB event occurs. For more information, see the Short-to-Battery (STB) Diagnostics section.

INPUT CONFIGURATION

The input format of the [ADV7282/ADV7282-M](#) is specified using the INSEL[4:0] bits (see Table 12). These bits also configure the SDP core to process CVBS, differential CVBS, Y/C (S-Video), or component (YPrPb) format. The INSEL[4:0] bits are located in the user sub map of the register space at Address 0x00[4:0]. For more information about the registers, see the Register Maps section.

The INSEL[4:0] bits specify predefined analog input routing schemes, eliminating the need for manual mux programming and allowing the user to route the various video signal types to the decoder. For example, if the CVBS input is selected, the remaining channels are powered down.

Table 12. Input Format Specified by the INSEL[4:0] Bits

INSEL[4:0] Bit Value	Video Format	Analog Inputs	
		ADV7282	ADV7282-M
00000	CVBS	CVBS input on A _{IN1}	CVBS input on A _{IN1}
00001	CVBS	CVBS input on A _{IN2}	CVBS input on A _{IN2}
00010	CVBS	Reserved	CVBS input on A _{IN3}
00011	CVBS	Reserved	CVBS input on A _{IN4}
00100	Reserved	Reserved	Reserved
00101	Reserved	Reserved	Reserved
00110	CVBS	CVBS input on A _{IN3}	CVBS input on A _{IN5}
00111	CVBS	CVBS input on A _{IN4}	CVBS input on A _{IN6}
01000	Y/C (S-Video)	Y input on A _{IN1} ; C input on A _{IN2}	Y input on A _{IN1} ; C input on A _{IN2}
01001	Y/C (S-Video)	Reserved	Y input on A _{IN3} ; C input on A _{IN4}
01010	Reserved	Reserved	Reserved
01011	Y/C (S-Video)	Y input on A _{IN3} ; C input on A _{IN4}	Y input on A _{IN5} ; C input on A _{IN6}
01100	YPrPb	Reserved ¹	Y input on A _{IN1} ; Pb input on A _{IN2} ; Pr input on A _{IN3}
01101	Reserved	Reserved	Reserved
01110	Differential CVBS	Positive input on A _{IN1} ; Negative input on A _{IN2}	Positive input on A _{IN1} ; Negative input on A _{IN2}
01111	Differential CVBS	Reserved	Positive input on A _{IN3} ; Negative input on A _{IN4}
10000	Reserved	Reserved	Reserved
10001	Differential CVBS	Positive input on A _{IN3} ; Negative input on A _{IN4}	Positive input on A _{IN5} ; Negative input on A _{IN6}
10010 to 11111	Reserved	Reserved	Reserved

¹ Note that it is possible for the [ADV7282](#) to receive YPbPr formats; however, a manual muxing scheme is required. In this case luma (Y) is fed in on A_{IN1} or A_{IN3}, blue chroma (Pb) is fed in on A_{IN4}, and red chroma (Pr) is fed in on A_{IN2}.

SHORT-TO-BATTERY (STB) DIAGNOSTICS

The ADV7282/ADV7282-M senses an STB event via the DIAG1 and DIAG2 pins. The DIAG1 and DIAG2 pins can sense an STB event on either the positive or negative differential input because of the negligible voltage drop across Resistor R1.

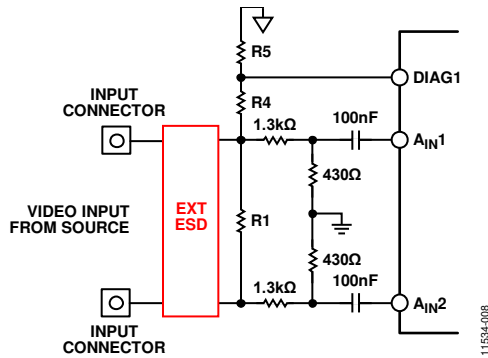


Figure 11. Diagnostic Connections

Resistors R4 and R5 divide down the voltage at the input connector to protect the DIAGx pin from an STB event. The DIAGx pin circuitry compares this voltage to a programmable reference voltage, known as the diagnostic slice level. When the diagnostic slice level is exceeded, an STB event has occurred.

When the DIAGx pin voltage exceeds the diagnostic slice level voltage, a hardware interrupt is triggered and indicated by the INTRQ pin. A readback register is also provided, which allows the user to determine the DIAGx pin on which the STB event occurred.

Use Equation 1 to find the trigger voltage for a selected diagnostic slice level.

$$V_{STB_TRIGGER} = \frac{R5 + R4}{R5} \times DIAGNOSTIC_SLICE_LEVEL \quad (1)$$

where:

$V_{STB_TRIGGER}$ is the minimum voltage required at the input connector to trigger the STB interrupt on the ADV7282/ADV7282-M.

$DIAGNOSTIC_SLICE_LEVEL$ is the programmable reference voltage.

PROGRAMMING THE STB DIAGNOSTIC FUNCTION

By default, the STB diagnostic function is disabled on the ADV7282/ADV7282-M. To enable the diagnostic function, follow the instructions in this section.

DIAG1 Pin

DIAG1_SLICER_PWRDN, User Sub Map, Address 0x5D[6]

This bit powers up or powers down the diagnostic circuitry for the DIAG1 pin.

Table 13. DIAG1_SLICER_PWRDN Function

DIAG1_SLICER_PWRDN	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG1 pin.
1 (default)	Power down the diagnostic circuitry for the DIAG1 pin.

DIAG1_SLICE_LEVEL[2:0], User Sub Map, Address 0x5D[4:2]

The DIAG1_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG1 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG1 pin, an STB interrupt is triggered.

In order for the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG1 pin must be powered up (see Table 13).

Table 14. DIAG1_SLICE_LEVEL[2:0] Settings

DIAG1_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

DIAG2 Pin**DIAG2_SLICER_PWRDN, User Sub Map, Address 0x5E[6]**

This bit powers up or powers down the diagnostic circuitry for the DIAG2 pin.

Table 15. DIAG2_SLICER_PWRDN Function

DIAG2_SLICER_PWRDN	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG2 pin.
1 (default)	Power down the diagnostic circuitry for the DIAG2 pin.

DIAG2_SLICE_LEVEL[2:0], User Sub Map, Address 0x5E[4:2]

The DIAG2_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG2 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG2 pin, an STB interrupt is triggered.

In order for the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG2 pin must be powered up (see Table 15).

Table 16. DIAG2_SLICE_LEVEL[2:0] Settings

DIAG2_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The [ADV7282/ADV7282-M](#) can increase the contrast of an image depending on the content of the picture, allowing bright areas to be made brighter and dark areas to be made darker. The optional ACE feature enables the contrast within dark areas to be increased without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 17. To disable the ACE function, execute the register writes shown in Table 18.

Table 17. Register Writes to Enable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x80	Enable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

Table 18. Register Writes to Disable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x00	Disable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

I2P FUNCTION

The advanced interlaced-to-progressive (I2P) function allows the [ADV7282/ADV7282-M](#) to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The [ADV7282/ADV7282-M](#) use edge adaptive technology to minimize video defects on low angle lines.

The I2P function is disabled by default. To enable the I2P function, use the recommended scripts from Analog Devices, Inc.

ITU-R BT.656 Tx CONFIGURATION (ADV7282 ONLY)

The **ADV7282** receives analog video and outputs digital video according to the ITU-R BT.656 specification. The **ADV7282** outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins and has a line-locked clock (LLC) pin.

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output is used to clock the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

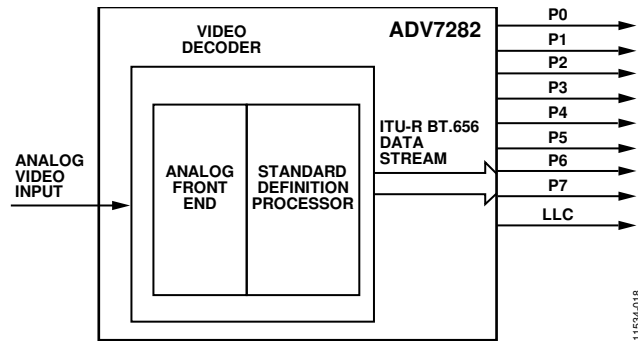


Figure 12. ITU-R BT.656 Output Stage of the **ADV7282**

MIPI CSI-2 OUTPUT (ADV7282-M ONLY)

The decoder in the [ADV7282-M](#) outputs an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a CSI-2 Tx module. Data from the CSI-2 Tx module is fed into a D-PHY physical layer and output serially from the device.

The output of the [ADV7282-M](#) consists of a single data channel on the D0P and D0N lanes and a clock channel on the CLKP and CLKN lanes.

Video data is output over the data lanes in high speed mode. The data lanes enter low power mode during the horizontal and vertical blanking periods.

The clock lanes are used to clock the output video. After the [ADV7282-M](#) is programmed, the clock lanes exit low power mode and remain in high speed mode until the part is reset or powered down.

The [ADV7282-M](#) outputs video data in an 8-bit YCrCb 4:2:2 format. When the I2P core is disabled, the video data is output in an interlaced format at a nominal data rate of 216 Mbps. When the I2P core is enabled, the video data is output in a progressive format at a nominal data rate of 432 Mbps (see the I2P Function section for more information).

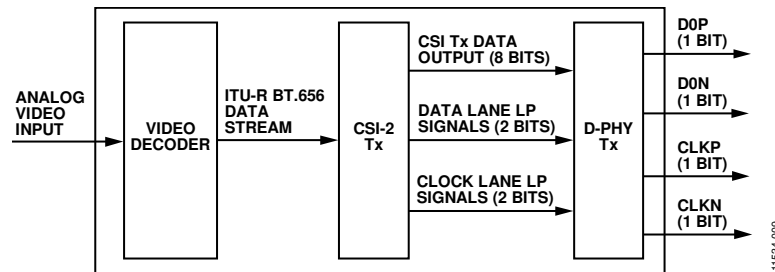


Figure 13. MIPI CSI-2 Output Stage of the [ADV7282-M](#)

I²C PORT DESCRIPTION

The ADV7282/ADV7282-M supports a 2-wire, I²C-compatible serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7282/ADV7282-M and the system I²C master controller. The I²C port of the ADV7282/ADV7282-M allows the user to set up and configure the decoder and to read back captured VBI data.

The ADV7282/ADV7282-M has a number of possible I²C slave addresses and subaddresses (see the Register Maps section). The main map of the ADV7282/ADV7282-M has four possible slave addresses for read and write operations, depending on the logic level of the ALSB pin (see Table 19).

Table 19. Main Map I²C Address for the ADV7282-M

ALSB Pin	R/W Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two ADV7282/ADV7282-M devices in an application without using the same I²C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, a specific protocol is followed.

1. The master initiates a data transfer by establishing a start condition, which is defined as a high to low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/W bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.
4. All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

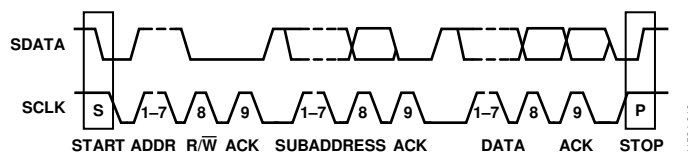


Figure 14. Bus Data Transfer

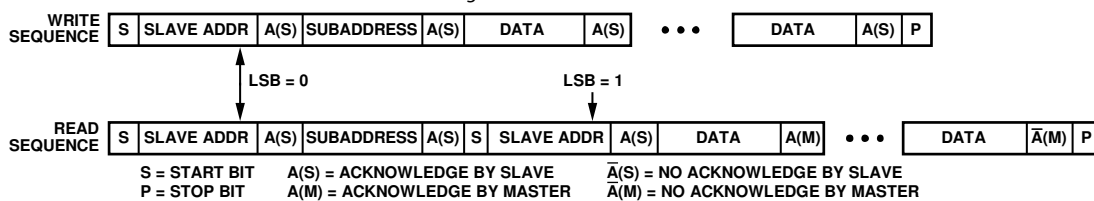


Figure 15. Read and Write Sequence

The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7282/ADV7282-M acts as a standard I²C slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/W bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7282/ADV7282-M does not issue an acknowledge and returns to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, one of the following actions is taken:

- In read mode, the register contents of the highest subaddress continue to be output until the master device issues a no acknowledge, which indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. A no acknowledge is issued by the ADV7282/ADV7282-M, and the part returns to the idle condition.