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Multiformat SD, Progressive Scan/HDTV Video Encoder with Six NSV™ 12-Bit DACs

ADV7300A/ADV7301A

FEATURES

High Definition Input Formats
- YCrCb Compliant to SMPTE293M (525 p), ITU-R.BT1358 (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), and Any Other High Definition Standard Using Async Timing Mode
- RGB in 3 × 10-Bit 4:4:4 Format
- BTA T-1004 EDTV2 525 p Parallel

High Definition Output Formats (525 p/625 p/720 p/1080 i)
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB + H/V (HDTV 5-Wire Format)
- CGMS-A (720 p/1080 i)
- Macrovision Rev 1.0 (525 p/625 p)*
  - CGMS-A (525 p)

Standard Definition Input Formats
- CCIR-656 4:2:2 8-/10-Bit Parallel Input
- CCIR-601 4:2:2 16-/20-Bit Parallel Input

Standard Definition Output Formats
- Composite NTSC M, N;
  - PAL M, N, B, D, G, H, I, PAL-60
- SMPTE170M NTSC Compatible Composite Video
- ITU-R.BT470 PAL Compatible Composite Video
- S-Video (Y/C)
- EuroScart RGB
- Component YUV (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1*
  - CGMS/WSS
  - Closed Captioning

GENERAL FEATURES

- Simultaneous SD and HD Inputs and Outputs
- Oversampling (108 MHz/148.5 MHz)
- On-Board Voltage Reference
- 6 NSV Precision Video 12-Bit DACs
- 2-Wire Serial MPU Interface
- Dual I/O Supply 2.5 V/3.3 V Operation
- Analog and Digital Supply 2.5 V
- On-Board PLL
- 64-LQFP Package
- Lead-Free Product

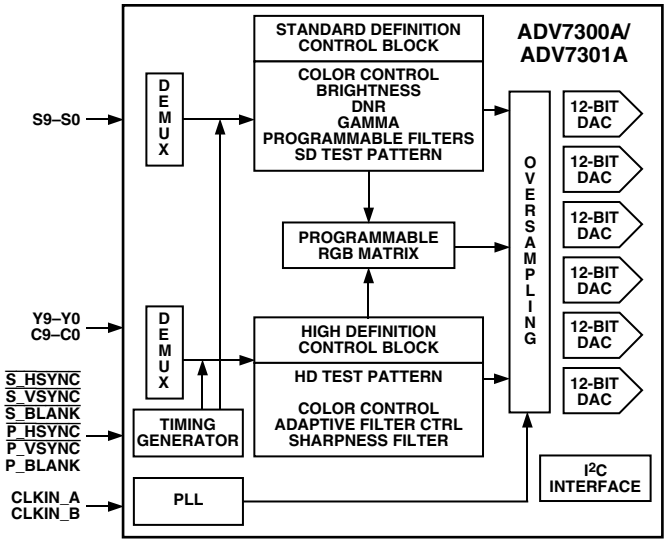
APPLICATIONS

- High End DVD Players
- SD/Program Scan/HDTV Display Devices
- SD/Program Scan/HDTV Set-Top Boxes
- SD/HDTV Studio Equipment

NSV (Noise Shaped Video) is a trademark of Analog Devices, Inc.
*ADV7300A Only

REV. A

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7300A/ADV7301A is a high speed, digital-to-analog encoder on a single monolithic chip. It includes six high speed video D/A converters with TTL compatible inputs.

The ADV7300A/ADV7301A has three separate 10-bit wide input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical, and blanking signals, or EAV/SAV timing codes, control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signals.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

DETAILED FEATURES

High Definition Programmable Features (720 p/1080 i)
- **2× Oversampling (148.5 MHz)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Field/Frame)**
- **Fully Programmable YCrCb to RGB Matrix**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Programmable Sharpness Filter Control**
- **CGMS-A (720 p/1080 i)**

High Definition Programmable Features (525 p/625 p)
- **4× Oversampling (108 MHz Output)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Frame)**
- **Individual Y and PrPb Output Delay**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Fully Programmable YCrCb to RGB Matrix**
- **Undershoot Limiter**
- **Macrovision Rev 1.0 (525 p/625 p)***
- **CGMS-A (525 p)**

Standard Definition Programmable Features
- **8× Oversampling (108 MHz)**
- **Internal Test Pattern Generator (Color Bars, Black Bar)**
- **Controlled Edge Rates for Sync, Active Video**
- **Individual Y and UV Output Delay**
- **Gamma Correction**
- **Digital Noise Reduction**
- **Multiple Chroma and Luma Filters**
- **Luma-SSAF™ Filter with Programmable Gain/ Attenuation**
- **UV SSAF**
- **Separate Pedestal Control on Component and Composite/S-Video Outputs**
- **VCR FF/RW Sync Mode**
- **Macrovision Rev 7.1***
- **CGMS/WSS**
- **Closed Captioning**

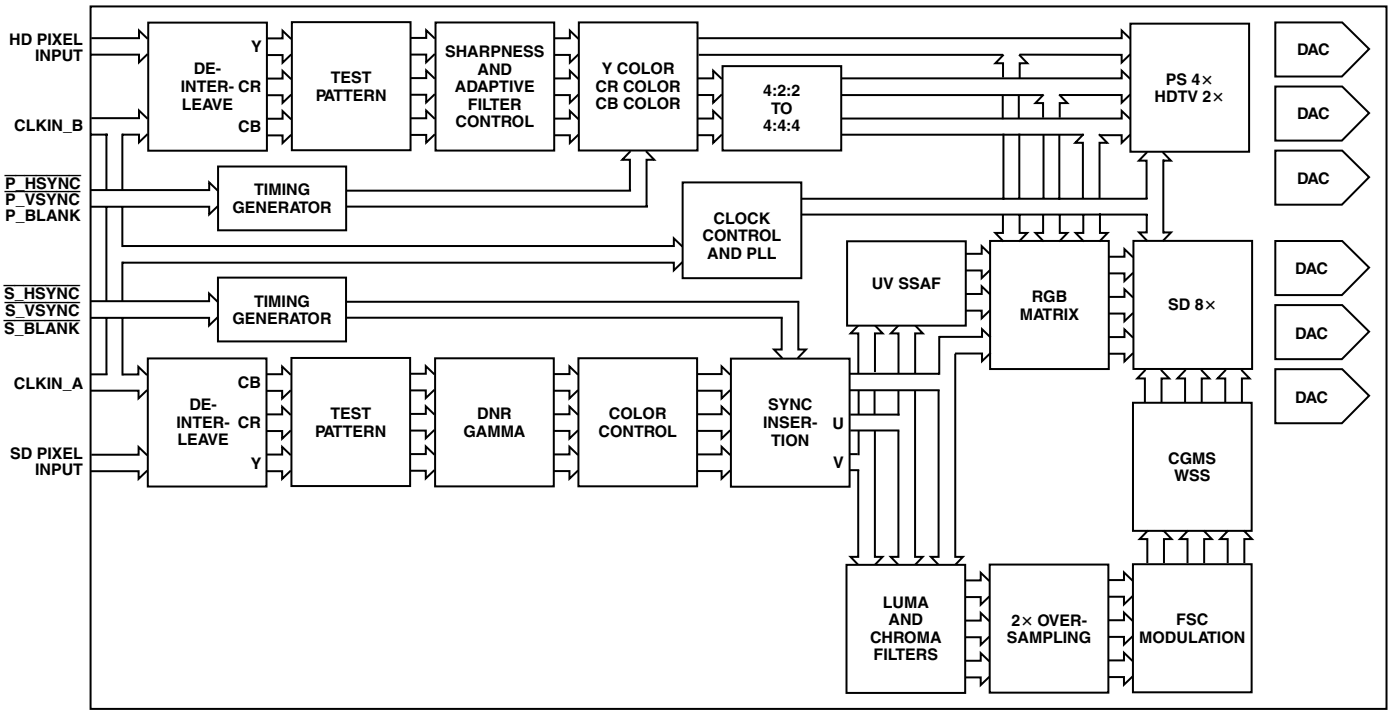


Figure 1. Functional Block Diagram

TERMS USED IN THIS DATA SHEET

SD Standard Definition Video, conforming to ITU-R.BT601/ITU-R.BT656.

HD High Definition Video, i.e., Progressive Scan or HDTV.

PS Progressive Scan Video, conforming to SMPTE293M or ITU-R.BT1358.

HDTV High Definition Television Video, conforming to SMPTE274M or SMPTE296M.

YCrCb SD or HD Component Digital Video.

YPrPb HD Component Analog Video.

YUV SD Component Analog Video.

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*ADV7300A Only

ADV7300A/ADV7301A–SPECIFICATIONS

(V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		12		Bits	
Integral Nonlinearity		±2.0		LSB	
Differential Nonlinearity, +ve[2]		0.25		LSB	V_{AA} = 2.5 V
Differential Nonlinearity, –ve[2]		2.0		LSB	V_{AA} = 2.5 V
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4 [2.0][3]			V	I_{SOURCE} = 400 µA
Three-State Leakage Current		±1.0		µA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		1		µA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	8.2	8.7	9.2	mA	
Output Current Range	8.2	8.7	9.2	mA	
Full-Scale Output Current	4.1	4.35	4.6	mA	$R_{SET1, 2}$ = 1520 Ω
Output Current Range	4.1	4.35	4.6	mA	$R_{SET1, 2}$ = 1520 Ω
DAC to DAC Matching		2.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Reference Range, V_{REF}	1.15	1.235	1.3	V	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[4]		93		mA	SD Only [8×]
		52		mA	PS Only [4×]
		84		mA	HDTV Only [2×]
		90	110	mA	SD and PS
		99		mA	SD [8×] and HDTV
		108		mA	SD and HDTV [2×]
I_{DD_IO}		0.2		mA	
I_{AA}[5,6]		70	75	mA	
Sleep Mode					
I_{DD}		130		µA	
I_{AA}		10		µA	
I_{DD_IO}		110		µA	
Power Supply Rejection Ratio		0.01		%/%	

NOTES

[1]Oversampling disabled. Static DAC performance will be improved with increased oversampling ratios.

[2]DNL measures the deviation of the actual DAC o/p voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step values lie below the ideal step value.

[3]Value in brackets for V_{DD_IO} = 2.375 V to 2.750 V.

[4]I_{DD} or the circuit current is the continuous current required to drive the digital core without the I_{PLL}.

[5]I_{AA} is the total current required to supply all DACs including the V_{REF} and PLL circuitry.

[6]All DACs on.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS

(V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
PROGRESSIVE SCAN MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		62		dB	Luma Ramp Unweighted
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
SNR		62		dB	Luma Ramp Unweighted
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth
STANDARD DEFINITION MODE					
Hue Accuracy		0.2		Degrees	
Color Saturation Accuracy		0.5		%	
Chroma Nonlinear Gain		±0.4		%	Referenced to 40 IRE
Chroma Nonlinear Phase		±0.3		Degrees	
Chroma/Luma Intermodulation		±0.05		%	
Chroma/Luma Gain Inequality		±98		%	
Chroma/Luma Delay Inequality		0.9		ns	
Luminance Nonlinearity		±0.4		%	
Chroma AM Noise		84		dB	
Chroma PM Noise		74		dB	
Differential Gain		0.6		%	NTSC
Differential Phase		1.4		Degrees	NTSC
SNR		62		dB	Luma Ramp
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First Clock Generated after This Period
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		8		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			27	MHz	Progressive Scan Mode
f_{CLK}		81		MHz	HDTV Mode/Async Mode
Clock High Time, t_9	40			% 1 clkcycle	
Clock Low Time, t_{10}	40			% 1 clkcycle	
Data Setup Time, t_{11}	2.0			ns	
Data Hold Time, t_{12}	2.0			ns	
Output Access Time, t_{13}			14	ns	
Output Hold Time, t_{14}	4.0			ns	
Pipeline Delay		61		clkcycles	SD [2×]
		62.5		clkcycles	SD [8×]
		66.5		clkcycles	SD Component Filter [8×]
		33		clkcycles	PS [1×], HD [1×], Async Timing Mode
		43.5		clkcycles	PS [4×]
		36		clkcycles	HD [2×]

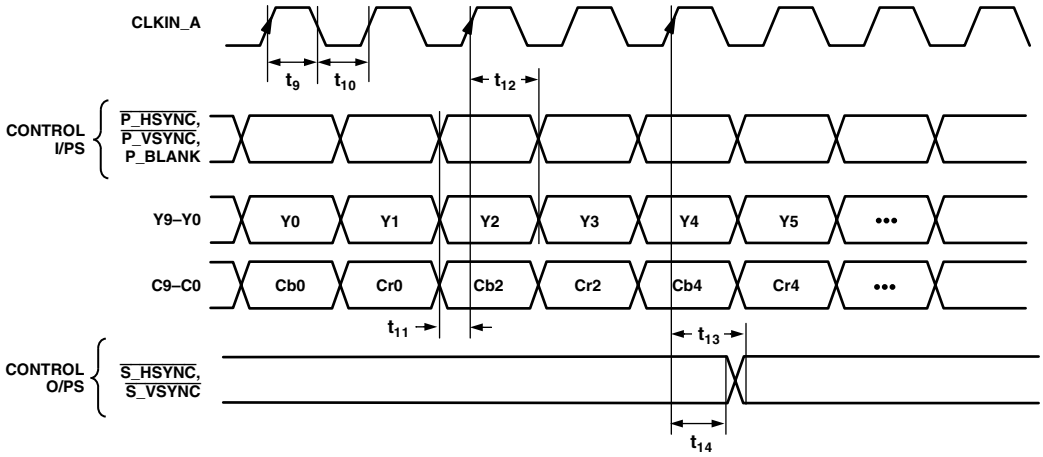
NOTES

[1]Guaranteed by characterization.

[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

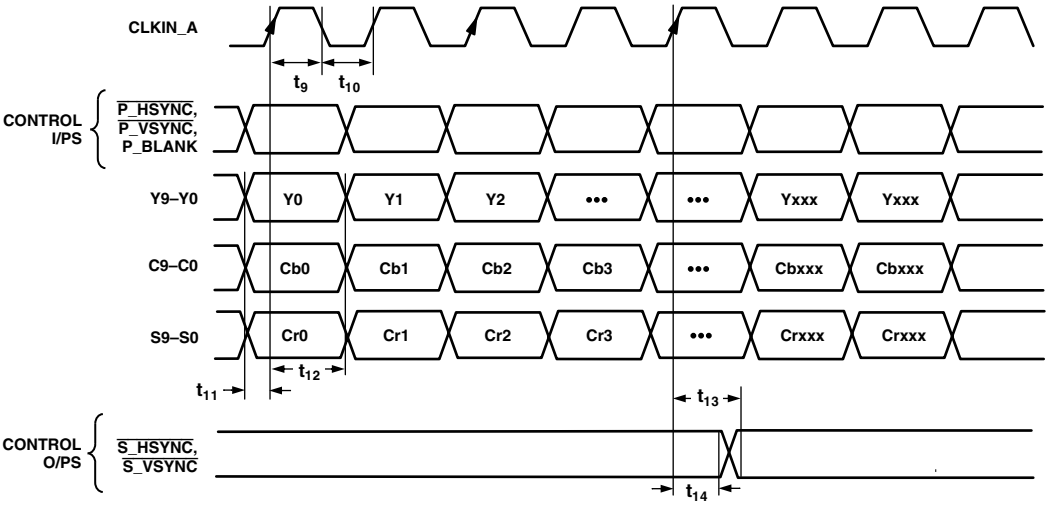
[3]Data: C[9:0]; S[9:0]; Y[9:0]
Control: $\overline{\text{P\_HSYNC}}$; $\overline{\text{P\_ VSYNC}}$; P_BLANK; $\overline{\text{S\_HSYNC}}$; $\overline{\text{S\_VSYNC}}$; $\overline{\text{S\_BLANK}}$

Specifications subject to change without notice.



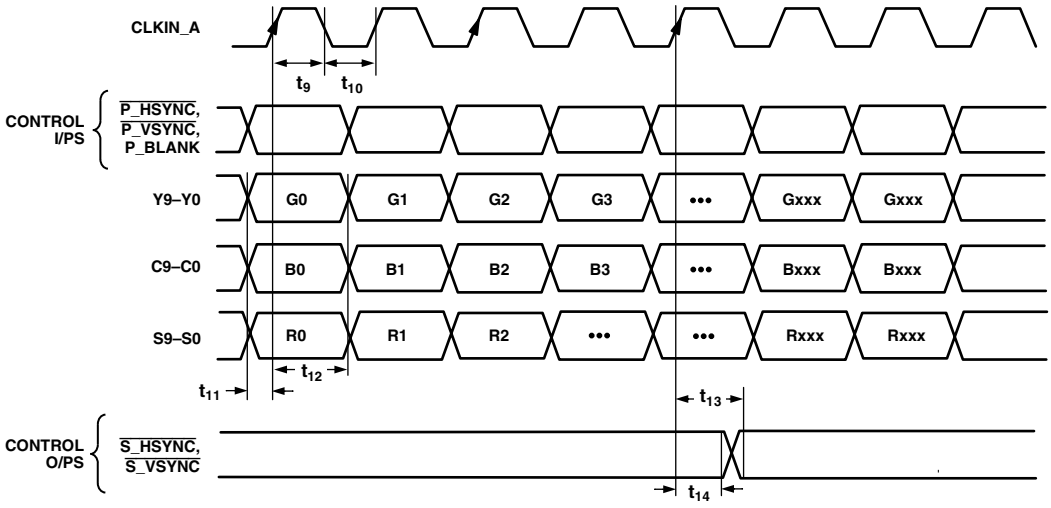
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 2. HD 4:2:2 Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



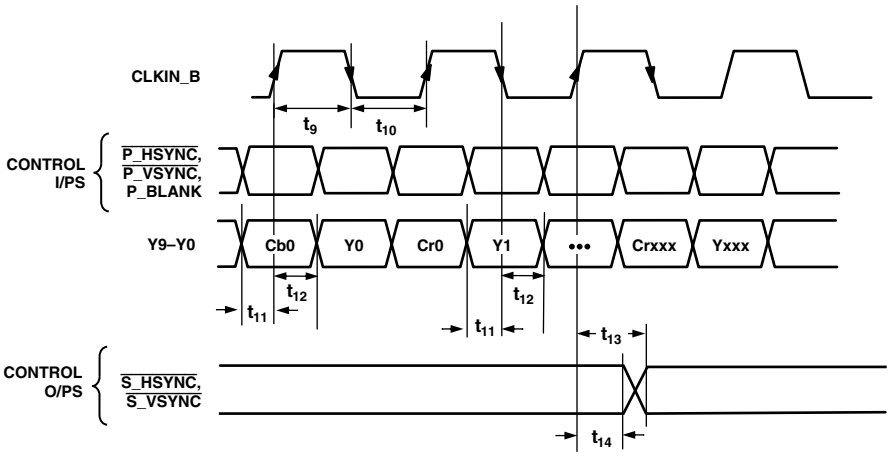
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 3. HD 4:4:4 YCrCb Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



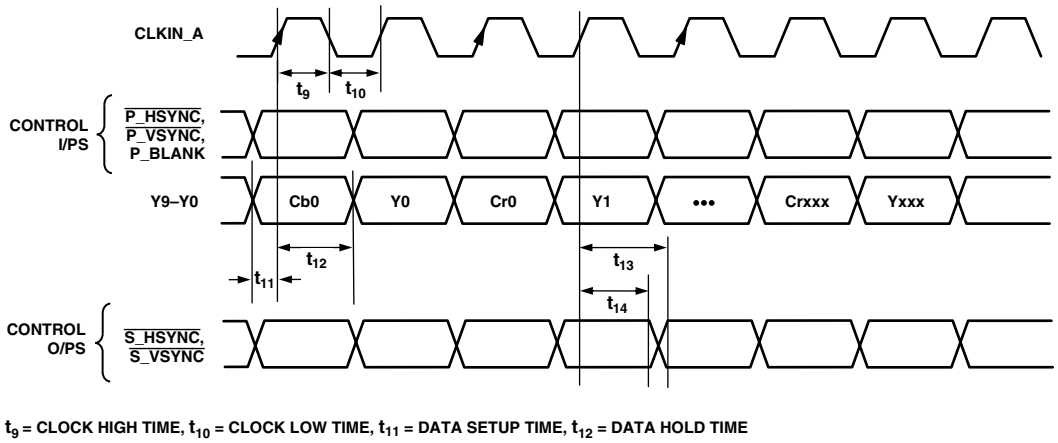
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 4. HD 4:4:4 RGB Input Data Format Timing Diagram, HD RGB Input Enabled (Input Mode at Subaddress 01h = 001 or 010)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 5. PS 4:2:2 1 × 10-Bit Interleaved @ 27 MHz, Input Mode: PS Input Only (Input Mode at Subaddress 01h = 100)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 6. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz, Input Mode: PS 54 MHz Input (Input Mode at Subaddress 01h = 111)

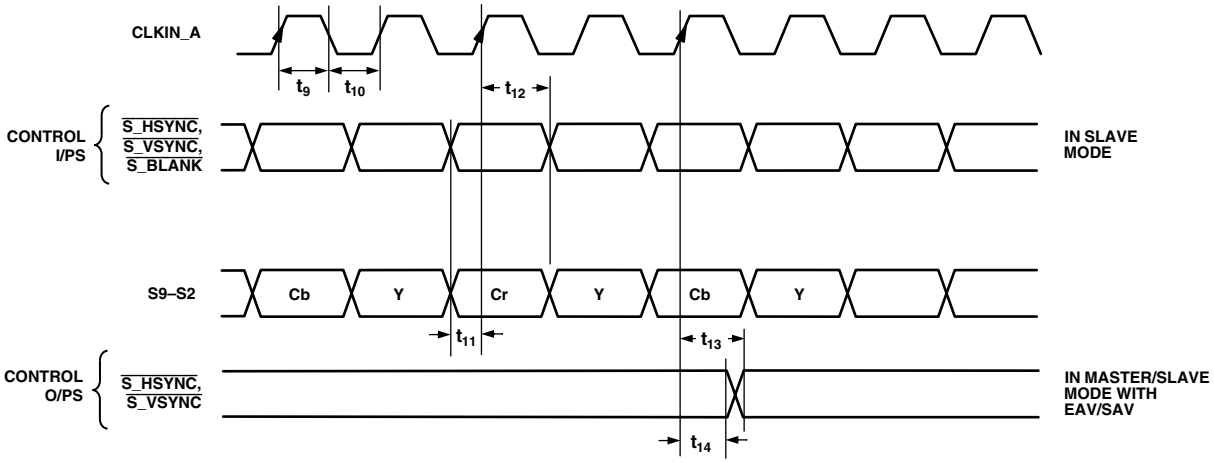


Figure 7. 8-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

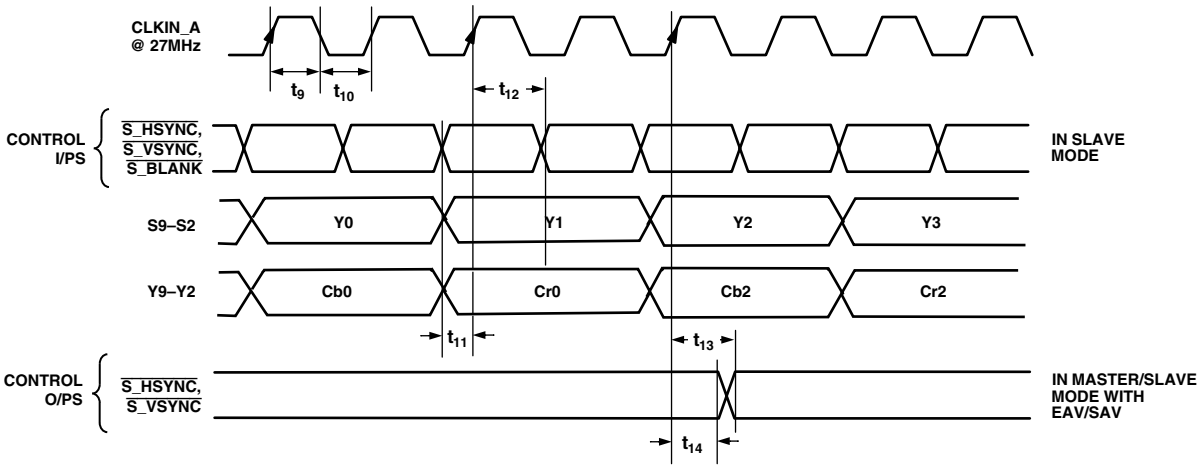


Figure 8. 16-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

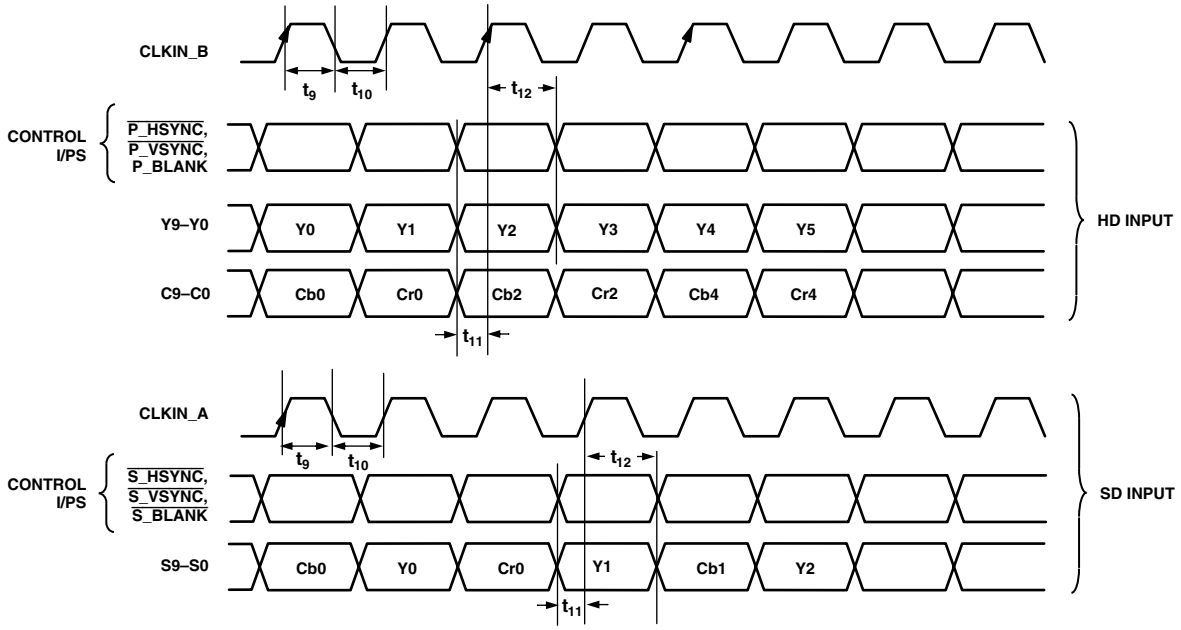


Figure 9. SD and HD Simultaneous Input, Input Mode: SD and PS 20-Bit or SD and HDTV (Input Mode at Subaddress 01h = 011, 101, or 110)

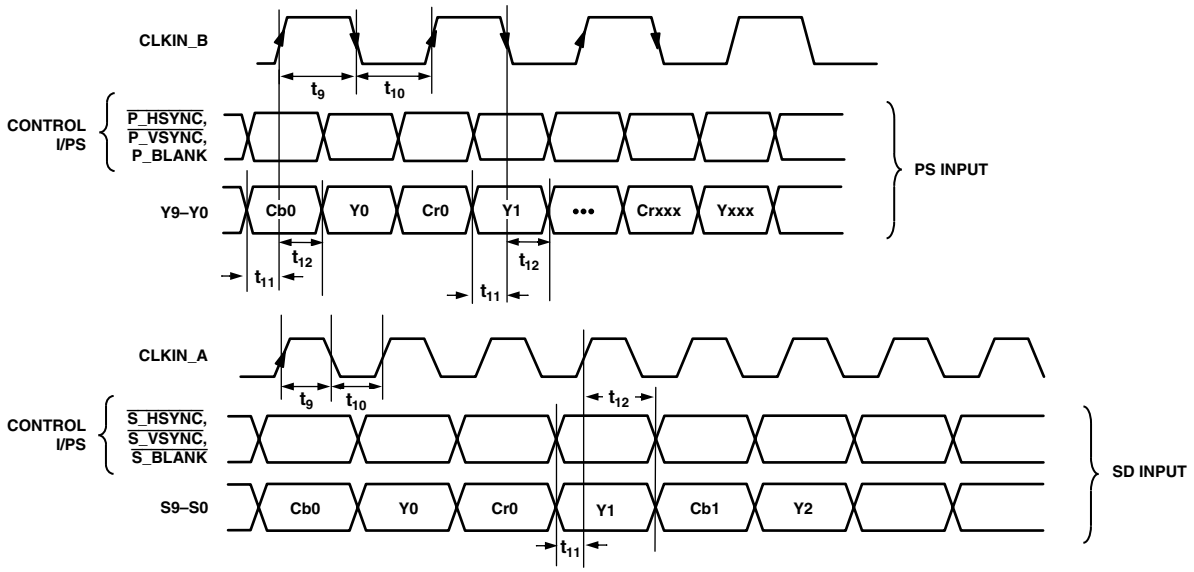


Figure 10. SD and HD Simultaneous Input, Input Mode: SD and PS 10-Bit (Input Mode at Subaddress 01h = 100)

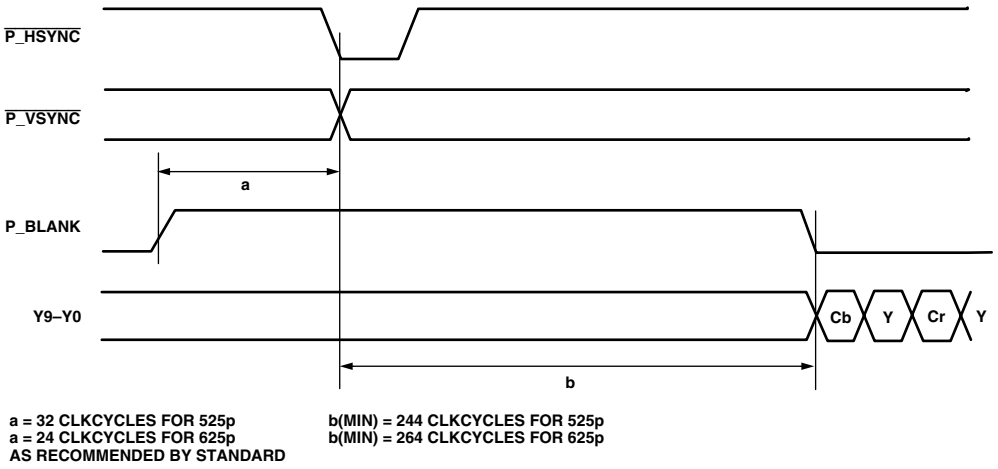
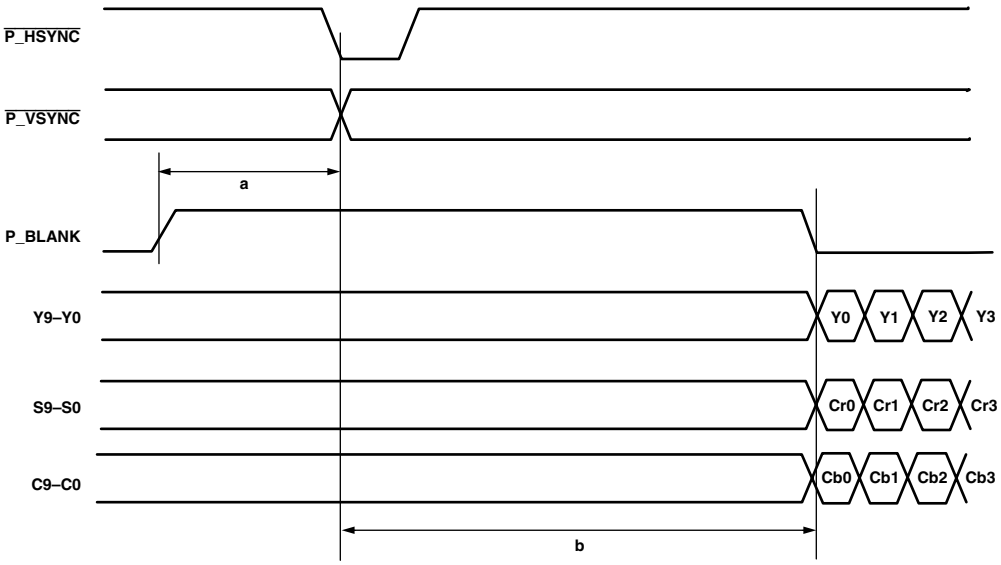


Figure 11. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz Input Timing Diagram



a = 16 CLKCYCLES FOR 525p
a = 12 CLKCYCLES FOR 626p
a = 44 CLKCYCLES FOR 1080i
a = 70 CLKCYCLES FOR 720p
AS RECOMMENDED BY STANDARD

b(MIN) = 122 CLKCYCLES FOR 525p
b(MIN) = 132 CLKCYCLES FOR 625p
b(MIN) = 236 CLKCYCLES FOR 1080i
b(MIN) = 300 CLKCYCLES FOR 720p

Figure 12. HD Input Timing Diagram

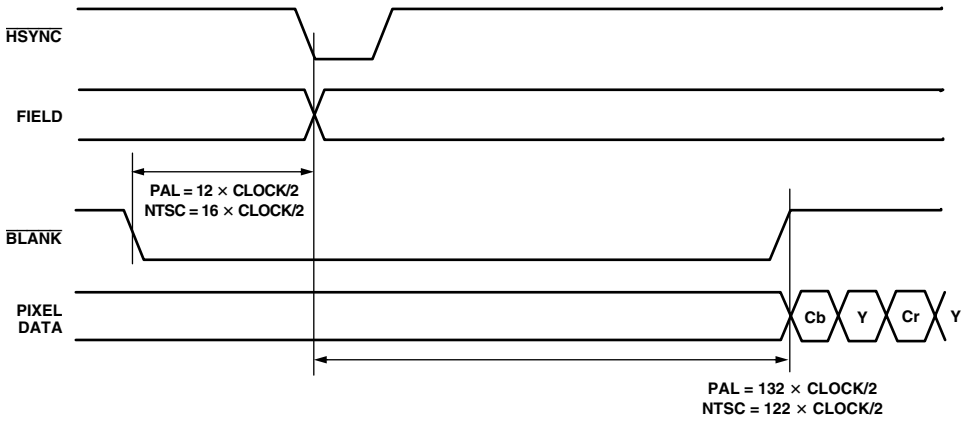


Figure 13. SD Timing Input for Timing Mode 1

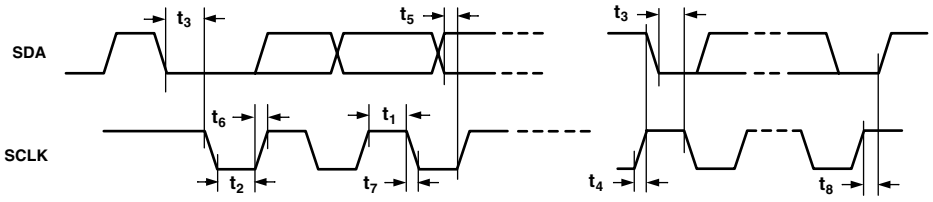


Figure 14. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to AGND . . . . . +3.0 V to –0.3 V
V_{DD} to GND . . . . . +3.0 V to –0.3 V
V_{DD_IO} to IO_GND . . . . . –0.3 V to V_{DD_IO} + 0.3 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Infrared Reflow Soldering (20 sec) . . . . . 260°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JC} = 11°C/W

θ_{JA} = 47°C/W

The ADV7300A/ADV7301A is a lead-free environmentally friendly product. It is manufactured using the most up to date materials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and is able to withstand surface-mount soldering up to 255°C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at conventional reflow temperatures of 220°C to 235°C.

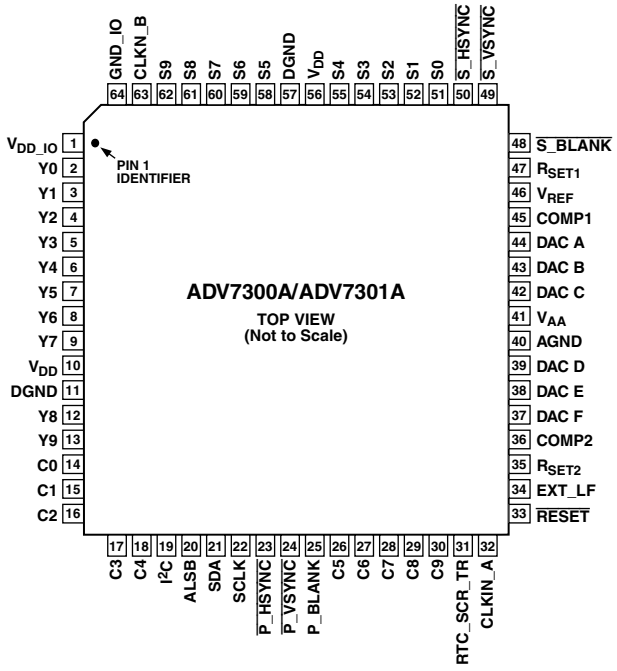
ORDERING GUIDE

Model	Package Description	Package Option
ADV7300AKST	Plastic Quad Flatpack	ST-64B
ADV7301AKST	Plastic Quad Flatpack	ST-64B

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7300A/ADV7301A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/Output	Function
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs
2–9, 12, 13	Y0–Y9	I	10-Bit Progressive Scan/HDTV Input Port for Y Data. The LSBs are set up on Pins Y0 and Y1. In Default Mode, the input on this port is output on DAC D.
10, 56	V_{DD}	P	Digital Power Supply
11, 57	DGND	G	Digital Ground

Pin No.	Mnemonic	Input/Output	Function
14–18, 26–30	C0–C9	I	10-Bit Progressive Scan/HDTV Input Port for CrCb color data in 4:2:2 Input Mode. In 4:4:4 Input Mode, this input port is used for the Cb (Blue/U) data. The LSBs are set up on Pins C0 and C1. In Default Mode, the input on this port is output on DAC E.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7300A/ADV7301A to interface over the I^2C port.
20	ALSB	I/O	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
21	SDA	I/O	MPU Port Serial Data Input/Output
22	SCLK	I	MPU Port Serial Interface Clock Input
23	$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
24	$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
25	P_BLANK	I	Video Blanking Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
31	RTC_SCR_TR	I	Multifunctional Input: Realtime Control (RTC) Input, Timing Reset Input, and Subcarrier Reset Input
32	CLKIN_A	I	Pixel Clock Input for HD Only or SD Only Modes
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7300A/ ADV7301A into default register setting. Reset is an active low signal.
34	EXT_LF	I	External Loop Filter for the internal PLL
35, 47	$R_{SET2, 1}$	I	A 760 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
36, 45	COMP2, 1	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V_{AA}.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output, in HD Only Mode and Simultaneous HD/SD: Pb/Blue (HD) Analog Output
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output, in HD Only Mode and Simultaneous HD/SD: Pr/Red (HD) Analog Output
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output, in HD Only Mode and Simultaneous HD/SD: Y/Green (HD) Analog Output
40	AGND	G	Analog Ground
41	V_{AA}	P	Analog Power Supply
42	DAC C	O	Chroma/Red/V SD Analog Output
43	DAC B	O	Luma/Blue/U SD Analog Output
44	DAC A	O	CVBS/Green/Y SD Analog Output
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
48	$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD
49	$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Control Signal for SD. Option to output SD VSYNC or SD HSYNC in SD Slave Mode 0 and/or any HD Mode.
50	$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Control Signal for SD. Option to output SD HSYNC or HD HSYNC in SD Slave Mode 0 and/or any HD Mode.
51–55, 58–62	S0–S9	I	10-Bit Standard Definition Input Port or Progressive Scan/HDTV Input Port for Cr (Red/V) color data in 4:4:4 Input Mode. The LSBs are set up on Pins S0 and S1. In Default Mode, the input on this port is output on DAC F.
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for Progressive Scan Mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV Mode. This clock input pin is only used in Simultaneous SD/HD Mode.
64	GND_IO		Digital Ground

MPU PORT DESCRIPTION

The ADV7300A/ADV7301A supports a 2-wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCLK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7300A/ADV7301A has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figures 15 and 16. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation, while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7300A/ADV7301A to Logic Level "0" or Logic Level "1." When ALSB is set to "1," there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to "0," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

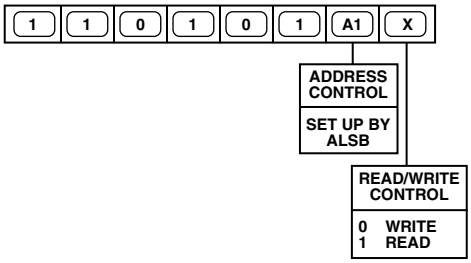


Figure 15. ADV7300A Slave Address = D4h

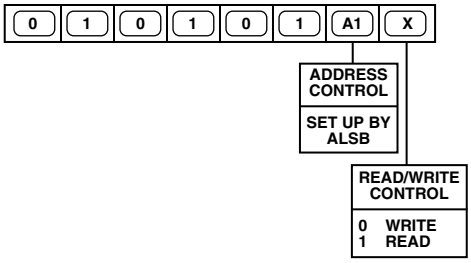


Figure 16. ADV7301A Slave Address = 54h

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCLK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next 8 bits (7-bit address + R/W Bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge Bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCLK lines waiting for the start condition and the correct transmitted address. The R/W Bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7300A/ADV7301A acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W Bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddress's autoincrement allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, it will cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7300A/ADV7301A will not issue an acknowledge and will return to the idle condition. If in Autoincrement Mode the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7300A/ADV7301A, and the part will return to the idle condition.

Before writing to the subcarrier frequency registers, it is a requirement that the ADV7300A/ADV7301A has been reset at least once since power-up.

The four subcarrier frequency registers must be updated starting with subcarrier frequency register 0. The subcarrier frequency will not update until the last subcarrier frequency register byte has been received by the ADV7300A/ADV7301A.

Figure 17 illustrates an example of data transfer for a read sequence and the start and stop conditions.

Figure 18 shows bus write and read sequences.

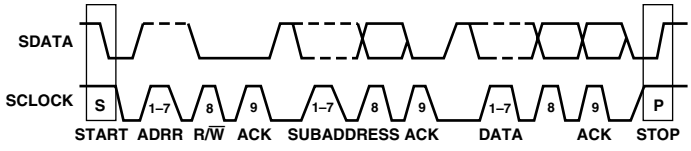


Figure 17. Bus Data Transfer

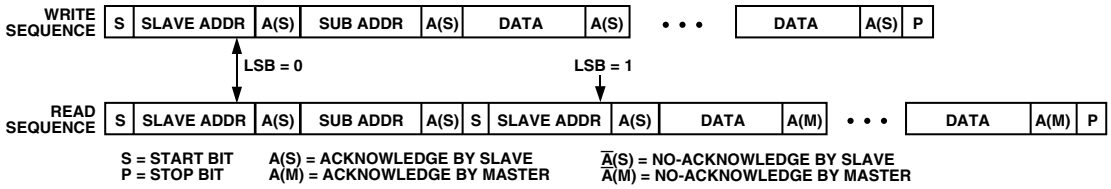


Figure 18. Read and Write Sequence

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7300A/ADV7301A except the subaddress registers that are write-only registers. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Then a read/write operation is performed from/to the target address which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to, unless otherwise stated.

Subaddress Register (SR7–SR0)

The Communications Register is an 8-bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Register Select (SR7–SR0)

These bits are set up to point to the required starting address.

Table I. Power Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
00h	Power Mode Register	Sleep Mode[1]								0	Sleep Mode Off	Fch
										1	Sleep Mode On	
		PLL and Oversampling Control[2]							0		PLL On	
									1		PLL Off	
		DAC F: Power On/Off						0			DAC F Off	
								1			DAC F On	
		DAC E: Power On/Off					0				DAC E Off	
							1				DAC E On	
		DAC D: Power On/Off				0					DAC D Off	
						1					DAC D On	
		DAC C: Power On/Off			0						DAC C Off	
					1						DAC C On	
		DAC B: Power On/Off		0							DAC B Off	
				1							DAC B On	
		DAC A: Power On/Off	0								DAC A Off	
			1								DAC A On	

NOTES
[1]When enabled, the current consumption is reduced to μA level. All DACs and the internal PLL circuit are disabled. I^2C registers can be read from and written to.
[2]This control allows the internal PLL circuit to be powered down and the oversampling to be switched off.

Table II. Input Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
01h	Input Mode Register	BTA T-1004 Compatibility								0	Disabled	38h
										1	Enabled	
		Reserved							0		Zero must be written to this bit.	
		Pixel Align						0			Video input data starts with a Y0 bit. Only for PS Interleaved Mode.	
								1			Video input data starts with a Cb0 bit.	
		Clock Align					0					
							1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns. Only if two input clocks are used.	
		Input Mode		0	0	0					SD Input Only	
				0	0	1					PS Input Only	
				0	1	0					HDTV Input Only	
				0	1	1					SD and PS (20-Bit)	
				1	0	0					SD and PS (10-Bit)	
				1	0	1					SD and HDTV (SD Oversampled)	
				1	1	0					SD and HDTV (HDTV Oversampled)	
				1	1	1					PS 54 MHz Input	
		Reserved	0								Zero must be written to this bit.	

Table III. Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
02h	Mode Register 0	Reserved							0	0	Zero must be written to these bits.	20h
		Test Pattern Black Bar						0			Disabled	
								1			Enabled. 0x11h, Bit 2 must also be enabled.	
		RGB Matrix					0				Disable Programmable RGB Matrix	
							1				Enable Programmable RGB Matrix	
		SYNC on RGB				0					No SYNC	
						1					SYNC on all RGB Outputs	
		RGB/YUV Output			0						RGB Component Outputs	
					1						YUV Component Outputs	
		SD SYNC		0							No SYNC Output	
				1							Output SD SYNCs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$	
		HD SYNC	0								No SYNC Output	
			1								Output HD SYNCs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$	
03h	RGB Matrix 0								X	X	LSB for GY	03h
04h	RGB Matrix 1								X	X	LSB for RV	F0h
							X	X			LSB for BU	
					X	X					LSB for GV	
			X	X							LSB for GU	
05h	RGB Matrix 2		X	X	X	X	X	X	X	X	Bits 9–2 for GY	4Eh
06h	RGB Matrix 3		X	X	X	X	X	X	X	X	Bits 9–2 for GU	0Eh
07h	RGB Matrix 4		X	X	X	X	X	X	X	X	Bits 9–2 for GV	24h
08h	RGB Matrix 5		X	X	X	X	X	X	X	X	Bits 9–2 for BU	92h
09h	RGB Matrix 6		X	X	X	X	X	X	X	X	Bits 9–2 for RV	7Ch
0Ah	Reserved											00h
0Bh	Reserved											00h
0Ch	Reserved											00h
0Dh	Reserved											00h
0Eh	Reserved											00h
0Fh	Reserved											00h

Table IV. HD Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
10h	HD Mode Register 1	HD Output Standard							0	0	EIA770.2 Output	00h
									0	1	EIA770.1 Output	
									1	0	Output Levels for Full Input Range	
									1	1	Reserved	
		HD Input Control Signals					0	0			$\overline{HSYNC}$,$\overline{VSYNC}$, $\overline{BLANK}$	
							0	1			EAV/SAV Codes[1]	
							1	0			Async Timing Mode	
							1	1			Reserved	
		HD 625 p				0					525 p	
						1					625 p	
		HD 720 p			0						1080 i	
					1						720 p	
		HD BLANK Polarity		0							BLANK Active High	
				1							BLANK Active Low	
		HD Macrovision for 525 p/625 p	0								Macrovision Off	
			1								Macrovision On	
11h	HD Mode Register 2	HD Pixel Data Valid								0	Pixel Data Valid Off	00h
										1	Pixel Data Valid On	
									0		Reserved	
		HD Test Pattern Enable						0			HD Test Pattern Off	
								1			HD Test Pattern On	
		HD Test Pattern Hatch/Field					0				Hatch	
							1				Field/Frame	
		HD VBI Open				0					Disabled	
						1					Enabled	
		HD Undershoot Limiter		0	0						Disabled	
				0	1						–11 IRE	
				1	0						–6 IRE	
				1	1						–1.5 IRE	
		HD Sharpness Filter	0								Disabled	
			1								Enabled	
12h	HD Mode Register 3	HDY Delay wrt Falling Edge of HSYNC						0	0	0	0 Clock Cycle	
								0	0	1	1 Clock Cycle	
								0	1	0	2 Clock Cycle	
								0	1	1	3 Clock Cycle	
								1	0	0	4 Clock Cycle	
		HD Color Delay wrt Falling Edge of HSYNC			0	0	0				0 Clock Cycle	
					0	0	1				1 Clock Cycle	
					0	1	0				2 Clock Cycle	
					0	1	1				3 Clock Cycle	
					1	0	0				4 Clock Cycle	
		HD CGMS		0							Disabled	
				1							Enabled	
		HD CGMS CRC	0								Disabled	
			1								Enabled	

Table IV. HD Mode Register (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
13h	HD Mode Register 4	HD Cr/Cb Sequence[2]								0	Cb after Falling Edge of $\overline{\text{HSYNC}}$	4Ch
										1	Cr after Falling Edge of $\overline{\text{HSYNC}}$	
									0		Reserved	
		HD Input Format						0			8-Bit Input	
								1			10-Bit Input	
		Sync Filter on DAC D, E, F					0				Disabled	
							1				Enabled	
						0					Reserved	
		HD Chroma SSAF[2]			0						Disabled	
					1						Enabled	
		HD Chroma Input		0							4:4:4	
				1							4:2:2	
		HD Double Buffering	0								Disabled	
			1								Enabled	
14h	HD Mode Register 5		0	0	0	0	0	0	0	X	A low-high-low transition resets the internal HD timing counters.	00h
15h	HD Mode Register 6	Reserved								0	Zero must be written to this bit.	00h
		HD RGB Input							0		Disabled	
									1		Enabled	
		HD Sync on PrPb						0			Disabled	
								1			Enabled	
		HD Color DAC Swap[3]					0				DAC E = Pr, DAC F = Pb	
							1				DAC F = Pr, DAC E = Pb	
		HD Gamma Curve A/B				0					Gamma Curve A	
						1					Gamma Curve B	
		HD Gamma Curve Enable			0						Disabled	
					1						Enabled	
		HD Adaptive Filter Mode		0							Mode A	
				1							Mode B	
		HD Adaptive Filter Enable	0								Disabled	
			1								Enabled	

NOTES
[1]EAV/SAV codes are not supported for PS 1 × 10-Bit Interleaved Mode at 54 MHz.
[2]4:2:2 Input Format Only
[3]4:4:4 Input Format Only

Table V. Register Settings

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
16h	HD Y Color		X	X	X	X	X	X	X	X	Y Color Value	A0h
17h	HD Cr Color		X	X	X	X	X	X	X	X	Cr Color Value	80h
18h	HD Cb Color		X	X	X	X	X	X	X	X	Cb Color Value	80h
19h	Reserved											00h
1Ah	Reserved											00h
1Bh	Reserved											00h
1Ch	Reserved											00h
1Dh	Reserved											00h
1Eh	Reserved											00h
1Fh	Reserved											00h
20h	HD Sharpness Filter Gain	HD Sharpness Filter Gain Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							…	…	…	…	…	
							1	1	1	1	Gain A = –1	
		HD Sharpness Filter Gain Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			…	…	…	…					…	
			1	1	1	1					Gain B = –1	
21h	HD CGMS Data 0	HD CGMS Data Bits	0	0	0	0	C19	C18	C17	C16	CGMS 19–16	00h
22h	HD CGMS Data 1	HD CGMS Data Bits	C15	C14	C13	C12	C11	C10	C9	C8	CGMS 15–8	00h
23h	HD CGMS Data 2	HD CGMS Data Bits	C7	C6	C5	C4	C3	C2	C1	C0	CGMS 7–0	00h
24h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A0	00h
25h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A1	00h
26h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A2	00h
27h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A3	00h
28h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A4	00h
29h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A5	00h
2Ah	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A6	00h
2Bh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A7	00h
2Ch	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A8	00h
2Dh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A9	00h
2Eh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B0	00h
2Fh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B1	00h
30h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B2	00h
31h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B3	00h
32h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B4	00h
33h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B5	00h
34h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B6	00h

Table VI. HD Adaptive Filters

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
38h	HD Adaptive Filter Gain 1	HD Adaptive Filter Gain 1 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 1 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
39h	HD Adaptive Filter Gain 2	HD Adaptive Filter Gain 2 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 2 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Ah	HD Adaptive Filter Gain 3	HD Adaptive Filter Gain 3 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 3 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Bh	HD Adaptive Filter Threshold A	HD Adaptive Filter Threshold A Value	X	X	X	X	X	X	X	X	Threshold A	00hex
3Ch	HD Adaptive Filter Threshold B	HD Adaptive Filter Threshold B Value	X	X	X	X	X	X	X	X	Threshold B	00hex
3Dh	HD Adaptive Filter Threshold C	HD Adaptive Filter Threshold C Value	X	X	X	X	X	X	X	X	Threshold C	00hex

Table VII. SD Mode Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
3Eh	Reserved											00h
3Fh	Reserved											00h
40h	SD Mode Register 0	SD Standard							0	0	NTSC	00h
									0	1	PAL B, D, G, H, I	
									1	0	PAL M	
									1	1	PAL N	
		SD Luma Filter				0	0	0			LPF NTSC	
						0	0	1			LPF PAL	
						0	1	0			Notch NTSC	
						0	1	1			Notch PAL	
						1	0	0			SSAF Luma	
						1	0	1			Luma CIF	
						1	1	0			Luma QCIF	
						1	1	1			Reserved	
		SD Chroma Filter	0	0	0						1.3 MHz	
			0	0	1						0.65 MHz	
			0	1	0						1.0 MHz	
			0	1	1						2.0 MHz	
			1	0	0						Reserved	
			1	0	1						Chroma CIF	
			1	1	0						Chroma QCIF	
			1	1	1						3.0 MHz	
41h	Reserved											00h
42h	SD Mode Register 1	SD UV SSAF								0	Disabled	08h
										1	Enabled	
		SD DAC Output 1*							0		DAC A, B, C: CVBS, L, C; DAC D, E, F: GBR or YUV	
									1		DAC A, B, C: GBR or YUV; DAC D, E, F: CVBS, L, C	
		SD DAC Output 2						0			Swap DAC A and DAC D Outputs	
								1				
		SD Pedestal					0				Disabled	
							1				Enabled	
		SD Square Pixel				0					Disabled	
						1					Enabled	
		SD VCR FF/RW Sync			0						Disabled	
					1						Enabled	
		SD Pixel Data Valid		0							Disabled	
				1							Enabled	
		SD Active Video Edge	0								Disabled	
			1								Enabled	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
43h	SD Mode Register 2	SD Pedestal YUV Output								0	No Pedestal on YUV	00h
										1	7.5 IRE Pedestal on YUV	
		SD Output Levels Y							0		Y = 700 mV/300 mV	
									1		Y = 714 mV/286 mV	
		SD Output Levels UV					0	0			700 mV p-p [PAL]; 1000 mV p-p [NTSC]	
							0	1			700 mV p-p	
							1	0			1000 mV p-p	
							1	1			648 mV p-p	
		SD VBI Open				0					Disabled	
						1					Enabled	
		SD CC Field Control		0	0						CC Disabled	
				0	1						CC on Odd Field Only	
				1	0						CC on Even Field Only	
				1	1						CC on Both Fields	
			1								Reserved	
44h	SD Mode Register 3	SD VSYNC-3H								0	Disabled	00h
										1	VSYNC = 2.5 lines [PAL]; VSYNC = 3 lines [NTSC]	
		SD RTC/TR/SCR						0	0		Genlock Disabled	
								0	1		Subcarrier Reset	
								1	0		Timing Reset	
								1	1		RTC Enabled	
		SD Active Video Length					0				720 Pixels	
							1				710 (NTSC); 702(PAL)	
		SD Chroma				0					Chroma Enabled	
						1					Chroma Disabled	
		SD Burst			0						Enabled	
					1						Disabled	
		SD Color Bars		0							Disabled	
				1							Enabled	
		Reserved	0								Zero must be written to this bit.	
45h	Reserved											00h
46h	Reserved											00h
47h	SD Mode Register 4	SD UV Scale								0	Disabled	00h
										1	Enabled	
		SD Y Scale							0		Disabled	
									1		Enabled	
		SD Hue Adjust						0			Disabled	
								1			Enabled	
		SD Brightness					0				Disabled	
							1				Enabled	
		SD Luma SSAF Gain				0					Disabled	
						1					Enabled	
		Reserved			0						Zero must be written to this bit.	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
48h	SD Mode Register 5	Reserved								0	Zero must be written to this bit.	
		Reserved							0		Zero must be written to this bit.	00h
		SD Double Buffering						0			Disabled	
								1			Enabled	
		SD Input Format				0	0				8-Bit Input	
						0	1				16-Bit Input	
						1	0				10-Bit Input	
						1	1				20-Bit Input	
		SD Digital Noise Reduction			0						Disabled	
					1						Enabled	
		SD Gamma Control		0							Disabled	
				1							Enabled	
		SD Gamma Curve	0								Gamma Curve A	
			1								Gamma Curve B	
49h	SD Mode Register 6	SD Undershoot Limiter							0	0	Disabled	00h
									0	1	–11 IRE	
									1	0	–6 IRE	
									1	1	–1.5 IRE	
		SD Black Burst Output on DAC Y						0			Disabled	
								1			Enabled	
		SD Black Burst Output on DAC Luma					0				Disabled	
							1				Enabled	
		SD Chroma Delay			0	0					Disabled	
					0	1					4 Clock Cycles	
					1	0					8 Clock Cycles	
					1	1					Reserved	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

*For more detail, see Input and Output Configuration section.

Table VIII. SD Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
4Ah	SD Timing Register 0	SD Slave/Master Mode								0	Slave Mode	08h
										1	Master Mode	
		SD Timing Mode						0	0		Mode 0	
								0	1		Mode 1	
								1	0		Mode 2	
								1	1		Mode 3	
		SD BLANK Input					0				Enabled	
							1				Disabled	
		SD Luma Delay			0	0					No Delay	
					0	1					2 Clock Cycles	
					1	0					4 Clock Cycles	
					1	1					6 Clock Cycles	
		SD Min. Luma Value		0							–40 IRE	
				1							–7.5 IRE	
		SD Timing Reset	X	0	0	0	0	0	0	0	A low-high-low transistion will reset the internal SD timing counters.	
4Bh	SD Timing Register 1	SD HSYNC Width							0	0	Ta = 1 Clock Cycle	00h
									0	1	Ta = 4 Clock Cycles	
									1	0	Ta = 16 Clock Cycles	
									1	1	Ta = 128 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Delay					0	0			Tb = 0 Clock Cycle	
							0	1			Tb = 4 Clock Cycles	
							1	0			Tb = 8 Clock Cycles	
							1	1			Tb = 18 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Rising Edge Delay (Mode 1 Only); VSYNC Width (Mode 2 Only)			X	0					Tc = Tb	
					X	1					Tc = Tb + 32 µs	
					0	0					1 Clock Cycle	
					0	1					4 Clock Cycles	
					1	0					16 Clock Cycles	
					1	1					128 Clock Cycles	
		$\overline{\text{HSYNC}}$ to Pixel Data Adjust	0	0							0 Clock Cycle	
			0	1							1 Clock Cycle	
			1	0							2 Clock Cycles	
			1	1							3 Clock Cycles	
4Ch	SD F_{SC} Register 0		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 7–0	16h
4Dh	SD F_{SC} Register 1		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 15–8	7Ch
4Eh	SD F_{SC} Register 2		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 23–16	F0h
4Fh	SD F_{SC} Register 3		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 31–24	21h
50h	SD F_{SC} Phase		X	X	X	X	X	X	X	X	Subcarrier Phase Bits 9–2	00h
51h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 7–0	00h
52h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 15–8	00h
53h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 7–0	00h
54h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 15–8	00h
55h	SD Pedestal Register 0	Pedestal on Odd Fields	17	16	15	14	13	12	11	10	Setting any of these bits to 1 will disable pedestal on the line number indicated by the bit settings.	00h
56h	SD Pedestal Register 1	Pedestal on Odd Fields	25	24	23	22	21	20	19	18		00h
57h	SD Pedestal Register 2	Pedestal on Even Fields	17	16	15	14	13	12	11	10		00h
58h	SD Pedestal Register 3	Pedestal on Even Fields	25	24	23	22	21	20	19	18		00h