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Multiformat 216 MHz Video Encoder with Six NSV™ 12-Bit DACs

ADV7310/ADV7311

FEATURES

High Definition Input Formats
- 8-/10-, 16-/20-, 24-/30-Bit (4:2:2, 4:4:4) Parallel YCrCb
- Compliant with:
  - SMPTE 293M (525p)
  - BTA T-1004 EDTV2 (525p)
  - ITU-R BT.1358 (625p/525p)
  - ITU-R BT.1362 (625p/525p)
  - SMPTE 274M (1080i) at 30 Hz and 25 Hz
  - SMPTE 296M (720p)
  - RGB in 3×10-Bit 4:4:4 Input Format
- HDTV RGB Supported:
  - RGB, RGBHV
  - Other High Definition Formats Using Async Timing Mode

High Definition Output Formats
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB, RGBHV
- CGMS-A (720p/1080i)
- Macrovision Rev 1.1 (525p/625p)*
- CGMS-A (525p)

Standard Definition Input Formats
- CCIR-656 4:2:2 8-/10-/16-/20-Bit Parallel Input

Standard Definition Output Formats
- Composite NTSC M/N
- Composite PAL M/N/B/D/G/H/I, PAL-60
- SMPTE 170M NTSC Compatible Composite Video
- ITU-R BT.470 PAL Compatible Composite Video
- S-Video (Y/C)
- EuroScart RGB
- Component YPrPb (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1.L1*
  - CGMS/WSS
  - Closed Captioning

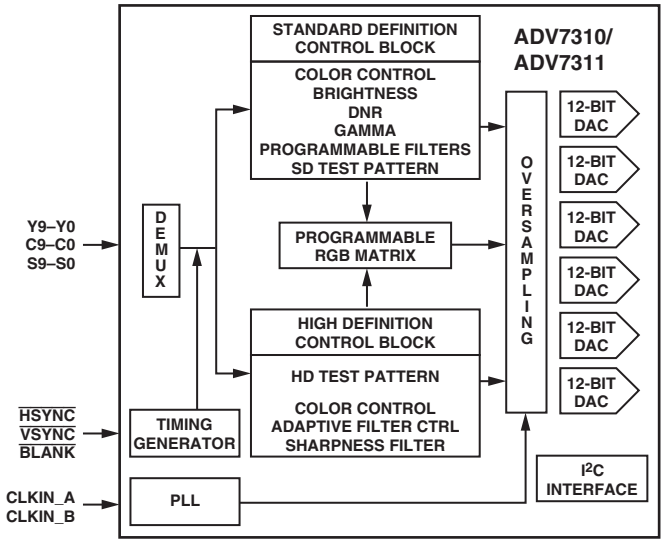
GENERAL FEATURES

Simultaneous SD and HD Inputs and Outputs
Oversampling up to 216 MHz
Programmable DAC Gain Control
Sync Outputs in All Modes
On-Board Voltage Reference
Six 12-Bit NSV Precision Video DACs
2-Wire Serial I²C® Interface
Dual I/O Supply 2.5 V/3.3 V Operation
Analog and Digital Supply 2.5 V
On-Board PLL
64-Lead LQFP Package
Lead (Pb) Free Product

APPLICATIONS

High End DVD
High End PS DVD Recorders/Players
SD/Prog Scan/HDTV Display Devices
SD/HDTV Set Top Boxes
Professional Video Systems

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV®7310/ADV7311 is a high speed, digital-to-analog encoder on a single monolithic chip. It includes six high speed NSV video D/A converters with TTL compatible inputs.

The ADV7310/ADV7311 has separate 8-/10-/16-/20-bit input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical, and blanking signals or EAV/SAV timing codes control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signal.

*ADV7310 Only

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

DETAILED FEATURES

High Definition Programmable Features (720p 1080i)
- **2× Oversampling (148.5 MHz)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Field/Frame)**
- **Fully Programmable YCrCb to RGB Matrix**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Programmable Sharpness Filter Control**
- **CGMS-A (720p/1080i)**

High Definition Programmable Features (525p/625p)
- **8× Oversampling (216 MHz Output)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Frame)**
- **Individual Y and PrPb Output Delay**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Fully Programmable YCrCb to RGB Matrix**
- **Undershoot Limiter**
- **Macrovision Rev 1.1 (525p/625p)***
- **CGMS-A (525p)**

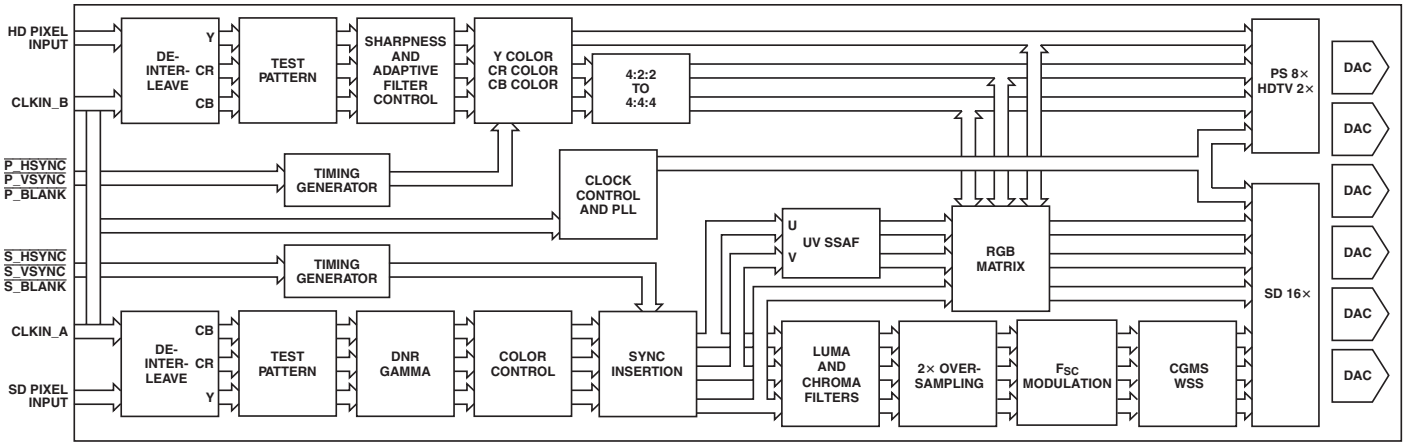
Standard Definition Programmable Features
- **16× Oversampling (216 MHz)**
- **Internal Test Pattern Generator (Color Bars, Black Bar)**
- **Controlled Edge Rates for Sync, Active Video**
- **Individual Y and PrPb Output Delay**
- **Gamma Correction**
- **Digital Noise Reduction (DNR)**
- **Multiple Chroma and Luma Filters**
- **Luma-SSAF™ Filter with Programmable Gain/Attenuation**
- **PrPb SSAF™**
- **Separate Pedestal Control on Component and Composite/S-Video Output**
- **VCR FF/RW Sync Mode**
- **Macrovision Rev 7.1.L1***
- **CGMS/WSS**
- **Closed Captioning**

Standards Directly Supported

Resolution	Frame Rate (Hz)	Clk Input (MHz)	Standard
720 × 480	29.97	27	ITU-R BT.656
720 × 576	25	27	ITU-R BT.656
720 × 483	59.94	27	SMPTE 293M
720 × 480	59.94	27	BTA T-1004
720 × 576	50	27	ITU-R BT.1362
1280 × 720	60	74.25	SMPTE 296M
1920 × 1080	30	74.25	SMPTE 274M
1920 × 1080	25	74.25	SMPTE 274M*

Other standards are supported in Async Timing Mode.
*SMPTE 274M-1998: System no. 6

DETAILED FUNCTIONAL BLOCK DIAGRAM



TERMINOLOGY

SD Standard Definition Video, conforming to ITU-R BT.601/ITU-R BT.656.

HD High Definition Video, i.e., Progressive Scan or HDTV.

PS Progressive Scan Video, conforming to SMPTE 293M, ITU-R BT.1358, BTAT-1004EDTV2, or BTA1362.

HDTV High Definition Television Video, conforming to SMPTE 274M or SMPTE 296M.

YCrCb SD, PS, or HD Component Digital Video.

YPrPb SD, PS, or HD Component Analog Video.

*ADV7310 Only

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ADV7310/ADV7311–SPECIFICATIONS (V_{AA} = 2.375 V–2.625 V, V_{DD} = 2.375 V–2.625 V; V_{DD_IO} = 2.375–3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		12		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity[2], +ve		0.25		LSB	
Differential Nonlinearity[2], –ve		1.5		LSB	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4[2.0][3]			V	I_{SOURCE} = 400 µA
Three-State Leakage Current		±1.0		µA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		3		µA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	4.1	4.33	4.6	mA	
Output Current Range	4.1	4.33	4.6	mA	
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Internal Reference Range, V_{REF}	1.15	1.235	1.3	V	
External Reference Range, V_{REF}	1.15	1.235	1.3	V	
V_{REF} Current[4]		±10		µA	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[5]		170		mA	SD Only [16×]
		110		mA	PS Only [8×]
		95		mA	HDTV Only [2×]
		172	190[8]	mA	SD[16×, 10-bit] + PS[8×, 20-bit]
I_{DD_IO}		1.0		mA	
I_{AA}[6, 7]		39	45	mA	
Sleep Mode					
I_{DD}		200		µA	
I_{AA}		10		µA	
I_{DD_IO}		250		µA	
POWER SUPPLY REJECTION RATIO		0.01		% / %	

NOTES

[1]Oversampling disabled. Static DAC performance will be improved with increased oversampling ratios.

[2]DNL measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step value lies below the ideal step value.

[3]Value in brackets for V_{DD_IO} = 2.375 V–2.75 V.

[4]External current required to overdrive internal V_{REF}.

[5]I_{DD}, the circuit current, is the continuous current required to drive the digital core.

[6]I_{AA} is the total current required to supply all DACs including the V_{REF} circuitry and the PLL circuitry.

[7]All DACs on.

[8]Guaranteed maximum by characterization.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (V_{AA} = 2.375 V–2.625 V, V_{DD} = 2.375 V–2.625 V; V_{DD_IO} = 2.375 V–3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
PROGRESSIVE SCAN MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		65.6		dB	Luma ramp unweighted
		72		dB	Flat field full bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
STANDARD DEFINITION MODE					
Hue Accuracy		0.2		°	
Color Saturation Accuracy		0.20		%	
Chroma Nonlinear Gain		0.84		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		–0.2		±°	
Chroma/Luma Intermodulation		0		±%	
Chroma/Luma Gain Inequality		96.7		±%	
Chroma/Luma Delay Inequality		–1.0		ns	
Luminance Nonlinearity		0.2		±%	
Chroma AM Noise		84		dB	
Chroma PM Noise		75.3		dB	
Differential Gain		0.25		%	NTSC
Differential Phase		0.2		°	NTSC
SNR		63.5		dB	Luma ramp
		77.7		dB	Flat field full bandwidth

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{AA} = 2.375 V–2.625 V, V_{DD} = 2.375 V–2.625 V; V_{DD_IO} = 2.375 V–3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First clock generated after this period
Setup Time (Start Condition), t_4	0.6			µs	relevant for repeated start condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
RESET Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		7		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			27	MHz	Progressive scan mode
f_{CLK}		81		MHz	HDTV mode/async mode
Clock High Time, t_9	40			% of one clk cycle	
Clock Low Time, t_{10}	40			% of one clk cycle	
Data Setup Time, t_{11}[1]	2.0			ns	
Data Hold Time, t_{12}[1]	2.0			ns	
SD Output Access Time, t_{13}			15	ns	
SD Output Hold Time, t_{14}	5.0			ns	
HD Output Access Time, t_{13}			14	ns	
HD Output Hold Time, t_{14}	5.0			ns	
PIPELINE DELAY[4]		63		clk cycles	SD [2×, 16×]
		76		clk cycles	SD component mode [16×]
		35		clk cycles	PS [1×]
		41		clk cycles	PS [8×]
		36		clk cycles	HD[2×, 1×]

NOTES

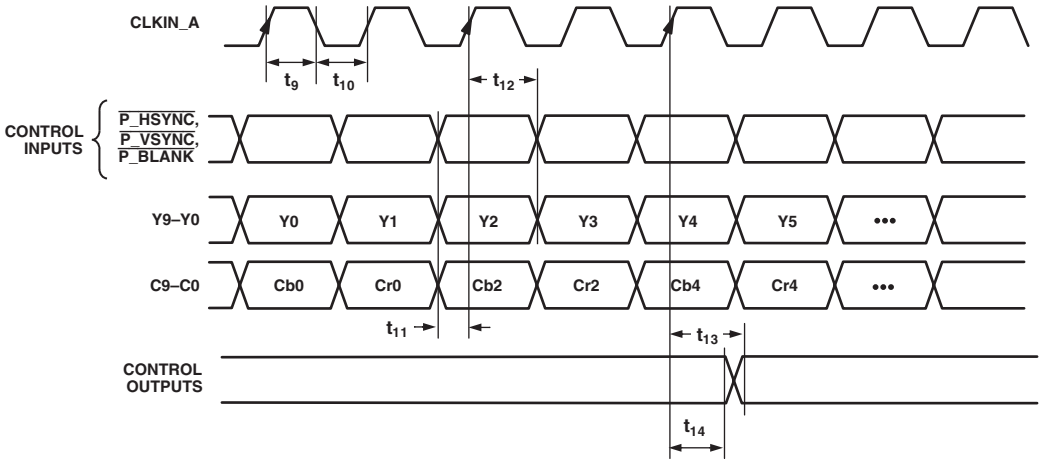
[1]Guaranteed by characterization.

[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

[3]Data: C[9:0]; Y[9:0], S[9:0]
Control: $\overline{\text{P\_HSYNC}}$, $\overline{\text{P\_VSYNC}}$, $\overline{\text{P\_BLANK}}$, $\overline{\text{S\_HSYNC}}$, $\overline{\text{S\_VSYNC}}$, $\overline{\text{S\_BLANK}}$.

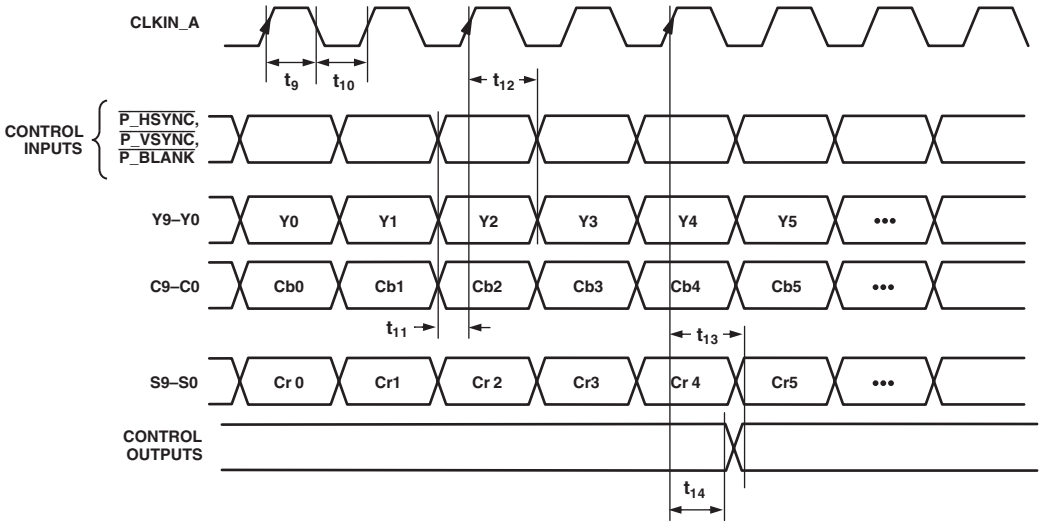
[4]SD, PS = 27 MHz, HD = 74.25 MHz.

Specifications subject to change without notice.



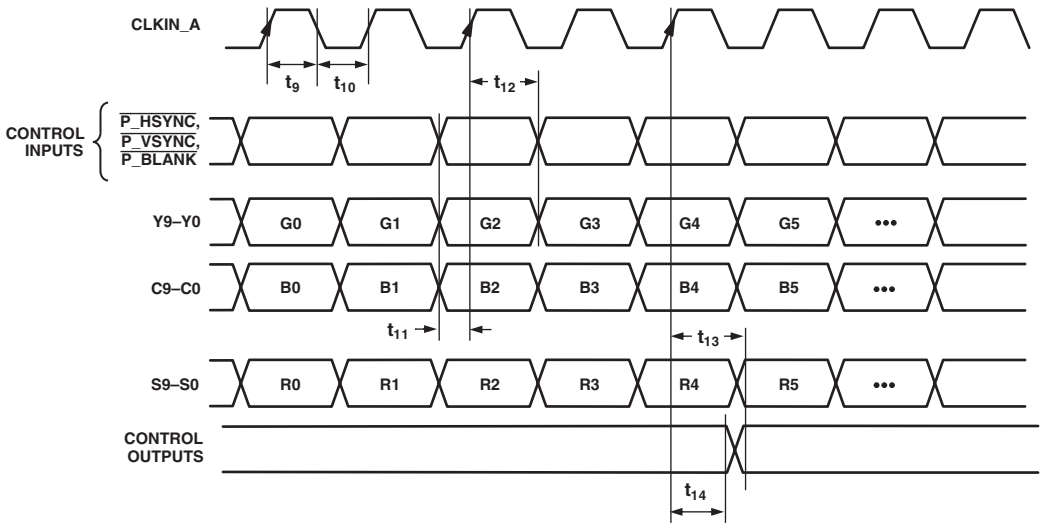
t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

Figure 1. HD Only 4:2:2 Input Mode [Input Mode 010]; PS Only 4:2:2 Input Mode [Input Mode 001]



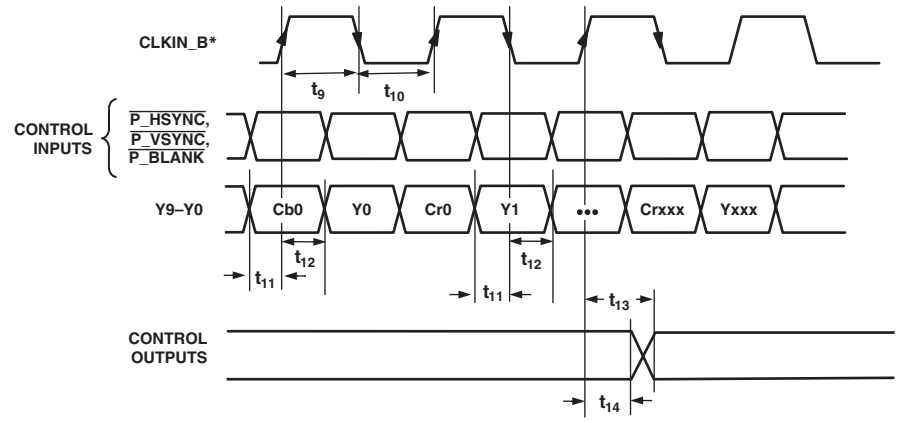
t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

Figure 2. HD Only 4:4:4 Input Mode [Input Mode 010]; PS Only 4:4:4 Input Mode [Input Mode 001]



t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

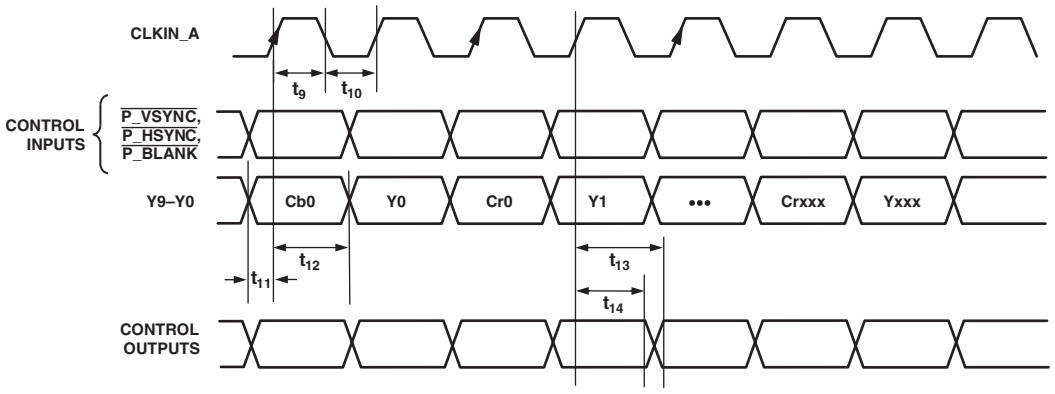
Figure 3. HD RGB 4:4:4 Input Mode [Input Mode 010]



t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

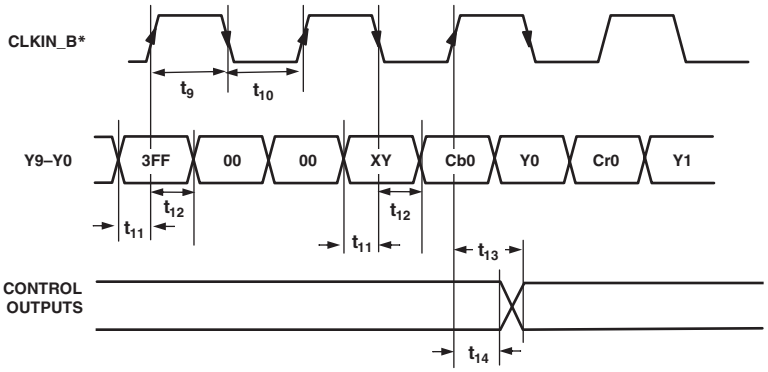
*CLKIN_B MUST BE USED IN THIS PS MODE.

Figure 4. PS 4:2:2 10-Bit Interleaved at 27 MHz $\overline{HSYNC}$/$\overline{VSYNC}$ Input Mode [Input Mode 100]



t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

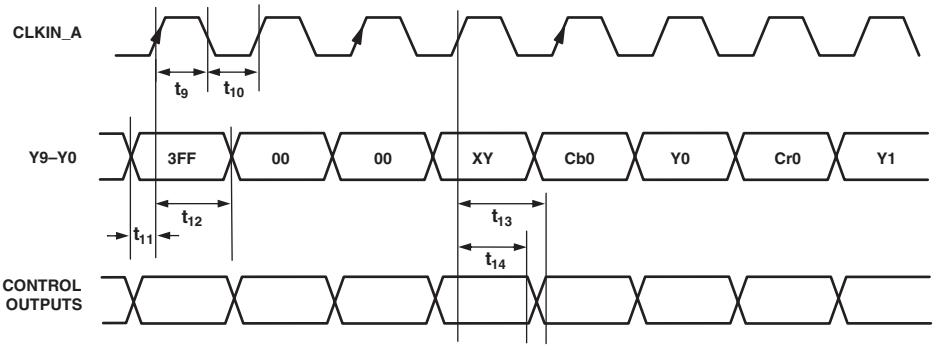
Figure 5. PS 4:2:2 1 × 10-Bit Interleaved at 54 MHz $\overline{HSYNC}$/$\overline{VSYNC}$ Input Mode [Input Mode 111]



t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

*CLKIN_B USED IN THIS PS ONLY MODE.

Figure 6. PS Only 4:2:2 1 × 10-Bit Interleaved at 27 MHz EAV/SAV Input Mode [Input Mode 100]



t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME

NOTE: Y0, Cb0 SEQUENCE AS PER SUBADDRESS 0 × 01 BIT-1

Figure 7. PS Only 4:2:2 1 × 10-Bit Interleaved at 54 MHz EAV/SAV Input Mode [Input Mode 111]

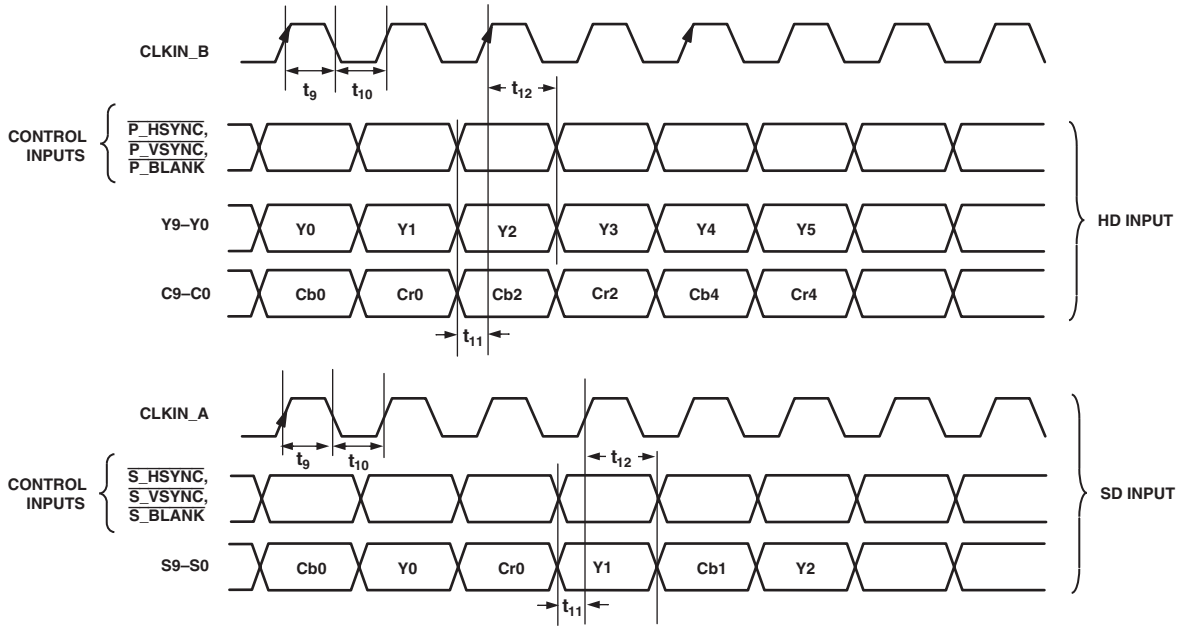


Figure 8. HD 4:2:2 and SD (10-Bit) Simultaneous Input Mode [Input Mode 101: SD Oversampled] [Input Mode 110: HD Oversampled]

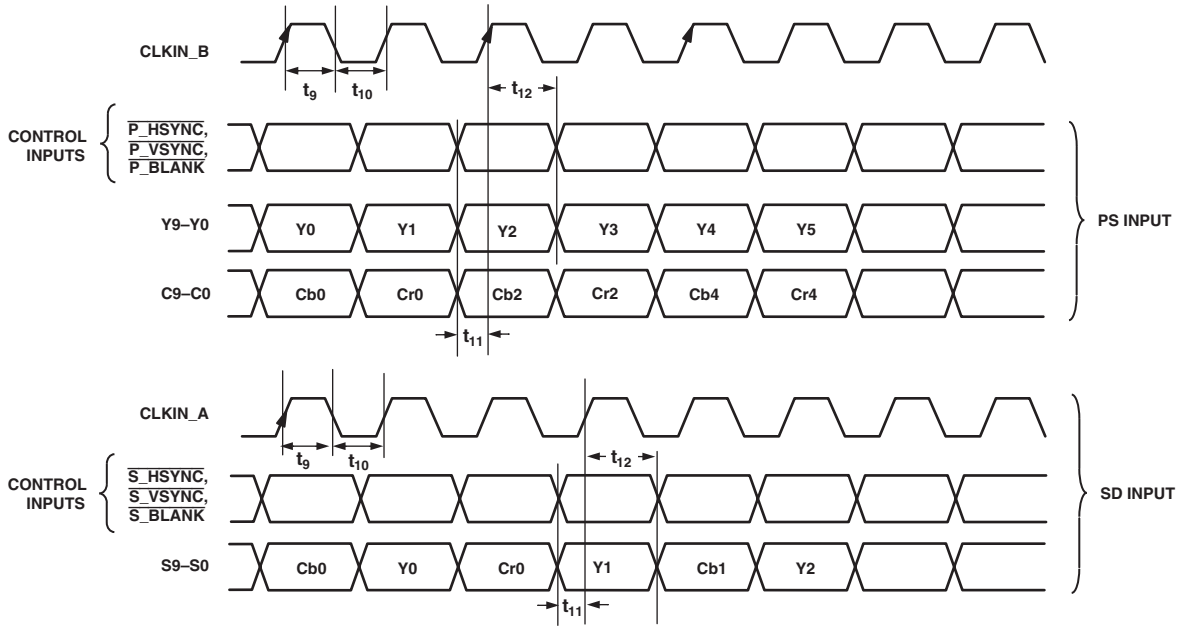


Figure 9. PS (4:2:2) and SD (10-Bit) Simultaneous Input Mode [Input Mode 011]

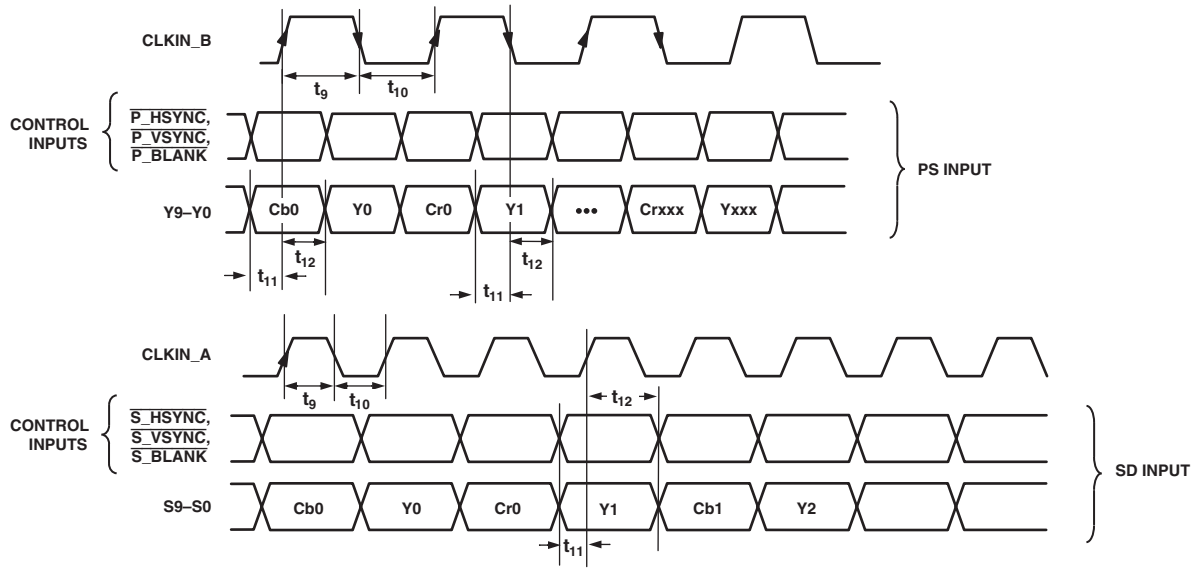


Figure 10. PS (10-Bit) and SD (10-Bit) Simultaneous Input Mode [Input Mode 100]

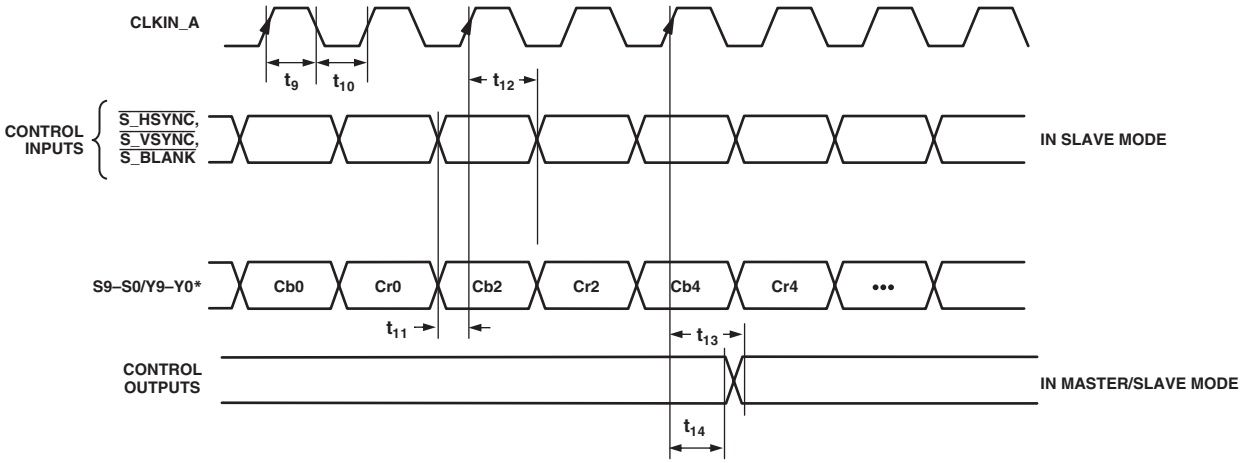


Figure 11. 10-/8-Bit SD Only Pixel Input Mode [Input Mode 000]

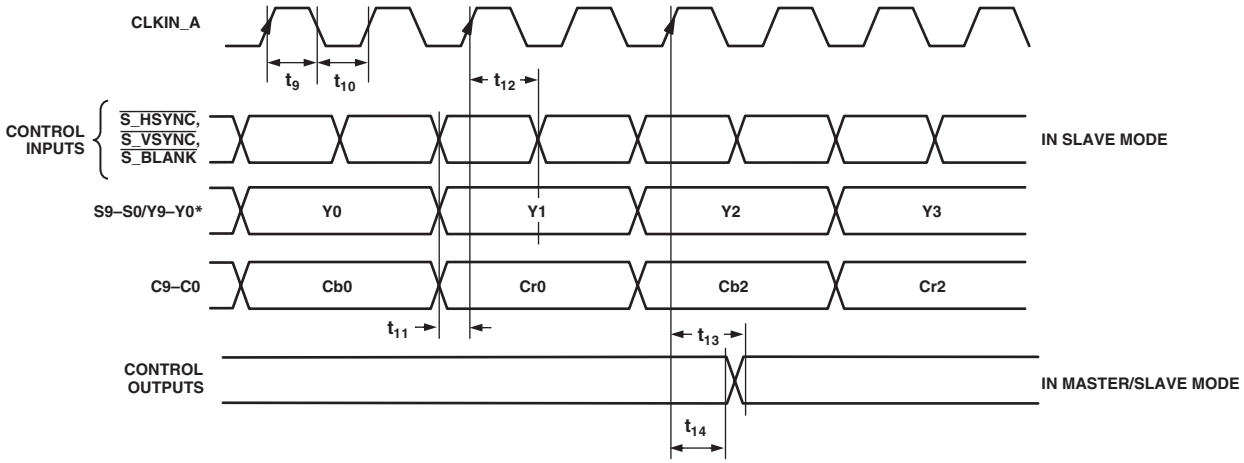
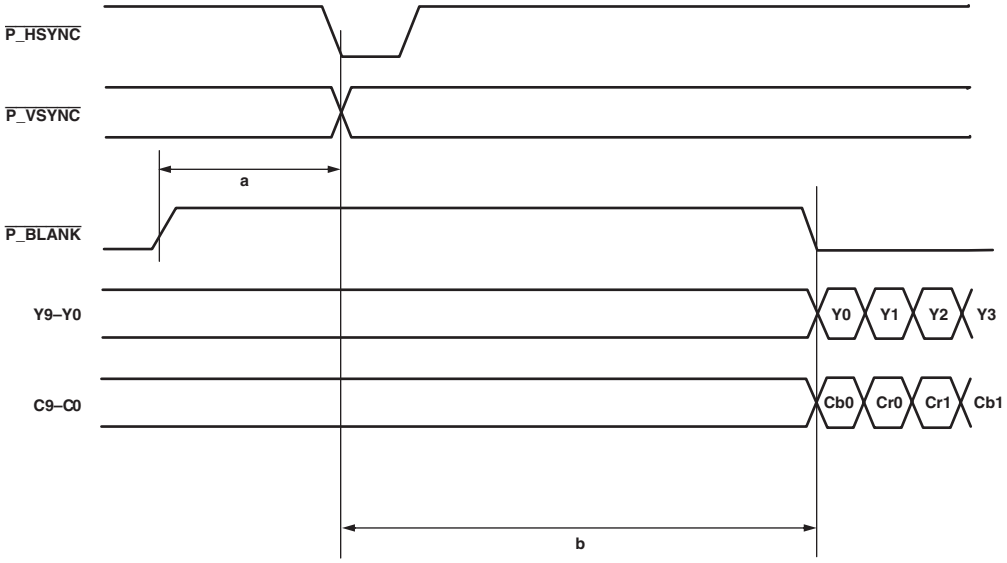


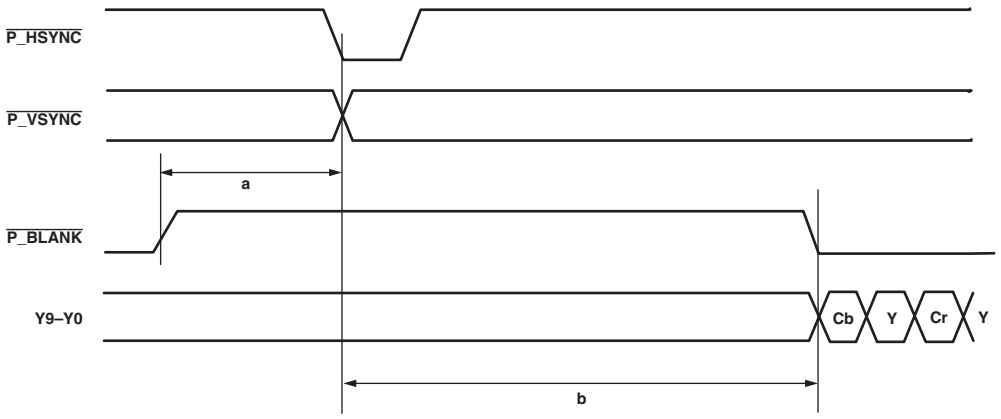
Figure 12. 20-/16-Bit SD Only Pixel Input Mode [Input Mode 000]



a = 16 CLKCYCLES FOR 525p
a = 12 CLKCYCLES FOR 626p
a = 44 CLKCYCLES FOR 1080i @ 30Hz, 25Hz
a = 70 CLKCYCLES FOR 720p
AS RECOMMENDED BY STANDARD

b(MIN) = 122 CLKCYCLES FOR 525p
b(MIN) = 132 CLKCYCLES FOR 625p
b(MIN) = 236 CLKCYCLES FOR 1080i @ 30Hz, 25Hz
b(MIN) = 300 CLKCYCLES FOR 720p

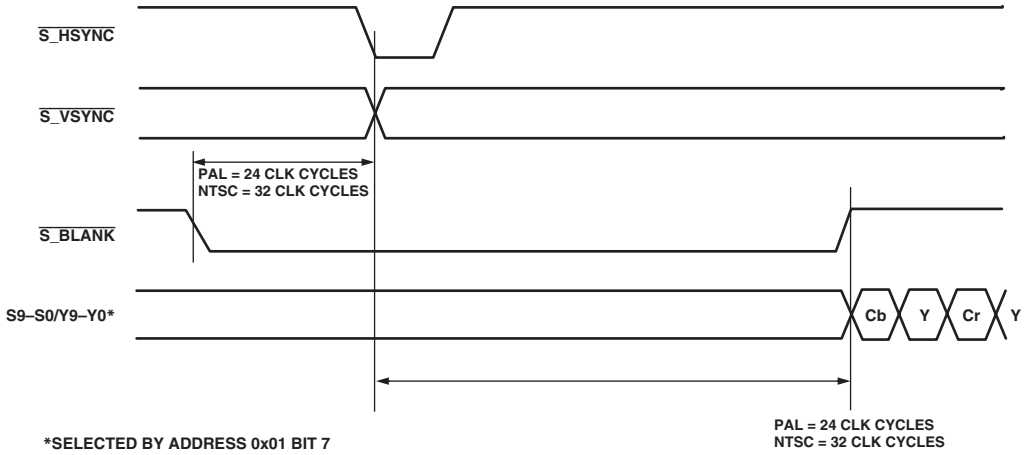
Figure 13. HD 4:2:2 Input Timing Diagram



a = 32 CLKCYCLES FOR 525p
a = 24 CLKCYCLES FOR 625p
AS RECOMMENDED BY STANDARD

b(MIN) = 244 CLKCYCLES FOR 525p
b(MIN) = 264 CLKCYCLES FOR 625p

Figure 14. PS 4:2:2 1 × 10-Bit Interleaved Input Timing Diagram



*SELECTED BY ADDRESS 0x01 BIT 7

Figure 15. SD Timing Input for Timing Mode 1

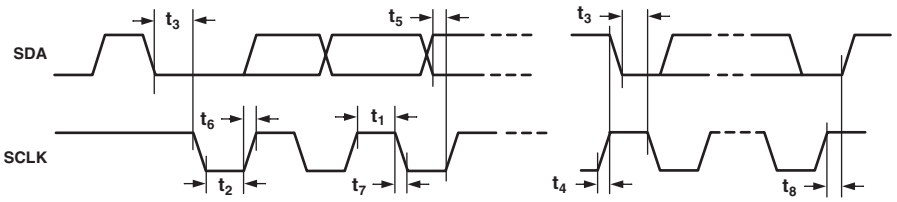


Figure 16. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to AGND . . . . . +3.0 V to –0.3 V
V_{DD} to GND . . . . . +3.0 V to –0.3 V
V_{DD_IO} to IO_GND . . . . . –0.3 V to V_{DD_IO} to +0.3 V
Ambient Operating Temperature (T_A) . . . . . 0°C to 70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Infrared Reflow Soldering (20 sec) . . . . . 260°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JC} = 11°C/W
θ_{JA} = 47°C/W

The ADV7310/ADV7311 is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and is able to withstand surface-mount soldering at up to 255°C (±5°C).

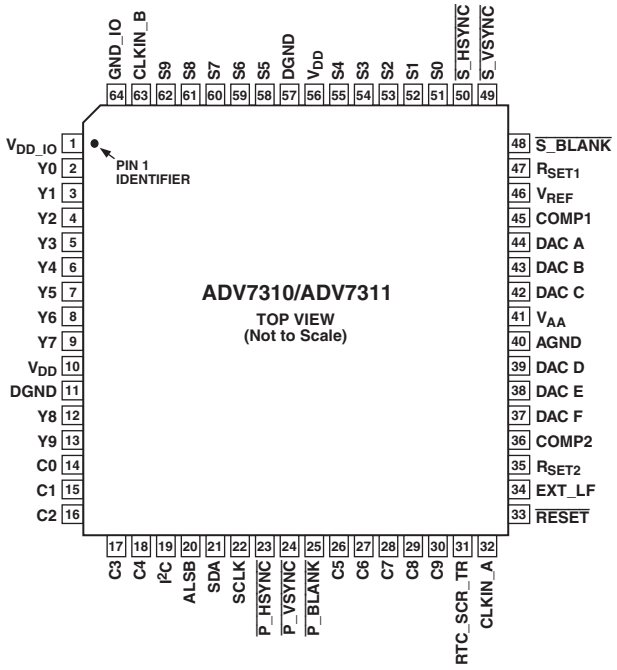
In addition it is backward compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ORDERING GUIDE*

Model	Package Description	Package Option
ADV7310KST	Plastic Quad Flat Package	ST-64
ADV7311KST	Plastic Quad Flat Package	ST-64
EVAL-ADV7310EB	Evaluation Board	
EVAL-ADV7311EB	Evaluation Board	

*Analog output short circuit to any power supply or common can be of an indefinite duration.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7310/ADV7311 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Mnemonic	Input/Output	Function
DGND	G	Digital Ground.
AGND	G	Analog Ground.
CLKIN_A	I	Pixel Clock Input for HD (74.25 MHz Only, PS Only (27 MHz), SD Only (27 MHz).
CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for progressive scan mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
COMP1,2	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V_{AA}.
DAC A	O	CVBS/Green/Y/Y Analog Output.
DAC B	O	Chroma/Blue/U/Pb Analog Output.
DAC C	O	Luma/Red/V/Pr Analog Output.
DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Y/Green [HD] Analog Output.
DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pr/Red Analog Output.
DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pb/Blue [HD] Analog Output.
$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{P\_BLANK}}$	I	Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD Only.
$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Sync Control Signal for SD Only.
$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Sync Control Signal for SD Only.
Y9–Y0	I	SD or Progressive Scan/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0. For 8-bit data input, LSB is set up on Y2.
C9–C0	I	Progressive Scan/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb[Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
S9–S0	I	SD or Progressive Scan/HDTV Input Port for Cr[Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7310/ADV7311 into default register setting. $\overline{\text{RESET}}$ is an active low signal.
$R_{SET1,2}$	I	A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
SCLK	I	I^2C Port Serial Interface Clock Input.
SDA	I/O	I^2C Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal sets up the LSB of the I^2C address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs.
V_{DD}	P	Digital Power Supply.
V_{AA}	P	Analog Power Supply.
V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
EXT_LF	I	External Loop Filter for the Internal PLL.
RTC_SCR_TR	I	Multifunctional Input. Real time control (RTC) input, timing reset input, subcarrier reset input.
I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7310/ADV7311 to interface over the I^2C port.
GND_IO		Digital Input/Output Ground.

MPU PORT DESCRIPTION

The ADV7310/ADV7311 support a 2-wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the ADV7310/ADV7311. Each slave device is recognized by a unique address. The ADV7310/ADV7311 have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 17. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7310/ADV7311 to Logic 0 or Logic 1. When ALSB is set to 1, there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to 0, there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

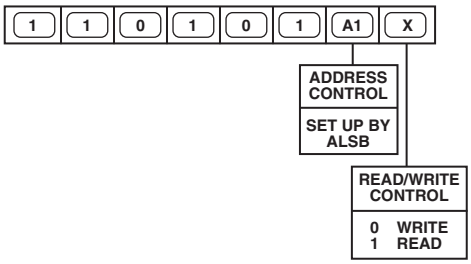


Figure 17. ADV7310 Slave Address = D4h

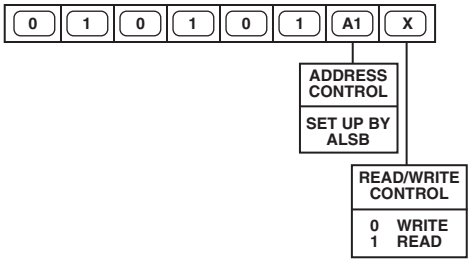


Figure 18. ADV7311 Slave Address = 54h

To control the various devices on the bus, the following protocol must be followed. First the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master will write information to the peripheral. A Logic 1 on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7310/ADV7311 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then they cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7310/ADV7311 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode the user exceeds the highest subaddress, the following action will be taken:

1. In read mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is when the SDA line is not pulled low on the ninth pulse.
2. In write mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7310/ADV7311, and the part will return to the idle condition.

Before writing to the subcarrier frequency registers, it is a requirement that the ADV7310/ADV7311 has been reset at least once after power-up.

The four subcarrier frequency registers must be updated, starting with subcarrier frequency register 0 through subcarrier frequency register 3. The subcarrier frequency will not update until the last subcarrier frequency register byte has been received by the ADV7310/ADV7311.

Figure 19 illustrates an example of data transfer for a write sequence and the start and stop conditions. Figure 20 shows bus write and read sequences.

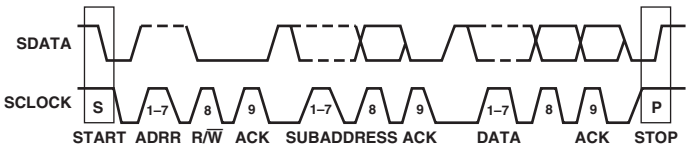


Figure 19. Bus Data Transfer

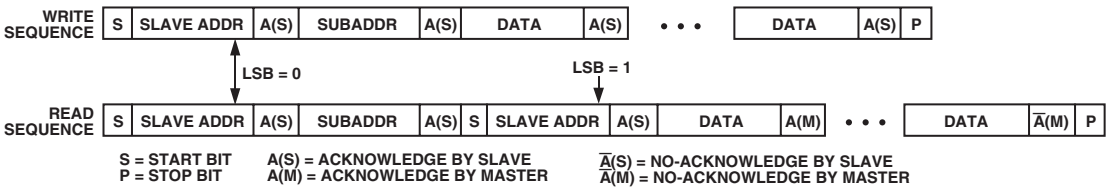


Figure 20. Read and Write Sequence

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7310/ADV7311 except the subaddress registers, which are write only registers. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is then performed from/to the target address, which increments to the next address until a stop command is performed on the bus.

Register Programming

The following tables describe the functionality of each register. All registers can be read from as well as written to, unless otherwise stated.

Subaddress Register (SR7–SR0)

The communications register is an 8-bit write only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place.

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Register Reset Values (Shaded)
00h	Power Mode Register	Sleep Mode. With this control enabled, the current consumption is reduced to μA level. All DACs and the internal PLL cct are disabled. I^2C registers can be read from and written to in Sleep Mode.								0	Sleep Mode off	FCh
										1	Sleep Mode on	
		PLL and Oversampling Control. This control allows the internal PLL cct to be powered down and the over-sampling to be switched off.							0		PLL on	
									1		PLL off	
		DAC F: Power On/Off						0			DAC F off	
								1			DAC F on	
		DAC E: Power On/Off					0				DAC E off	
							1				DAC E on	
		DAC D: Power On/Off				0					DAC D off	
						1					DAC D on	
		DAC C: Power On/Off			0						DAC D off	
					1						DAC C on	
		DAC B: Power On/Off		0							DAC B off	
				1							DAC B on	
		DAC A: Power On/Off	0								DAC A off	
			1								DAC A on	
01h	Mode Select Register	BTA T-1004 or BT.1362 Compatibility								0	Disabled	Only for PS dual edge clk mode
										1	Enabled	
		Clock Edge							0		Cb clocked on rising edge	Only for PS interleaved input at 27 MHz
									1		Y clocked on rising edge	
		Reserved						0				
		Clock Align					0					
							1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns.	Only if two input clocks are used
		Input Mode		0	0	0					SD input only	38h
				0	0	1					PS input only	
				0	1	0					HDTV input only	
				0	1	1					SD and PS [20-bit]	
				1	0	0					SD and PS [10-bit]	
				1	0	1					SD and HDTV [SD oversampled]	
				1	1	0					SD and HDTV [HDTV oversampled]	
				1	1	1					PS only [at 54 MHz]	
		Y/S Bus Swap	0								10-bit data on S bus	SD Mode 10-bit/20-bit Modes
			1								10-bit data on Y bus	

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
02h	Mode Register 0	Reserved							0	0	Zero must be written to these bits	20h
		Test Pattern Black Bar						0			Disabled	
								1			Enabled	0x11h, Bit 2 must also be enabled
		RGB Matrix					0				Disable Programmable RGB matrix	
							1				Enable Programmable RGB matrix	
		Sync on RGB[1]				0					No Sync	
						1					Sync on all RGB outputs	
		RGB/YUV Output			0						RGB component outputs	
					1						YUV component outputs	
		SD Sync		0							No Sync output	
				1							Output SD Syncs on $\overline{\text{HSYNC}}$ output, $\overline{\text{VSYNC}}$ output, $\overline{\text{BLANK}}$ output	
		HD Sync	0								No Sync output	
			1								Output HD Syncs on $\overline{\text{HSYNC}}$ output, $\overline{\text{VSYNC}}$ output, $\overline{\text{BLANK}}$ output	
03h	RGB Matrix 0								x	x	LSB for GY	03h
04h	RGB Matrix 1								x	x	LSB for RV	F0h
							x	x			LSB for BU	
					x	x					LSB for GV	
			x	x							LSB for GU	
05h	RGB Matrix 2		x	x	x	x	x	x	x	x	Bit 9–2 for GY	4Eh
06h	RGB Matrix 3		x	x	x	x	x	x	x	x	Bit 9–2 for GU	0Eh
07h	RGB Matrix 4		x	x	x	x	x	x	x	x	Bit 9–2 for GV	24h
08h	RGB Matrix 5		x	x	x	x	x	x	x	x	Bit 9–2 for BU	92h
09h	RGB Matrix 6		x	x	x	x	x	x	x	x	Bit 9–2 for RV	7Ch
0Ah	DAC A, B, C Output Level[2]	Positive Gain to DAC Output Voltage	0	0	0	0	0	0	0	0	0%	00h
			0	0	0	0	0	0	0	1	+0.018%	
			0	0	0	0	0	0	1	0	0.036%	
										…	……	
			0	0	1	1	1	1	1	1	+7.382%	
			0	1	0	0	0	0	0	0	+7.5%	
		Negative Gain to DAC Output Voltage	1	1	0	0	0	0	0	0	–7.5%	
			1	1	0	0	0	0	0	1	–7.382%	
			1	0	0	0	0	0	1	0	–7.364%	
										…	…….	
			1	1	1	1	1	1	1	1	–0.018%	
0Bh	DAC D, E, F Output Level	Positive Gain to DAC Output Voltage	0	0	0	0	0	0	0	0	0%	00h
			0	0	0	0	0	0	0	1	+0.018%	
			0	0	0	0	0	0	1	0	0.036%	
										…	……	
			0	0	1	1	1	1	1	1	+7.382%	
			0	1	0	0	0	0	0	0	+7.5%	
		Negative Gain to DAC Output Voltage	1	1	0	0	0	0	0	0	–7.5%	
			1	1	0	0	0	0	0	1	–7.382%	
			1	0	0	0	0	0	1	0	–7.364%	
										…	…….	
			1	1	1	1	1	1	1	1	–0.018%	
0Ch		Reserved										00h
0Dh		Reserved										00h
0Eh		Reserved										00h
0Fh		Reserved										00h

NOTES
[1]For more detail, refer to Appendix 7.
[2]For more detail on the programmable output levels, refer to the Programmable DAC Gain Control section.

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
10h	HD Mode Register 1	HD Output Standard							0	0	EIA770.2 output	00h
									0	1	EIA770.1 output	
									1	0	Output levels for full input range	
									1	1	Reserved	
		HD Input Control Signals					0	0			$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$	
							0	1			EAV/SAV codes	
							1	0			Async Timing Mode	
							1	1			Reserved	
		HD 625p				0					525p	
						1					625p	
		HD 720p			0						1080i	
					1						720p	
		HD BLANK Polarity		0							$\overline{\text{BLANK}}$ active high	
				1							BLANK active low	
		HD Macrovision for 525p/625p	0								Macrovision off	
			1								Macrovision on	
11h	HD Mode Register 2	HD Pixel Data Valid								0	Pixel data valid off	00h
										1	Pixel data valid on	
									0		Reserved	
		HD Test Pattern Enable						0			HD test pattern off	
								1			HD test pattern on	
		HD Test Pattern Hatch/Field					0				Hatch	
							1				Field/frame	
		HD VBI Open				0					Disabled	
						1					Enabled	
		HD Undershoot Limiter		0	0						Disabled	
				0	1						–11 IRE	
				1	0						–6 IRE	
				1	1						–1.5 IRE	
		HD Sharpness Filter	0								Disabled	
			1								Enabled	
12h	HD Mode Register 3	HD Y Delay with Respect to Falling Edge of $\overline{\text{HSYNC}}$						0	0	0	0 clk cycles	
								0	0	1	1 clk cycles	
								0	1	0	2 clk cycles	
								0	1	1	3 clk cycles	
								1	0	0	4 clk cycles	
		HD Color Delay with Respect to Falling Edge of $\overline{\text{HSYNC}}$			0	0	0				0 clk cycles	
					0	0	1				1 clk cycle	
					0	1	0				2 clk cycles	
					0	1	1				3 clk cycles	
					1	0	0				4 clk cycles	
		HD CGMS		0							Disabled	
				1							Enabled	
		HD CGMS CRC	0								Disabled	
			1								Enabled	

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
13h	HD Mode Register 4	HD Cr/Cb Sequence								0	Cb after falling edge of $\overline{\text{HSYNC}}$	
										1	Cr after falling edge of $\overline{\text{HSYNC}}$	
		Reserved							0		0 must be written to this bit	
		HD Input Format						0			8-bit input	
								1			10-bit input	
		Sinc Filter on DAC D, E, F					0				Disabled	
							1				Enabled	
		Reserved				0					0 must be written to this bit	
		HD Chroma SSAF			0						Disabled	
					1						Enabled	
		HD Chroma Input		0							4:4:4	
				1							4:2:2	
		HD Double Buffering	0								Disabled	
			1								Enabled	
14h	HD Mode Register 5	HD Timing Reset								x	A low-high-low transition resets the internal HD timing counters	00h
		1080i Frame Rate						0	0		30 Hz/2200 total samples/lines	
								0	1		25 Hz/2640 total samples/lines	
		Reserved		0	0	0	0				0 must be written to these bits	
		HD $\overline{\text{VSYNC}}$/Field Input		0							0 = Field Input	
				1							1 = $\overline{\text{VSYNC}}$ Input	
		Lines/Frame[1]	0								Update field/line counter	
			1								Field/line counter free running	
15h	HD Mode Register 6	Reserved								0	0 must be written to this bit	00h
		HD RGB Input							0		Disabled	
									1		Enabled	
		HD Sync on PrPb						0			Disabled	
								1			Enabled	
		HD Color DAC Swap					0				DAC E = Pb; DAC F = Pr	
							1				DAC E = Pr; DAC F = Pb	
		HD Gamma Curve A/B				0					Gamma Curve A	
						1					Gamma Curve B	
		HD Gamma Curve Enable			0						Disabled	
					1						Enabled	
		HD Adaptive Filter Mode[2]		0							Mode A	
				1							Mode B	
		HD Adaptive Filter Enable[2]	0								Disabled	
			1								Enabled	

NOTES
[1]When set to 0, the line and field counters automatically wrap around at the end of the field/frame of the standard selected. When set to 1, the field/line counters are free running and wrap around when external sync signals indicate so.
[2]Adaptive Filter mode is not available in PS only @ 54 MHz input mode.

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
16h	HD Y Level*		x	x	x	x	x	x	x	x	Y level value	A0h
17h	HD Cr Level*		x	x	x	x	x	x	x	x	Cr level value	80h
18h	HD Cb Level*		x	x	x	x	x	x	x	x	Cb level value	80h
19h		Reserved										00h
1Ah		Reserved										00h
1Bh		Reserved										00h
1Ch		Reserved										00h
1Dh		Reserved										00h
1Eh		Reserved										00h
1Fh		Reserved										00h
20h	HD Sharpness Filter Gain	HD Sharpness Filter Gain Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							..	..	..	..	……	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							..	..	..	..	……	
							1	1	1	1	Gain A = –1	
		HD Sharpness Filter Gain Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			..	..	..	..					…….	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			..	..	..	..					……..	
			1	1	1	1					Gain B = –1	
21h	HD CGMS Data 0	HD CGMS Data Bits	0	0	0	0	C19	C18	C17	C16	CGMS 19–16	00h
22h	HD CGMS Data 1	HD CGMS Data Bits	C15	C14	C13	C12	C11	C10	C9	C8	CGMS 15–8	00h
23h	HD CGMS Data 2	HD CGMS Data Bits	C7	C6	C5	C4	C3	C2	C1	C0	CGMS 7–0	00h
24h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A0	00h
25h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A1	00h
26h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A2	00h
27h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A3	00h
28h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A4	00h
29h	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A5	00h
2Ah	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A6	00h
2Bh	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A7	00h
2Ch	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A8	00h
2Dh	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A9	00h
2Eh	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B0	00h
2Fh	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B1	00h
30h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B2	00h
31h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B3	00h
32h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B4	00h
33h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B5	00h
34h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B6	00h
35h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B7	00h
36h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B8	00h
37h	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B9	00h

NOTES
Programmable gamma correction is not available in PS only @ 54 MHz input mode.
*For use with internal test pattern only.

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
38h	HD Adaptive Filter Gain 1	HD Adaptive Filter Gain 1 Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							..	..	..	..	.....	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							..	..	..	..	.....	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 1 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			..	..	..	..					.....	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			..	..	..	..					.....	
			1	1	1	1					Gain B = –1	
39h	HD Adaptive Filter Gain 2	HD Adaptive Filter Gain 2 Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							..	..	..	..	.....	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							..	..	..	..	.....	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 2 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			..	..	..	..					.....	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			..	..	..	..					.....	
			1	1	1	1					Gain B = –1	
3Ah	HD Adaptive Filter Gain 3	HD Adaptive Filter Gain 3 Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							..	..	..	..	.....	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							..	..	..	..	.....	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 3 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			..	..	..	..					.....	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			..	..	..	..					.....	
			1	1	1	1					Gain B = –1	
3Bh	HD Adaptive Filter Threshold A	HD Adaptive Filter Threshold A Value	x	x	x	x	x	x	x	x	Threshold A	00h
3Ch	HD Adaptive Filter Threshold B	HD Adaptive Filter Threshold B Value	x	x	x	x	x	x	x	x	Threshold B	00h
3Dh	HD Adaptive Filter Threshold C	HD Adaptive Filter Threshold C Value	x	x	x	x	x	x	x	x	Threshold C	00h

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
3Eh		Reserved										00h
3Fh		Reserved										00h
40h	SD Mode Register 0	SD Standard							0	0	NTSC	00h
									0	1	PAL B, D, G, H, I	
									1	0	PAL M	
									1	1	PAL N	
		SD Luma Filter				0	0	0			LPF NTSC	
						0	0	1			LPF PAL	
						0	1	0			Notch NTSC	
						0	1	1			Notch PAL	
						1	0	0			SSAF Luma	
						1	0	1			Luma CIF	
						1	1	0			Luma QCIF	
						1	1	1			Reserved	
		SD Chroma Filter	0	0	0						1.3 MHz	
			0	0	1						0.65 MHz	
			0	1	0						1.0 MHz	
			0	1	1						2.0 MHz	
			1	0	0						Reserved	
			1	0	1						Chroma CIF	
			1	1	0						Chroma QCIF	
			1	1	1						3.0 MHz	
41h		Reserved										00h
42h	SD Mode Register 1	SD PrPb SSAF								0	Disabled	08h
										1	Enabled	
		SD DAC Output 1							0		Refer to output configuration section	
									1			
		SD DAC Output 2						0			Refer to output configuration section	
								1				
		SD Pedestal					0				Disabled	
							1				Enabled	
		SD Square Pixel				0					Disabled	
						1					Enabled	
		SD VCR FF/RW Sync			0						Disabled	
					1						Enabled	
		SD Pixel Data Valid		0							Disabled	
				1							Enabled	
		SD SAV/EAV Step Edge Control	0								Disabled	
			1								Enabled	
43h	SD Mode Register 2	SD Pedestal YPrPb Output								0	No pedestal on YUV	00h
										1	7.5 IRE pedestal on YUV	
		SD Output Levels Y							0		Y = 700 mV/300 mV	
									1		Y = 714 mV/286 mV	
		SD Output Levels PrPb					0	0			700 mV p-p[PAL]; 1000 mV p-p[NTSC]	
							0	1			700 mV p-p	
							1	0			1000 mV p-p	
							1	1			648 mV p-p	
		SD VBI Open				0					Disabled	
						1					Enabled	
		SD CC Field Control		0	0						CC disabled	
				0	1						CC on odd field only	
				1	0						CC on odd field only	
				1	1						CC on both fields	
		Reserved	1								Reserved	

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
44h	SD Mode Register 3	SD VSYNC-3H								0	Disabled	00h
										1	$\overline{\text{VSYNC}}$ = 2.5 lines [PAL] $\overline{\text{VSYNC}}$ = 3 lines [NTSC]	
		SD RTC/TR/SCR						0	0		Genlock disabled	
								0	1		Subcarrier Reset	
								1	0		Timing Reset	
								1	1		RTC enabled	
		SD Active Video Length					0				720 pixels	
							1				710 [NTSC]/702[PAL]	
		SD Chroma				0					Chroma enabled	
						1					Chroma disabled	
		SD Burst			0						Enabled	
					1						Disabled	
		SD Color Bars		0							Disabled	
				1							Enabled	
		SD DAC Swap	0								DAC A = Luma, DAC B = Chroma	
			1								DAC A = Chroma, DAC B = Luma	
45h	Reserved											00h
46h	Reserved											00h
47h	SD Mode Register 4	SD PrPb Scale								0	Disabled	00h
										1	Enabled	
		SD Y Scale							0		Disabled	
									1		Enabled	
		SD Hue Adjust						0			Disabled	
								1			Enabled	
		SD Brightness					0				Disabled	
							1				Enabled	
		SD Luma SSAF Gain				0					Disabled	
						1					Enabled	
		Reserved			0						0 must be written to this bit	
		Reserved		0							0 must be written to this bit	
		Reserved	0								0 must be written to this bit	
48h	SD Mode Register 5	Reserved								0		00h
		Reserved							0		0 must be written to this bit	
		SD Double Buffering						0			Disabled	
								1			Enabled	
		SD Input Format				0	0				8-bit Input	
						0	1				16-bit Input	
						1	0				10-bit Input	
						1	1				20-bit Input	
		SD Digital Noise Reduction			0						Disabled	
					1						Enabled	
		SD Gamma Control		0							Disabled	
				1							Enabled	
		SD Gamma Curve	0								Gamma Curve A	
			1								Gamma Curve B	
49h	SD Mode Register 6	SD Undershoot Limiter							0	0	Disabled	00h
									0	1	– 11 IRE	
									1	0	– 6 IRE	
									1	1	– 1.5 IRE	
		Reserved						0			0 must be written to this bit	
		SD Black Burst Output on DAC Luma					0				Disabled	
							1				Enabled	
		SD Chroma Delay			0	0					Disabled	
					0	1					4 clk cycles	
					1	0					8 clk cycles	
					1	1					Reserved	
		Reserved		0							0 must be written to this bit	
		Reserved	0								0 must be written to this bit	