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Multiformat 216 MHz Video Encoder with Six NSV® 12-Bit DACs

ADV7320/ADV7321

FEATURES

High definition (HD) input formats
- 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb

Fully compliant with
- SMPTE 274M (1080i, 1080p @ 74.25 MHz)
- SMPTE 296M (720p)
- SMPTE 240M (1035i)
- RGB in 3-bit × 10-bit 4:4:4 input format

HDTV RGB supported
- RGB, RGBHV
- Other HD formats using async timing mode

Enhanced definition (ED) input formats
- 8-/10-, 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb
- SMPTE 293M (525p)
- BTA T-1004 EDTV2 (525p)
- ITU-R BT.1358 (625p/525p)
- ITU-R BT.1362 (625p/525p)
- RGB in 3-bit × 10-bit 4:4:4 input format

Standard definition (SD) input formats
- CCIR-656 4:2:2 8-/10-bit or 16-/20-bit parallel input

HD output formats
- YPrPb HDTV (EIA 770.3)
- RGB, RGBHV
- CGMS-A (720p/1080i)

ED output formats
- Macrovision® Rev 1.2 (525p/625p) (ADV7320 only)
- CGMS-A (525p/625p)
- YPrPb progressive scan (PS) (EIA-770.1, EIA-770.2)
- RGB, RGBHV

SD output formats
- Composite NTSC M/N
- Composite PAL M/N/B/D/G/H/I, PAL-60
- SMPTE 170M NTSC-compatible composite video
- ITU-R BT.470 PAL-compatible composite video
- S-video (Y/C)
- EuroScart RGB
- Component YPrPb (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1.L1 (ADV7320 only)
  - CGMS/WSS
  - Closed captioning

GENERAL FEATURES

Simultaneous SD/HD or PS/SD inputs and outputs
Oversampling up to 216 MHz
Programmable DAC gain control
Sync outputs in all modes
On-board voltage reference
Six 12-bit NSV (noise shaped video) precision video DACs
2-wire serial I²C® interface, open-drain configuration
Dual I/O supply 2.5 V/3.3 V operation
Analog and digital supply 2.5 V
On-board PLL
64-lead LQFP package
Lead (Pb) free product

APPLICATIONS

EVD (enhanced versatile disk) players
High-end SD/PS DVD recorders/players
SD/PS/HDTV display devices
SD/HDTV set top boxes
Professional video systems

FUNCTIONAL BLOCK DIAGRAM

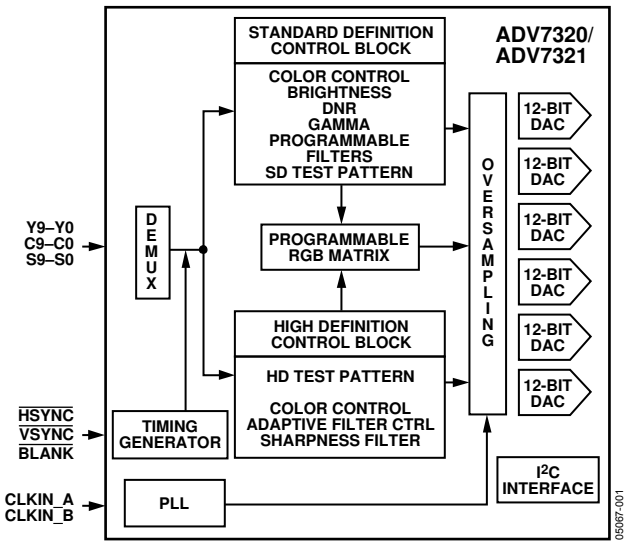

Figure 1.

GENERAL DESCRIPTION

The ADV®7320/ADV7321 are high speed, digital-to-analog encoders on single monolithic chips. They include six high speed NSV video DACs with TTL-compatible inputs. They have separate 8-/10-, 16-/20-, and 24-/30-bit input ports that accept data in high definition (HD) and/or standard definition (SD) video format. For all standards, external horizontal, vertical, and blanking signals, or EAV/SAV timing codes, control the insertion of appropriate synchronization signals into the digital data stream and, therefore, the output signal.

Rev. A

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REVISION HISTORY

5/06—Rev. 0 to Rev. A

Replaced Figure 11....12
Changes to Table 25....41

10/04—Revision 0: Initial Version

DETAILED FEATURES

HD programmable features (720p/1080i/1035i)
- **2× oversampling (148.5 MHz)**
- **Internal test pattern generator**
- **Color hatch, black bar, flat field/frame**
- **Fully programmable YCrCb to RGB matrix**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Programmable sharpness filter control**
- **CGMS-A (720p/1080i)**

ED programmable features (525p/625p)
- **8× oversampling (216 MHz output)**
- **Internal test pattern generator**
- **Color hatch, black bar, flat frame**
- **Individual Y and PrPb output delay**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Fully programmable YCrCb to RGB matrix**
- **Undershoot limiter**
- **Macrovision Rev 1.2 (525p/625p) (ADV7320 only)**
- **CGMS-A (525p/625p)**

SD programmable features
- **16× oversampling (216 MHz)**
- **Internal test pattern generator**
  - **Color bars, black bar**
- **Controlled edge rates for start and end of active video**
- **Individual Y and PrPb output delay**
- **Undershoot limiter**
- **Gamma correction**
- **Digital noise reduction (DNR)**
- **Multiple chroma and luma filters**
- **Luma-SSAF™ filter with programmable gain/attenuation**
- **PrPb SSAF™**
- **Separate pedestal control on component and composite/S-video output**
- **VCR FF/RW sync mode**
- **Macrovision Rev 7.1.L1 (ADV7320 only)**
  - **CGMS/WSS**
  - **Closed captioning**

Table 1. Standards Directly Supported[1]

Resolution	Interlace/PS	Frame Rate (Hz)	Clock Input (MHz)	Standard
720 × 480	I	29.97	27	ITU-R BT.656
720 × 576	I	25	27	ITU-R BT.656
720 × 480	I	29.97	24.54	NTSC Square Pixel
720 × 576	I	25	29.5	PAL Square Pixel
720 × 483	P	59.94	27	SMPTE 293M
720 × 483	P	59.94	27	BTA T-1004
720 × 483	P	59.94	27	ITU-R BT.1358
720 × 576	P	50	27	ITU-R BT.1358
720 × 483	P	59.94	27	ITU-R BT.1362
720 × 576	P	50	27	ITU-R BT.1362
1920 × 1035	I	30	74.25	SMPTE 240M
		29.97	74.1758	
1280 × 720	P	60, 50, 30, 25, 24	74.25	SMPTE 296M
		23.97, 59.94, 29.97	74.1758	
1920 × 1080	I	30, 25	74.25	SMPTE 274M
		29.97	74.1758	
1920 × 1080	P	30, 25, 24	74.25	SMPTE 274M
		23.98, 29.97	74.1758	

[1] Other standards are supported in async timing mode.

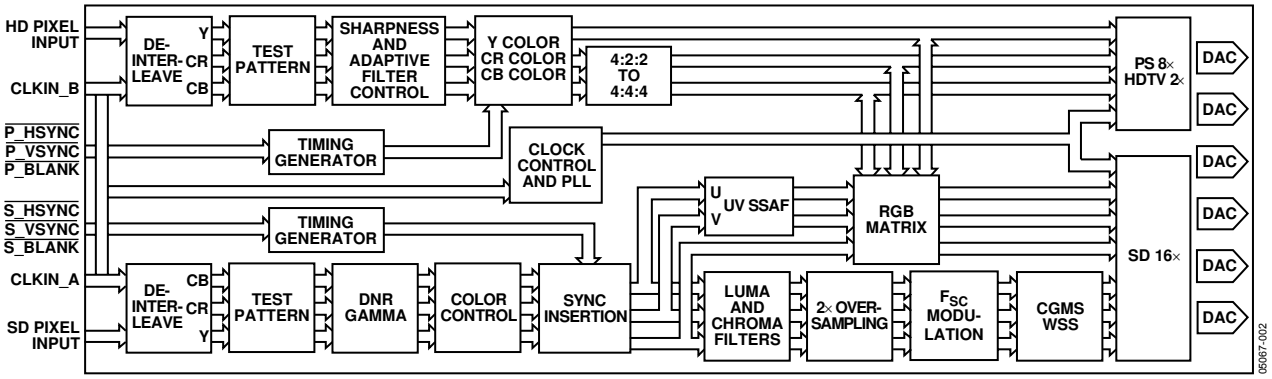


Figure 2. Detailed Functional Block Diagram

TERMINOLOGY

SD: standard definition video, conforming to ITU-R BT.601/ITU-R BT.656.

HD: high definition video, that is, 720p/1080i/1035i.

EDTV: enhanced definition television (525p/625p).

PS: progressive scan video, conforming to SMPTE 293M, ITU-R BT.1358, BTA T-1004 EDTV2, or ITU-R BT.13621362.

HDTV: high definition television video, conforming to SMPTE 274M, or SMPTE 296M and SMPTE 240M.

YCrCb SD, PS, or HD component: digital video.

YPrPb SD, PS, or HD component: analog video.

SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		12		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity,[2] +ve		0.25		LSB	
Differential Nonlinearity,[2] –ve		1.5		LSB	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4 [2.0][3]			V	I_{SOURCE} = 400 µA
Three-State Leakage Current		±1.0		µA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		10		µA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	4.1	4.33	4.6	mA	
Output Current Range	4.1	4.33	4.6	mA	
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Internal Reference Range, V_{REF}	1.15	1.235	1.3	V	
External Reference Range, V_{REF}	1.15	1.235	1.3	V	
V_{REF} Current[4]		±10		µA	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[5]		137		mA	SD only (16×)
		78		mA	PS only (8×)
		73		mA	HDTV only (2×)
		140	190[6]	mA	SD (16×, 10 bit) + PS (8×, 20 bit)
I_{DD_IO}		1.0		mA	
I_{AA}[7, 8]		37	45	mA	
Sleep Mode					
I_{DD}		80		µA	
I_{AA}		7		µA	
I_{DD_IO}		250		µA	
POWER SUPPLY REJECTION RATIO		0.01		%/%	

[1] Oversampling disabled. Static DAC performance improves with increased oversampling ratios.
[2] DNL measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step value lies below the ideal step value.
[3] For values in brackets, V_{DD_IO} = 2.375 V to 2.75 V.
[4] External current required to overdrive internal V_{REF}.
[5] I_{DD}, the circuit current, is the continuous current required to drive the digital core.
[6] Guaranteed maximum by characterization.
[7] All DACs on.
[8] I_{AA} is the total current required to supply all DACs, including the V_{REF} circuitry and the PLL circuitry.

DYNAMIC SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
PS MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		65.6		dB	Luma ramp unweighted
		72		dB	Flat field full bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
SD MODE					
Hue Accuracy		0.2		Degrees	
Color Saturation Accuracy		0.20		%	
Chroma Nonlinear Gain		0.84		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		−0.2		±Degrees	
Chroma/Luma Intermodulation		0		±%	
Chroma/Luma Gain Inequality		96.7		±%	
Chroma/Luma Delay Inequality		−1.0		ns	
Luminance Nonlinearity		0.2		±%	
Chroma AM Noise		84		dB	
Chroma PM Noise		75.3		dB	
Differential Gain		0.25		%	NTSC
Differential Phase		0.2		Degrees	NTSC
SNR		63.5		dB	Luma ramp
		77.7		dB	Flat field full bandwidth

TIMING SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First clock generated after this period relevant for repeated start condition
Setup Time (Start Condition), t_4	0.6			µs	
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		7		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			29.5	MHz	SD PAL square pixel mode
f_{CLK}		81		MHz	PS/HD async mode
Clock High Time, t_9	40			% of one clock cycle	
Clock Low Time, t_{10}	40			% of one clock cycle	
Data Setup Time, t_{11}[1]	2.0			ns	
Data Hold Time, t_{12}[1]	2.0			ns	
SD Output Access Time, t_{13}			15	ns	
SD Output Hold Time, t_{14}	5.0			ns	
HD Output Access Time, t_{13}			14	ns	
HD Output Hold Time, t_{14}	5.0			ns	
PIPELINE DELAY[4]		63		Clock cycles	SD (2×, 16×)
		76		Clock cycles	SD component mode (16×)
		35		Clock cycles	PS (1×)
		41		Clock cycles	PS (8×)
		36		Clock cycles	HD (2×, 1×)

[1] Guaranteed by characterization.
[2] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
[3] Data: C[9:0], Y[9:0], S[9:0]; Control: P_HSYNC, P_VSYNC, P_BLANK, S_HSYNC, S_VSYNC, S_BLANK.
[4] SD, PS = 27 MHz; HD = 74.25 MHz.

TIMING DIAGRAMS

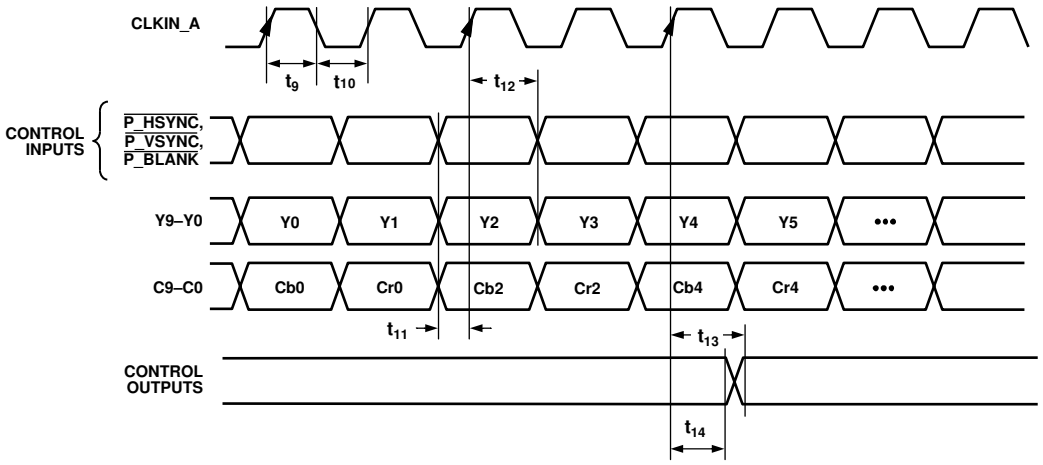


Figure 3. HD Only 4:2:2 Input Mode (Input Mode 010); PS Only 4:2:2 Input Mode (Input Mode 001)

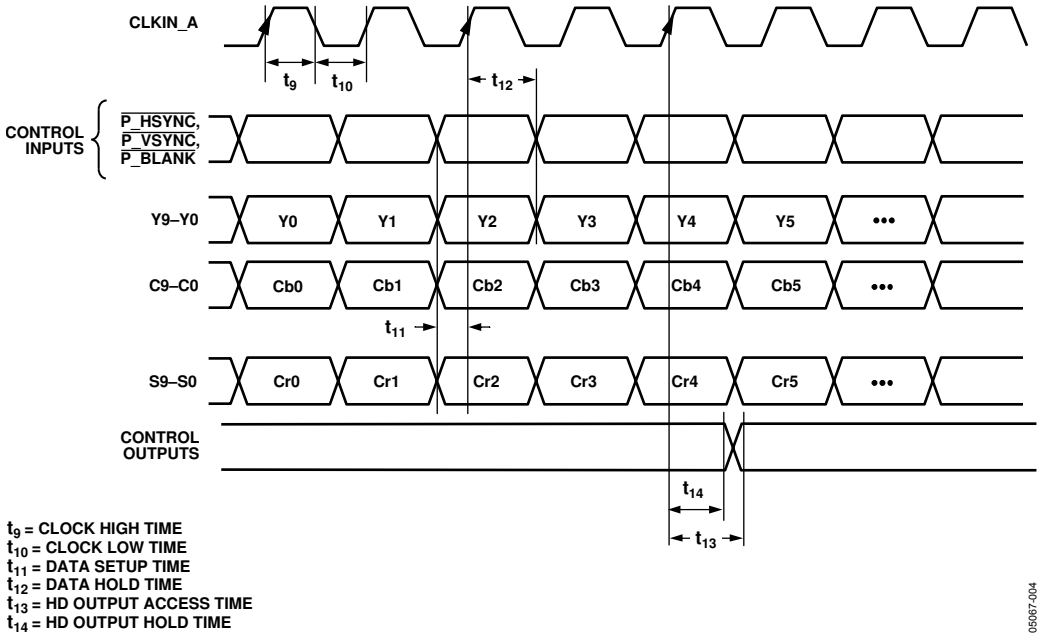


Figure 4. HD Only 4:4:4 Input Mode (Input Mode 010); PS Only 4:4:4 Input Mode (Input Mode 001)

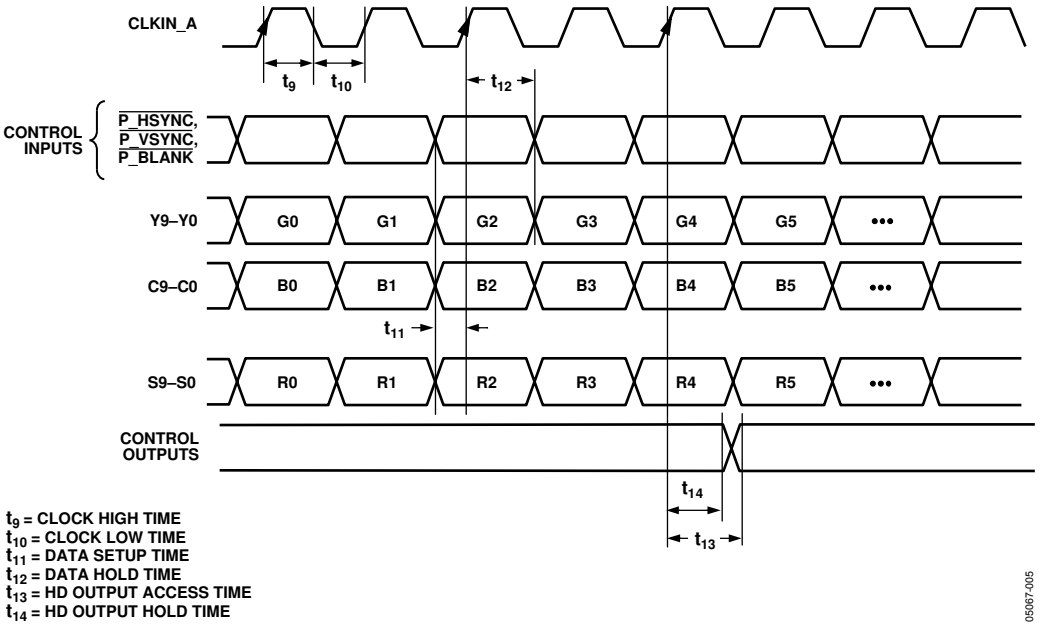


Figure 5. HD RGB 4:4:4 Input Mode (Input Mode 010)

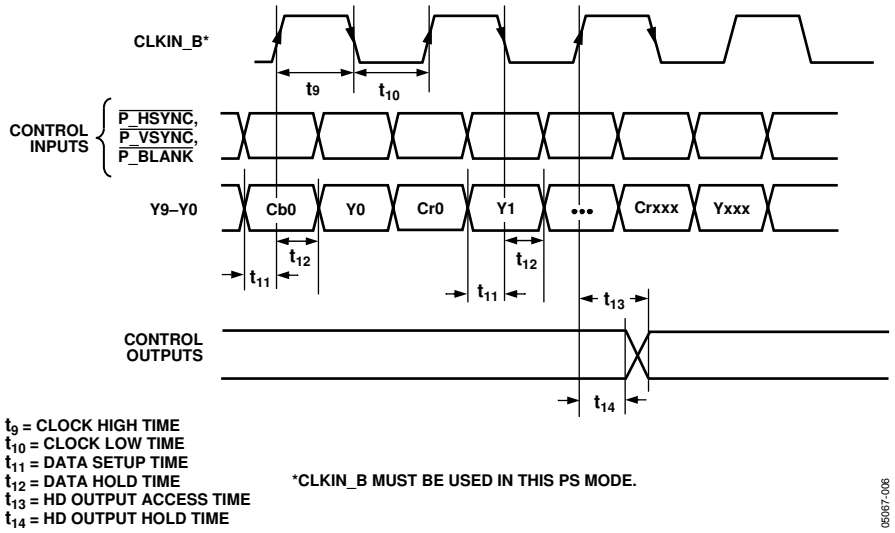


Figure 6. PS 4:2:2 10-Bit Interleaved at 27 MHz $\overline{HSYNC}$/$\overline{VSYNC}$ Input Mode (Input Mode 100)

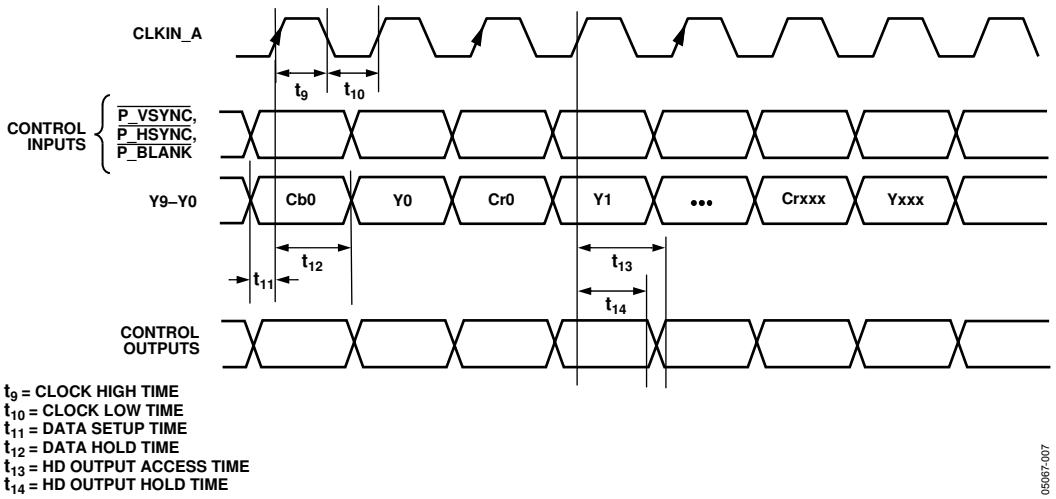


Figure 7. PS 4:2:2 10-Bit Interleaved at 54 MHz $\overline{HSYNC}$ /$\overline{VSYNC}$ Input Mode (Input Mode 111)

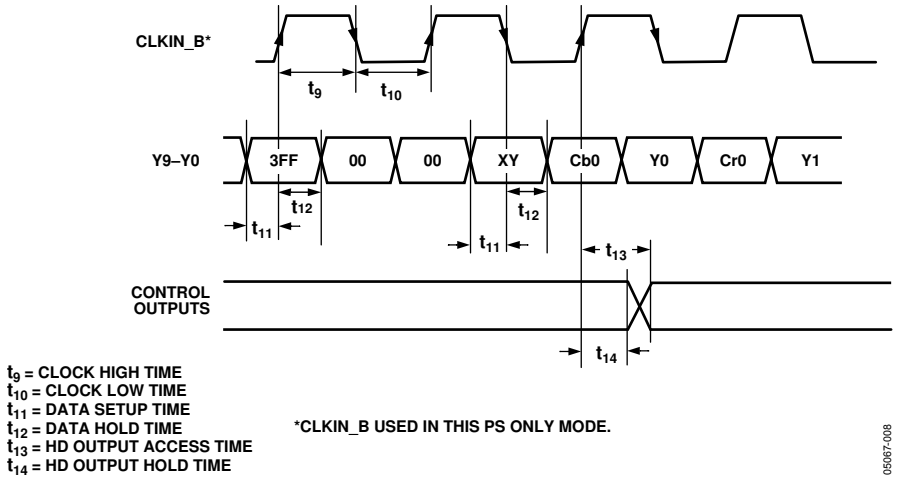


Figure 8. PS Only 4:2:2 10-Bit Interleaved at 27 MHz EAV/SAV Input Mode (Input Mode 100)

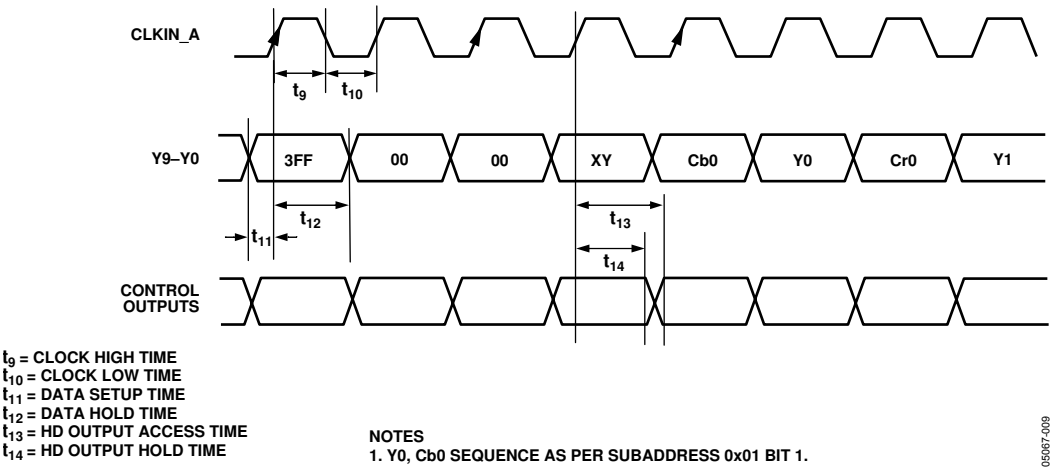


Figure 9. PS Only 4:2:2 10-Bit Interleaved at 54 MHz EAV/SAV Input Mode (Input Mode 111)

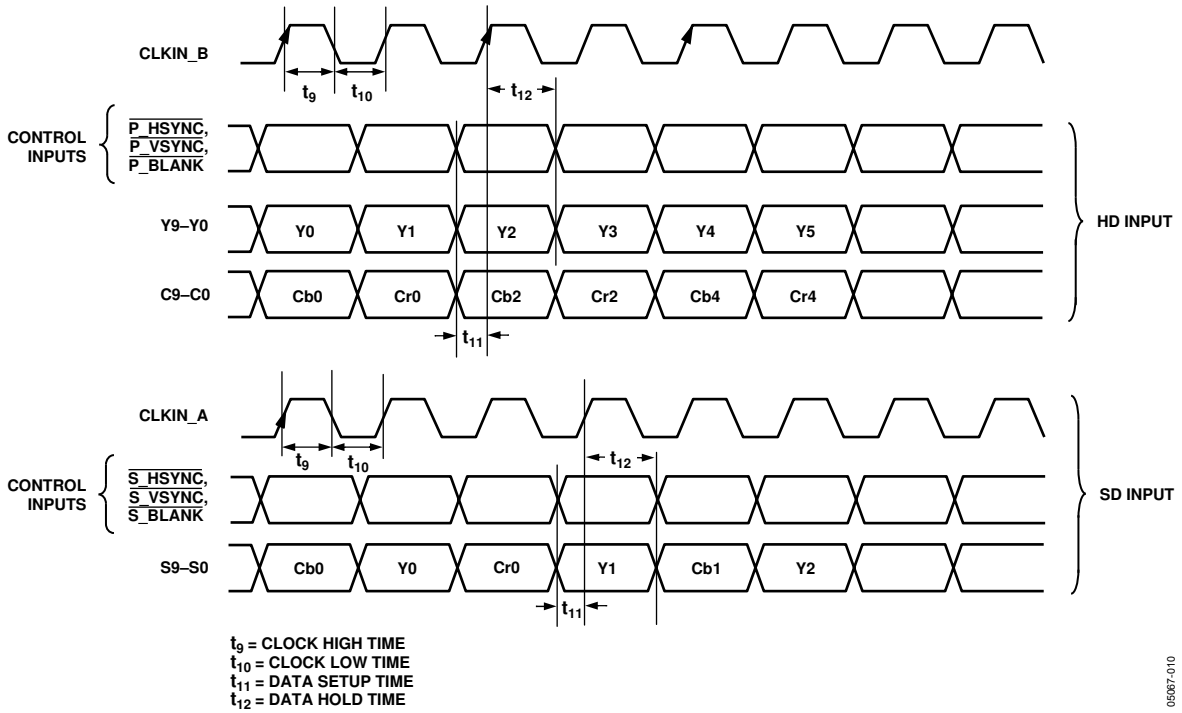


Figure 10. HD 4:2:2 and SD 10-Bit Simultaneous Input Mode (Input Mode 101: SD Oversampled) (Input Mode 110: HD Oversampled)

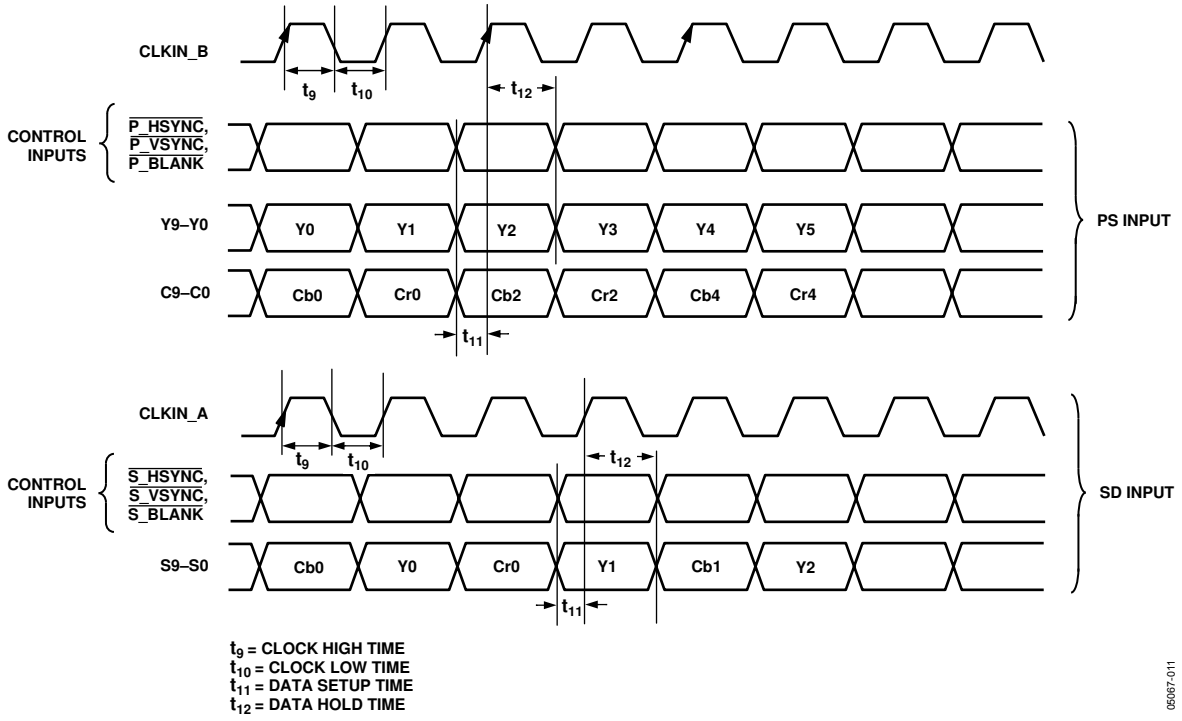


Figure 11. PS 4:2:2 and SD 10-Bit Simultaneous Input Mode (Input Mode 011)

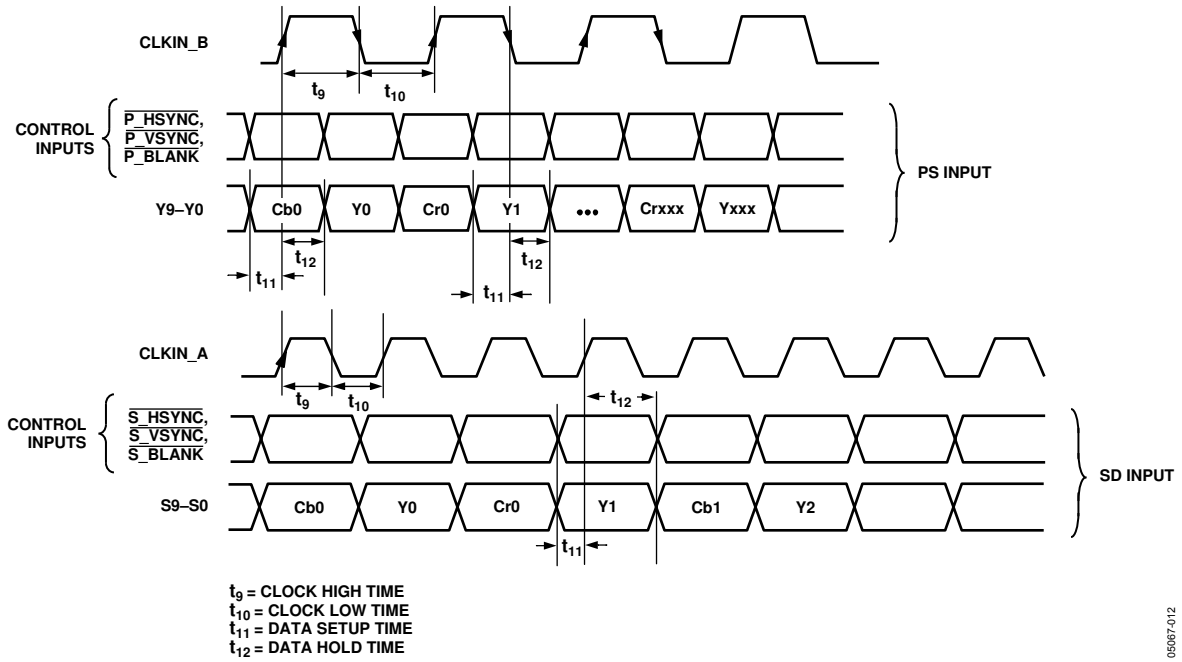


Figure 12. PS 10-Bit and SD 10-Bit Simultaneous Input Mode (Input Mode 100)

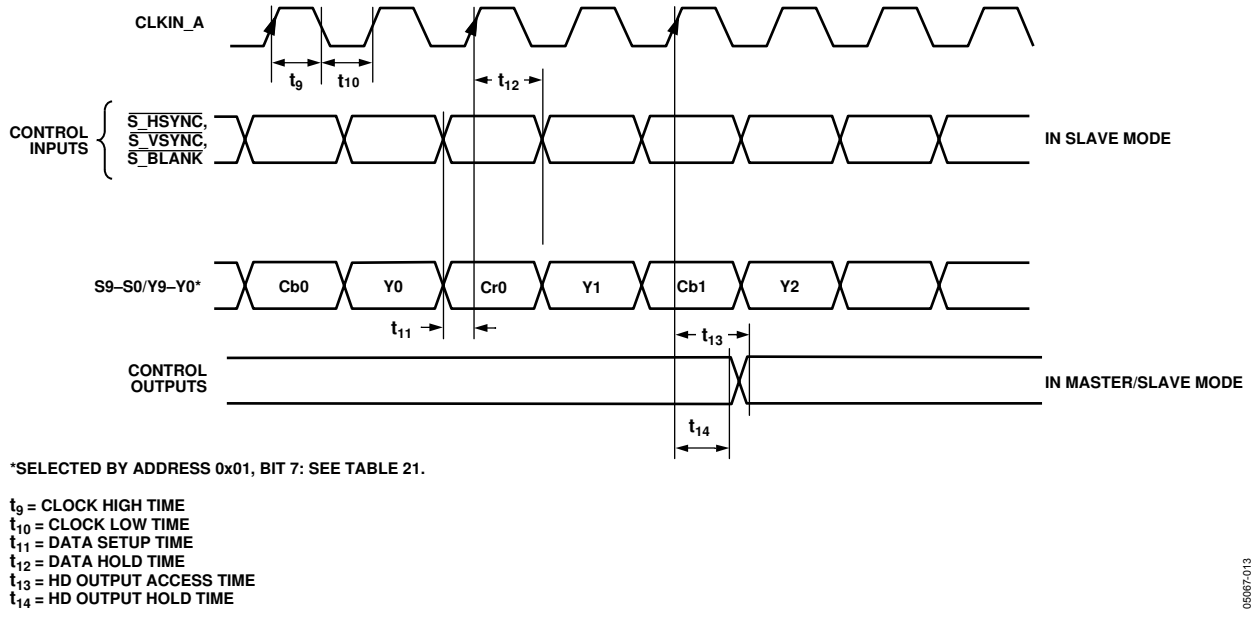
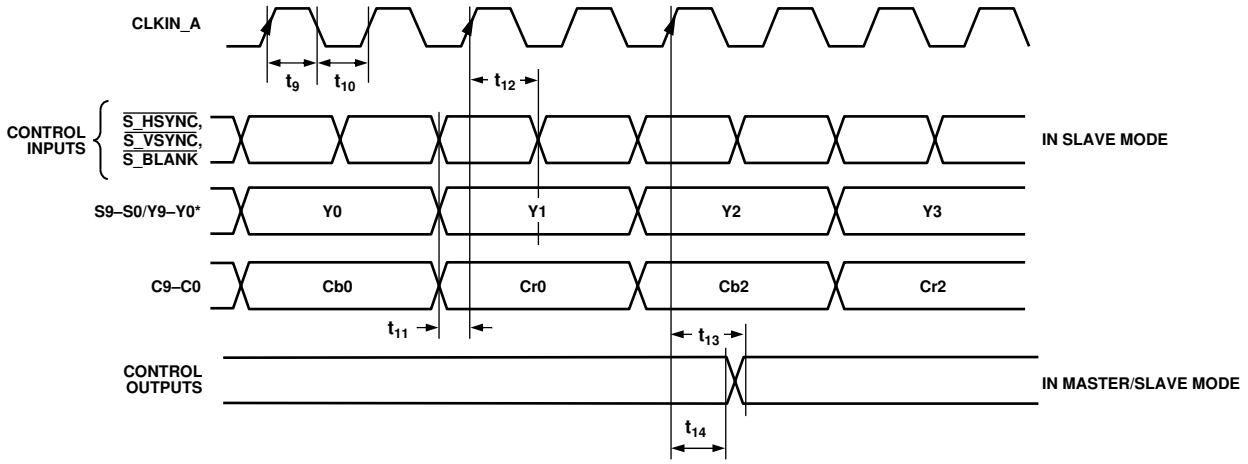


Figure 13. 8-/10-Bit SD Only Pixel Input Mode (Input Mode 000)

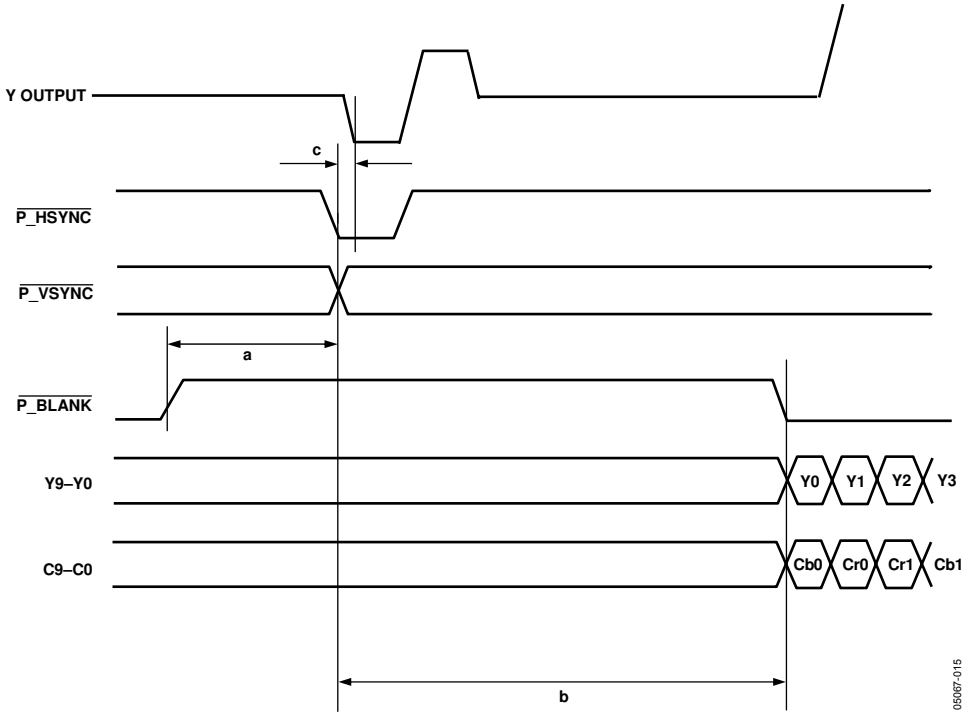


*SELECTED BY ADDRESS 0x01, BIT 7: SEE TABLE 21.

t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME
t_{13} = HD OUTPUT ACCESS TIME
t_{14} = HD OUTPUT HOLD TIME

05067-014

Figure 14. 16-/20-Bit SD Only Pixel Input Mode (Input Mode 000)



05067-015

a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF HSYNC INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

Figure 15. HD 4:2:2 Input Timing Diagram

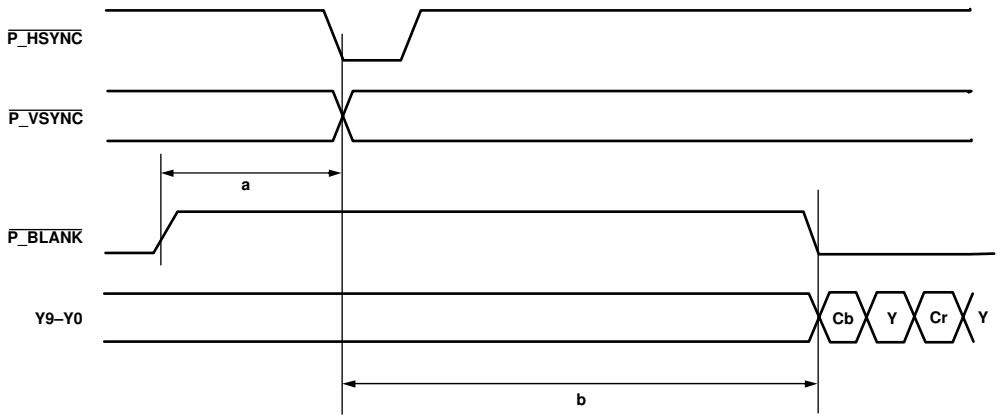


Figure 16. PS 4:2:2 10-Bit Interleaved Input Timing Diagram

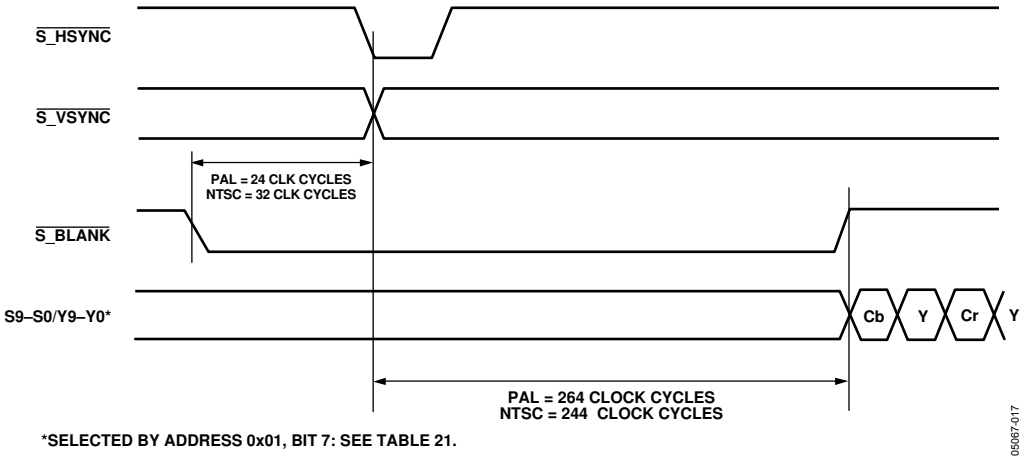


Figure 17. SD Timing Input for Timing Mode 1

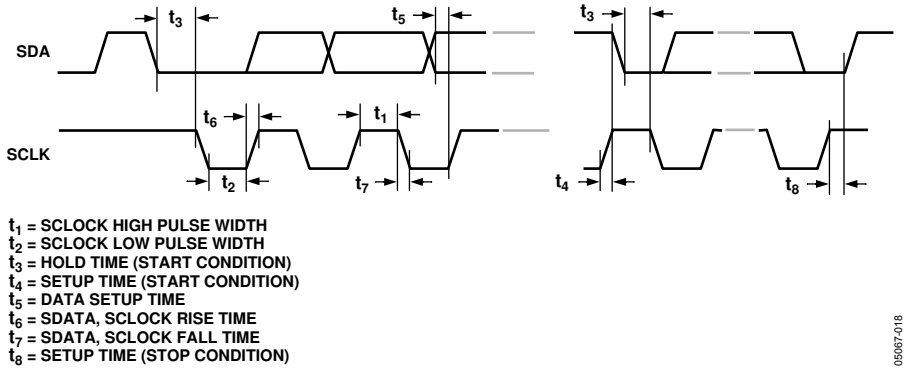


Figure 18. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Value
V_{AA} to AGND	−0.3 V to +3.0 V
V_{DD} to DGND	−0.3 V to +3.0 V
V_{DD_IO} to GND_IO	−0.3 V to +4.6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD_IO} +0.3 V
V_{AA} to V_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to GND_IO	−0.3 V to +0.3 V
AGND to GND_IO	−0.3 V to +0.3 V
Ambient Operating Temperature (T_A)	0°C to 70°C
Storage Temperature (T_S)	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JC} = 11°C/W

θ_{JA} = 47°C/W

The ADV7320/ADV7321 are Pb-free, environmentally friendly products. They are manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The devices are suitable for Pb-free applications and are able to withstand surface-mount soldering up to 255°C (±5°C).

In addition, they are backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

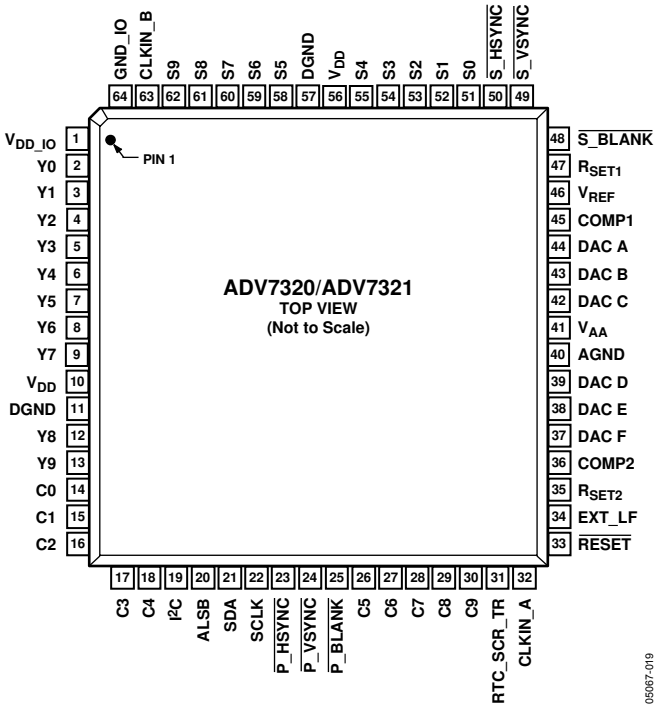


Figure 19. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output	Description
11, 57	DGND	G	Digital Ground.
40	AGND	G	Analog Ground.
32	CLKIN_A	I	Pixel Clock Input for HD Only (74.25 MHz), PS Only (27 MHz), and SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for PS mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
45, 36	COMP1, COMP2	O	Compensation Pin for DACs. Connect 0.1 µF capacitor from COMP pin to V_{AA}.
44	DAC A	O	CVBS/Green/Y/Y Analog Output.
43	DAC B	O	Chroma/Blue/U/Pb Analog Output.
42	DAC C	O	Luma/Red/V/Pr Analog Output.
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Y/Green [HD] Analog Output.
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pr/Red Analog Output.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pb/Blue [HD] Analog Output.
23	$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
24	$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
25	$\overline{\text{P\_BLANK}}$	I	Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
48	$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD Only.
49	$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Sync Control Signal for SD Only.
50	$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Sync Control Signal for SD Only.
13, 12, 9 to 2	Y9 to Y0	I	SD or PS/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0. For 8-bit data input, LSB is set up on Pin Y2.
30 to 26, 18 to 14	C9 to C0	I	PS/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb[Blue/U] data. The LSB is set up on Pin C0. For 8-bit data input, LSB is set up on Pin C2.

Pin No.	Mnemonic	Input/Output	Description
62 to 58, 55 to 51	S9 to S0	I	SD or PS/HDTV Input Port for Cr[Red/V] Data in 4:4:4 Input Mode. LSB is set up on Pin S0. For 8-bit data input, LSB is set up on Pin S2.
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7320/ADV7321 into default register setting. $\overline{\text{RESET}}$ is an active low signal.
47, 35	R_{SET1}, R_{SET2}	I	A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
22	SCLK	I	I^2C Port Serial Interface Clock Input.
21	SDA	I/O	I^2C Port Serial Data Input/Output.
20	ALSB	I	TTL Address Input. This signal sets up the LSB of the I^2C address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs.
10, 56	V_{DD}	P	Digital Power Supply.
41	V_{AA}	P	Analog Power Supply.
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
34	EXT_LF	I	External Loop Filter for the Internal PLL.
31	RTC_SCR_TR	I	Multifunctional Input. Real-time control (RTC) input, timing reset input, subcarrier reset input.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7320/ADV7321 to interface over the I^2C port.
64	GND_IO		Digital Input/Output Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

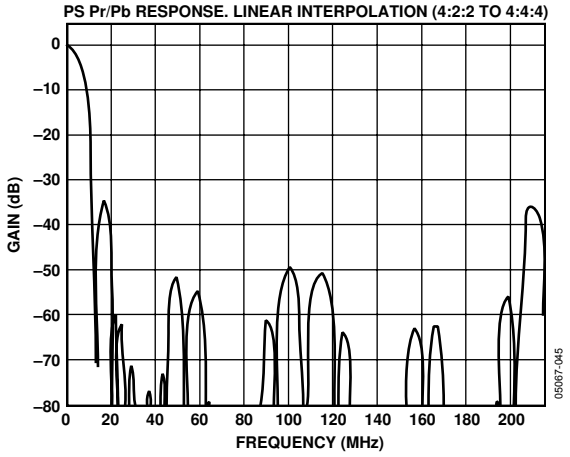


Figure 20. PS—UV 8× Oversampling Filter (Linear)

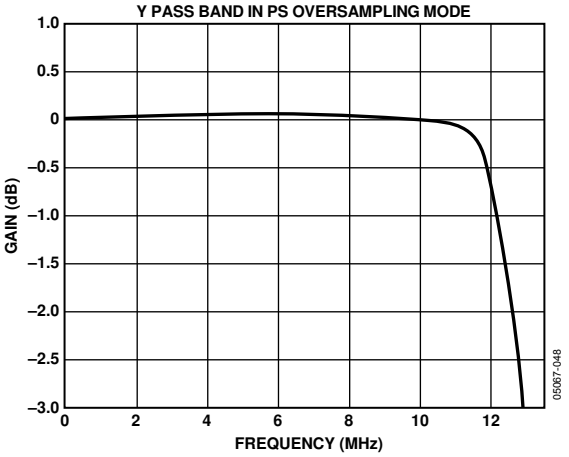


Figure 23. PS—Y 8× Oversampling Filter (Pass Band)

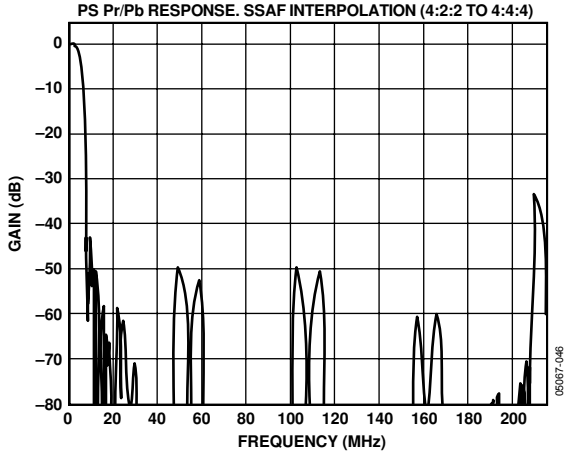


Figure 21. PS—UV 8× Oversampling Filter (SSAF)

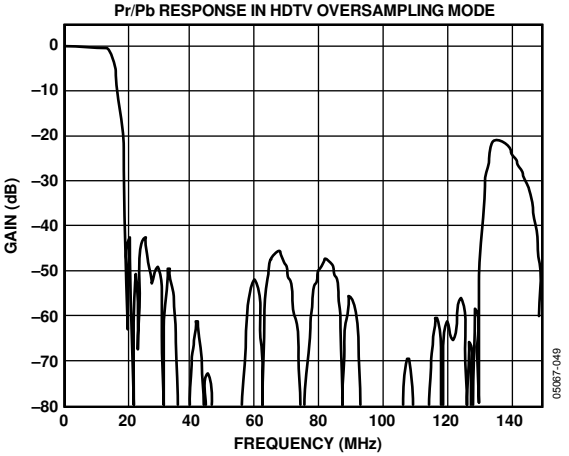


Figure 24. HDTV—UV 2× Oversampling Filter

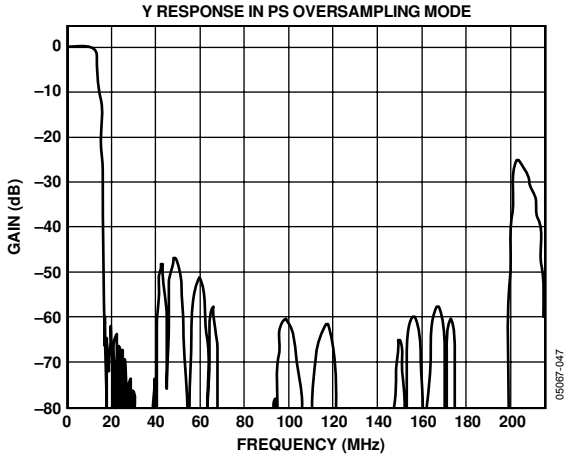


Figure 22. PS—Y 8× Oversampling Filter

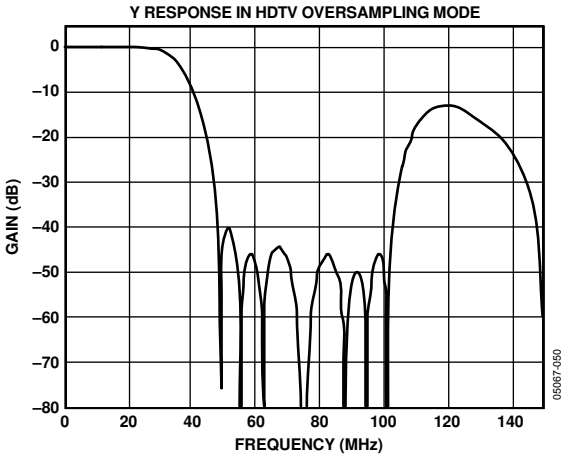


Figure 25. HDTV—Y 2× Oversampling Filter

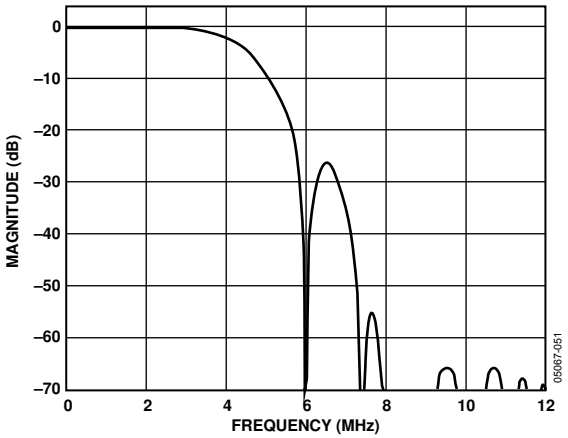


Figure 26. Luma NTSC Low-Pass Filter

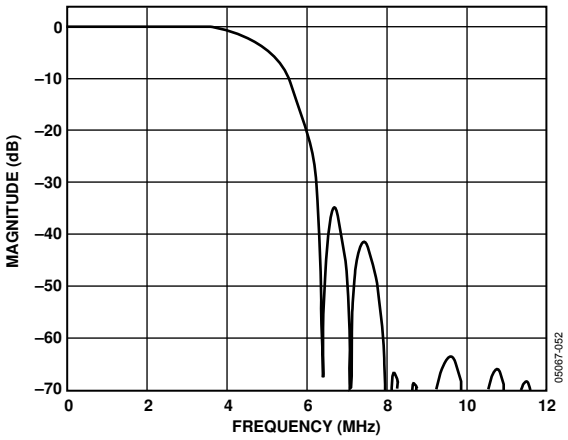


Figure 27. Luma PAL Low-Pass Filter

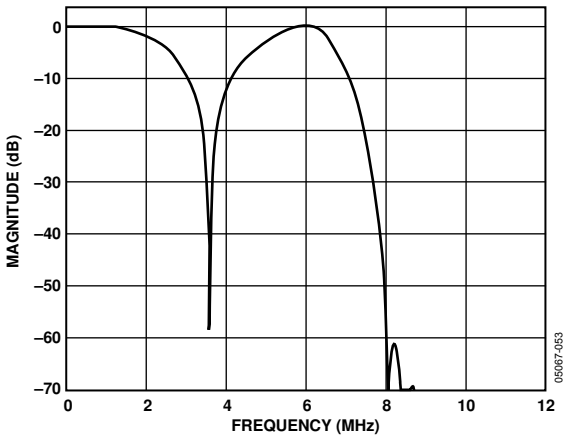


Figure 28. Luma NTSC Notch Filter

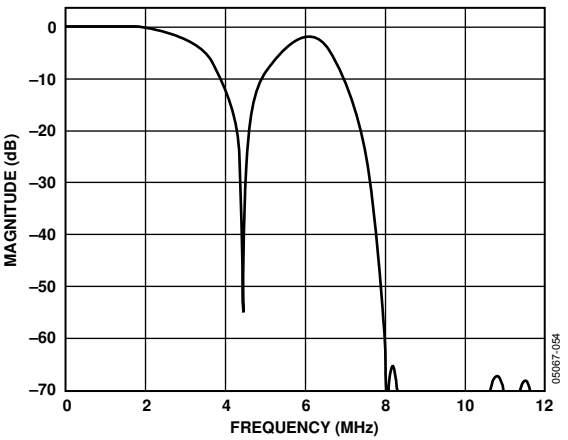


Figure 29. Luma PAL Notch Filter

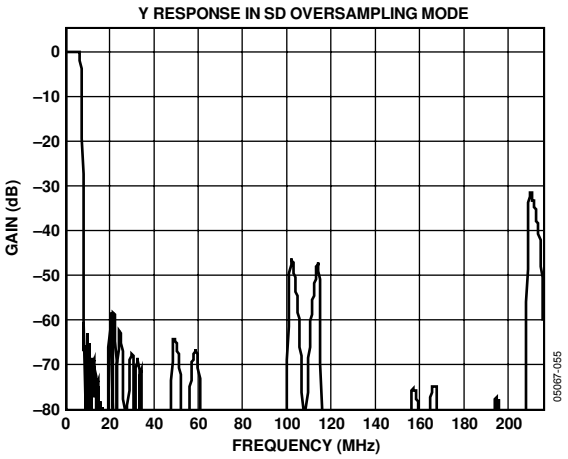


Figure 30. Y—16× Oversampling Filter

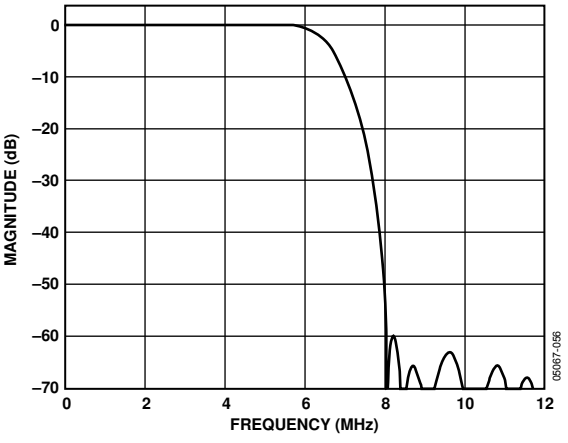


Figure 31. Luma SSAF Filter up to 12 MHz

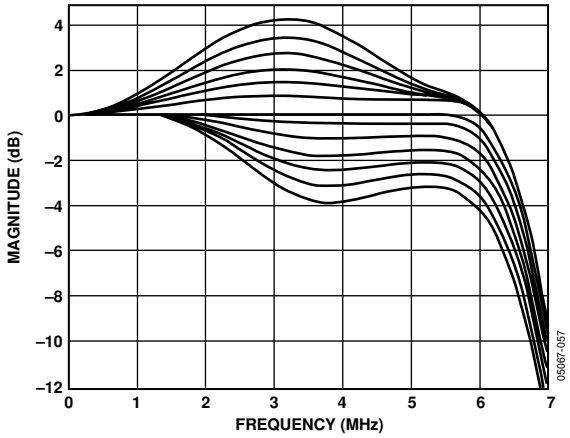


Figure 32. Luma SSAF Filter—Programmable Responses

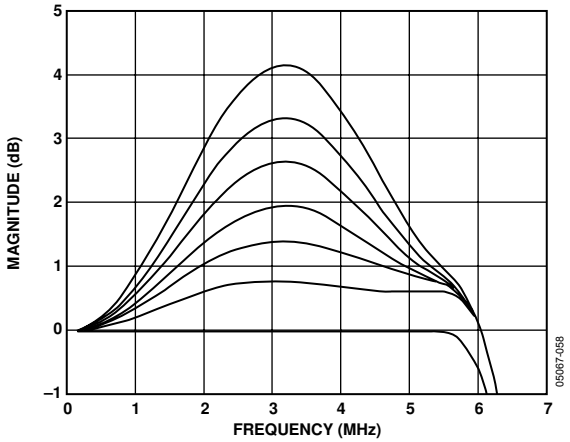


Figure 33. Luma SSAF Filter—Programmable Gain

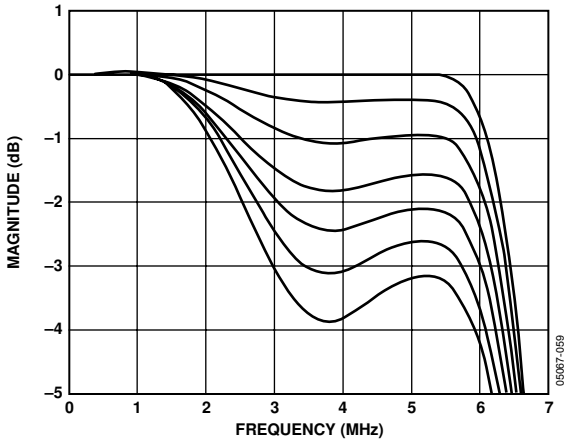


Figure 34. Luma SSAF Filter—Programmable Attenuation

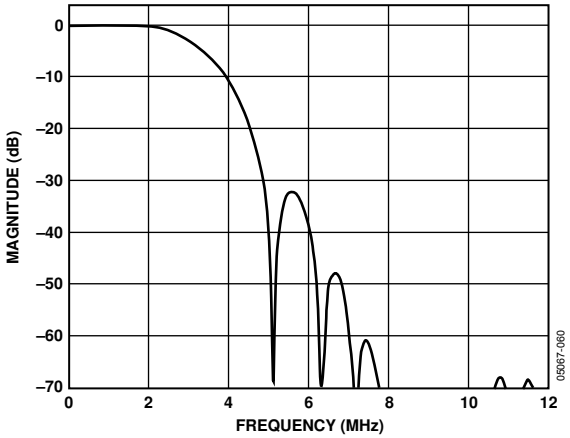


Figure 35. Luma CIF Low-Pass Filter

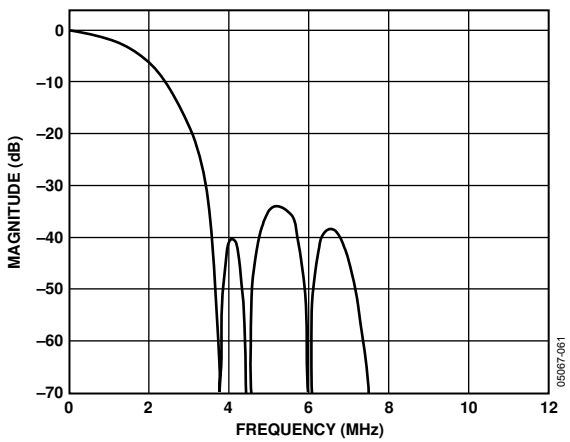


Figure 36. Luma QCIF Low-Pass Filter

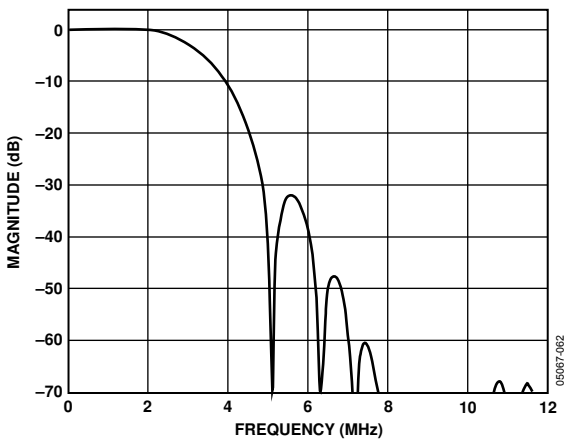


Figure 37. Chroma 3.0 MHz Low-Pass Filter

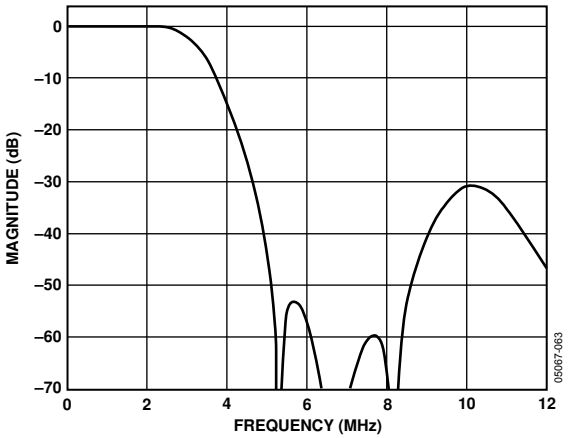


Figure 38. Chroma 2.0 MHz Low-Pass Filter

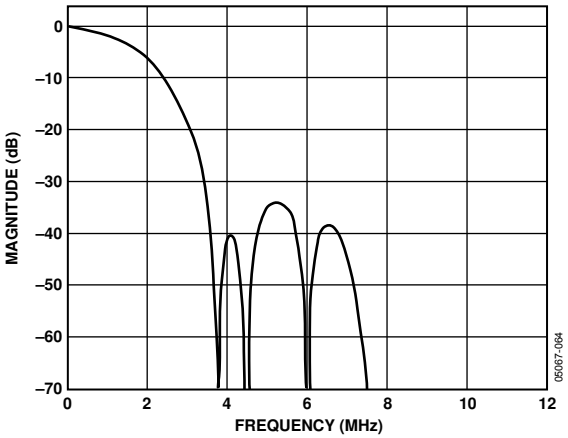


Figure 39. Chroma 1.3 MHz Low-Pass Filter

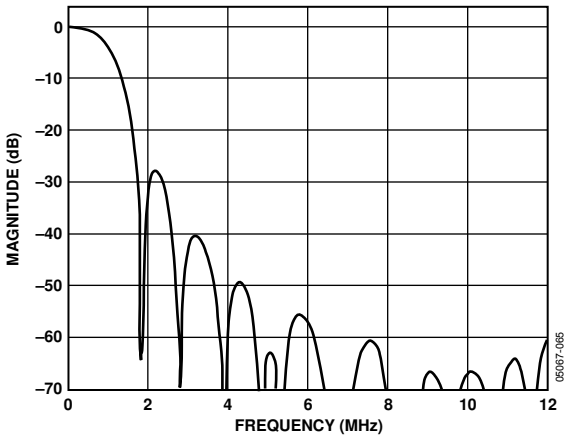


Figure 40. Chroma 1.0 MHz Low-Pass Filter

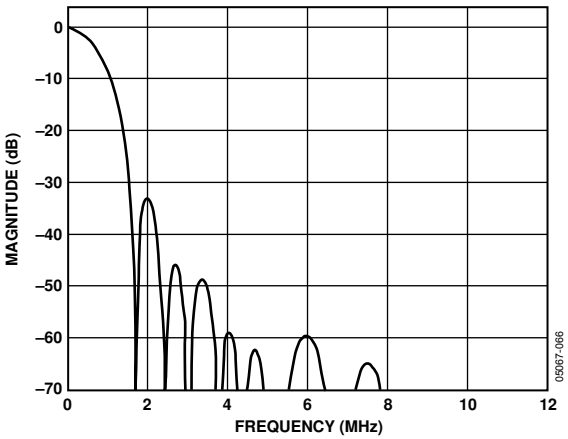


Figure 41. Chroma 0.65 MHz Low-Pass Filter

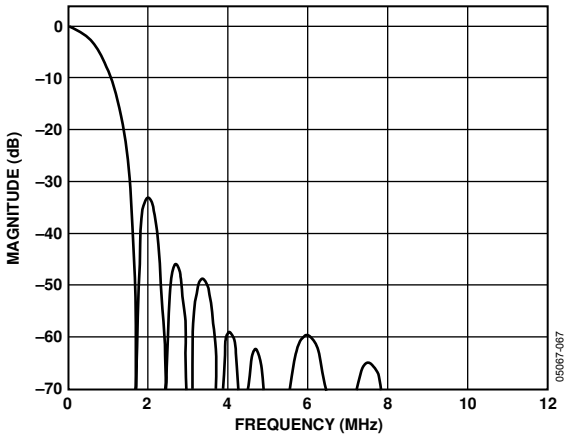


Figure 42. Chroma CIF Low-Pass Filter

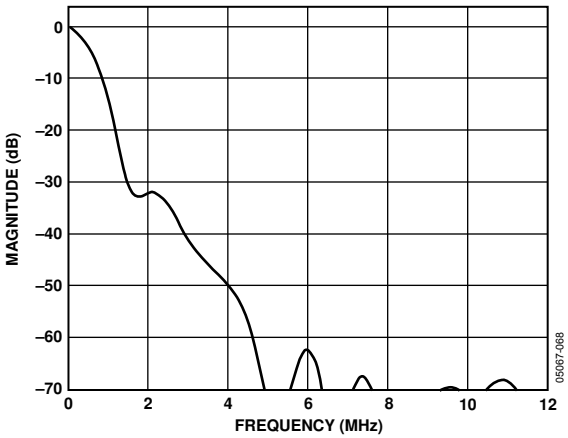


Figure 43. Chroma QCIF Low-Pass Filter

MPU PORT DESCRIPTION

The ADV7320/ADV7321 support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. This port operates in an open-drain configuration. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the ADV7320/ADV7321. Each slave device is recognized by a unique address. The ADV7320/ADV7321 have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 44 and Figure 45. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is enabled by setting the ALSB pin of the ADV7320/ADV7321 to Logic 0 or Logic 1. When ALSB is set to 1, there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to 0, there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns do not pass into the I^2C internal controller. This mode is recommended for noisy systems.

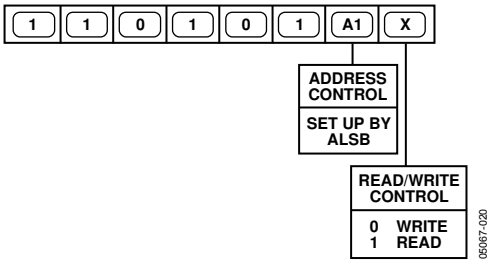


Figure 44. ADV7320 Slave Address = 0xD4

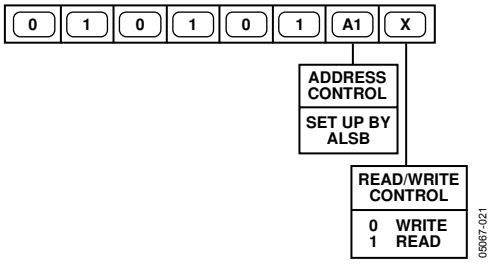


Figure 45. ADV7321 Slave Address = 0x54

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7320/ADV7321 act as standard slave devices on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all of the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause the device to immediately jump to the idle condition. During a given SCL high period, the user should only issue a start condition, a stop condition, or a stop condition followed by a start condition. If an invalid subaddress is issued by the user, the ADV7320/ADV7321 do not issue an acknowledge and return to the idle condition. If the user utilizes the auto-increment method of addressing the encoder and exceeds the highest subaddress, the following actions are taken:

- In read mode, the highest subaddress register contents are output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition is when the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7320/ADV7321, and the part returns to the idle condition.

Before writing to the subcarrier frequency registers, it is required to reset ADV7320/ADV7321 at least once after power-up.

The four subcarrier frequency registers must be updated, starting with Subcarrier Frequency Register 0 and ending with Subcarrier Frequency Register 3. The subcarrier frequency will only update after the last subcarrier frequency register byte has been received by the ADV7320/ADV7321.

Figure 46 illustrates an example of data transfer for a write sequence and the start and stop conditions. Figure 47 shows bus write and read sequences.

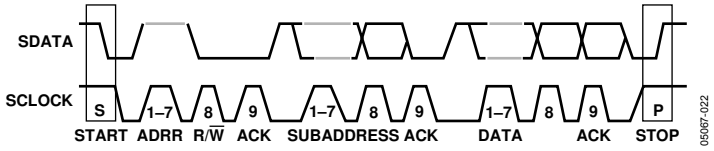


Figure 46. Bus Data Transfer

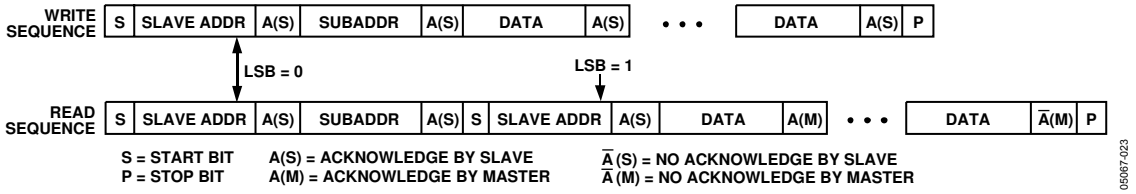


Figure 47. Read and Write Sequences

REGISTER ACCESS

The MPU can write to or read from all registers of the ADV7320/ADV7321 except the subaddress registers, which are write only registers. The subaddress register selected determines which register the next read or write operation will access. All communication with the part through the bus starts with an access to the subaddress register. A read/write operation is then performed from/to the target address, which increments to the next address until a stop command is performed on the bus.

REGISTER PROGRAMMING

The following tables describe the functionality of each register. All registers can be read from and written to, unless otherwise stated.

SUBADDRESS REGISTER (SR7 TO SR0)

Each subaddress register is an 8-bit write only register. After the encoder's bus is accessed and a read or write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place.

Table 7. Registers 0x00 to 0x01

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Value (Shaded)
0x00	Power Mode Register	Sleep Mode. With this control enabled, the current consumption is reduced to µA level. All DACs and the internal PLL cct are disabled. I^2C registers can be read from and written to in sleep mode.								0 1	Sleep mode off. Sleep mode on.	0xFC
		PLL and Oversampling Control. This control allows the internal PLL cct to be powered down and the oversampling to be switched off.							0 1		PLL on. PLL off.	
		DAC F: Power On/Off.						0 1			DAC F off. DAC F on.	
		DAC E: Power On/Off.					0 1				DAC E off. DAC E on.	
		DAC D: Power On/Off.				0 1					DAC D off. DAC D on.	
		DAC C: Power On/Off.			0 1						DAC C off. DAC C on.	
		DAC B: Power On/Off.		0 1							DAC B off. DAC B on.	
		DAC A: Power On/Off.	0 1								DAC A off. DAC A on.	
0x01	Mode Select Register	Reserved.								0	Reserved.	
		Clock Edge.							0 1		Cb clocked upon rising edge. Y clocked upon rising edge.	Only for PS interleaved input at 27 MHz.
		Reserved.						0				
		Clock Align.					0 1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns.	Only if two input clocks are used.
		Input Mode.		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1					SD input only. PS input only. HDTV input only. SD and PS (20-bit). SD and PS (10-bit). SD and HDTV (SD oversampled). SD and HDTV (HDTV oversampled). PS only (at 54 MHz).	0x38
		Y/C/S Bus Swap.	0 1								Allows data to be applied to data ports in various configurations (SD feature only).	See Table 21.