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# Multiformat Video Encoder, Six 12-Bit *Noise Shaped Video* DACS

Data Sheet

# ADV7340/ADV7341

## FEATURES

- 74.25 MHz 20-/30-bit high definition input support
  - Compliant with SMPTE 274 M (1080i), 296 M (720p), and 240 M (1035i)
- 6 *Noise Shaped Video*® (NSV) 12-bit video DACs
  - 16× (216 MHz) DAC oversampling for SD
  - 8× (216 MHz) DAC oversampling for ED
  - 4× (297 MHz) DAC oversampling for HD
  - 37 mA maximum DAC output current
- NTSC M, PAL B/D/G/H/I/M/N, PAL 60 support
- NTSC and PAL square pixel operation (24.54 MHz/29.5 MHz)
- Multiformat video input support
  - 4:2:2 YCrCb (SD, ED, and HD)
  - 4:4:4 YCrCb (ED and HD)
  - 4:4:4 RGB (SD, ED, and HD)
- Multiformat video output support
  - Composite (CVBS) and S-Video (Y-C)
  - Component YPrPb (SD, ED, and HD)
  - Component RGB (SD, ED, and HD)
- Macrovision Rev 7.1.L1 (SD) and Rev 1.2 (ED) compliant
- Simultaneous SD and ED/HD operation
- EIA/CEA-861B compliance support
- Copy generation management system (CGMS)
- Closed captioning and wide screen signaling (WSS)
- Integrated subcarrier locking to external video source
- Complete on-chip video timing generator
- On-chip test pattern generation
- On-board voltage reference (optional external input)
- Programmable features
  - Luma and chroma filter responses
  - Vertical blanking interval (VBI)
  - Subcarrier frequency ($F_{SC}$) and phase
  - Luma delay
- High definition (HD) programmable features (720p/1080i/1035i)
  - 4× oversampling (297 MHz)
  - Internal test pattern generator
  - Fully programmable YCrCb to RGB matrix
  - Gamma correction
  - Programmable adaptive filter control
  - Programmable sharpness filter control
  - CGMS (720p/1080i) and CGMS Type B (720p/1080i)
  - Undershoot limiter
  - Dual data rate (DDR) input support
- Enhanced definition (ED) programmable features (525p/625p)
  - 8× oversampling (216 MHz output)
  - Internal test pattern generator
    - Black bar, hatch, flat field/frame
  - Individual Y and PrPb output delay
  - Gamma correction
  - Programmable adaptive filter control
  - Fully programmable YCrCb to RGB matrix
  - Undershoot limiter
  - Macrovision Rev 1.2 (525p/625p) (ADV7340 only)
  - CGMS (525p/625p) and CGMS Type B (525p)
  - Dual data rate (DDR) input support
- Standard definition (SD) programmable features
  - 16× oversampling (216 MHz)
  - Internal test pattern generator
    - Color and black bar
  - Controlled edge rates for start and end of active video
  - Individual Y and PrPb output delay
  - Undershoot limiter
  - Gamma correction
  - Digital noise reduction (DNR)
  - Multiple chroma and luma filters
  - Luma-SSAF filter with programmable gain/attenuation
  - PrPb SSAF
  - Separate pedestal control on component and composite/S-Video output
  - VCR FF/RW sync mode
  - Macrovision Rev 7.1.L1 (ADV7340 only)
  - Copy generation management system (CGMS)
  - Wide screen signaling (WSS)
  - Closed captioning
- Serial MPU interface with $I^2C$ compatibility
- 3.3 V analog operation
- 1.8 V digital operation
- 1.8 V or 3.3 V I/O operation
- Temperature range: −40°C to +85°C

## APPLICATIONS

- DVD recorders and players
- High definition Blu-ray DVD players

Rev. C


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## GENERAL DESCRIPTION

The ADV7340/ADV7341 are high speed, digital-to-analog video encoders in a 64-lead LQFP package. Six high speed, NSV, 3.3 V, 12-bit video DACs provide support for composite (CVBS), S-Video (Y-C), and component (YPrPb/RGB) analog outputs in standard definition (SD), enhanced definition (ED), or high definition (HD) video formats.

The ADV7340/ADV7341 have a 30-bit pixel input port that can be configured in a variety of ways. SD video formats are supported over an SDR interface, and ED/HD video formats are supported over SDR and DDR interfaces. Pixel data can be supplied in either the YCrCb or RGB color space.

The parts also support embedded EAV/SAV timing codes, external video synchronization signals, and I²C® communication protocol.

In addition, simultaneous SD and ED/HD input and output are supported. Full-drive DACs ensure that external output buffering is not required, while 216 MHz (SD and ED) and 297 MHz (HD) oversampling ensures that external output filtering is not required.

Cable detection and DAC autopower-down features keep power consumption to a minimum.

Table 1 lists the video standards directly supported by the ADV7340/ADV7341.

**Table 1. Standards Directly Supported by the ADV7340/ ADV7341**

| Active Resolution | I/P[1] | Frame Rate (Hz) | Clock Input (MHz) | Standard |
|---|---|---|---|---|
| 720 × 240 | P | 59.94 | 27 | |
| 720 × 288 | P | 50 | 27 | |
| 720 × 480 | I | 29.97 | 27 | ITU-R BT.601/656 |
| 720 × 576 | I | 25 | 27 | ITU-R BT.601/656 |
| 640 × 480 | I | 29.97 | 24.54 | NTSC Square Pixel |
| 768 × 576 | I | 25 | 29.5 | PAL Square Pixel |
| 720 × 483 | P | 59.94 | 27 | SMPTE 293M |
| 720 × 483 | P | 59.94 | 27 | BTA T-1004 |
| 720 × 483 | P | 59.94 | 27 | ITU-R BT.1358 |
| 720 × 576 | P | 50 | 27 | ITU-R BT.1358 |
| 720 × 483 | P | 59.94 | 27 | ITU-R BT.1362 |
| 720 × 576 | P | 50 | 27 | ITU-R BT.1362 |
| 1920 × 1035 | I | 30 | 74.25 | SMPTE 240M |
| 1920 × 1035 | I | 29.97 | 74.1758 | SMPTE 240M |
| 1280 × 720 | P | 60, 50, 30, 25, 24 | 74.25 | SMPTE 296M |
| 1280 × 720 | P | 23.97, 59.94, 29.97 | 74.1758 | SMPTE 296M |
| 1920 × 1080 | I | 30, 25 | 74.25 | SMPTE 274M |
| 1920 × 1080 | I | 29.97 | 74.1758 | SMPTE 274M |
| 1920 × 1080 | P | 30, 25, 24 | 74.25 | SMPTE 274M |
| 1920 × 1080 | P | 23.98, 29.97 | 74.1758 | SMPTE 274M |
| 1920 × 1080 | P | 24 | 74.25 | ITU-R BT.709-5 |

[1] I = interlaced, P = progressive.

## FUNCTIONAL BLOCK DIAGRAM

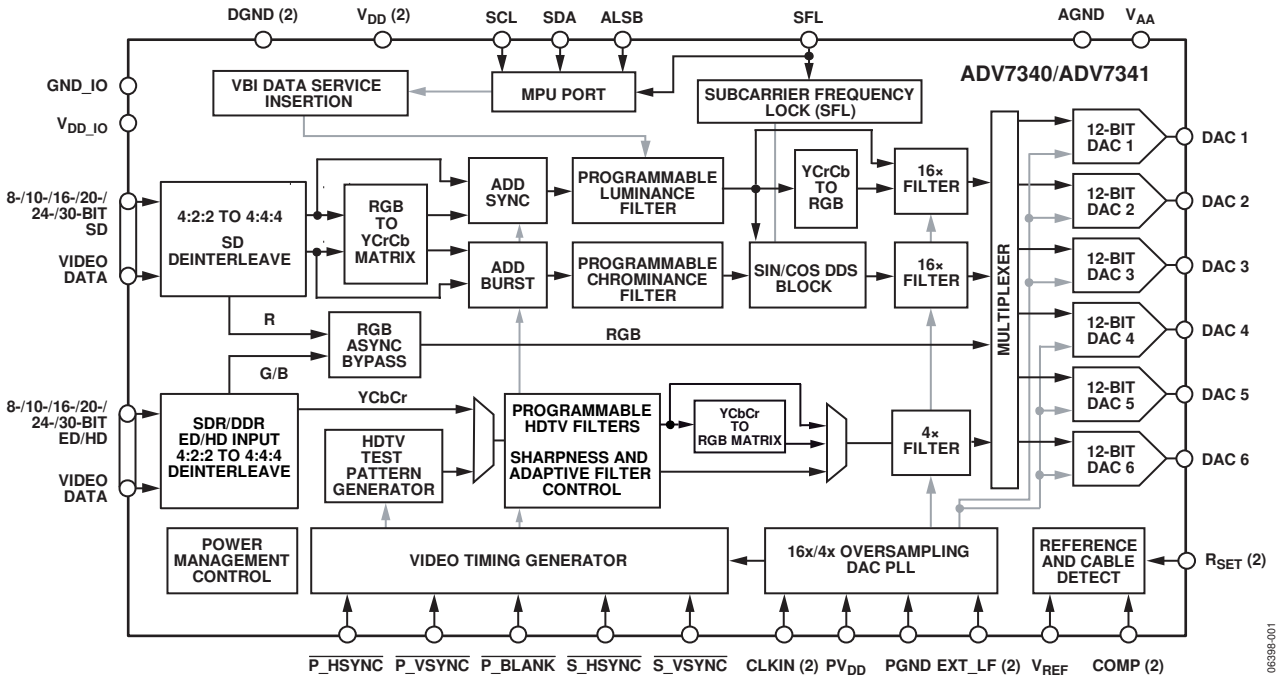



*Figure 1.*

# SPECIFICATIONS

## POWER SUPPLY AND VOLTAGE SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| SUPPLY VOLTAGES | | | | |
| $V_{DD}$ | 1.71 | 1.8 | 1.89 | V |
| $V_{DD\_IO}$ | 1.71 | 3.3 | 3.63 | V |
| $PV_{DD}$ | 1.71 | 1.8 | 1.89 | V |
| $V_{AA}$ | 2.6 | 3.3 | 3.465 | V |
| POWER SUPPLY REJECTION RATIO | | 0.002 | | %/% |

## VOLTAGE REFERENCE SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 3.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Internal Reference Range, $V_{REF}$ | 1.186 | 1.248 | 1.31 | V |
| External Reference Range, $V_{REF}$ | 1.15 | 1.235 | 1.31 | V |
| External $V_{REF}$ Current[1] | | ±10 | | µA |

[1] External current required to overdrive internal $V_{REF}$.

## INPUT CLOCK SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 1.71 V to 3.63 V.
All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 4.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLKIN\_A}$ | SD/ED | | 27 | | MHz |
| $f_{CLKIN\_A}$ | ED (at 54 MHz) | | 54 | | MHz |
| $f_{CLKIN\_A}$ | HD | | 74.25 | | MHz |
| $f_{CLKIN\_B}$ | ED | | 27 | | MHz |
| $f_{CLKIN\_B}$ | HD | | 74.25 | | MHz |
| CLKIN_A High Time, $t_9$ | | 40 | | | % of one clock cycle |
| CLKIN_A Low Time, $t_{10}$ | | 40 | | | % of one clock cycle |
| CLKIN_B High Time, $t_9$ | | 40 | | | % of one clock cycle |
| CLKIN_B Low Time, $t_{10}$ | | 40 | | | % of one clock cycle |
| CLKIN_A Peak-to-Peak Jitter Tolerance | | | 2 | | ±ns |
| CLKIN_B Peak-to-Peak Jitter Tolerance | | | 2 | | ±ns |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition.

## ANALOG OUTPUT SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 1.71 V to 3.63 V. $V_{REF}$ = 1.235 V (driven externally). All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 5.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Full-Drive Output Current (Full-Scale) | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω DAC 1, DAC 2, DAC 3 enabled[1] | 33 | 34.6 | 37 | mA |
| | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω DAC 1 enabled only[2] | 33 | 33.5 | 37 | mA |
| Low-Drive Output Current (Full-Scale)[3] | $R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω | 4.1 | 4.3 | 4.5 | mA |
| DAC-to-DAC Matching | DAC 1 to DAC 6 | | 1.0 | | % |
| Output Compliance, $V_{OC}$ | | 0 | | 1.4 | V |
| Output Capacitance, $C_{OUT}$ | DAC 1, DAC 2, DAC 3 | | 10 | | pF |
| | DAC 4, DAC 5, DAC 6 | | 6 | | pF |
| Analog Output Delay[4] | DAC 1, DAC 2, DAC 3 | | 8 | | ns |
| | DAC 4, DAC 5, DAC 6 | | 6 | | ns |
| DAC Analog Output Skew | DAC 1, DAC 2, DAC 3 | | 2 | | ns |
| | DAC 4, DAC 5, DAC 6 | | 1 | | ns |

[1] Applicable to full-drive capable DACs only, that is, DAC 1, DAC 2, DAC 3.
[2] The recommended method of bringing this typical value back to the ideal value is by adjusting Register 0x0B to the recommended value of 0x12.
[3] Applicable to all DACs.
[4] Output delay measured from the 50% point of the rising edge of the input clock to the 50% point of the DAC output full-scale transition.

## DIGITAL INPUT/OUTPUT SPECIFICATIONS—3.3 V

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 2.97 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 6.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage, $V_{IH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{IL}$ | | | | 0.8 | V |
| Input Leakage Current, $I_{IN}$ | $V_{IN} = V_{DD\_IO}$ | | | ±10 | µA |
| Input Capacitance, $C_{IN}$ | | | 4 | | pF |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 400 µA | 2.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| Three-State Leakage Current | $V_{IN}$ = 0.4 V, 2.4 V | | | ±1.0 | µA |
| Three-State Output Capacitance | | | 4 | | pF |

## DIGITAL INPUT/OUTPUT SPECIFICATIONS—1.8 V

When $V_{DD\_IO}$ is set to 1.8 V, all the digital video inputs and control inputs, such as $I^2C$, HS, VS, should use 1.8 V levels.

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 1.71 V to 1.89 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 7.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage, $V_{IH}$ | | 0.7 $V_{DD\_IO}$ | | | V |
| Input Low Voltage, $V_{IL}$ | | | | 0.3 $V_{DD\_IO}$ | V |
| Input Capacitance, $C_{IN}$ | | | 4 | | pF |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 400 µA | $V_{DD\_IO}$ − 0.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| Three-State Output Capacitance | | | 4 | | pF |

## DIGITAL TIMING SPECIFICATIONS—3.3 V

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 2.97 V to 3.63 V.
All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 8.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIDEO DATA AND VIDEO CONTROL PORT[2, 3] | | | | | |
| Data Input Setup Time, $t_{11}$[4] | SD | 2.1 | | | ns |
| | ED/HD-SDR | 2.3 | | | ns |
| | ED/HD-DDR | 2.3 | | | ns |
| | ED (at 54 MHz) | 1.7 | | | ns |
| Data Input Hold Time, $t_{12}$[4] | SD | 1.0 | | | ns |
| | ED/HD-SDR | 1.1 | | | ns |
| | ED/HD-DDR | 1.1 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Input Setup Time, $t_{11}$[4] | SD | 2.1 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 2.3 | | | ns |
| | ED (at 54 MHz) | 1.7 | | | ns |
| Control Input Hold Time, $t_{12}$[4] | SD | 1.0 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.1 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Output Access Time, $t_{13}$[4] | SD | | | 12 | ns |
| | ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz) | | | 10 | ns |
| Control Output Hold Time, $t_{14}$[4] | SD | 4.0 | | | ns |
| | ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz) | 3.5 | | | ns |
| PIPELINE DELAY[5] | | | | | |
| SD[1] | | | | | |
| CVBS/YC Outputs (2×) | SD oversampling disabled | | 68 | | Clock cycles |
| CVBS/YC Outputs (16×) | SD oversampling enabled | | 67 | | Clock cycles |
| Component Outputs (2×) | SD oversampling disabled | | 78 | | Clock cycles |
| Component Outputs (16×) | SD oversampling enabled | | 84 | | Clock cycles |
| ED[1] | | | | | |
| Component Outputs (1×) | ED oversampling disabled | | 41 | | Clock cycles |
| Component Outputs (8×) | ED oversampling enabled | | 46 | | Clock cycles |
| HD[1] | | | | | |
| Component Outputs (1×) | HD oversampling disabled | | 40 | | Clock cycles |
| Component Outputs (4×) | HD oversampling enabled | | 44 | | Clock cycles |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: C[9:0], Y[9:0], and S[9:0].
[3] Video control: P_HSYNC, P_VSYNC, P_BLANK, S_HSYNC, and S_VSYNC.
[4] Guaranteed by characterization.
[5] Guaranteed by design.

## DIGITAL TIMING SPECIFICATIONS—1.8 V

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 1.71 V to 1.89 V.
All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 9.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIDEO DATA AND VIDEO CONTROL PORT[2, 3] | | | | | |
| Data Input Setup Time, $t_{11}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR | 1.9 | | | ns |
| | ED/HD-DDR | 1.9 | | | ns |
| | ED (at 54 MHz) | 1.6 | | | ns |
| Data Input Hold Time, $t_{12}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR | 1.5 | | | ns |
| | ED/HD-DDR | 1.5 | | | ns |
| | ED (at 54 MHz) | 1.3 | | | ns |
| Control Input Setup Time, $t_{11}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.2 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Input Hold Time, $t_{12}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.0 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Output Access Time, $t_{13}$[4] | SD | | | 13 | ns |
| | ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz) | | | 12 | ns |
| Control Output Hold Time, $t_{14}$[4] | SD | 4.0 | | | ns |
| | ED/HD-SDR, ED/HD-DDR or ED (at 54 MHz) | 5.0 | | | ns |
| PIPELINE DELAY[5] | | | | | |
| SD[1] | | | | | |
| CVBS/YC Outputs (2×) | SD oversampling disabled | | 68 | | Clock cycles |
| CVBS/YC Outputs (16×) | SD oversampling enabled | | 67 | | Clock cycles |
| Component Outputs (2×) | SD oversampling disabled | | 78 | | Clock cycles |
| Component Outputs (16×) | SD oversampling enabled | | 84 | | Clock cycles |
| ED[1] | | | | | |
| Component Outputs (1×) | ED oversampling disabled | | 41 | | Clock cycles |
| Component Outputs (8×) | ED oversampling enabled | | 46 | | Clock cycles |
| HD[1] | | | | | |
| Component Outputs (1×) | HD oversampling disabled | | 40 | | Clock cycles |
| Component Outputs (4×) | HD oversampling enabled | | 44 | | Clock cycles |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: C[9:0], Y[9:0], and S[9:0].
[3] Video control: P_HSYNC, P_VSYNC, P_BLANK, S_HSYNC, and S_VSYNC.
[4] Guaranteed by characterization.
[5] Guaranteed by design.

## MPU PORT TIMING SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V. $PV_{DD}$ = 1.71 V to 1.89 V. $V_{AA}$ = 2.6 V to 3.465 V. $V_{DD\_IO}$ = 1.71 V to 3.63 V.
All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 10.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MPU PORT, $I^2C$ MODE[1] | See Figure 19 | | | | |
| SCL Frequency | | 0 | | 400 | kHz |
| SCL High Pulse Width, $t_1$ | | 0.6 | | | µs |
| SCL Low Pulse Width, $t_2$ | | 1.3 | | | µs |
| Hold Time (Start Condition), $t_3$ | | 0.6 | | | µs |
| Setup Time (Start Condition), $t_4$ | | 0.6 | | | µs |
| Data Setup Time, $t_5$ | | 100 | | | ns |
| SDA, SCL Rise Time, $t_6$ | | | | 300 | ns |
| SDA, SCL Fall Time, $t_7$ | | | | 300 | ns |
| Setup Time (Stop Condition), $t_8$ | | 0.6 | | | µs |

[1] Guaranteed by characterization.

## POWER SPECIFICATIONS

$V_{DD}$ = 1.8 V, $PV_{DD}$ = 1.8 V, $V_{AA}$ = 3.3 V, $V_{DD\_IO}$ = 3.3 V, $T_A$ = 25°C.

**Table 11.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| NORMAL POWER MODE[1, 2] | | | | | |
| $I_{DD}$[3] | SD only (16× oversampling) | | 90 | | mA |
| | ED only (8× oversampling)[4] | | 65 | | mA |
| | HD only (4× oversampling)[4] | | 91 | | mA |
| | SD (16× oversampling) and ED (8× oversampling) | | 95 | | mA |
| | SD (16× oversampling) and HD (4× oversampling) | | 122 | | mA |
| $I_{DD\_IO}$ | | | 1 | | mA |
| $I_{AA}$[5] | Three DACs enabled (ED/HD only) | | 124 | | mA |
| | Six DACs enabled (SD only and simultaneous modes ) | | 140 | | mA |
| $I_{PLL}$ | SD only, ED only, or HD only modes | | 5 | | mA |
| | Simultaneous modes | | 10 | | mA |
| SLEEP MODE | | | | | |
| $I_{DD}$ | | | 5 | | µA |
| $I_{AA}$ | | | 0.3 | | µA |
| $I_{DD\_IO}$ | | | 0.2 | | µA |
| $I_{PLL}$ | | | 0.1 | | µA |

[1] $R_{SET1}$ = 510 Ω (DAC 1, DAC 2, and DAC 3 operating in full-drive mode). $R_{SET2}$ = 4.12 kΩ (DAC 4, DAC 5, and DAC 6 operating in low-drive mode).
[2] 75% color bar test pattern applied to pixel data pins.
[3] $I_{DD}$ is the continuous current required to drive the digital core.
[4] Applicable to both single data rate (SDR) and dual data rate (DDR) input modes.
[5] $I_{AA}$ is the total current required to supply all DACs.

## VIDEO PERFORMANCE SPECIFICATIONS

$V_{DD}$ = 1.8 V, $PV_{DD}$ = 1.8 V, $V_{AA}$ = 3.3 V, $V_{DD\_IO}$ = 3.3 V, $T_A$ = 25°C, $V_{REF}$ driven externally.

**Table 12.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity | $R_{SET1}$ = 510 Ω, $R_{L1}$ = 37.5 Ω | | 0.75 | | LSBs |
| | $R_{SET2}$ = 4.12 kΩ, $R_{L2}$ = 300 Ω | | 1 | | LSBs |
| Differential Nonlinearity[1] +ve | $R_{SET1}$ = 510 Ω, $R_{L1}$ = 37.5 Ω | | 0.25 | | LSBs |
| | $R_{SET2}$ = 4.12 kΩ, $R_{L2}$ = 300 Ω | | 0.8 | | LSBs |
| Differential Nonlinearity[1] −ve | $R_{SET1}$ = 510 Ω, $R_{L1}$ = 37.5 Ω | | 0.43 | | LSBs |
| | $R_{SET2}$ = 4.12 kΩ, $R_{L2}$ = 300 Ω | | 0.35 | | LSBs |
| STANDARD DEFINTION (SD) MODE | | | | | |
| Luminance Nonlinearity | | | 0.35 | | ±% |
| Differential Gain | NTSC | | 0.3 | | % |
| Differential Phase | NTSC | | 0.4 | | Degrees |
| SNR | Luma ramp | | 63 | | dB |
| SNR | Flat field full bandwidth | | 79.5 | | dB |
| ENHANCED DEFINITION (ED) MODE | | | | | |
| Luma Bandwidth | | | 12.5 | | MHz |
| Chroma Bandwidth | | | 5.8 | | MHz |
| HIGH DEFINITION (HD) MODE | | | | | |
| Luma Bandwidth | | | 30 | | MHz |
| Chroma Bandwidth | | | 13.75 | | MHz |

[1] Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For −ve DNL, the actual step value lies below the ideal step value.

# TIMING DIAGRAMS

The following abbreviations are used in Figure 2 to Figure 13:

- $t_9$ = clock high time
- $t_{10}$ = clock low time
- $t_{11}$ = data setup time
- $t_{12}$ = data hold time
- $t_{13}$ = control output access time
- $t_{14}$ = control output hold time

In addition, refer to Table 36 for the ADV7340/ADV7341 input configuration.

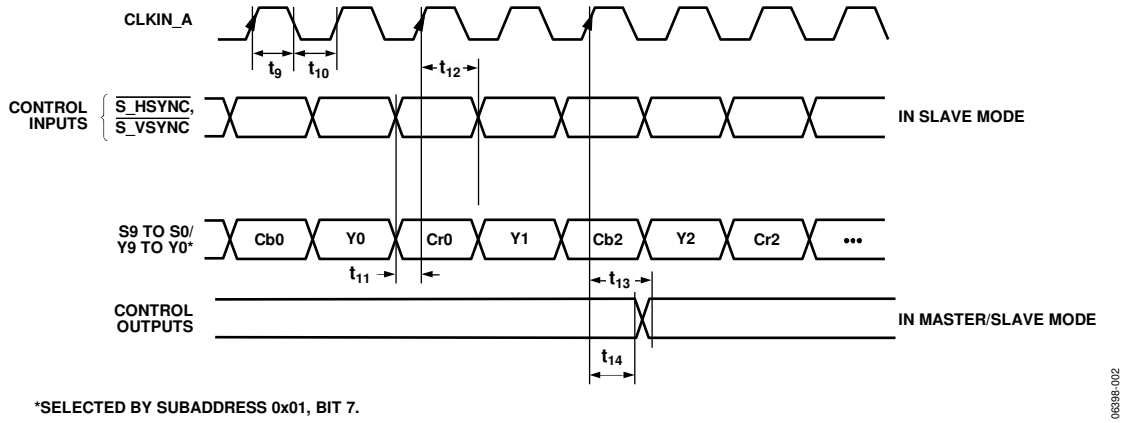



*Figure 2. SD Only, 8-/10-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 000)*

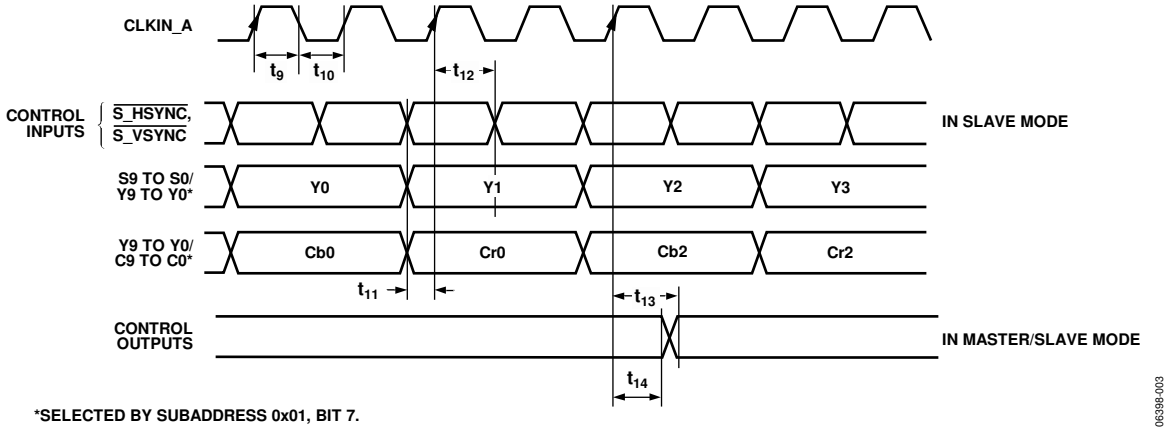



*Figure 3. SD Only, 16-/20-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 000)*

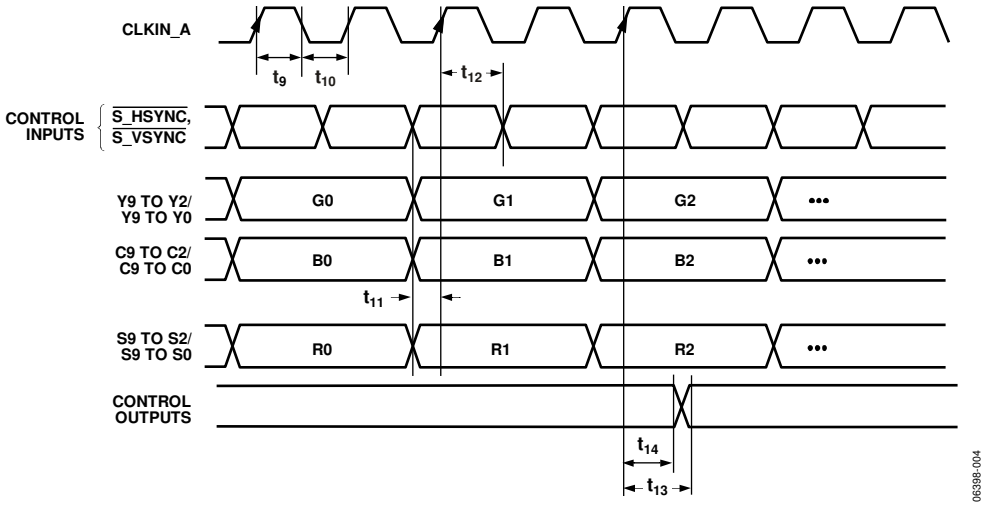



*Figure 4. SD Only, 24-/30-Bit, 4:4:4 RGB Pixel Input Mode (Input Mode 000)*

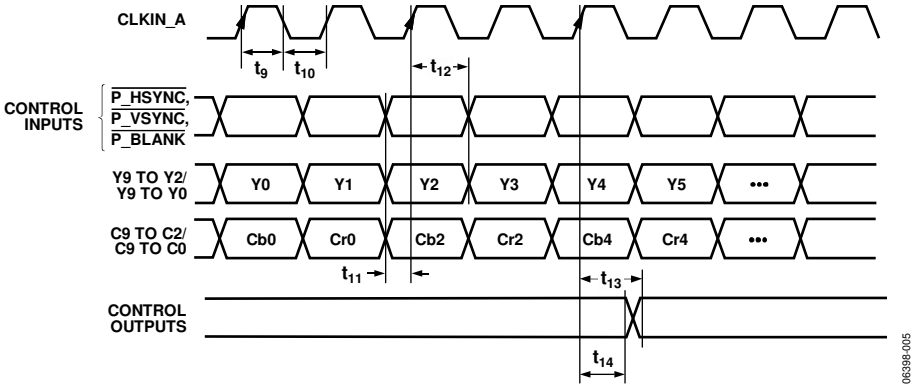



*Figure 5. ED/HD-SDR Only, 16-/20-Bit, 4:2:2 YCrCb Pixel Input Mode (Input Mode 001)*

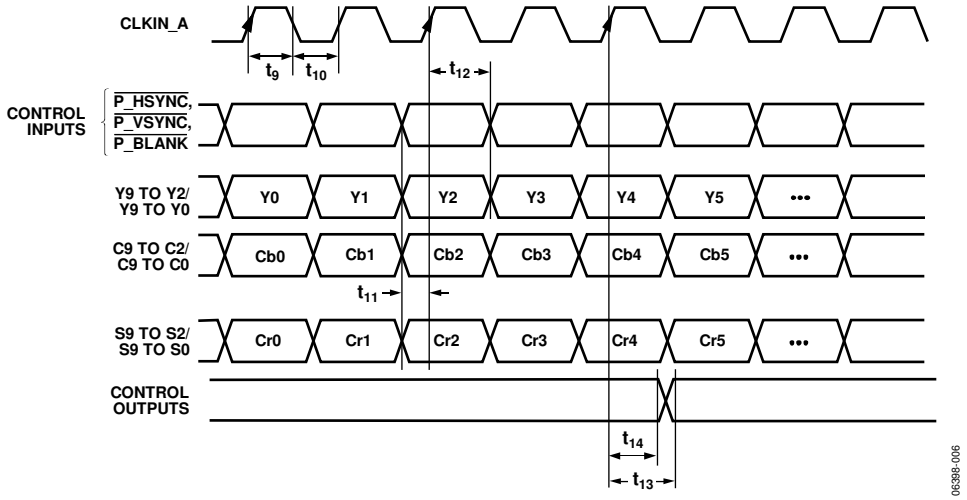



*Figure 6. ED/HD-SDR Only, 24-/30-Bit, 4:4:4 YCrCb Pixel Input Mode (Input Mode 001)*

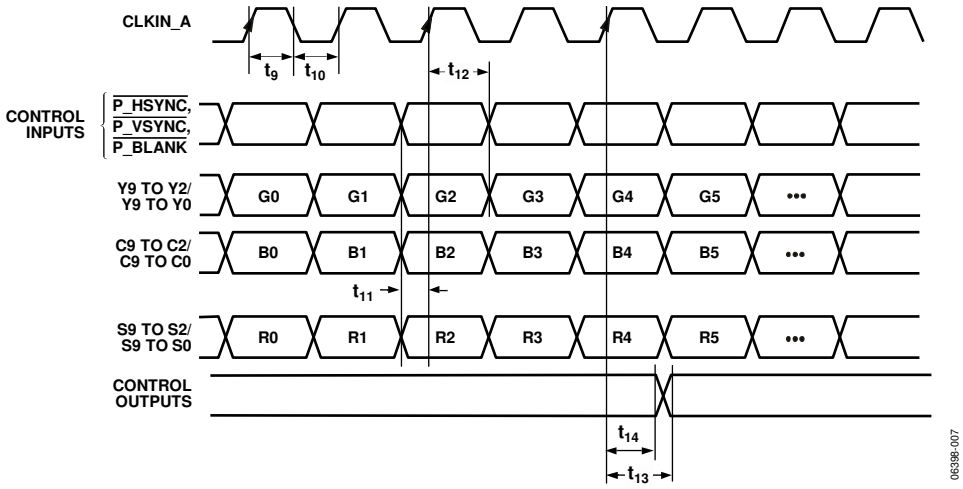



*Figure 7. ED/HD-SDR Only, 24-/30-Bit, 4:4:4 RGB Pixel Input Mode (Input Mode 001)*

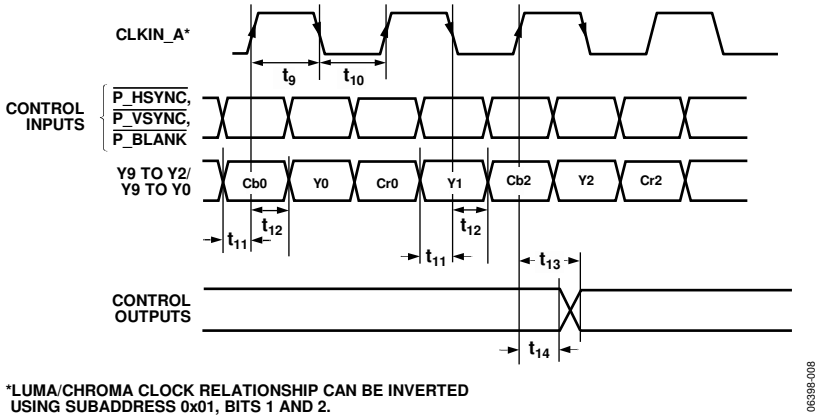



*Figure 8. ED/HD-DDR Only, 8-/10-Bit, 4:2:2 YCrCb ($\overline{HSYNC}$/$\overline{VSYNC}$) Pixel Input Mode (Input Mode 010)*

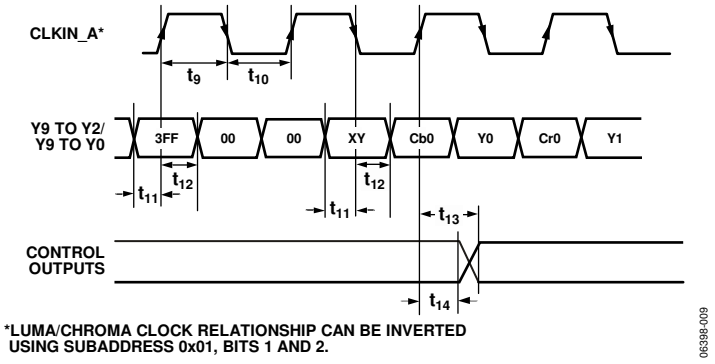



*Figure 9. ED/HD-DDR Only, 8-/10-Bit, 4:2:2 YCrCb (EAV/SAV) Pixel Input Mode (Input Mode 010)*

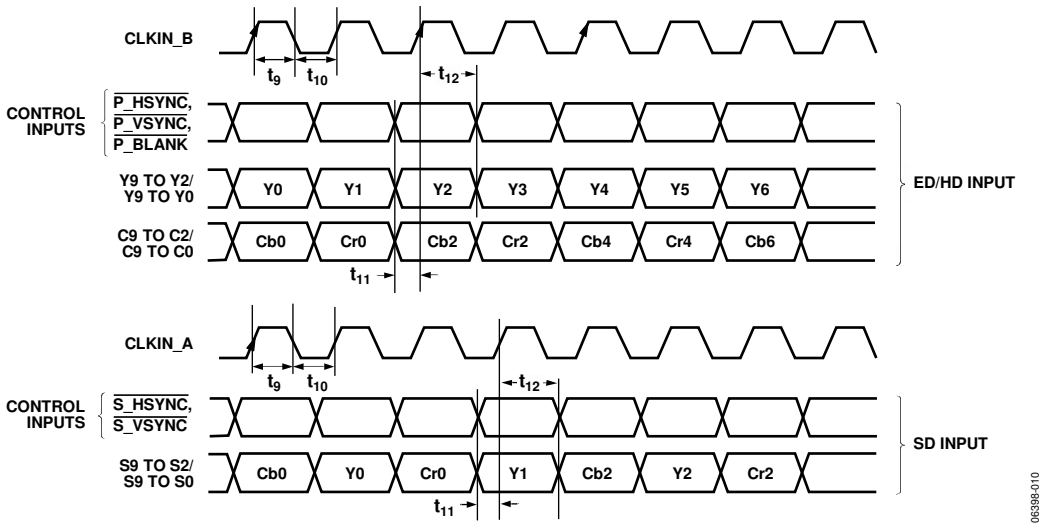



*Figure 10. SD, ED/HD-SDR Input Mode, 16-/20-Bit, 4:2:2 ED/HD and 8-/10-Bit, SD Pixel Input Mode (Input Mode 011)*

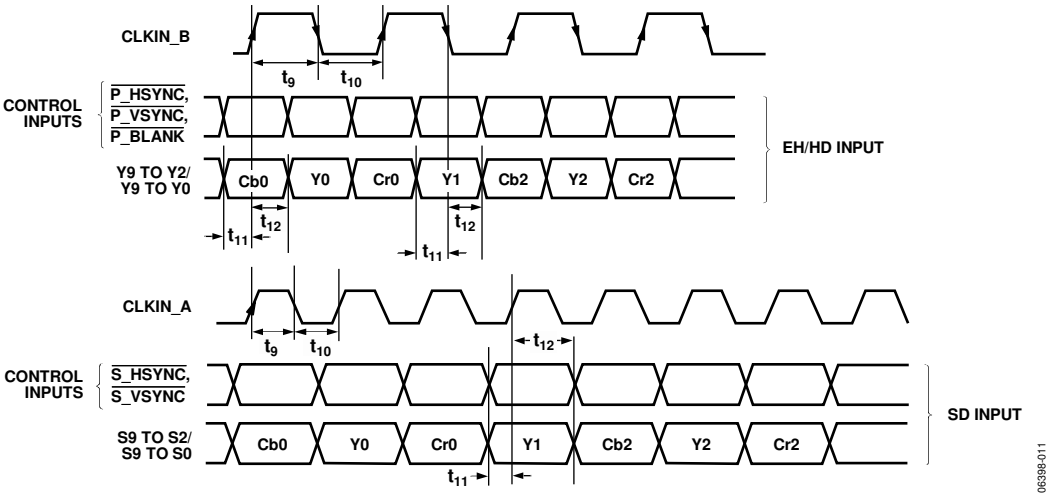



*Figure 11. SD, ED/HD-DDR Input Mode, 8-/10-Bit, 4:2:2 ED/HD and 8-/10-Bit, SD Pixel Input Mode (Input Mode 100)*

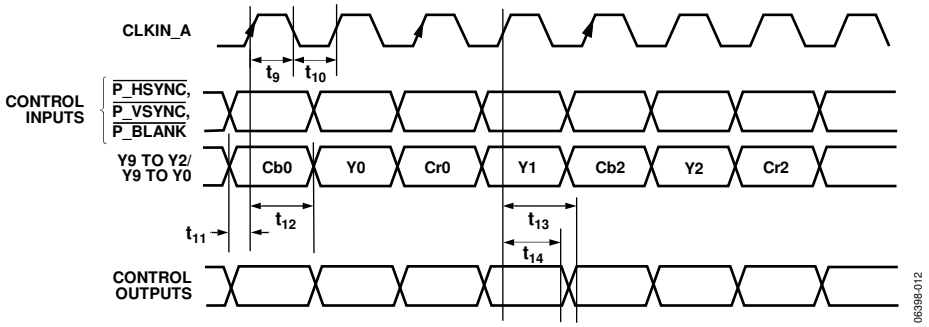



*Figure 12. ED Only (at 54 MHz), 8-/10-Bit, 4:2:2 YCrCb ($\overline{HSYNC}$/$\overline{VSYNC}$) Pixel Input Mode (Input Mode 111)*

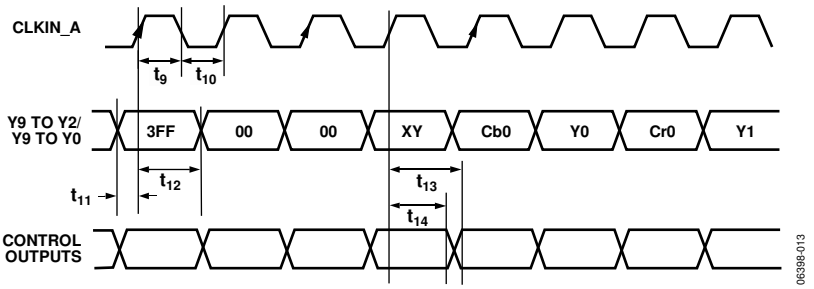



*Figure 13. ED Only (at 54 MHz), 8-/10-Bit, 4:2:2 YCrCb (EAV/SAV) Pixel Input Mode (Input Mode 111)*

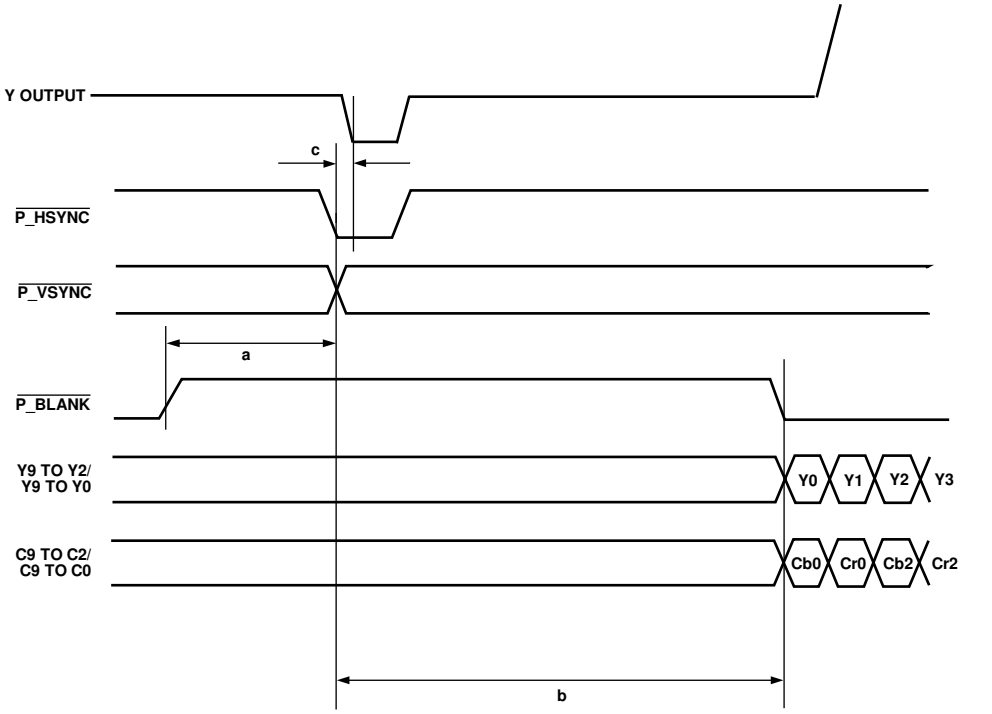
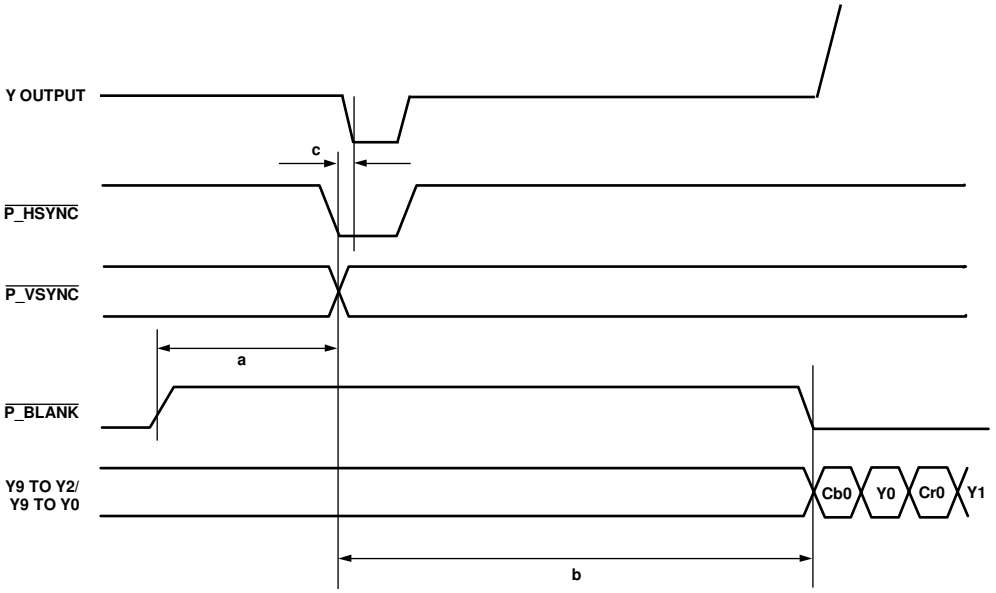



*Figure 14. ED-SDR, 16-/20-Bit, 4:2:2 YCrCb (HSYNC/VSYNC) Input Timing Diagram*




a = 32 CLKCYCLES FOR 525p
a = 24 CLKCYCLES FOR 625p
AS RECOMMENDED BY STANDARD

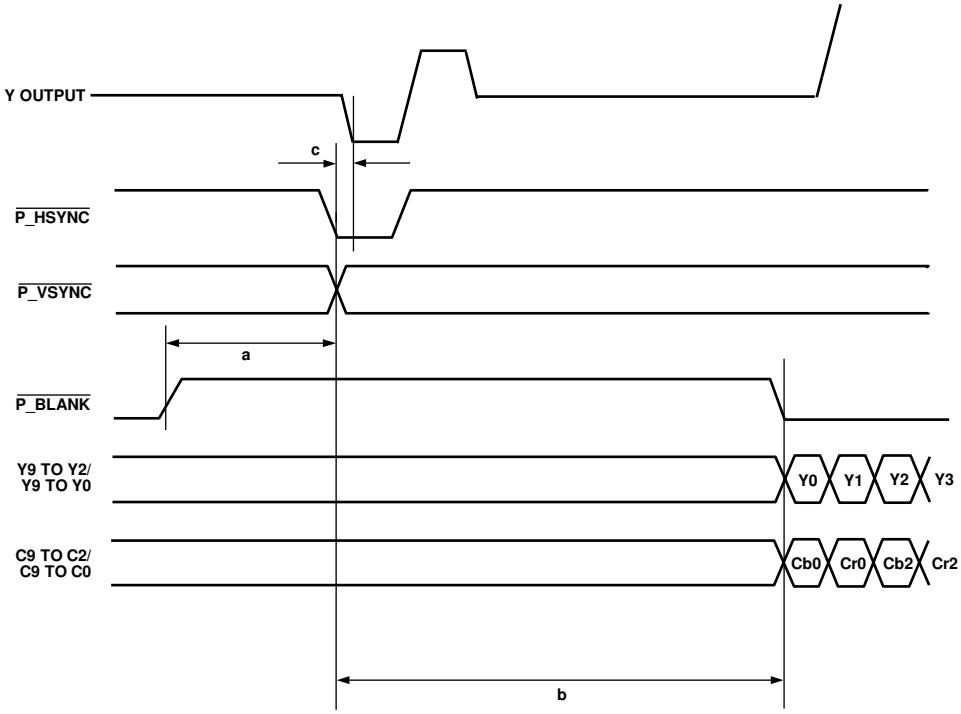
b(MIN) = 244 CLKCYCLES FOR 525p
b(MIN) = 264 CLKCYCLES FOR 625p

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06398-015

*Figure 15. ED-DDR, 8-/10-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*



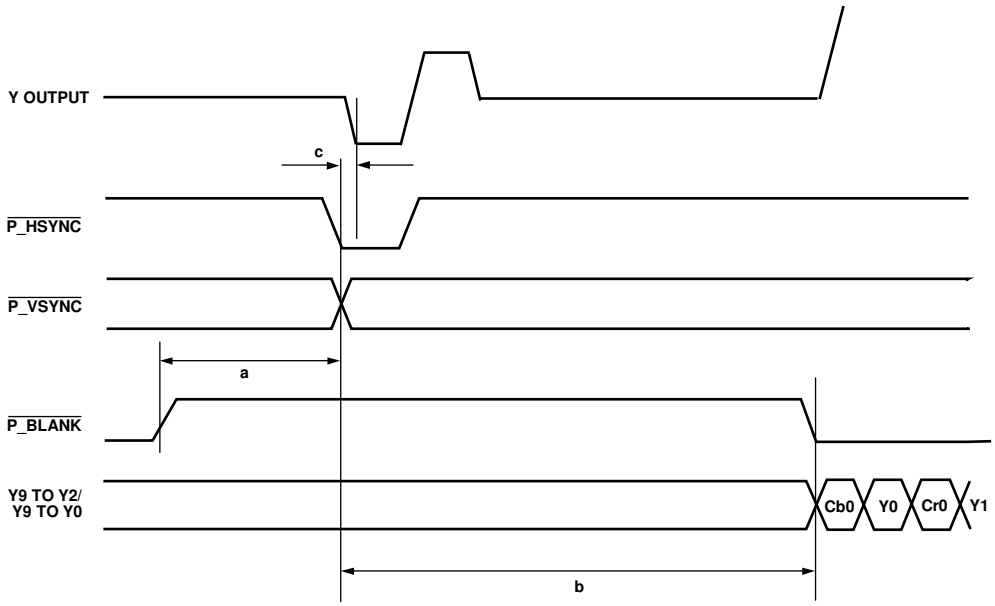

a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06398-016

*Figure 16. HD-SDR, 16-/20-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*



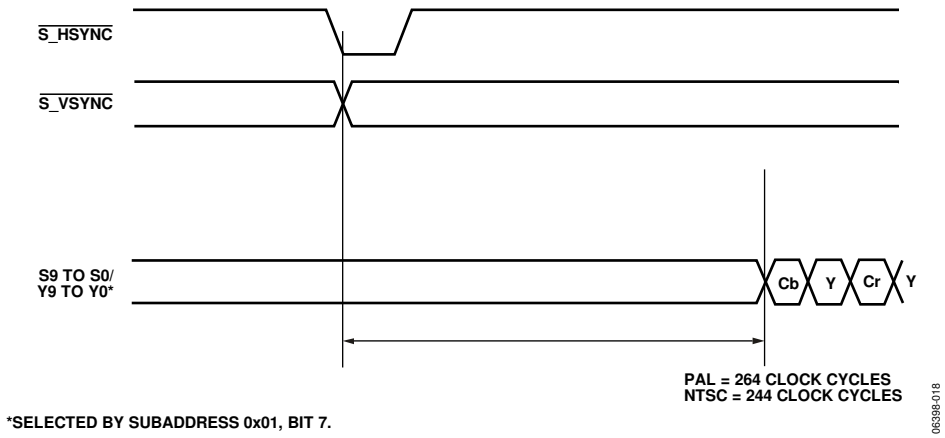

a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06398-017

*Figure 17. HD-DDR, 8-/10-Bit, 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*




*SELECTED BY SUBADDRESS 0x01, BIT 7.

*Figure 18. SD Input Timing Diagram (Timing Mode 1)*

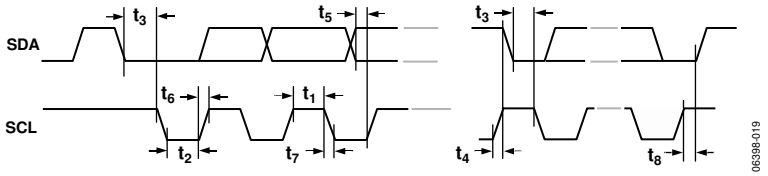



*Figure 19. MPU Port Timing Diagram ($I^2C$ Mode)*

# ABSOLUTE MAXIMUM RATINGS

**Table 13.**

| Parameter[1] | Rating |
|---|---|
| $V_{AA}$ to AGND | −0.3 V to +3.9 V |
| $V_{DD}$ to DGND | −0.3 V to +2.3 V |
| $PV_{DD}$ to PGND | −0.3 V to +2.3 V |
| $V_{DD\_IO}$ to GND_IO | −0.3 V to +3.9 V |
| AGND to DGND | −0.3 V to +0.3 V |
| AGND to PGND | −0.3 V to +0.3 V |
| AGND to GND_IO | −0.3 V to +0.3 V |
| DGND to PGND | −0.3 V to +0.3 V |
| DGND to GND_IO | −0.3 V to +0.3 V |
| PGND to GND_IO | −0.3 V to +0.3 V |
| Digital Input Voltage to GND_IO | −0.3 V to $V_{DD\_IO}$ + 0.3 V |
| Analog Outputs to AGND | −0.3 V to $V_{AA}$ |
| Maximum CLKIN Input Frequency | 80 MHz |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | 150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C |

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The ADV7340/ADV7341 are high performance integrated circuits with an ESD rating of <1 kV, and they are ESD sensitive. Proper precautions should be taken for handling and assembly.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 14. Thermal Resistance[1]**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 64-Lead LQFP | 47 | 11 | °C/W |

[1] Values are based on a JEDEC 4-layer test board.

The ADV7340/ADV7341 are RoHS-compliant, Pb-free products. The lead finish is 100% pure Sn electroplate. The devices are suitable for Pb-free applications up to 255°C (±5°C) IR reflow (JEDEC STD-20).

Each part is backward compatible with conventional SnPb soldering processes. The electroplated Sn coating can be soldered with Sn/Pb solder paste at conventional reflow temperatures of 220°C to 235°C.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

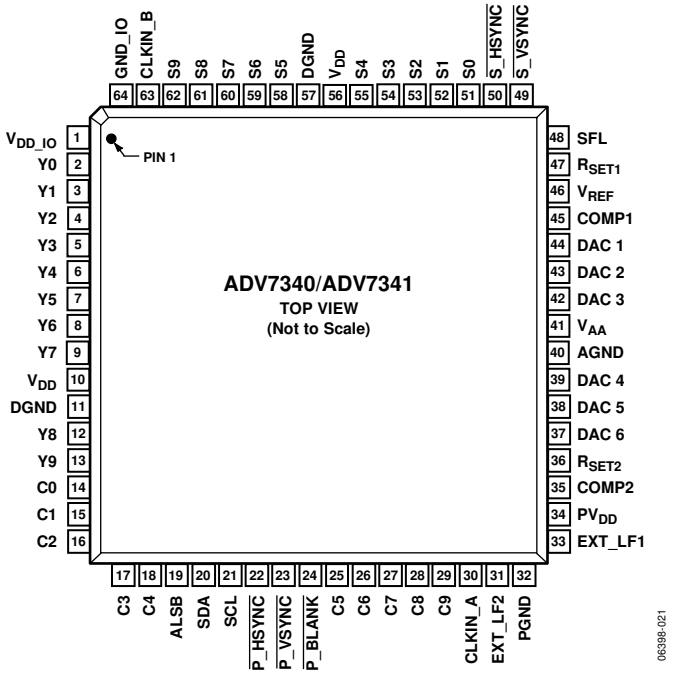



*Figure 20. Pin Configuration*

**Table 15. Pin Function Descriptions**

| Pin No. | Mnemonic | Input/ Output | Description |
|---|---|---|---|
| 13, 12, 9 to 2 | Y9 to Y0 | I | 10-Bit Pixel Port (Y9 to Y0). Y0 is the LSB. Refer to Table 36 for input modes. |
| 29 to 25, 18 to 14 | C9 to C0 | I | 10-Bit Pixel Port (C9 to C0). C0 is the LSB. Refer to Table 36 for input modes. |
| 62 to 58, 55 to 51 | S9 to S0 | I | 10-Bit Pixel Port (S9 to S0). S0 is the LSB. Refer to Table 36 for input modes. |
| 30 | CLKIN_A | I | Pixel Clock Input for HD Only (74.25 MHz), ED[1] Only (27 MHz or 54 MHz), or SD Only (27 MHz). |
| 63 | CLKIN_B | I | Pixel Clock Input for Dual Modes Only. Requires a 27 MHz reference clock for ED operation or a 74.25 MHz reference clock for HD operation. |
| 50 | $\overline{\text{S\_HSYNC}}$ | I/O | SD Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section. |
| 49 | $\overline{\text{S\_VSYNC}}$ | I/O | SD Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section. |
| 22 | $\overline{\text{P\_HSYNC}}$ | I | ED/HD Horizontal Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section. |
| 23 | $\overline{\text{P\_VSYNC}}$ | I | ED/HD Vertical Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section. |
| 24 | $\overline{\text{P\_BLANK}}$ | I | ED/HD Blanking Signal. See the External Horizontal and Vertical Synchronization Control section. |
| 48 | SFL | I/O | Subcarrier Frequency Lock (SFL) Input. |
| 47 | $R_{SET1}$ | I | This pin is used to control the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from $R_{SET1}$ to AGND. For low-drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from $R_{SET1}$ to AGND. |
| 36 | $R_{SET2}$ | I | This pin is used to control the amplitudes of the DAC 4, DAC 5, and DAC 6 outputs. A 4.12 kΩ resistor must be connected from $R_{SET2}$ to AGND. |

| Pin No. | Mnemonic | Input/ Output | Description |
|---|---|---|---|
| 45, 35 | COMP1, COMP2 | O | Compensation Pins. Connect a 2.2 nF capacitor from both COMP pins to $V_{AA}$. |
| 44, 43, 42 | DAC 1, DAC 2, DAC 3 | O | DAC Outputs. Full- and low-drive capable DACs. |
| 39, 38, 37 | DAC 4, DAC 5, DAC 6 | O | DAC Outputs. Low-drive only capable DACs. |
| 21 | SCL | I | $I^2C$ Clock Input. |
| 20 | SDA | I/O | $I^2C$ Data Input/Output. |
| 19 | ALSB | I | This signal sets up the LSB[2] of the MPU $I^2C$ address (see the Power Supply Sequencing section for more information). |
| 46 | $V_{REF}$ | | Optional External Voltage Reference Input for DACs or Voltage Reference Output. |
| 41 | $V_{AA}$ | P | Analog Power Supply (3.3 V). |
| 10, 56 | $V_{DD}$ | P | Digital Power Supply (1.8 V). For dual-supply configurations, $V_{DD}$ can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering. |
| 1 | $V_{DD\_IO}$ | P | Input/Output Digital Power Supply (1.8 V or 3.3 V). |
| 34 | $PV_{DD}$ | P | PLL Power Supply (1.8 V). For dual-supply configurations, $PV_{DD}$ can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering. |
| 33 | EXT_LF1 | I | External Loop Filter for On-Chip PLL 1. |
| 31 | EXT_LF2 | I | External Loop Filter for On-Chip PLL 2. |
| 32 | PGND | G | PLL Ground Pin. |
| 40 | AGND | G | Analog Ground Pin. |
| 11, 57 | DGND | G | Digital Ground Pin. |
| 64 | GND_IO | G | Input/Output Supply Ground Pin. |

[1] ED = enhanced definition = 525p and 625p.
[2] LSB = least significant bit. In the ADV7340, setting the LSB to 0 sets the $I^2C$ address to 0xD4. Setting it to 1 sets the $I^2C$ address to 0xD6. In the ADV7341, setting the LSB to 0 sets the $I^2C$ address to 0x54. Setting it to 1 sets the $I^2C$ address to 0x56.

# TYPICAL PERFORMANCE CHARACTERISTICS

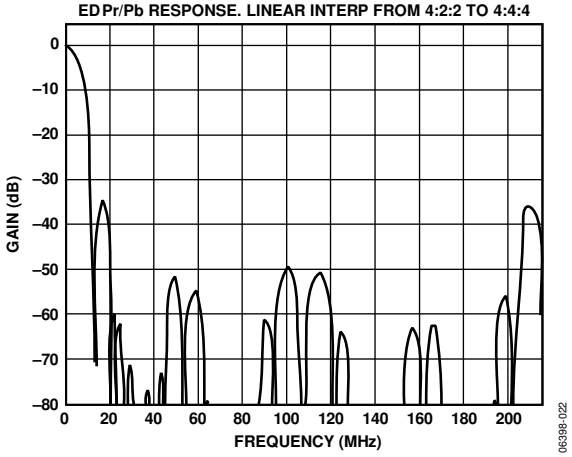



Figure 21. ED 8× Oversampling, PrPb Filter (Linear) Response

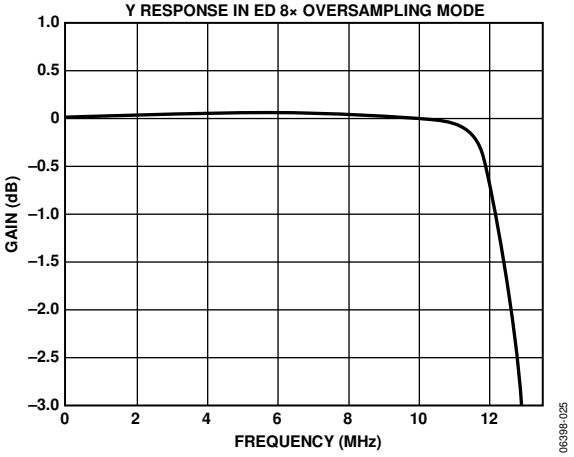



Figure 24. ED 8× Oversampling, Y Filter Response (Focus on Pass Band)

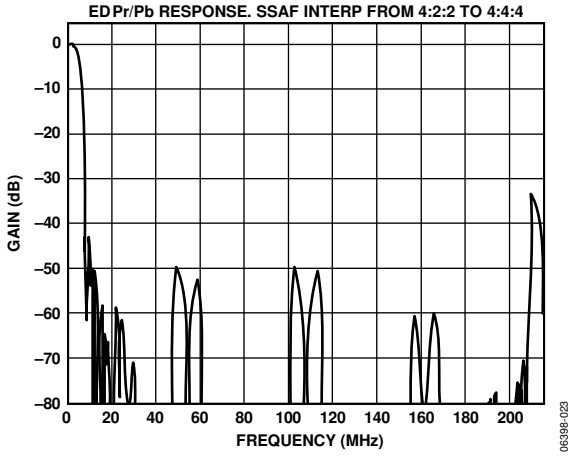



Figure 22. ED 8× Oversampling, PrPb Filter (SSAF™) Response

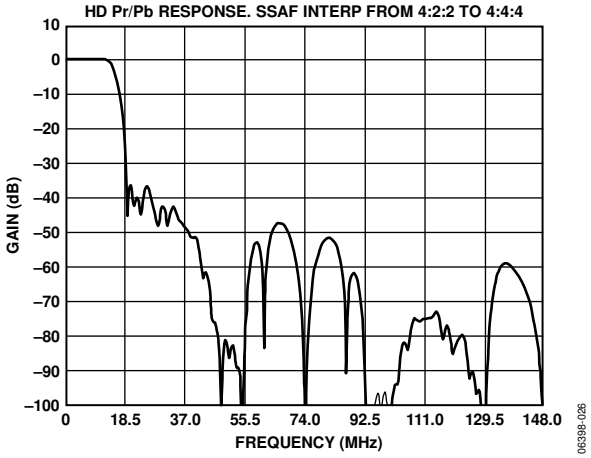



Figure 25. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:2:2 Input)

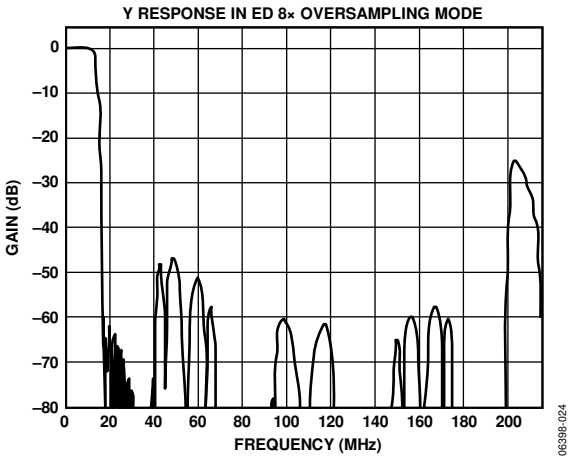



Figure 23. ED 8× Oversampling, Y Filter Response

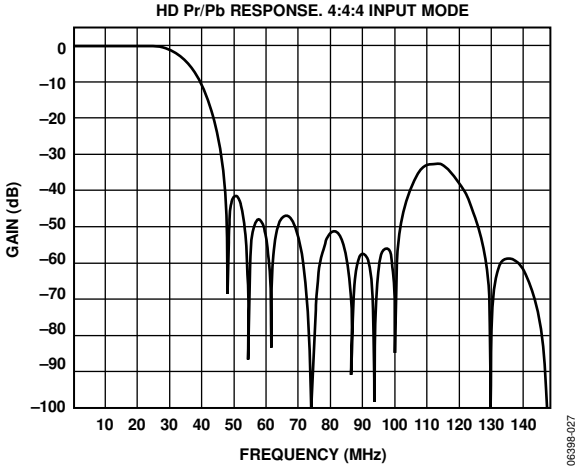



Figure 26. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:4:4 Input)

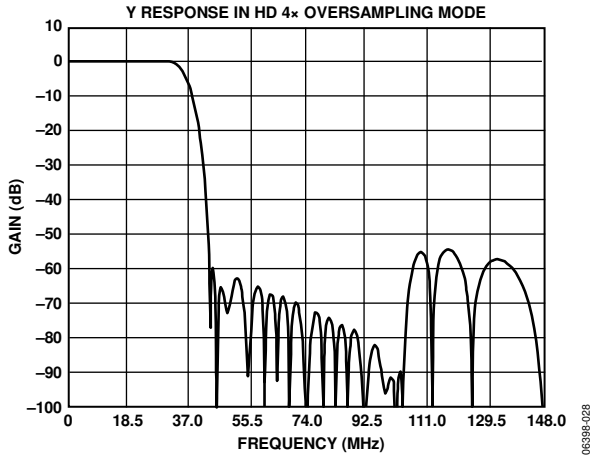



Figure 27. HD 4× Oversampling, Y Filter Response

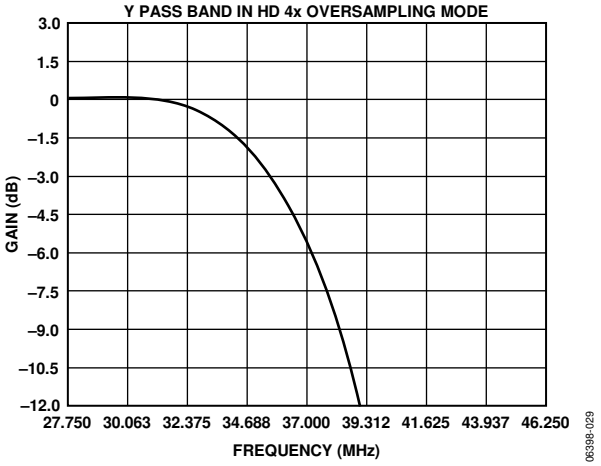



Figure 28. HD 4× Oversampling, Y Filter Response (Focus on Pass Band)

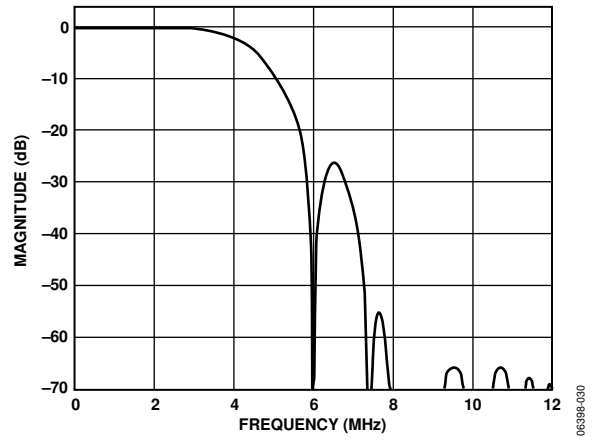



Figure 29. SD NTSC, Luma Low-Pass Filter Response

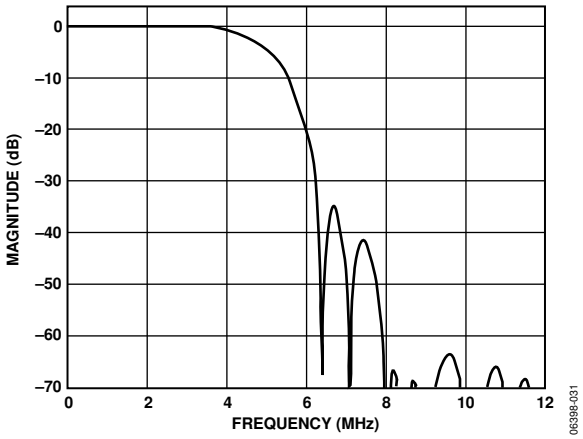



Figure 30. SD PAL, Luma Low-Pass Filter Response

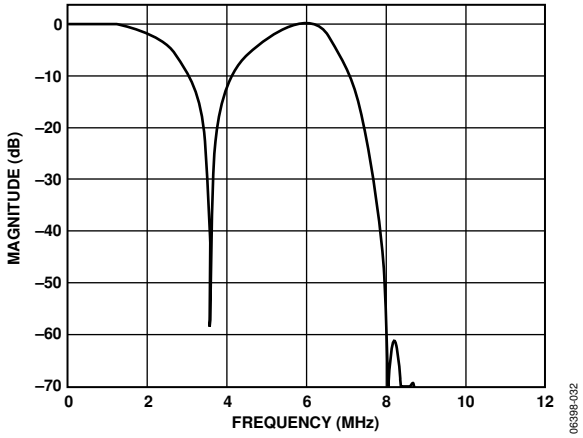



Figure 31. SD NTSC, Luma Notch Filter Response

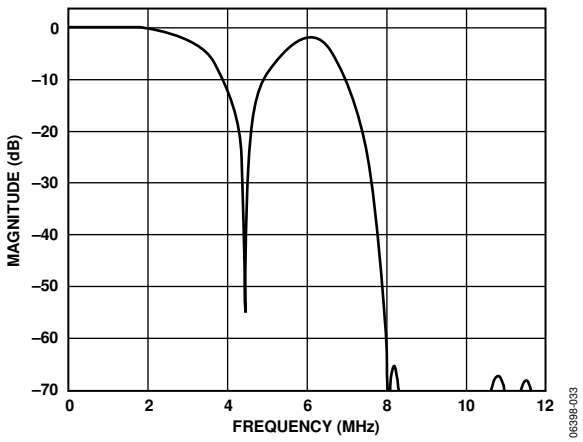



Figure 32. SD PAL, Luma Notch Filter Response