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Low Power, Chip Scale, 10-Bit SD/HD Video Encoder

Data Sheet

ADV7390/ADV7391/ADV7392/ADV7393

FEATURES

- 3 high quality, 10-bit video DACs
  - 16× (216 MHz) DAC oversampling for SD
  - 8× (216 MHz) DAC oversampling for ED
  - 4× (297 MHz) DAC oversampling for HD
  - 37 mA maximum DAC output current
- Multiformat video input support
  - 4:2:2 YCrCb (SD, ED, and HD)
  - 4:4:4 RGB (SD)
- Multiformat video output support
  - Composite (CVBS) and S-Video (Y-C)
  - Component YPrPb (SD, ED, and HD)
  - Component RGB (SD, ED, and HD)
- Lead frame chip scale package (LFCSP) options
  - 32-lead, 5 mm × 5 mm LFCSP
  - 40-lead, 6 mm × 6 mm LFCSP
- Wafer level chip scale package (WLCSP) option
  - 30-ball, 5 × 6 WLCSP with single DAC output
- Advanced power management
  - Patented content-dependent low power DAC operation
  - Automatic cable detection and DAC power-down
  - Individual DAC on/off control
  - Sleep mode with minimal power consumption
- 74.25 MHz 8-/10-/16-bit high definition input support
  - Compliant with SMPTE 274M (1080i), 296M (720p), and 240M (1035i)
- EIA/CEA-861B compliance support
- NTSC M, PAL B/D/G/H/I/M/N, PAL 60 support
- NTSC and PAL square pixel operation (24.54 MHz/29.5 MHz)
- Macrovision Rev 7.1.L1 (SD) and Rev 1.2 (ED) compliant
- Copy generation management system (CGMS)
- Closed captioning and wide screen signaling (WSS)
- Integrated subcarrier locking to external video source
- Complete on-chip video timing generator
- On-chip test pattern generation
- Programmable features
  - Luma and chroma filter responses
  - Vertical blanking interval (VBI)
  - Subcarrier frequency (f_{SC}) and phase
  - Luma delay
- High definition (HD) programmable features (720p/1080i/1035i)
  - 4× oversampling (297 MHz)
  - Internal test pattern generator
    - Color and black bar, hatch, flat field/frame
  - Fully programmable YCrCb to RGB matrix
  - Gamma correction
  - Programmable adaptive filter control
  - Programmable sharpness filter control
  - CGMS (720p/1080i) and CGMS Type B (720p/1080i)
  - Dual data rate (DDR) input support
- Enhanced definition (ED) programmable features (525p/625p)
  - 8× oversampling (216 MHz output)
  - Internal test pattern generator
    - Black bar, hatch, flat field/frame
  - Individual Y and PrPb output delay
  - Gamma correction
  - Programmable adaptive filter control
  - Fully programmable YCrCb to RGB matrix
  - Undershoot limiter
  - Macrovision Rev 1.2 (525p/625p) (ADV7390/ADV7392 only)
  - CGMS (525p/625p) and CGMS Type B (525p)
  - Dual data rate (DDR) input support
- Standard definition (SD) programmable features
  - 16× oversampling (216 MHz)
  - Internal test pattern generator
    - Color and black bar
  - Controlled edge rates for start and end of active video
  - Individual Y and PrPb output delay
  - Undershoot limiter
  - Gamma correction
  - Digital noise reduction (DNR)
  - Multiple chroma and luma filters
  - Luma-SSAF filter with programmable gain/attenuation
  - PrPb SSAF
  - Separate pedestal control on component and composite/S-Video output
  - VCR FF/RW sync mode
  - Macrovision Rev 7.1.L1 (ADV7390/ADV7392 only)
  - Copy generation management system (CGMS)
  - Wide screen signaling (WSS)
  - Closed captioning
- Serial MPU interface with I²C compatibility
- 2.7 V or 3.3 V analog operation
- 1.8 V digital operation
- 1.8 V or 3.3 V I/O operation
- Temperature range: −40°C to +85°C
- W Grade automotive range: −40°C to +105°C
- Qualified for automotive applications

Rev. I
Document Feedback

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10/06—Revision 0: Initial Version

APPLICATIONS

Mobile handsets
Digital still cameras
Portable media and DVD players
Portable game consoles
Digital camcorders
Set-top box (STB)
Automotive infotainment (ADV7392 and ADV7393 only)

GENERAL DESCRIPTION

The ADV7390/ADV7391/ADV7392/ADV7393 are a family of high speed, digital-to-analog video encoders on single monolithic chips. Three 2.7 V/3.3 V, 10-bit video DACs (a single DAC for the WLCSP package) provide support for composite (CVBS), S-Video (Y-C), or component (YPrPb/RGB) analog outputs in either standard definition (SD) or high definition (HD) video formats. The single DAC WLCSP package supports CVBS (NTSC and PAL) output only in SD resolution (see Table 2).

Optimized for low power operation, occupying a minimal footprint, and requiring few external components, these encoders are ideally suited to portable and power-sensitive applications requiring TV-out functionality. Cable detection and DAC autopower-down features ensure that power consumption is kept to a minimum.

The ADV7390/ADV7391 have an 8-bit video input port that supports SD video formats over an SDR interface and HD video formats over a DDR interface. The ADV7392/ADV7393 have a 16-bit video input port that can be configured in a variety of ways. SD RGB input is supported.

All members of the family support embedded EAV/SAV timing codes, external video synchronization signals, and the I²C® and communication protocol. Table 1 and Table 2 list the video standards directly supported by the ADV7390/ADV7391/ADV7392/ADV7393 family.

Table 1. Standards Directly Supported by the LFCSP Packages

Active Resolution	I/P[1]	Frame Rate (Hz)	Clock Input (MHz)	Standard
720 × 240	P	59.94	27	
720 × 288	P	50	27	
720 × 480	I	29.97	27	ITU-R BT.601/656
720 × 576	I	25	27	ITU-R BT.601/656
640 × 480	I	29.97	24.54	NTSC Square Pixel
768 × 576	I	25	29.5	PAL Square Pixel
720 × 483	P	59.94	27	SMPTE 293M
720 × 483	P	59.94	27	BTA T-1004
720 × 483	P	59.94	27	ITU-R BT.1358
720 × 576	P	50	27	ITU-R BT.1358
720 × 483	P	59.94	27	ITU-R BT.1362
720 × 576	P	50	27	ITU-R BT.1362
1920 × 1035	I	30	74.25	SMPTE 240M
1920 × 1035	I	29.97	74.1758	SMPTE 240M
1280 × 720	P	60, 50, 30, 25, 24	74.25	SMPTE 296M
1280 × 720	P	23.97, 59.94, 29.97	74.1758	SMPTE 296M
1920 × 1080	I	30, 25	74.25	SMPTE 274M
1920 × 1080	I	29.97	74.1758	SMPTE 274M
1920 × 1080	P	30, 25, 24	74.25	SMPTE 274M
1920 × 1080	P	23.98, 29.97	74.1758	SMPTE 274M
1920 × 1080	P	24	74.25	ITU-R BT.709-5

[1] I = interlaced, P = progressive.

Table 2. Standards Directly Supported by the WLCSP Package

Active Resolution	I/P[1]	Frame Rate (Hz)	Clock Input (MHz)	Standard
720 × 480	I	29.97	27	ITU-R BT.601/656
720 × 576	I	25	27	ITU-R BT.601/656
640 × 480	I	29.97	24.54	NTSC Square Pixel
768 × 576	I	25	29.5	PAL Square Pixel

[1] I = interlaced, P = progressive.

FUNCTIONAL BLOCK DIAGRAMS

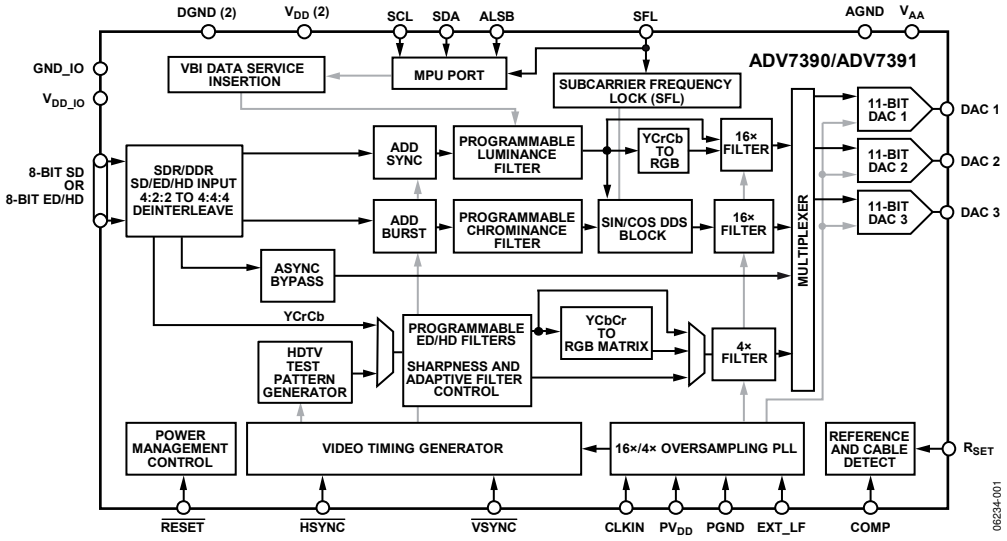


Figure 1. ADV7390/ADV7391 (32-Lead LFCSP)

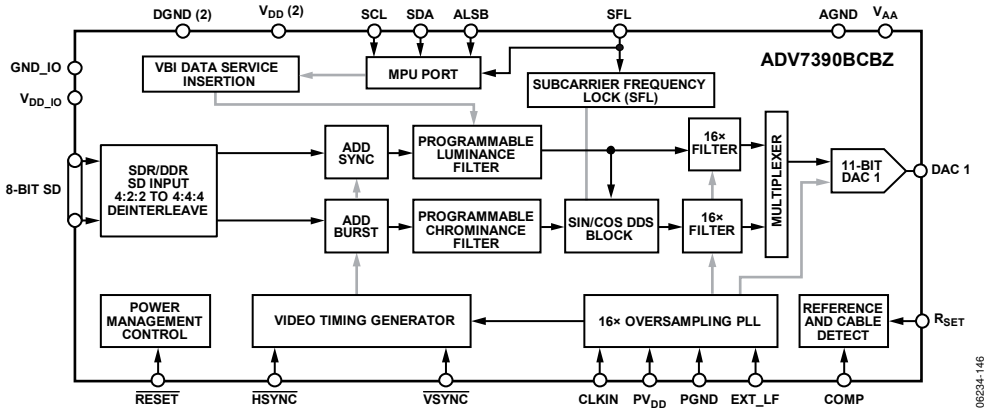


Figure 2. ADV7390BCBZ-A (30-Ball WLCSP)

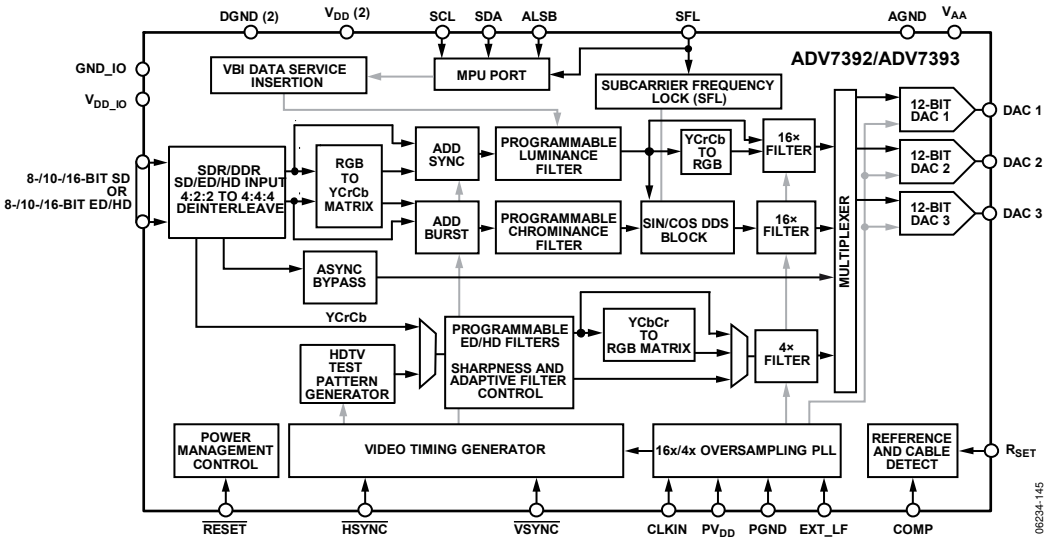


Figure 3. ADV7392/ADV7393 (40-Lead LFCSP)

SPECIFICATIONS

POWER SUPPLY SPECIFICATIONS

All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGES				
V_{DD}	1.71	1.8	1.89	V
V_{DD_IO}	1.71	3.3	3.63	V
PV_{DD}	1.71	1.8	1.89	V
V_{AA}	2.6	3.3	3.465	V
POWER SUPPLY REJECTION RATIO		0.002		%/%

INPUT CLOCK SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 1.71 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 4.

Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CLKIN}	SD/ED		27		MHz
	ED (at 54 MHz)		54		MHz
	HD		74.25		MHz
CLKIN High Time, t_9		40			% of one clock cycle
CLKIN Low Time, t_{10}		40			% of one clock cycle
CLKIN Peak-to-Peak Jitter Tolerance			2		±ns

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition.

ANALOG OUTPUT SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 1.71 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
Full-Drive Output Current	R_{SET} = 510 Ω, R_L = 37.5 Ω	33	34.6	37	mA
	All DACs enabled				
	R_{SET} = 510 Ω, R_L = 37.5 Ω	31.5	33.5	37	mA
	DAC 1 enabled only[1]				
Low-Drive Output Current	R_{SET} = 4.12 kΩ, R_L = 300 Ω		4.3		mA
DAC-to-DAC Matching	DAC 1, DAC 2, DAC 3		2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Capacitance, C_{OUT}			10		pF
Analog Output Delay[2]			6		ns
DAC Analog Output Skew	DAC 1, DAC 2, DAC 3		1		ns

[1] The recommended method of bringing this value back to the ideal value is by adjusting Register 0x0B to the recommended value of 0x12.
[2] Output delay measured from the 50% point of the rising edge of the input clock to the 50% point of the DAC output full-scale transition.

DIGITAL INPUT/OUTPUT SPECIFICATIONS—3.3 V

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 2.97 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
Input Leakage Current, I_{IN}	$V_{IN} = V_{DD\_IO}$			±10	µA
Input Capacitance, C_{IN}			4		pF
Output High Voltage, V_{OH}	I_{SOURCE} = 400 µA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current	V_{IN} = 0.4 V, 2.4 V			±1	µA
Three-State Output Capacitance			4		pF

DIGITAL INPUT/OUTPUT SPECIFICATIONS—1.8 V

When V_{DD_IO} is set to 1.8 V, all the digital video inputs and control inputs, such as I^2C, HS, and VS, should use 1.8 V levels.
V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 1.71 V to 1.89 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 7.

Parameter	Conditions	Min	Typ	Max	Unit
Input High Voltage, V_{IH}		0.7 V_{DD_IO}			V
Input Low Voltage, V_{IL}				0.3 V_{DD_IO}	V
Input Capacitance, C_{IN}			4		pF
Output High Voltage, V_{OH}	I_{SOURCE} = 400 µA	V_{DD_IO} − 0.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Output Capacitance			4		pF

MPU PORT TIMING SPECIFICATIONS

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 1.71 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 8.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT, I^2C MODE[1]	See Figure 17				
SCL Frequency		0		400	kHz
SCL High Pulse Width, t_1		0.6			µs
SCL Low Pulse Width, t_2		1.3			µs
Hold Time (Start Condition), t_3		0.6			µs
Setup Time (Start Condition), t_4		0.6			µs
Data Setup Time, t_5		100			ns
SDA, SCL Rise Time, t_6				300	ns
SDA, SCL Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs

[1] Guaranteed by characterization.

DIGITAL TIMING SPECIFICATIONS—3.3 V

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 2.97 V to 3.63 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 9.

Parameter	Conditions[1]	Min	Typ	Max	Unit
VIDEO DATA AND VIDEO CONTROL PORT[2, 3]					
Data Input Setup Time, t_{11}[4]	SD	2.1			ns
	ED/HD-SDR	2.3			ns
	ED/HD-DDR	2.3			ns
	ED (at 54 MHz)	1.7			ns
Data Input Hold Time, t_{12}[4]	SD	1.0			ns
	ED/HD-SDR	1.1			ns
	ED/HD-DDR	1.1			ns
	ED (at 54 MHz)	1.0			ns
Control Input Setup Time, t_{11}[4]	SD	2.1			ns
	ED/HD-SDR or ED/HD-DDR	2.3			ns
	ED (at 54 MHz)	1.7			ns
Control Input Hold Time, t_{12}[4]	SD	1.0			ns
	ED/HD-SDR or ED/HD-DDR	1.1			ns
	ED (at 54 MHz)	1.0			ns
Control Output Access Time, t_{13}[4]	SD			12	ns
	ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz)			10	ns
Control Output Hold Time, t_{14}[4]	SD	4.0			ns
	ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz)	3.5			ns
PIPELINE DELAY[5]					
SD[1]					
CVBS/Y-C Outputs (2×)	SD oversampling disabled		68		Clock cycles
CVBS/Y-C Outputs (8×)	SD oversampling enabled		79		Clock cycles
CVBS/Y-C Outputs (16×)	SD oversampling enabled		67		Clock cycles
Component Outputs (2×)	SD oversampling disabled		78		Clock cycles
Component Outputs (8×)	SD oversampling enabled		69		Clock cycles
Component Outputs (16×)	SD oversampling enabled		84		Clock cycles
ED[1]					
Component Outputs (1×)	ED oversampling disabled		41		Clock cycles
Component Outputs (4×)	ED oversampling enabled		49		Clock cycles
Component Outputs (8×)	ED oversampling enabled		46		Clock cycles
HD[1]					
Component Outputs (1×)	HD oversampling disabled		40		Clock cycles
Component Outputs (2×)	HD oversampling enabled		42		Clock cycles
Component Outputs (4×)	HD oversampling enabled		44		Clock cycles
$\overline{\text{RESET}}$ CONTROL					
$\overline{\text{RESET}}$ Low Time		100			ns

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: P[15:0] for ADV7392/ADV7393 or P[7:0] for ADV7390/ADV7391.
[3] Video control: $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$.
[4] Guaranteed by characterization.
[5] Guaranteed by design.

DIGITAL TIMING SPECIFICATIONS—1.8 V

V_{DD} = 1.71 V to 1.89 V, PV_{DD} = 1.71 V to 1.89 V, V_{AA} = 2.6 V to 3.465 V, V_{DD_IO} = 1.71 V to 1.89 V.
All specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 10.

Parameter	Conditions[1]	Min	Typ	Max	Unit
VIDEO DATA AND VIDEO CONTROL PORT[2, 3]					
Data Input Setup Time, t_{11}[4]	SD	1.4			ns
	ED/HD-SDR	1.9			ns
	ED/HD-DDR	1.9			ns
	ED (at 54 MHz)	1.6			ns
Data Input Hold Time, t_{12}[4]	SD	1.4			ns
	ED/HD-SDR	1.5			ns
	ED/HD-DDR	1.5			ns
	ED (at 54 MHz)	1.3			ns
Control Input Setup Time, t_{11}[4]	SD	1.4			ns
	ED/HD-SDR or ED/HD-DDR	1.2			ns
	ED (at 54 MHz)	1.0			ns
Control Input Hold Time, t_{12}[4]	SD	1.4			ns
	ED/HD-SDR or ED/HD-DDR	1.0			ns
	ED (at 54 MHz)	1.0			ns
Control Output Access Time, t_{13}[4]	SD			13	ns
	ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz)			12	ns
Control Output Hold Time, t_{14}[4]	SD	4.0			ns
	ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz)	5.0			ns
PIPELINE DELAY[5]					
SD[1]					
CVBS/Y-C Outputs (2×)	SD oversampling disabled		68		Clock cycles
CVBS/Y-C Outputs (8×)	SD oversampling enabled		79		Clock cycles
CVBS/Y-C Outputs (16×)	SD oversampling enabled		67		Clock cycles
Component Outputs (2×)	SD oversampling disabled		78		Clock cycles
Component Outputs (8×)	SD oversampling enabled		69		Clock cycles
Component Outputs (16×)	SD oversampling enabled		84		Clock cycles
ED[1]					
Component Outputs (1×)	ED oversampling disabled		41		Clock cycles
Component Outputs (4×)	ED oversampling enabled		49		Clock cycles
Component Outputs (8×)	ED oversampling enabled		46		Clock cycles
HD[1]					
Component Outputs (1×)	HD oversampling disabled		40		Clock cycles
Component Outputs (2×)	HD oversampling enabled		42		Clock cycles
Component Outputs (4×)	HD oversampling enabled		44		Clock cycles
$\overline{\text{RESET}}$ CONTROL					
$\overline{\text{RESET}}$ Low Time		100			ns

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: P[15:0] for ADV7392/ADV7393 or P[7:0] for ADV7390/ADV7391.
[3] Video control: $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$.
[4] Guaranteed by characterization.
[5] Guaranteed by design.

VIDEO PERFORMANCE SPECIFICATIONS

V_{DD} = 1.8 V, PV_{DD} = 1.8 V, V_{AA} = 3.3 V, V_{DD_IO} = 3.3 V, T_A = +25°C.

Table 11.

Parameter	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution			10		Bits
Integral Nonlinearity (INL)[1]	R_{SET} = 510 Ω, R_L = 37.5 Ω		0.5		LSBs
Differential Nonlinearity (DNL)[1, 2]	R_{SET} = 510 Ω, R_L = 37.5 Ω		0.5		LSBs
STANDARD DEFINTION (SD) MODE					
Luminance Nonlinearity			0.5		±%
Differential Gain	NTSC		0.5		%
Differential Phase	NTSC		0.6		Degrees
Signal-to-Noise Ratio (SNR)[3]	Luma ramp		58		dB
	Flat field full bandwidth		75		dB
ENHANCED DEFINITION (ED) MODE					
Luma Bandwidth			12.5		MHz
Chroma Bandwidth			5.8		MHz
HIGH DEFINITION (HD) MODE					
Luma Bandwidth			30.0		MHz
Chroma Bandwidth			13.75		MHz

[1] Measured on DAC 1, DAC 2, and DAC 3.
[2] Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For −ve DNL, the actual step value lies below the ideal step value.
[3] Measured on the ADV7392/ADV7393 operating in 10-bit input mode.

POWER SPECIFICATIONS

V_{DD} = 1.8 V, PV_{DD} = 1.8 V, V_{AA} = 3.3 V, V_{DD_IO} = 3.3 V, T_A = +25°C.

Table 12.

Parameter	Conditions	Min	Typ	Max	Unit
NORMAL POWER MODE[1, 2]					
I_{DD}[3]	SD (16× oversampling enabled), CVBS (only one DAC turned on)		33		mA
	SD (16× oversampling enabled), YPrPb (three DACs turned on)		68		mA
	ED (8× oversampling enabled)[4]		59		mA
	HD (4× oversampling enabled)[4]		81	101	mA
I_{DD_IO}			1	10	mA
I_{AA}[5]	One DAC enabled		50		mA
	All DACs enabled		122	151	mA
I_{PLL}			4	10	mA
SLEEP MODE					
I_{DD}			5		µA
I_{AA}			0.3		µA
I_{DD_IO}			0.2		µA
I_{PLL}			0.1		µA

[1] R_{SET} = 510 Ω (all DACs operating in full-drive mode).
[2] 75% color bar test pattern applied to pixel data pins.
[3] I_{DD} is the continuous current required to drive the digital core.
[4] Applicable to both single data rate (SDR) and dual data rate (DDR) input modes.
[5] I_{AA} is the total current required to supply all DACs.

TIMING DIAGRAMS

The following abbreviations are used in Figure 4 to Figure 11:

- t_9 = clock high time
- t_{10} = clock low time
- t_{11} = data setup time
- t_{12} = data hold time
- t_{13} = control output access time
- t_{14} = control output hold time

In addition, see Table 35 for the ADV7390/ADV7391 pixel port input configuration and Table 36 for the ADV7392/ADV7393 pixel port input configuration.

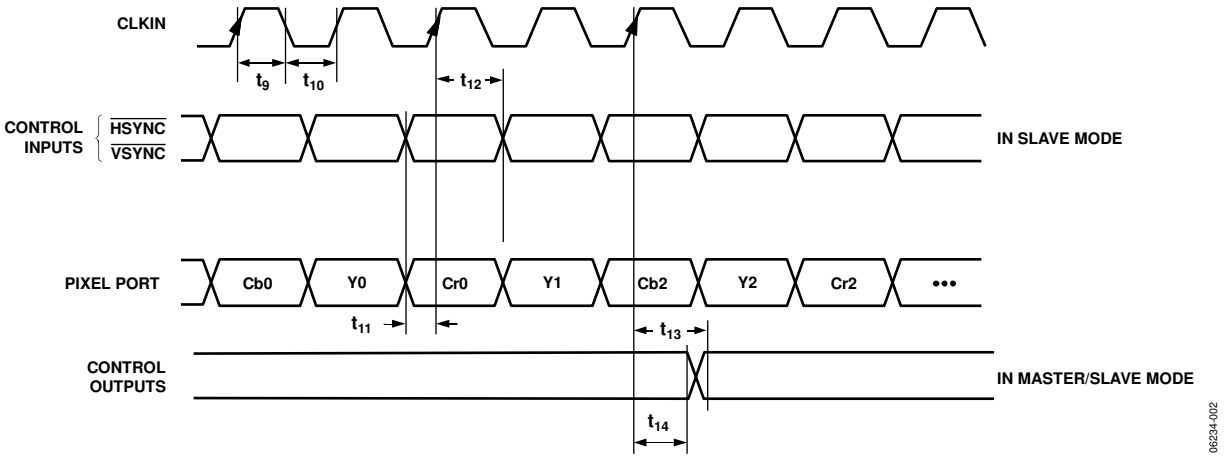


Figure 4. SD Input, 8-/10-Bit 4:2:2 YCrCb, Input Mode 000

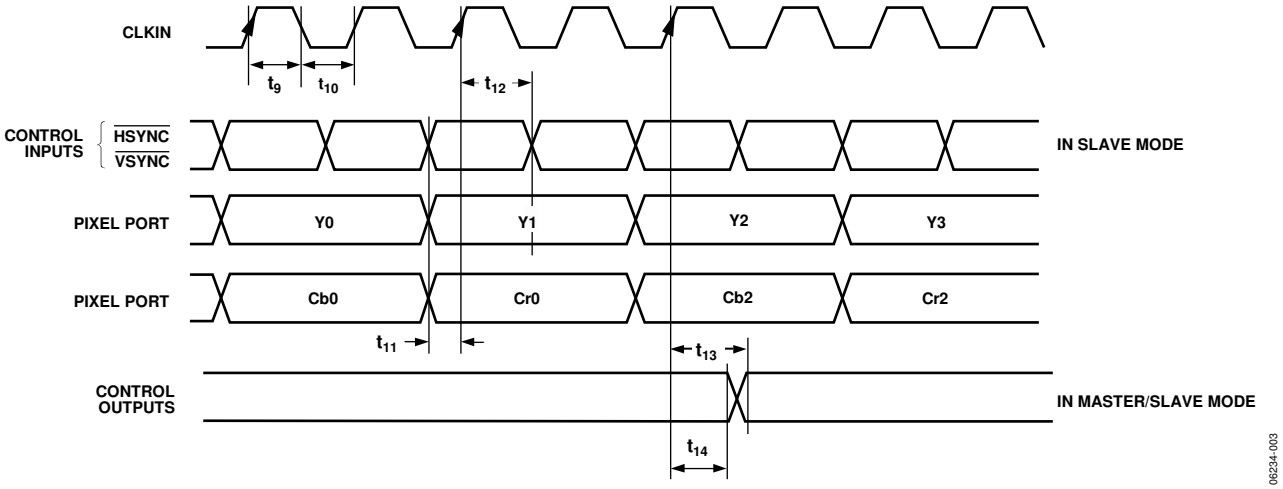


Figure 5. SD Input, 16-Bit 4:2:2 YCrCb, Input Mode 000

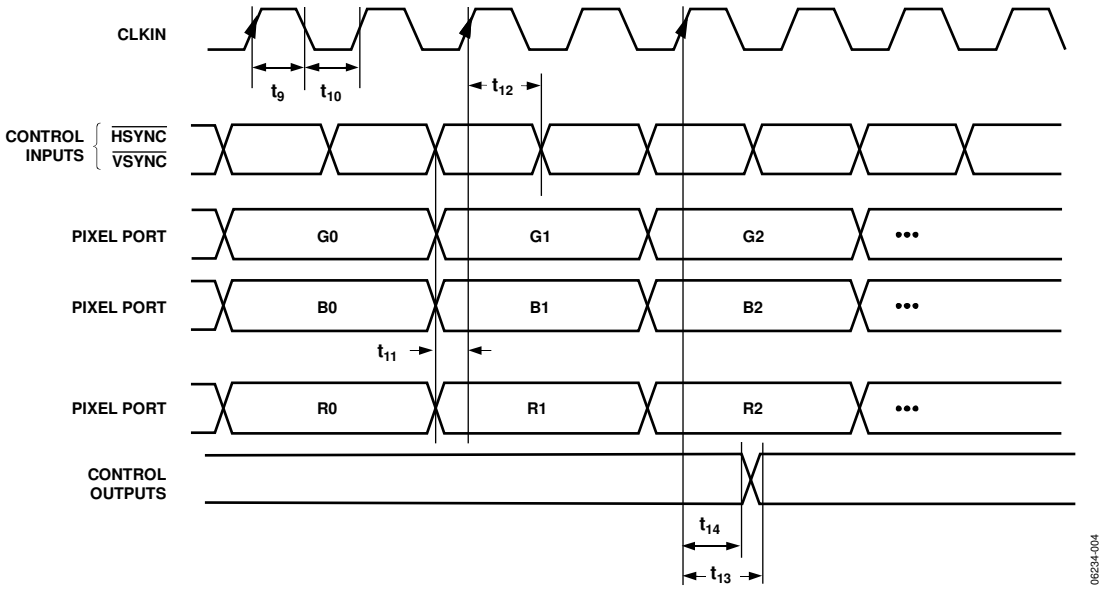


Figure 6. SD Input, 16-Bit 4:4:4 RGB, Input Mode 000

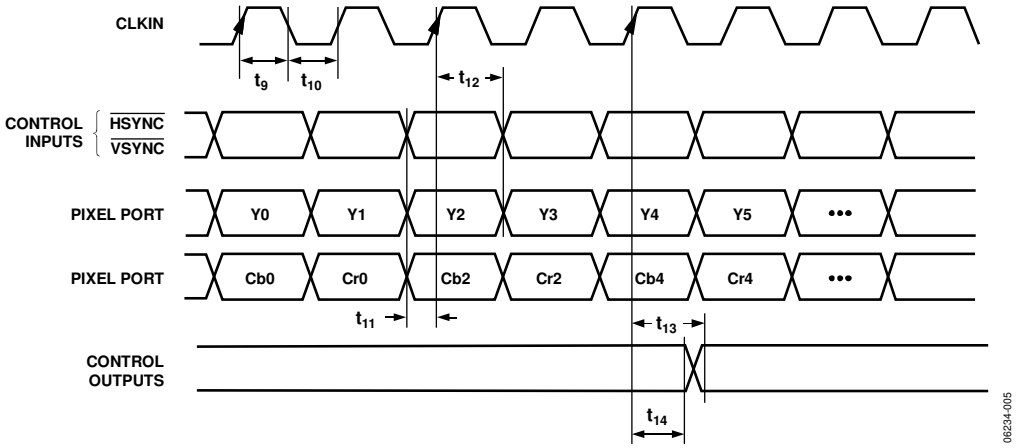


Figure 7. ED/HD-SDR Input, 16-Bit 4:2:2 YCrCb, Input Mode 001

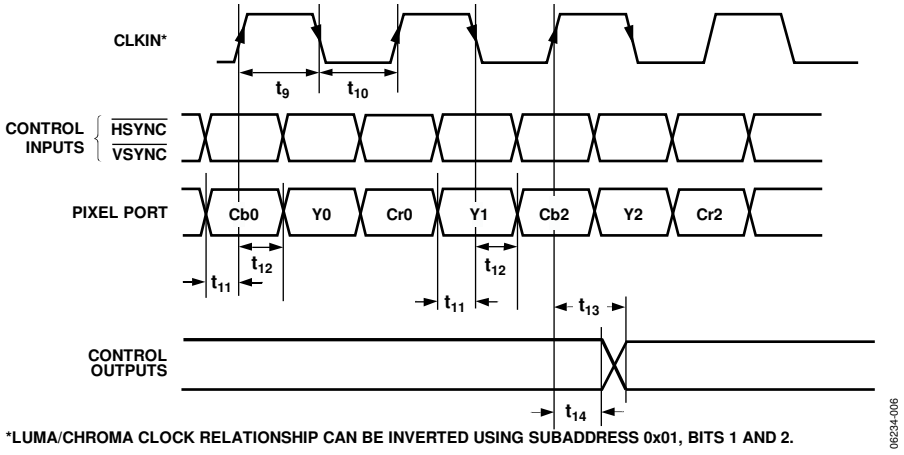


Figure 8. ED/HD-DDR Input, 8-/10-Bit 4:2:2 YCrCb ($\overline{HSYNC}$/$\overline{VSYNC}$), Input Mode 010

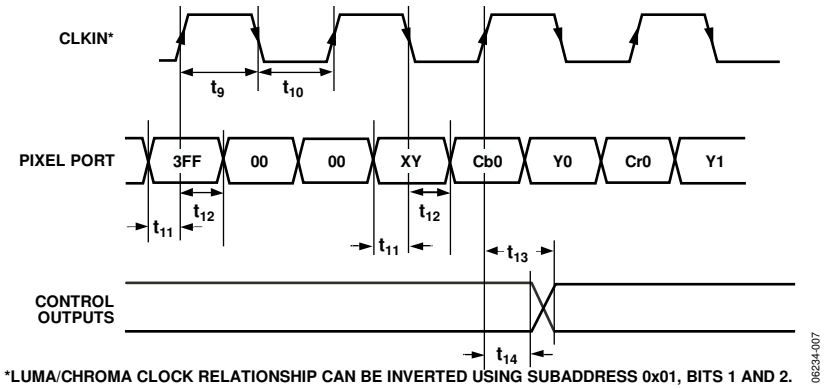


Figure 9. ED/HD-DDR Input, 8-/10-Bit 4:2:2 YCrCb (EAV/SAV), Input Mode 010

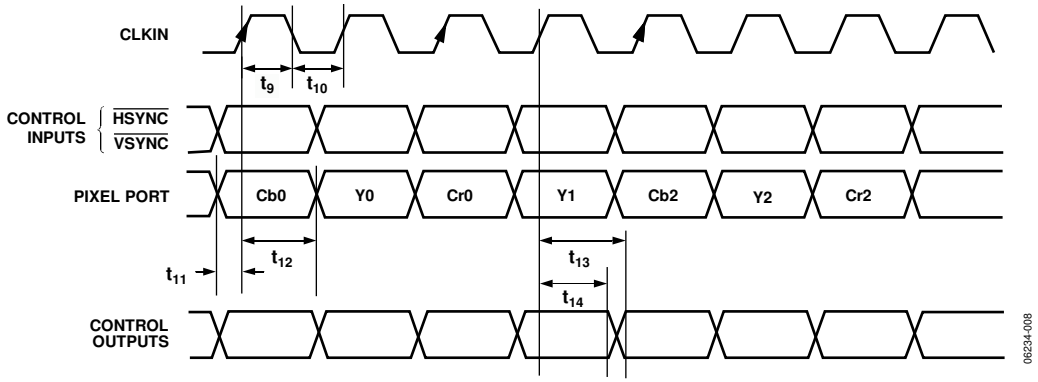


Figure 10. ED (at 54 MHz) Input, 8-/10-Bit 4:2:2 YCrCb (HSYNC/VSYNC), Input Mode 111

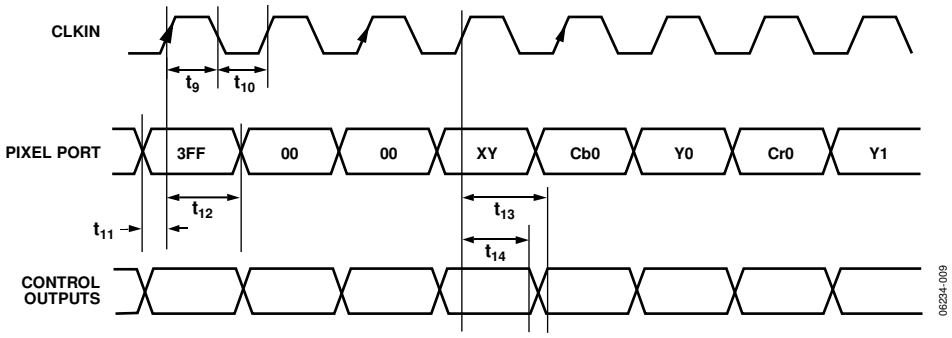
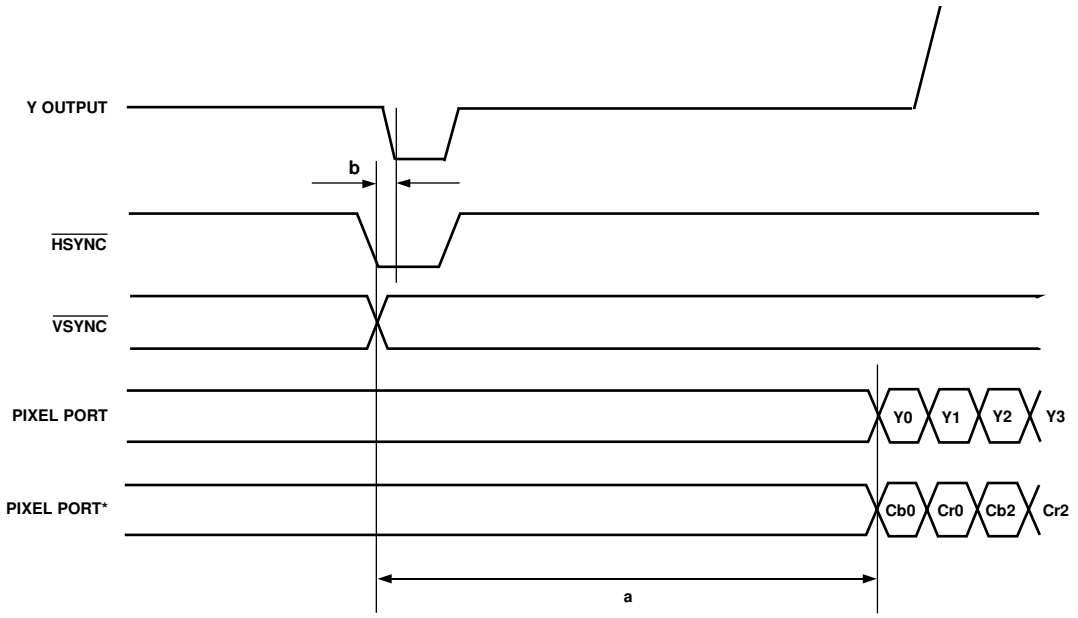


Figure 11. ED (at 54 MHz) Input, 8-/10-Bit 4:2:2 YCrCb (EAV/SAV), Input Mode 111



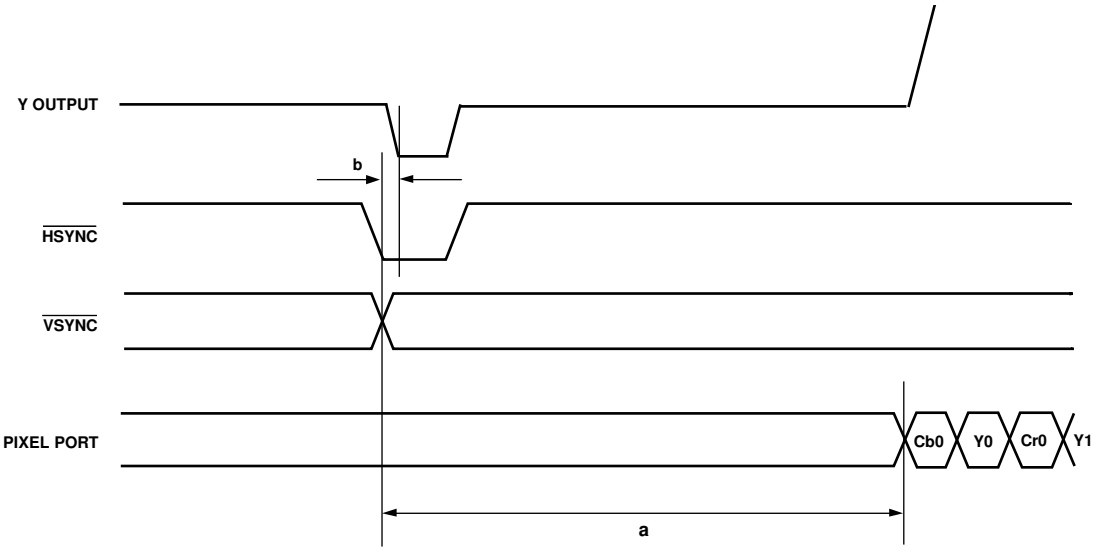
a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-010

Figure 12. ED-SDR, 16-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



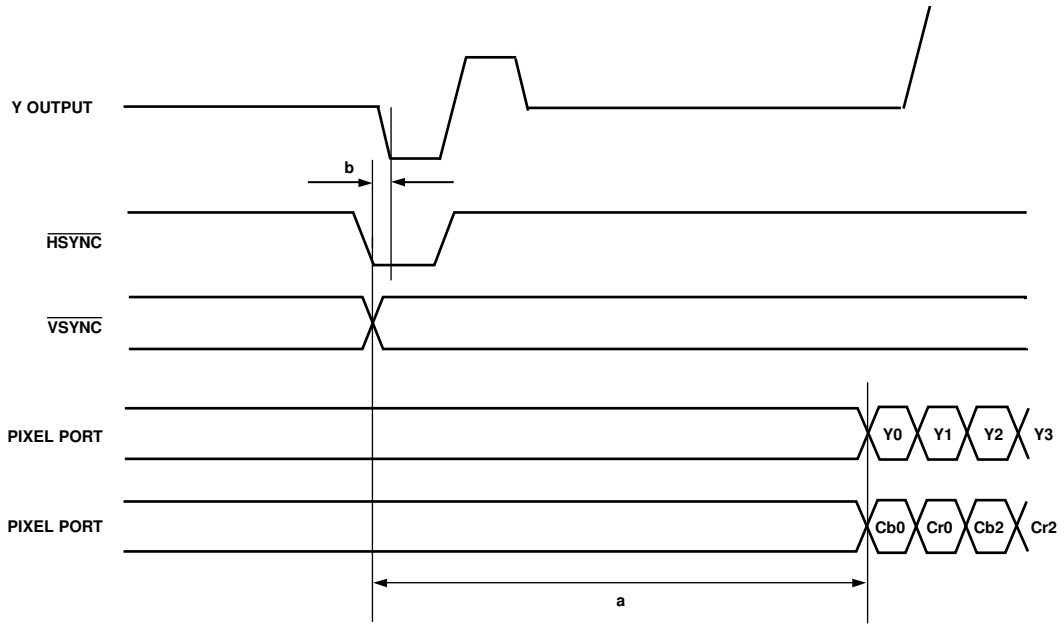
a(MIN) = 244 CLOCK CYCLES FOR 525p.
a(MIN) = 264 CLOCK CYCLES FOR 625p.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-011

Figure 13. ED-DDR, 8-/10-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



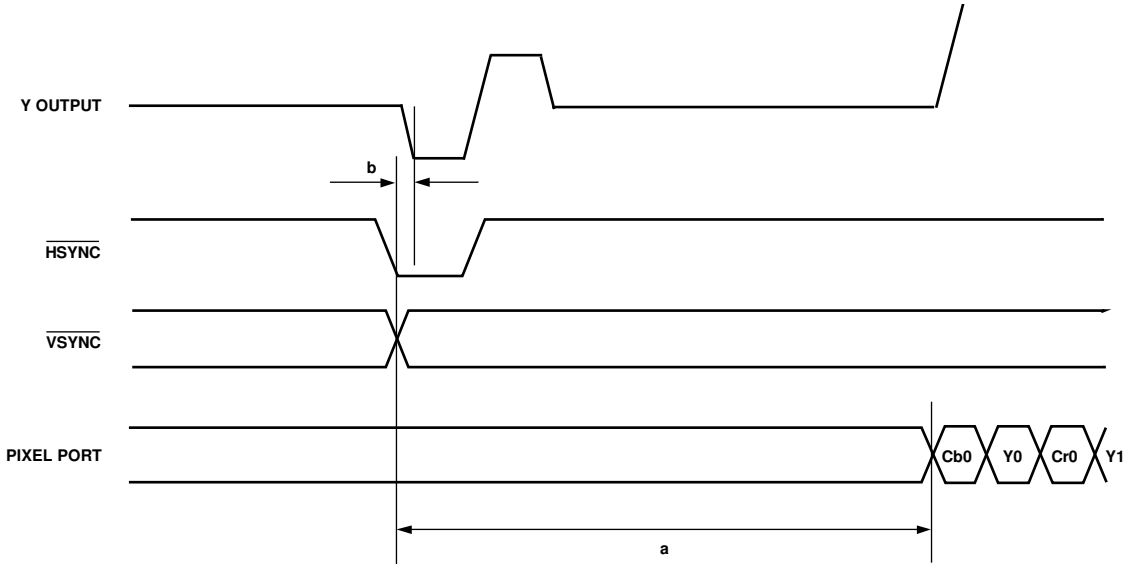
a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-012

Figure 14. HD-SDR, 16-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram



a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-013

Figure 15. HD-DDR, 8-/10-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram

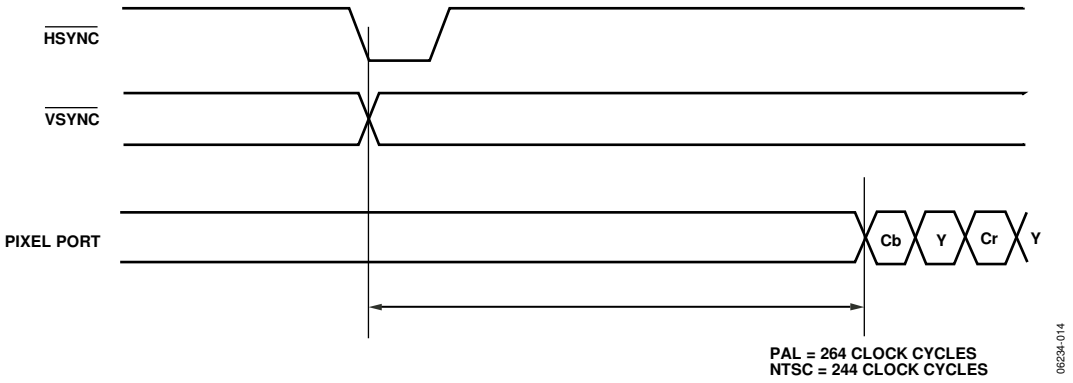


Figure 16. SD Input Timing Diagram (Timing Mode 1)

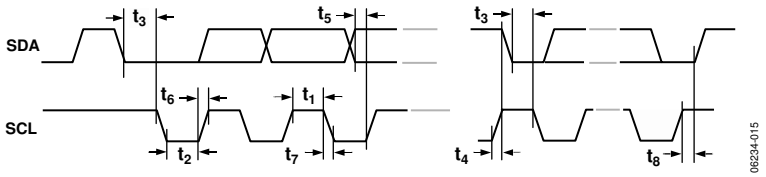


Figure 17. MPU Port Timing Diagram (I^2C Mode)

ABSOLUTE MAXIMUM RATINGS

Table 13.

Parameter[1]	Rating
V_{AA} to AGND	−0.3 V to +3.9 V
V_{DD} to DGND	−0.3 V to +2.3 V
PV_{DD} to PGND	−0.3 V to +2.3 V
V_{DD_IO} to GND_IO	−0.3 V to +3.9 V
AGND to DGND	−0.3 V to +0.3 V
AGND to PGND	−0.3 V to +0.3 V
AGND to GND_IO	−0.3 V to +0.3 V
DGND to PGND	−0.3 V to +0.3 V
DGND to GND_IO	−0.3 V to +0.3 V
PGND to GND_IO	−0.3 V to +0.3 V
Digital Input Voltage to GND_IO	−0.3 V to V_{DD_IO} + 0.3 V
Analog Outputs to AGND	−0.3 V to V_{AA}
Max CLKIN Input Frequency	80 MHz
Storage Temperature Range (t_S)	−60°C to +150°C
Junction Temperature (t_J)	150°C
Lead Temperature (Soldering, 10 sec)	260°C

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 14. Thermal Resistance[1]

Package Type	θ_{JA}[2]	$\theta_{JC\text{-}TOP}$[3]	$\theta_{JC\text{-}BOTTOM}$[4]	Unit
30-Ball WLCSP	35	1	N/A	°C/W
32-Lead LFCSP	27	32	1.2	°C/W
40-Lead LFCSP	26	32	1	°C/W

[1] Values are based on a JEDEC 4-layer test board.
[2] With the exposed metal paddle on the underside of the LFCSP soldered to the PCB ground.
[3] This is the thermal resistance of the junction to the top of the package.
[4] This is the thermal resistance of the junction to the bottom of the package.

The ADV7390/ADV7391/ADV7392/ADV7393 are RoHS-compliant, Pb-free products. The lead finish is 100% pure Sn electroplate. The device is suitable for Pb-free applications up to 255°C (±5°C) IR reflow (JEDEC STD-20).

The ADV7390/ADV7391/ADV7392/ADV7393 are backward compatible with conventional SnPb soldering processes. The electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

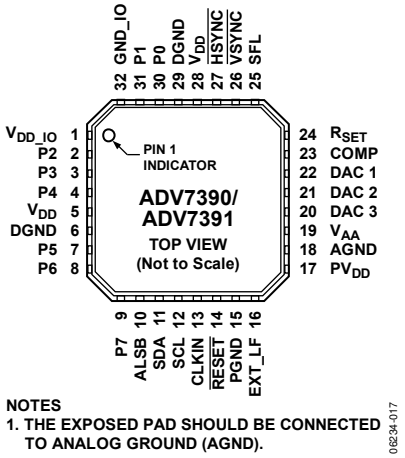


Figure 18. ADV7390/ADV7391 Pin Configuration

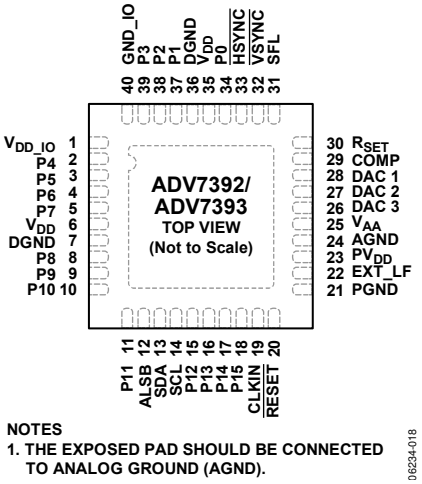


Figure 19. ADV7392/ADV7393 Pin Configuration

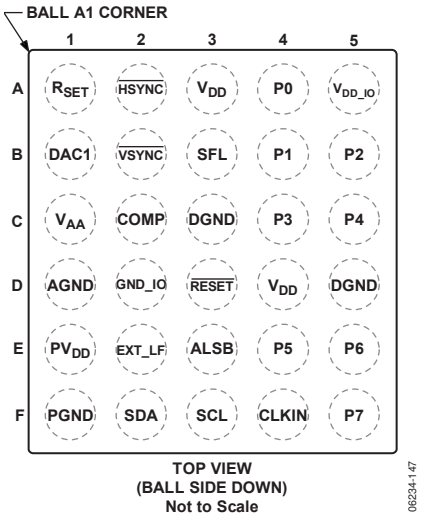


Figure 20. ADV7390BCBZ-A Pin Configuration

Table 15. Pin Function Descriptions

Pin No.[1]					
ADV7390/ ADV7391	ADV7392/ ADV7393	ADV7390 WLCSP	Mnemonic	Input/ Output	Description
9 to 7, 4 to 2, 31, 30	N/A	F5, E5, E4, C5, C4, B5, B4, A4	P7 to P0	I	8-Bit Pixel Port (P7 to P0). P0 is the LSB. See Table 35 for input modes (ADV7390/ADV7391).
N/A	18 to 15, 11 to 8, 5 to 2, 39 to 37, 34	N/A	P15 to P0	I	16-Bit Pixel Port (P15 to P0). P0 is the LSB. See Table 36 for input modes (ADV7392/ADV7393).
13	19	F4	CLKIN	I	Pixel Clock Input for HD (74.25 MHz), ED[2] (27 MHz or 54 MHz), or SD (27 MHz).
27	33	A2	$\overline{\text{HSYNC}}$	I/O	Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
26	32	B2	$\overline{\text{VSYNC}}$	I/O	Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
25	31	B3	SFL	I/O	Subcarrier Frequency Lock (SFL) Input.

Pin No.[1]			Mnemonic	Input/ Output	Description
ADV7390/ ADV7391	ADV7392/ ADV7393	ADV7390 WLCSP			
24	30	A1	R_{SET}	I	Controls the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from R_{SET} to AGND. For low-drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from R_{SET} to AGND.
23	29	C2	COMP	O	Compensation Pin. Connect a 2.2 nF capacitor from COMP to V_{AA}.
N/A	N/A	B1	DAC 1	O	DAC Output. Full-drive and low-drive capable DAC
22, 21, 20	28, 27, 26	N/A	DAC 1, DAC 2, DAC 3	O	DAC Outputs. Full-drive and low-drive capable DACs.
12	14	F3	SCL	I	I^2C Clock Input.
11	13	F2	SDA	I/O	I^2C Data Input/Output.
10	12	E3	ALSB	I	ALSB sets up the LSB[3] of the MPU I^2C address.
14	20	D3	$\overline{\text{RESET}}$	I	Resets the on-chip timing generator and sets the ADV7390/ADV7391/ADV7392/ADV7393 into its default mode.
19	25	C1	V_{AA}	P	Analog Power Supply (2.7 V or 3.3 V).
5, 28	6, 35	A3, D4	V_{DD}	P	Digital Power Supply (1.8 V). For dual-supply configurations, V_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
1	1	A5	V_{DD_IO}	P	Input/Output Digital Power Supply (1.8 V or 3.3 V).
17	23	E1	PV_{DD}	P	PLL Power Supply (1.8 V). For dual-supply configurations, PV_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
16	22	E2	EXT_LF	I	External Loop Filter for the Internal PLL.
15	21	F1	PGND	G	PLL Ground Pin.
18	24	D1	AGND	G	Analog Ground Pin.
6, 29	7, 36	C3, D5	DGND	G	Digital Ground Pin.
32	40	D2	GND_IO	G	Input/Output Supply Ground Pin.
			EPAD	G	Exposed Pad. Connect to analog ground (AGND).

[1] N/A means not applicable.
[2] ED = enhanced definition = 525p and 625p.
[3] LSB = least significant bit. In the ADV7390/ADV7392, setting the LSB to 0 sets the I^2C address to 0xD4. Setting it to 1 sets the I^2C address to 0xD6. In the ADV7391/ADV7393, setting the LSB to 0 sets the I^2C address to 0x54. Setting it to 1 sets the I^2C address to 0x56.

TYPICAL PERFORMANCE CHARACTERISTICS

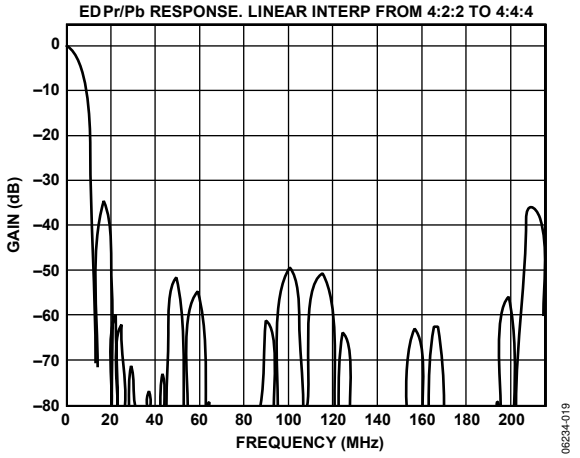


Figure 21. ED 8× Oversampling, PrPb Filter (Linear) Response

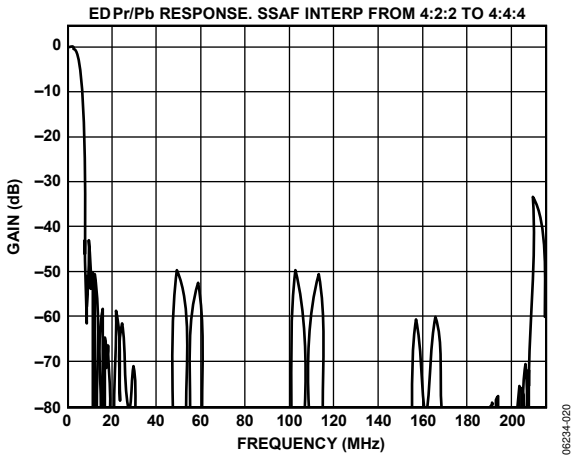


Figure 22. ED 8× Oversampling, PrPb Filter (SSAF™) Response

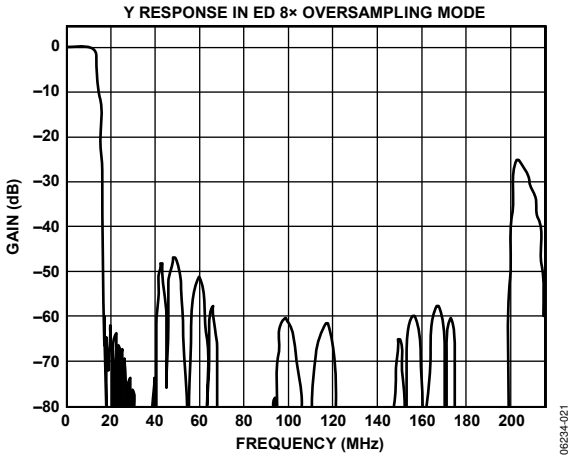


Figure 23. ED 8× Oversampling, Y Filter Response

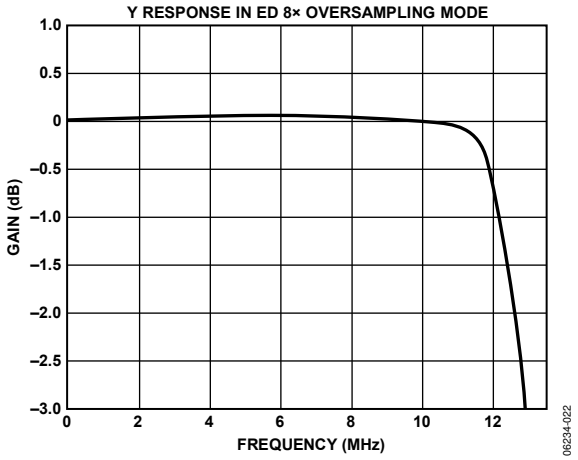


Figure 24. ED 8× Oversampling, Y Filter Response (Focus on Pass Band)

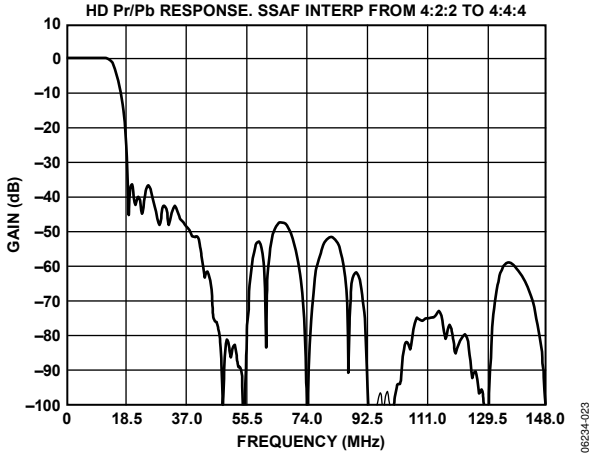


Figure 25. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:2:2 Input)

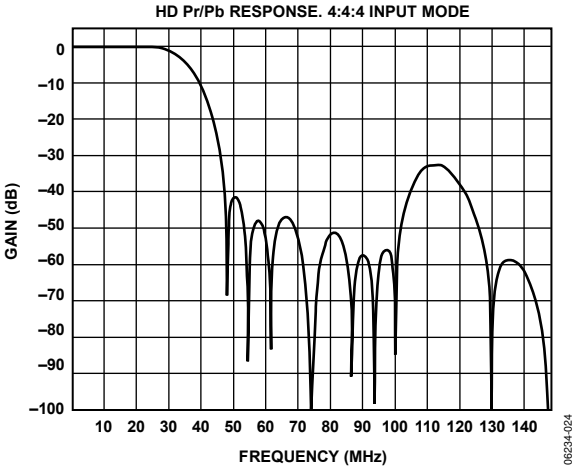


Figure 26. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:4:4 Input)

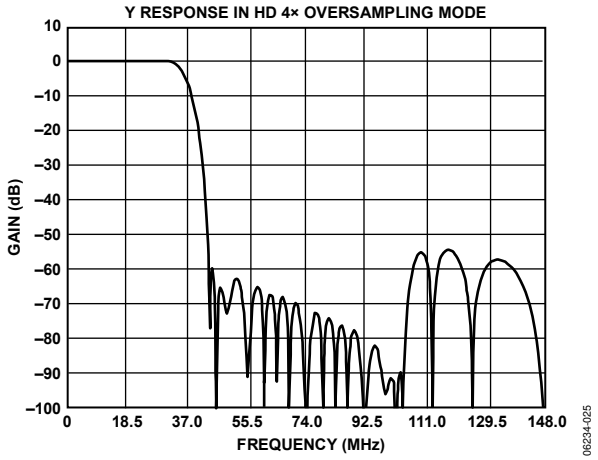


Figure 27. HD 4× Oversampling, Y Filter Response

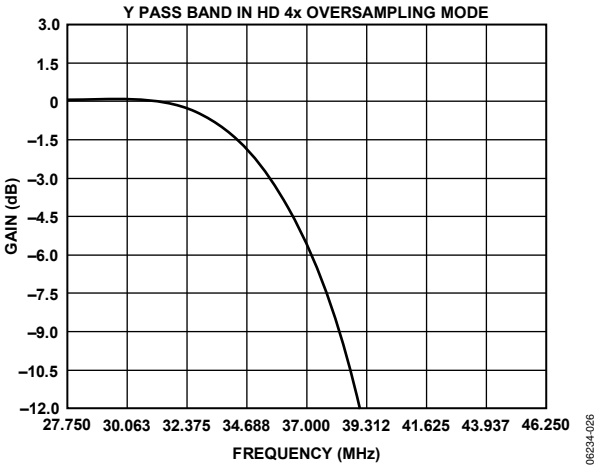


Figure 28. HD 4× Oversampling, Y Filter Response (Focus on Pass Band)

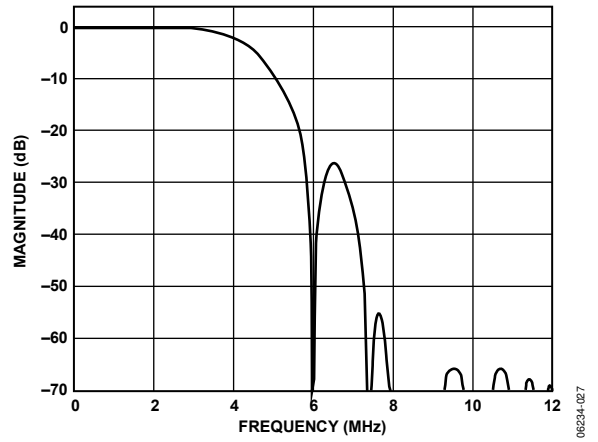


Figure 29. SD NTSC, Luma Low-Pass Filter Response

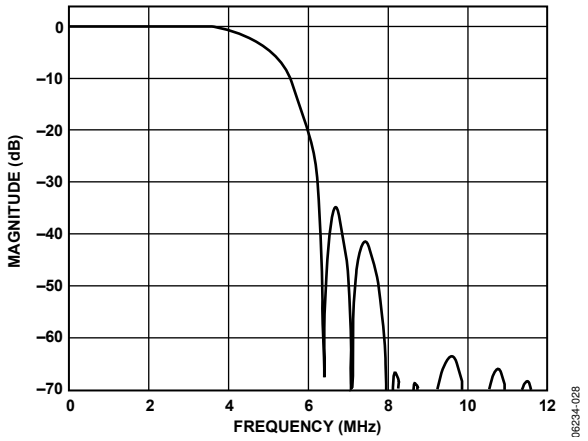


Figure 30. SD PAL, Luma Low-Pass Filter Response

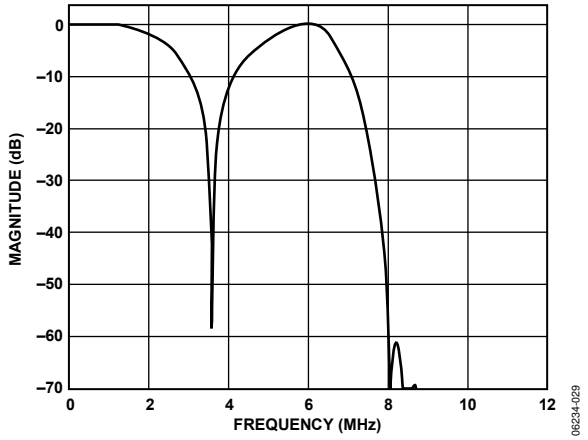


Figure 31. SD NTSC, Luma Notch Filter Response

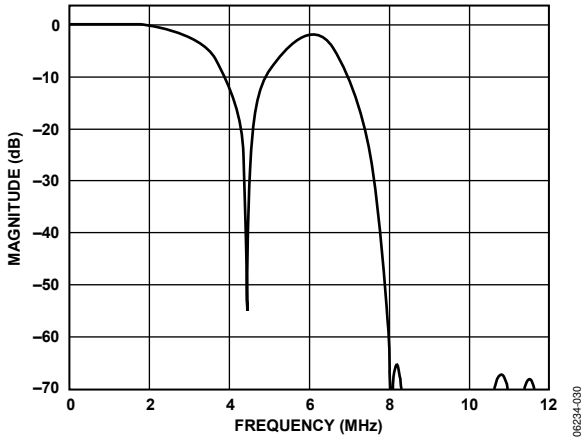


Figure 32. SD PAL, Luma Notch Filter Response

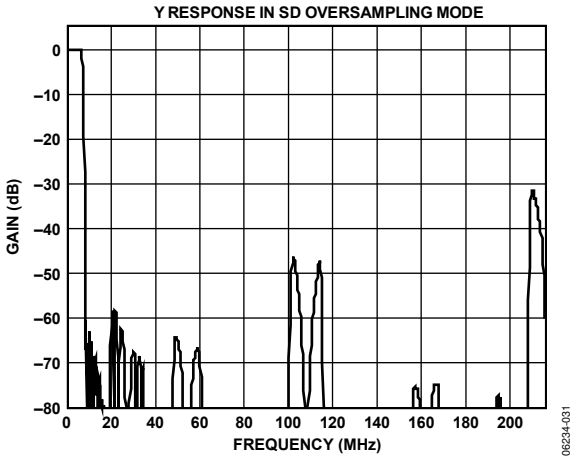


Figure 33. SD 16× Oversampling, Y Filter Response

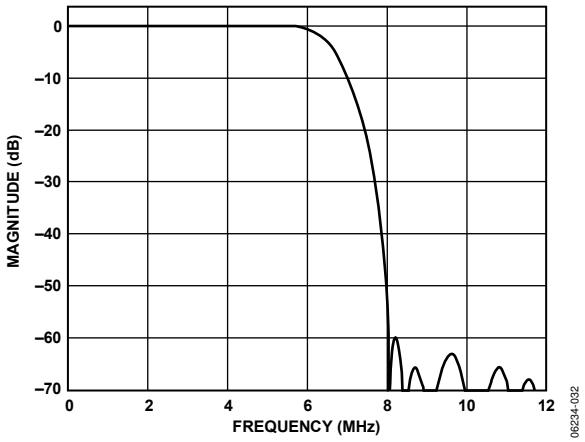


Figure 34. SD Luma SSAF Filter Response up to 12 MHz

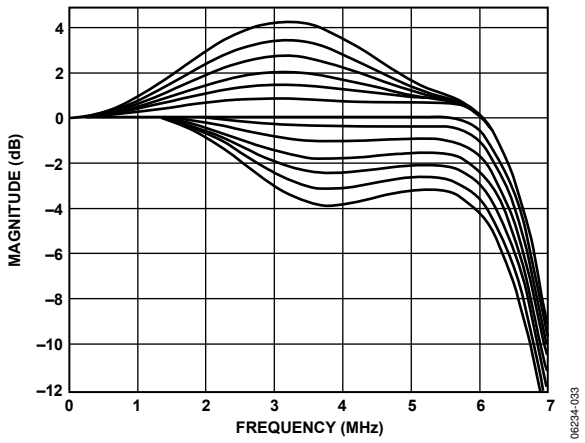


Figure 35. SD Luma SSAF Filter, Programmable Responses

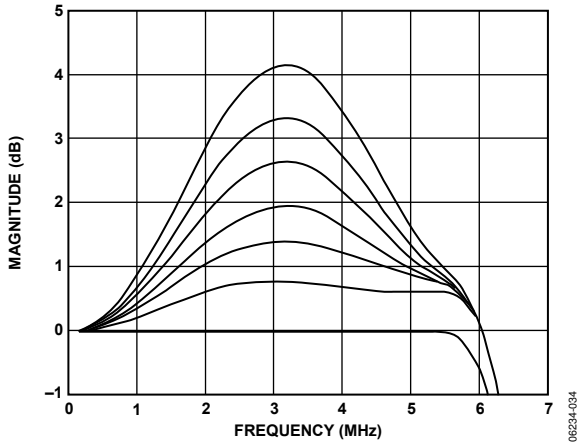


Figure 36. SD Luma SSAF Filter, Programmable Gain

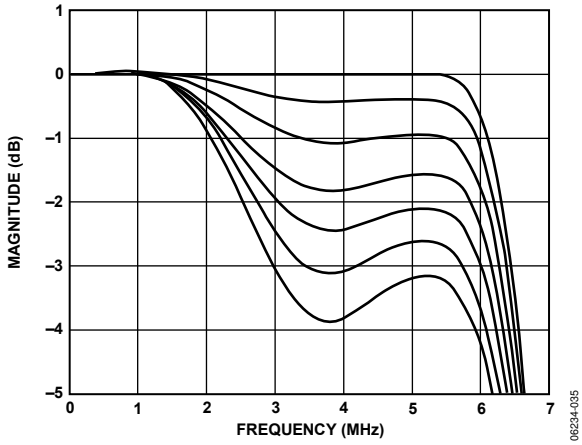


Figure 37. SD Luma SSAF Filter, Programmable Attenuation

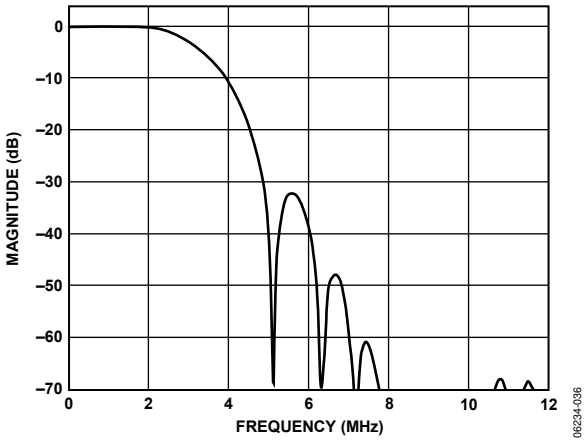


Figure 38. SD Luma CIF Low-Pass Filter Response

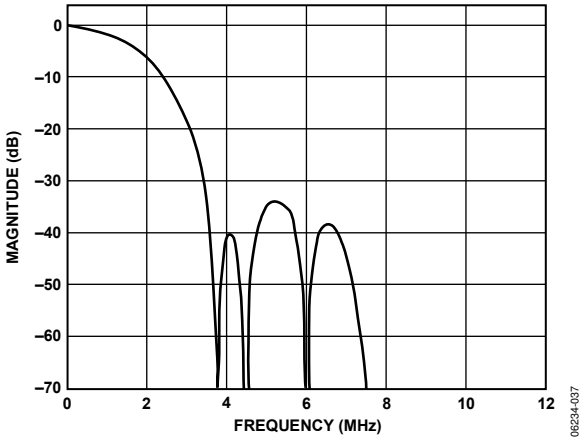


Figure 39. SD Luma QCIF Low-Pass Filter Response

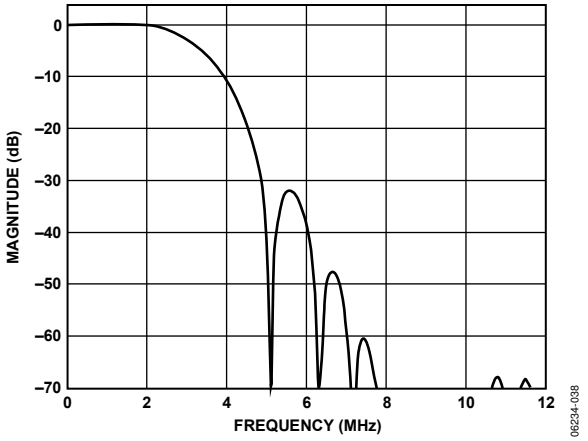


Figure 40. SD Chroma 3.0 MHz Low-Pass Filter Response

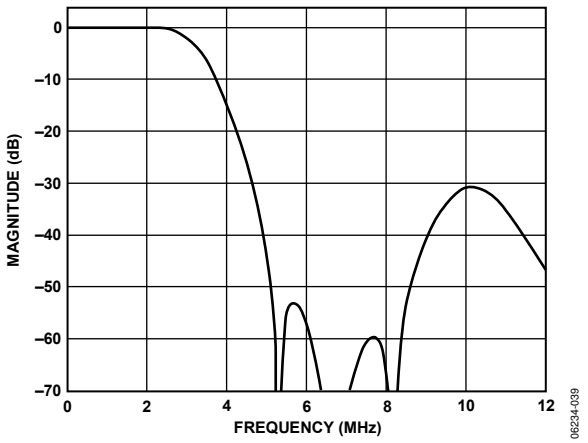


Figure 41. SD Chroma 2.0 MHz Low-Pass Filter Response

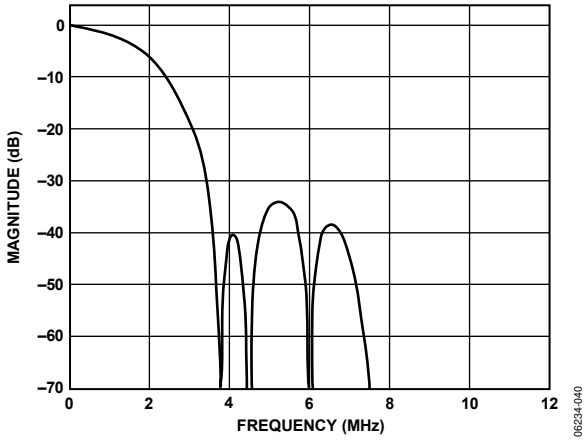


Figure 42. SD Chroma 1.3 MHz Low-Pass Filter Response

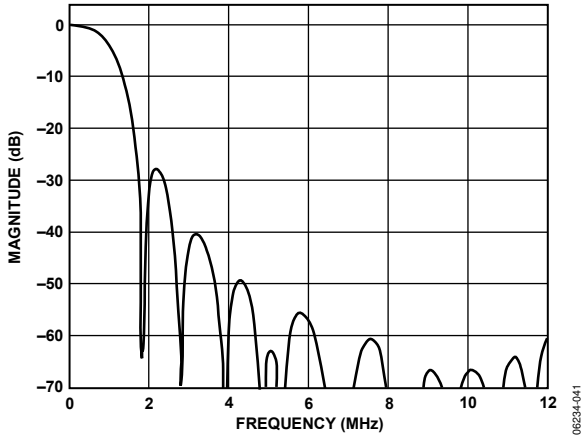


Figure 43. SD Chroma 1.0 MHz Low-Pass Filter Response

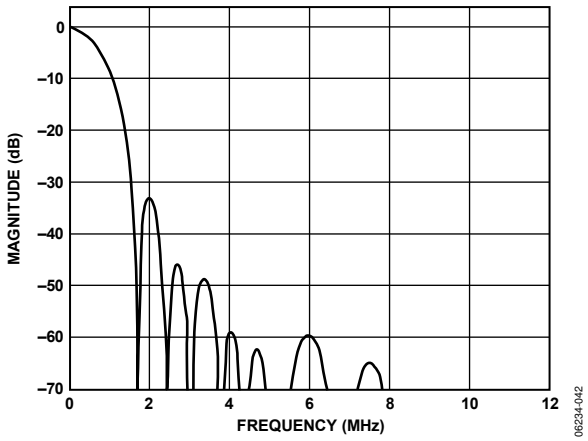


Figure 44. SD Chroma 0.65 MHz Low-Pass Filter Response

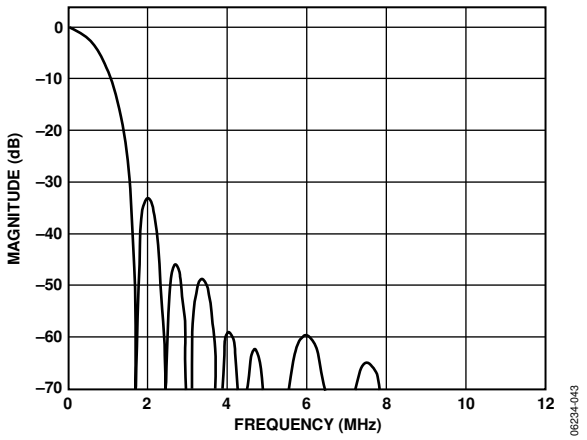


Figure 45. SD Chroma CIF Low-Pass Filter Response

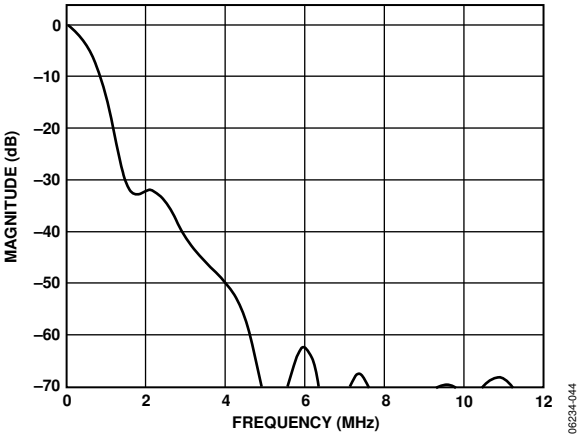


Figure 46. SD Chroma QCIF Low-Pass Filter Response