Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NatureVue Video Signal Processor with Bitmap OSD, Dual HDMI Tx, and Encoder

Data Sheet **ADV8005**

FEATURES

- Video signal processor
  - Full 12-bit, 4:4:4 YCbCr (color space) internal processing
  - Motion adaptive deinterlacing with ultralow angle interpolation
  - Multiple video processing paths with up to 3 simultaneous video streams including picture-in-picture (PiP) support
  - Upscaling and downscaling to/from 4k × 2k
  - Aspect ratio conversion/panorama scaling
  - Cadence detection for the recovery of original frames from film-based content
  - Dual video scalers enable simultaneous output of multiple different resolutions
  - Sharpness and detail enhancement
  - Noise reduction for random, mosquito, and block noise
  - Frame rate converter (FRC)
  - Video metrics readback to enable correct phase and frequency selection for graphics inputs
- On-screen display (OSD)
  - Internally generated bitmap-based OSD allowing overlay on one or more video outputs
  - Overlay on 3D and 4k × 2k video formats
  - Dedicated OSD scaler
  - Alpha blending of OSD data on video data
  - Disturbance free blending of OSD on either of 2 zones
  - Support for external OSD
  - Easy to use software tool for developing OSDs
- HDMI transmitters
  - Dual 4k × 2k HDMI transmitters
  - Audio return channel (ARC) support
  - Dual audio insertion from TMDS Rx or from audio input pins
  - Support for serial audio using the S/PDIF audio pin
  - 8-channel I^2S audio inputs supporting up to 192 kHz sample frequency
  - 6-channel direct stream digital (DSD) audio inputs
- Noise shaped video (NSV) 6-DAC video encoder
  - Six 12-bit NSV video DACs supporting SD, ED and HD video
  - Rovi Rev. 7.1.L1 (SD) and Rev. 1.4 (ED) compliant
- Professional video features
  - Capability to output up to 36-bit TTL pixel data
  - Full color space converter on the output TTL pixel data
  - TTL video, audio, SPI, and interrupt pins disabled by default
  - Ability to synchronize output video to externally applied reference sync signals

APPLICATIONS

- High end A/V receivers
- Upconverting DVD players/recorders
- Video conferencing and distribution
- HDMI splitters
- Video walls

FUNCTIONAL BLOCK DIAGRAM

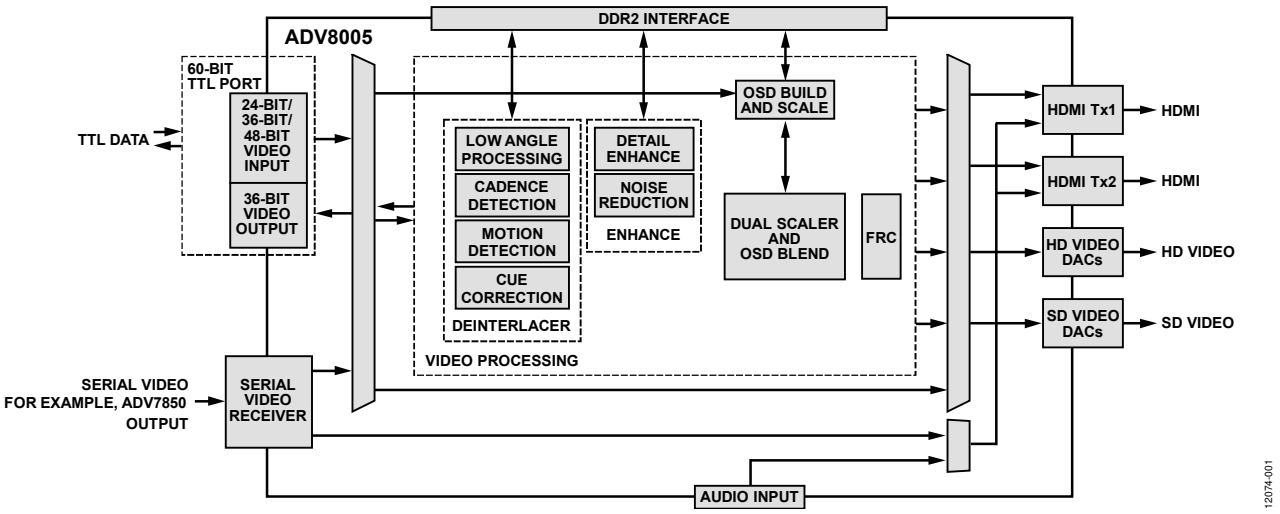

Figure 1.

Advantiv® Advanced Television Solutions by Analog Devices | NatureVue™ Video Upconversion and Enhancement by Analog Devices

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV8005 is a multiple input video signal processor that can deinterlace and scale standard definition (SD), enhanced definition (ED), or high definition (HD) video data to ultra HD formats; generate a bitmap on-screen display (OSD); and output the video with OSD overlaid on two High-Definition Multimedia Interface (HDMI®) transmitters and a video encoder.

The 60-bit TTL video port can be used to input video to the ADV8005 in a number of ways: using the 48-bit TTL pixel port, using the 24-bit external OSD TTL pixel port, or from a device with an HDMI transmitter such as the ADV7850. The ADV8005 supports many of the formats outlined in the CEA-861-F and VESA specifications, as well as several other widely used timing formats.

The ADV8005 features primary and secondary video scalers that enable simultaneous output of multiple different resolutions. The primary video scaler can upscale to 4k × 2k modes. The secondary video scaler can upscale to 1080p or UXGA graphics. 4k × 2k downscaling is performed using the secondary video scaler, leaving the primary video scaler available for other video processing.

The ADV8005 primary video scaler can perform high performance, motion adaptive interlaced to progressive conversion on SD and HD content. Additional functionality has also been added to ADV8005 to facilitate upscaling and downscaling to VESA formats with pixel clock frequencies below 300 MHz.

Detail enhancement and image enhancing techniques such as random, mosquito, and block noise reduction allow improved final image quality. The frame rate converter of the ADV8005 allows the conversion between common frame rates with support to output two different frame rates simultaneously under certain conditions.

The ADV8005 can accept OSD information from an external OSD source on one of its inputs, or it can internally generate a high quality, bitmap-based OSD. The internal OSD is highly flexible and allows the system designer to easily incorporate features like scrolling text and animation in various color depths up to 24-bit true color.

Analog Devices, Inc., provides an OSD development tool (Blimp) to assist in the design, debug, and emulation of the OSD prior to integration with the system application. When the design is complete, the OSD development tool automatically generates code to which system application programming interfaces (APIs) can be added before integration with the system application and an OSD design resource, which must be downloaded to an external SPI flash memory.

Video can be output from the ADV8005 using one or both of the HDMI transmitters and/or the six-DAC SD/HD video encoder. The six 12-bit NSV® video DACs allow composite (CVBS), S-Video (Y/C), and component (YPrPb) analog outputs in standard, enhanced, and high definition video formats. Oversampling of 216 MHz (SD and ED) and 297 MHz (HD) removes the requirement for external output filtering. Rovi® and non-Rovi variants of the ADV8005 are available.

Both of the HDMI transmitters on the ADV8005 support 4k × 2k and all mandatory and many optional 3D video resolutions. Each transmitter features an audio return channel receiver (ARC). The ADV8005 can receive up to eight channels of I²S, S/PDIF, direct stream digital (DSD), and high bit rate (HBR) audio passed from either the serial video Rx or from the externally available audio input pins.

The ADV8005 supports the I²C protocol for communication with the system microcontroller.

ADV8005 MODELS

The ADV8005 includes a number of models, each featuring different capabilities; all are provided in the same 19 mm × 19 mm, 425-ball CSP_BGA package (see Table 9).

Note that the functionality of the ADV8005KBCZ-8A is described throughout this data sheet. Some sections are not relevant to other models because not all of the blocks found in the ADV8005KBCZ-8A are included in those models. Table 9 lists the functionality for each model.

DETAILED FUNCTIONAL BLOCK DIAGRAM

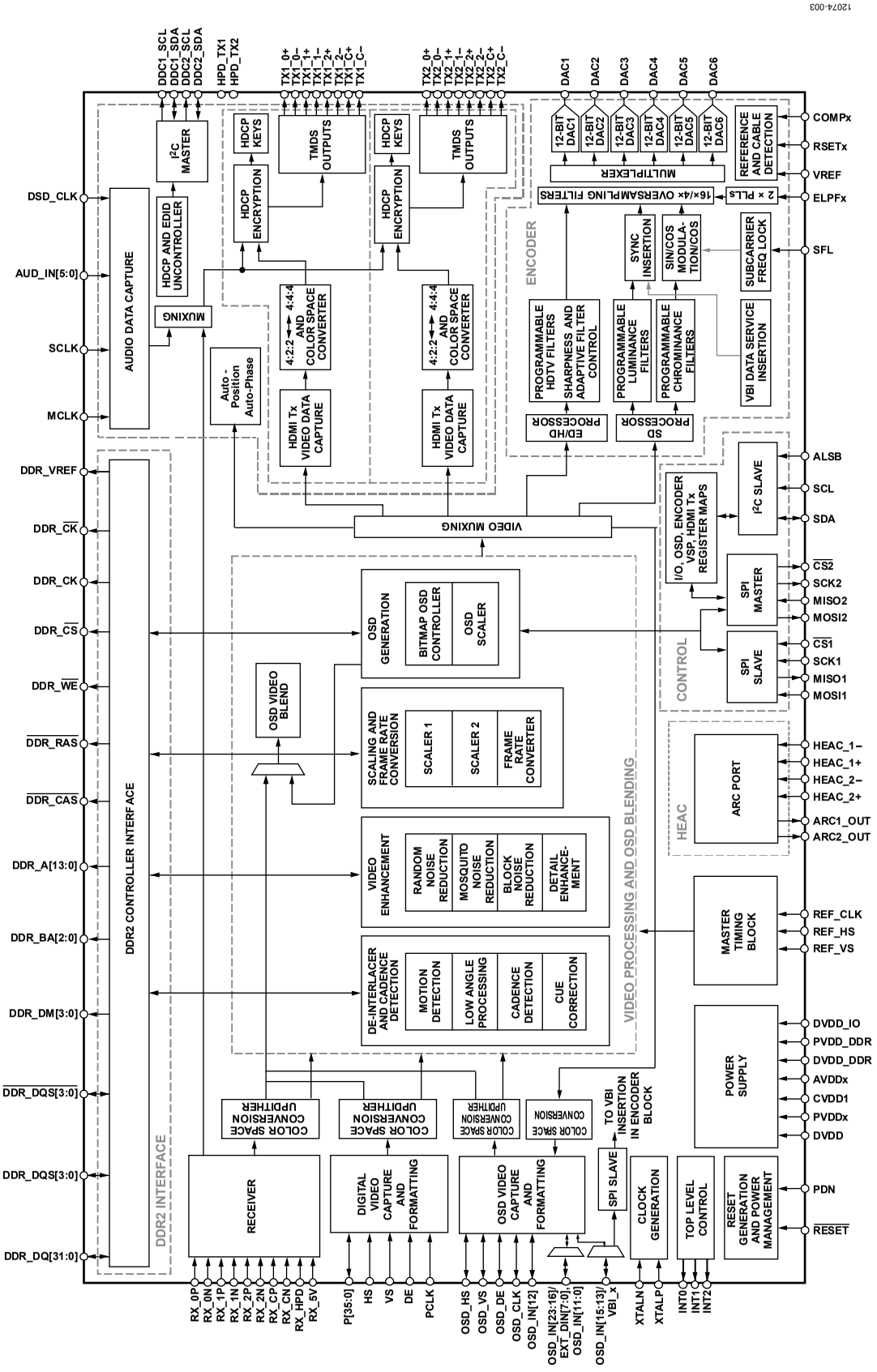

Figure 2. ADV8005KBCZ-8A Functional Block Diagram

SPECIFICATIONS

Measured at DVDD = 1.746 V to 1.854 V, DVDD_DDR = 1.746 V to 1.854 V, PVDD1 = 1.746 V to 1.854 V, PVDD2 = 1.746 V to 1.854 V, PVDD3 = 1.746 V to 1.854 V, PVDD5 = 1.789 V to 1.90 V, PVDD6 = 1.789 V to 1.90 V, PVDD_DDR = 1.746 V to 1.854 V, AVDD3 = 1.746 V to 1.854 V, AVDD4 = 1.746 V to 1.854 V, CVDD1 = 1.746 V to 1.854 V, AVDD1 = 3.20 V to 3.40 V, AVDD2 = 3.20 V to 3.40 V, DVDD_IO = 3.20 V to 3.40 V, T_{MIN} to T_{MAX} = 0°C to 70°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each DAC)				12		Bits
Integral Nonlinearity, +ve[1]	INL	DAC outputs sampled at 500 kHz		0.389		LSB
Integral Nonlinearity, −ve[1]	INL	DAC outputs sampled at 500 kHz		−0.322		LSB
Differential Nonlinearity, +ve[2]	DNL	DAC outputs sampled at 500 kHz		0.183		LSB
Differential Nonlinearity, −ve[2]	DNL	DAC outputs sampled at 500 kHz		−0.208		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 × DVDD_IO			V
Input Low Voltage	V_{IL}				0.3 × DVDD_IO	V
Input Leakage Current	I_{IN}	HDMI Ethernet and audio channel (HEAC_x±) inputs			±60	µA
		DDR_DQS[x] inputs			±60	µA
		Other digital inputs			±10	µA
		$\overline{\text{RESET}}$			±60	µA
Input Capacitance	C_{IN}			13		pF
DIGITAL INPUTS (5 V TOLERANT)						
Input High Voltage	V_{IH}		3.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}				±60	µA
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
High Impedance Leakage Current	I_{LEAK}				±10	µA
Output Capacitance	C_{OUT}			13		pF
POWER REQUIREMENTS[3, 4]						
Digital Power Supplies	DVDD, DVDD_DDR, PVDD_DDR		1.746	1.8	1.854	V
PLL Analog Supply	PVDD1		1.746	1.8	1.854	V
PLL Digital Supply	PVDD2		1.746	1.8	1.854	V
Encoder PLL Supply	PVDD3		1.746	1.8	1.854	V
HDMI PLL Power Supply[5]						
Transmitter 1 (Tx1)	PVDD5		1.789	1.845	1.90	V
Transmitter 2 (Tx2)	PVDD6		1.789	1.845	1.90	V
HDMI Analog Power Supply						
Tx1	AVDD3		1.746	1.8	1.854	V
Tx2	AVDD4		1.746	1.8	1.854	V
Comparator Power Supply	CVDD1		1.746	1.8	1.854	V
HDMI Rx Inputs Analog Supply	AVDD1		3.20	3.3	3.40	V
Encoder Analog Power Supply	AVDD2		3.20	3.3	3.40	V
Digital Interface Supply	DVDD_IO		3.20	3.3	3.40	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Digital Power Supply Currents	I_{DVDD}, I_{DVDD_DR}, I_{PVDD_DDR}	Mode 1		1693.9		mA
		Mode 2		1508.1		mA
		Power-down mode		11.7		mA
PLL Analog Supply Current	I_{PVDD1}	Mode 1		23.0		mA
		Mode 2		20.5		mA
		Power-down mode		0.9		mA
PLL Digital Supply Current	I_{PVDD2}	Mode 1		21.3		mA
		Mode 2		19.26		mA
		Power-down mode		0.06		mA
Encoder PLL Supply Current	I_{PVDD3}	Mode 1		13.8		mA
		Mode 2		3.27		mA
		Power-down mode		0.01		mA
HDMI Tx1 PLL Supply Current	I_{PVDD5}	Mode 1		74.9		mA
		Mode 2		59.0		mA
		Power-down mode		0		mA
HDMI Tx2 PLL Supply Current	I_{PVDD6}	Mode 1		75.0		mA
		Mode 2		0.5		mA
		Power-down mode		0		mA
HDMI Tx1 Analog Power Supply Current	I_{AVDD3}	Mode 1		29.4		mA
		Mode 2		19.7		mA
		Power-down mode		0		mA
HDMI Tx2 Analog Power Supply Current	I_{AVDD4}	Mode 1		26.6		mA
		Mode 2		0.6		mA
		Power-down mode		0		mA
Comparator Power Supply Current	I_{CVDD1}	Mode 1		78.4		mA
		Mode 2		73.4		mA
		Power-down mode		1.1		mA
HDMI Rx Inputs Analog Supply Current	I_{AVDD1}	Mode 1		63.1		mA
		Mode 2		57.6		mA
		Power-down mode		0.2		mA
Encoder Analog Power Supply	I_{AVDD2}	Mode 1		38.0		mA
		Mode 2		34.9		mA
		Power-down mode		2.1		mA
Digital Interface Supply Current	I_{DVDD_IO}	Mode 1		3.0		mA
		Mode 2		1.3		mA
		Power-down mode		0		mA

[1] Integral nonlinearity (INL) measures the deviation of the actual DAC transfer function from the ideal. For +ve INL, the actual line lies above the ideal line value. For −ve INL, the actual line lies below the ideal line value.

[2] Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For −ve DNL, the actual step value lies below the ideal step value.

[3] Mode 1 involves a 1080i, 60 Hz input to the ADV8005 receiver and a 720p, 60 Hz input to the ADV8005 TTL external OSD input. Both inputs are run through the front-end color space converters. The 1080i, 60 Hz video stream is deinterlaced and upscaled to 4k × 2k at 24 Hz. The 720p video stream is input to the OSD block and is blended onto the 4k × 2k at 24 Hz video stream using the OSD block scaler. Both HDMI transmitters are then driven using the 4k × 2k at 24 Hz output.

[4] Mode 2 involves a 1080i, 60 Hz input to the ADV8005 receiver. This input is run through the front-end color space converter. The 1080i, 60 Hz video stream is deinterlaced and is output to HDMI Tx1. The secondary VSP is used to convert the 1080p video stream to 480i and is output using the SD encoder.

[5] For normal operation, set the Tx PVDD5 and PVDD6 supplies to 1.845 V ± 3%. However, if the ADV8005 die temperature is kept below 100°C, it is possible to use PVDD5 and PVDD6 with a reduced nominal voltage supply level of 1.8 V ± 3%. It is possible to measure the die temperature (T_J) of the ADV8005 using the method outlined in the Thermal Considerations section. If using this reduced voltage level with Tx PVDD5 and PVDD6, it is the responsibility of the customer to ensure that the die temperature is below 100°C when used in the highest power mode of the application and at its highest ambient temperature.

ANALOG SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT						
Low Drive Output Current (Full Scale)		R_{SET} = 4.12 kΩ, R_L = 300 Ω	3.95	4.3	4.5	mA
Output Compliance	V_{OC}		0		1.4	V
Output Capacitance	C_{OUT}	DAC1, DAC2, DAC3		9		pF
		DAC4, DAC5, DAC6		9		pF
DAC						
DAC-to-DAC Matching		DAC1 to DAC6		0.9		%
DAC Analog Output Skew		DAC1 to DAC6		0.2		ns

DATA AND I²C TIMING CHARACTERISTICS

For input timing measurements, V_{IH} = DVDD_IO and V_{IL} = GND.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TMDS CLOCK						
TMDS Input Clock Frequency			25		297	MHz
TMDS Output Clock Frequency			25		297	MHz
CLOCK AND CRYSTAL						
Crystal (XTAL) Frequency				27		MHz
Stability					±50	ppm
Video Input Clock Frequency Range						
Primary			13.5		162	MHz
Secondary			13.5		162	MHz
Video Output Clock Frequency Range			13.5		162	MHz
Serial Clock Frequency						
Serial Port 1 (SCK1)					50	MHz
Serial Port 2 (SCK2)			11.5		81	MHz
Serial Port 3 (VBI_SCK)					27	MHz
Audio Frequency						
SCLK					49.152	MHz
MCLK					98.304	MHz
DSD_CLK					5.6448	MHz
FAST I²C PORTS[1]		See Figure 3				
SCL Frequency					400	kHz
SCL Minimum Pulse Width High	t_1		600			ns
SCL Minimum Pulse Width Low	t_2		1.3			µs
Start Condition Hold Time	t_3		600			ns
Start Condition Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA Rise Time	t_6				300	ns
SCL and SDA Fall Time	t_7				300	ns
Stop Condition Setup Time	t_8		0.6			µs
SERIAL PORT[2, 3]						
Master Serial Port (Serial Port 2)		See Figure 4, Figure 5, and Figure 6				
$\overline{CS2}$ Falling Edge to SCK2 Rising/Falling Edge	t_9, t_{10}	t_9 or t_{10}, depending on the values of CPHA and CPOL	1 × SCK2[4]		1.5 × SCK2[4]	ns
SCK2 Rising/Falling Edge to $\overline{CS2}$ Rising Edge	t_{11}, t_{12}	t_{11} or t_{12}, depending on the values of CPHA and CPOL	1 × SCK2[4]		1.5 × SCK2[4]	ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{CS2}$ Pulse Width	t_{13}		1880		1900	ns
SCK2 High Time	t_{14}		0.45 × SCK2[4]		0.55 × SCK2[4]	% duty cycle
SCK2 Low Time			0.45 × SCK2[4]		0.55 × SCK2[4]	% duty cycle
MOSI2 Start of Data Invalid to SCK2 Falling Edge	t_{15}	SPI Mode 0, SPI Mode 3			1.45	ns
$\overline{CS2}$ Start of Data Invalid to SCK2 Falling Edge	t_{15}	SPI Mode 0, SPI Mode 3			1.21	ns
SCK2 Falling Edge to MOSI2 End of Data Invalid	t_{16}	SPI Mode 0, SPI Mode 3			0.08	ns
SCK2 Falling Edge to $\overline{CS2}$ End of Data Invalid	t_{16}	SPI Mode 0, SPI Mode 3			0.19	ns
MISO2 Setup Time	t_{17}	Valid regardless of the SCK2 active edge used	11.19			ns
MISO2 Hold Time	t_{18}	Valid regardless of the SCK2 active edge used	0.0			ns
MOSI2 Start of Data Invalid to SCK2 Rising Edge	t_{19}	SPI Mode 1, SPI Mode 2			1.45	ns
$\overline{CS2}$ Start of Data Invalid to SCK2 Rising Edge	t_{19}	SPI Mode 1, SPI Mode 2			1.21	ns
SCK2 Rising Edge to MOSI2 End of Data Invalid	t_{20}	SPI Mode 1, SPI Mode 2			0.08	ns
SCK2 Rising Edge to $\overline{CS2}$ End of Data Invalid	t_{20}	SPI Mode 1, SPI Mode 2			0.19	ns
MISO2 Setup Time	t_{21}	Valid regardless of the SCK2 active edge used	11.19			ns
MISO2 Hold Time	t_{22}	Valid regardless of the SCK2 active edge used	0.0			ns
Slave Mode (Serial Port 1)		See Figure 7, Figure 8, and Figure 9				
$\overline{CS1}$ Falling Edge to SCK1 Rising/Falling Edge	t_{23}, t_{24}	t_{23} or t_{24}, depending on the values of CPHA and CPOL	50.0			ns
SCK1 Rising/Falling Edge to $\overline{CS1}$ Rising Edge	t_{25}, t_{26}	t_{25} or t_{26}, depending on the values of CPHA and CPOL	50.0			ns
$\overline{CS1}$ Pulse Width	t_{27}			5 × SCK1[4]		ns
SCK1 High Time	t_{30}		0.45 × SCK1[4]		0.55 × SCK1[4]	% duty cycle
SCK1 Low Time			0.45 × SCK1[4]		0.55 × SCK1[4]	% duty cycle
MOSI1 Setup Time	t_{31}	SPI Mode 0, SPI Mode 3	1.63			ns
MOSI1 Hold Time	t_{32}	SPI Mode 0, SPI Mode 3	0.66			ns
SCK1 Falling Edge to MISO1 Start of Data Invalid	t_{33}	SPI Mode 0, SPI Mode 3			5.7	ns
SCK1 Falling Edge to MISO1 End of Data Invalid	t_{34}	SPI Mode 0, SPI Mode 3			12.16	ns
MOSI1 Setup Time	t_{35}	SPI Mode 1, SPI Mode 2	1.63			ns
MOSI1 Hold Time	t_{36}	SPI Mode 1, SPI Mode 2	0.66			ns
SCK1 Rising Edge to MISO1 Start of Data Invalid	t_{37}	SPI Mode 1, SPI Mode 2			5.7	ns
SCK1 Rising Edge to MISO1 End of Data Invalid	t_{38}	SPI Mode 1, SPI Mode 2			12.16	ns
Slave Mode (Serial Port 3)		See Figure 10				
VBI_SCK High Time	t_{39}		0.45 × VBI_SCK[4]		0.55 × VBI_SCK[4]	% duty cycle
VBI_SCK Low Time			0.45 × VBI_SCK[4]		0.55 × VBI_SCK[4]	% duty cycle
VBI_$\overline{CS}$ Pulse Width				5 × VBI_SCK		ns
VBI_$\overline{CS}$, VBI_MOSI Setup Time	t_{40}	SPI Mode 0 only	1.27			ns
VBI_$\overline{CS}$, VBI_MOSI Hold Time	t_{41}	SPI Mode 0 only	0.15			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI Passthrough Mode		See Figure 11				
Data Transition on SCK1 to Start of Data Invalid on SCK2	t_{42}				4.97	ns
Data Transition on SCK1 to End of Data Invalid on SCK2	t_{43}				10.10	ns
Data Transition on MOSI1 to Start of Data Invalid on MOSI2	t_{42}				5.32	ns
Data Transition on MOSI1 to End of Data Invalid on MOSI2	t_{43}				10.82	ns
Data Transition on MISO2 to Start of Data Invalid on MISO1	t_{42}				4.36	ns
Data Transition on MISO2 to End of Data Invalid on MISO1	t_{43}				8.85	ns
Data Transition on $\overline{CS1}$ to Start of Data Invalid on $\overline{CS2}$	t_{42}				5.32	ns
Data Transition on $\overline{CS1}$ to End of Data Invalid on $\overline{CS2}$	t_{43}				10.91	ns
RESET FUNCTION						
Reset Pulse Width			5			ms
VIDEO DATA AND CONTROL INPUTS[3]		See Figure 12 to Figure 16				
PCLK High Time	t_{44}		0.45 × PCLK[4]		0.55 × PCLK[4]	% duty cycle
PCLK Low Time			0.45 × PCLK[4]		0.55 × PCLK[4]	% duty cycle
OSD_CLK High Time	t_{51}	OSD_CLK signal of Pin A3	0.45 × OSD_CLK[4]		0.55 × OSD_CLK[4]	% duty cycle
OSD_CLK Low Time		OSD_CLK signal of Pin A3	0.45 × OSD_CLK[4]		0.55 × OSD_CLK[4]	% duty cycle
Main Video Input, SDR and DDR Modes Setup Time (Data Latched on Rising Edge)	t_{45}		1.28			ns
Main Video Input, SDR and DDR Modes Hold Time (Data Latched on Rising Edge)	t_{46}		1.67			ns
Main Video Input, DDR Mode Setup Time (Data Latched on Falling Edge)	t_{47}		1.28			ns
Main Video Input, DDR Mode Hold Time (Data Latched on Falling Edge)	t_{48}		1.67			ns
Interleaved Video Input, SDR Setup Time (Data Latched on Rising Edge)	t_{49}	Used for 300 MHz TTL data	1.28			ns
Interleaved Video Input, SDR Hold Time (Data Latched on Rising Edge)	t_{50}	Used for 300 MHz TTL data	1.67			ns
External OSD Input, SDR and DDR Modes Setup Time (Data Latched on Rising Edge)	t_{52}		1.28			ns
External OSD Input, SDR and DDR Modes Hold Time (Data Latched on Rising Edge)	t_{53}		1.67			ns
External OSD Input, DDR Mode Setup Time (Data Latched on Rising Edge)	t_{54}		1.28			ns
External OSD Input, DDR Mode Hold Time (Data Latched on Rising Edge)	t_{55}		1.67			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIDEO DATA AND CONTROL OUTPUTS[3]		See Figure 17 and Figure 18				
OSD_CLK High Time	t_{56}		0.40 × OSD_CLK[4]		0.60 × OSD_CLK[4]	% duty cycle
OSD_CLK Low Time			0.40 × OSD_CLK[4]		0.60 × OSD_CLK[4]	% duty cycle
Data and Control Start of Data Invalid to OSD_CLK Active Edge (Data Latched on Falling Edge)	t_{57}				0.3	ns
OSD_CLK Active Edge to Data and Control End of Data Invalid (Data Latched on Falling Edge)	t_{58}				1.66	ns
Data and Control Start of Data Invalid to OSD_CLK Active Edge (Data Latched on Rising Edge)	t_{59}				0.62	ns
OSD_CLK Active Edge to Data and Control End of Data Invalid (Data Latched on Rising Edge)	t_{60}				1.12	ns
S/PDIF INPUT[3]		See Figure 19 and Figure 20				
MCLK High Time	t_{61}		0.45 × MCLK[4]		0.55 × MCLK[4]	% duty cycle
MCLK Low Time			0.45 × MCLK[4]		0.55 × MCLK[4]	% duty cycle
S/PDIF Data Setup Time	t_{62}		1.4			ns
S/PDIF Data Hold Time	t_{63}		1.38			ns
I²S PORT, SLAVE MODE[3]		See Figure 21				
SCLK High Time	t_{64}		0.45 × SCLK[4]		0.55 × SCLK[4]	% duty cycle
SCLK Low Time			0.45 × SCLK[4]		0.55 × SCLK[4]	% duty cycle
I²S Data Setup Time	t_{65}		1.91			ns
I²S Data Hold Time	t_{66}		1.1			ns
DSD PORT[3]		See Figure 26				
DSD_CLK High Time	t_{67}		0.45 × DSD_CLK[4]		0.55 × DSD_CLK[4]	% duty cycle
DSD_CLK Low Time			0.45 × DSD_CLK[4]		0.55 × DSD_CLK[4]	% duty cycle
DSD Data Setup Time	t_{68}		1.66			ns
DSD Data Hold Time	t_{69}		1.44			ns
EXTERNAL SYNC TIMING MODE[3]		See Figure 27				
REF_CLK High Time	t_{70}		0.45 × REF_CLK[4]		0.55 × REF_CLK[4]	% duty cycle
REF_CLK Low Time			0.45 × REF_CLK[4]		0.55 × REF_CLK[4]	% duty cycle
REF Data Setup Time	t_{71}		1.35			ns
REF Data Hold Time	t_{72}		1.33			ns

[1] It is possible to run I²C at faster speeds; however, it has been characterized to run only in fast mode.
[2] All serial port measurements are for the default polarity and phase settings (clock low in idle state and negative edge used).
[3] All measurements are guaranteed by design only.
[4] Specification is in clock periods; for example, 1 × SCK2 periods.

Timing Diagrams

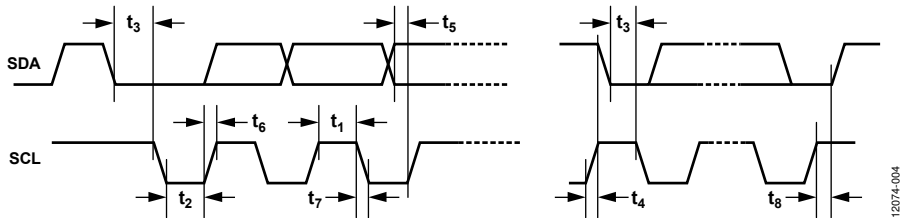

Figure 3. I²C Timing

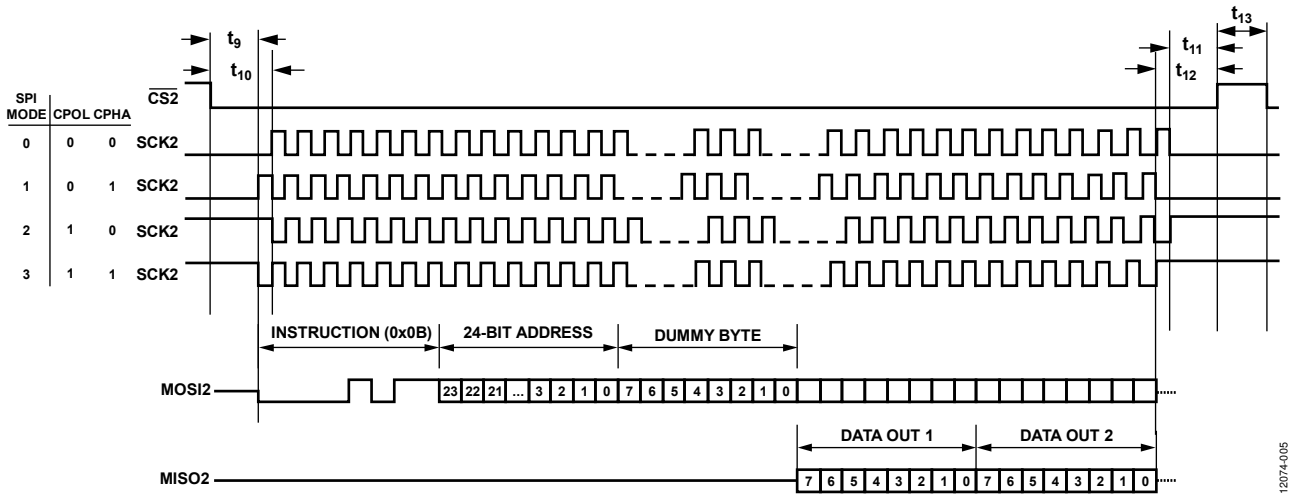

Figure 4. Detailed SPI Master Timing Diagram (Serial Port 2)

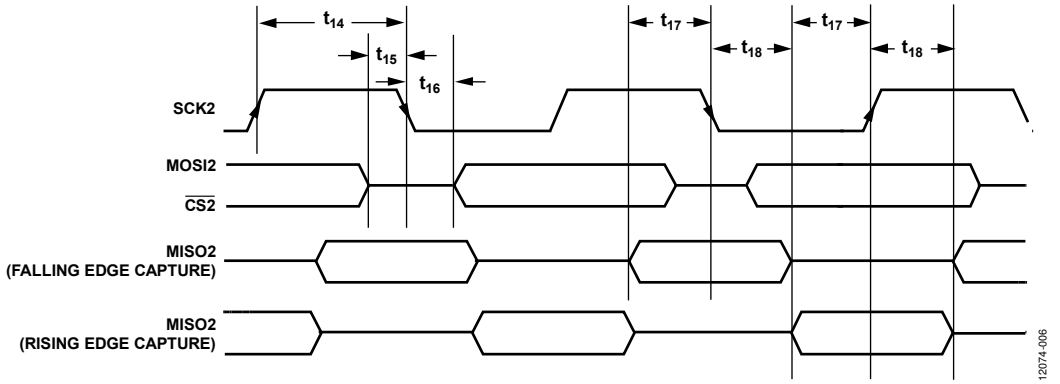

Figure 5. Serial Port 2 Master Mode Timing (SPI Mode 0 and SPI Mode 3)

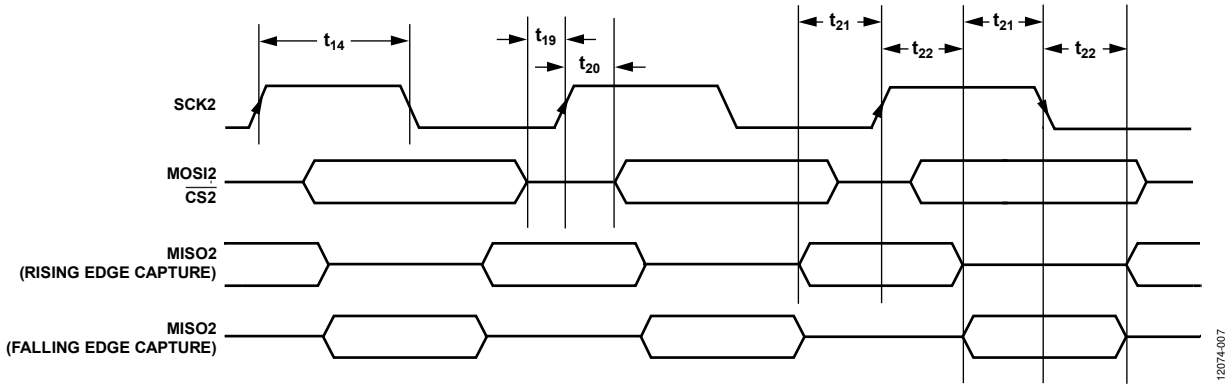

Figure 6. Serial Port 2 Master Mode Timing (SPI Mode 1 and SPI Mode 2)

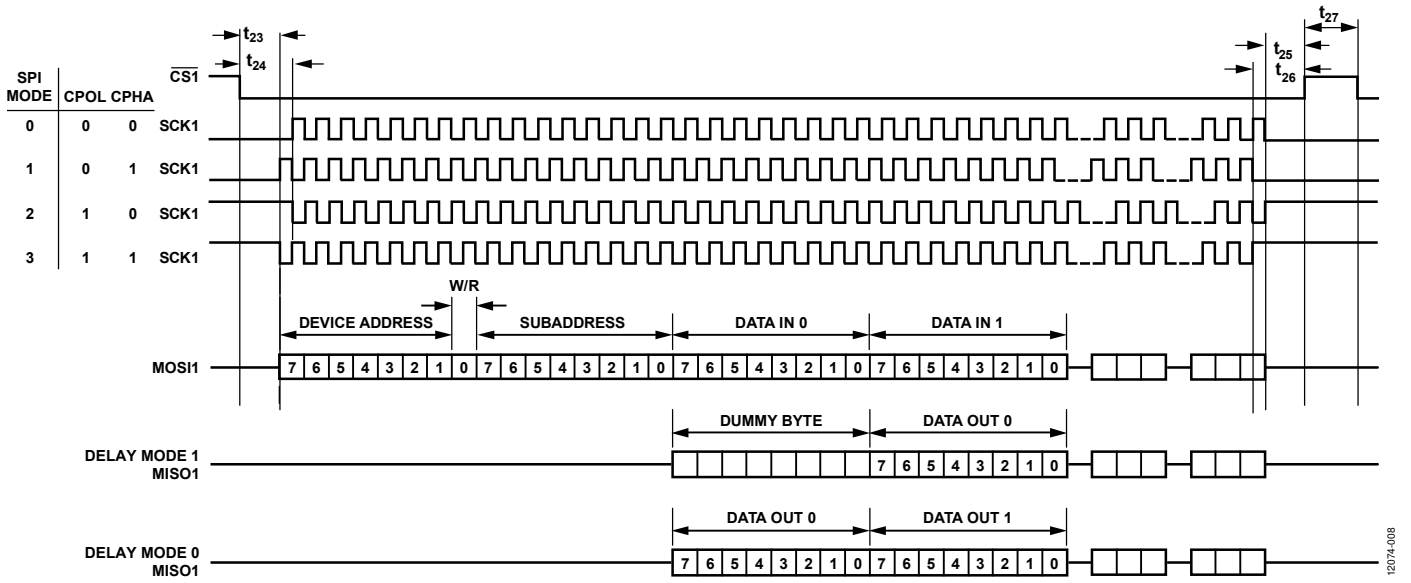

Figure 7. Detailed SPI Slave Timing Diagram (Serial Port 1)

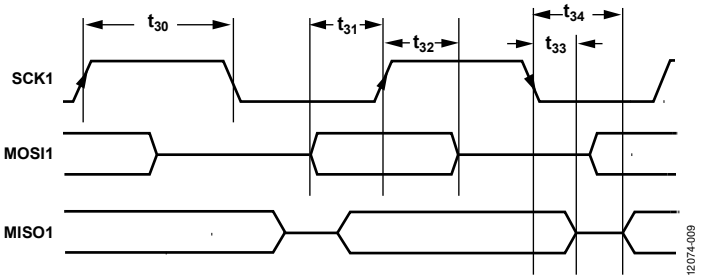

Figure 8. Serial Port 1 Slave Mode Timing (SPI Mode 0 and SPI Mode 3)

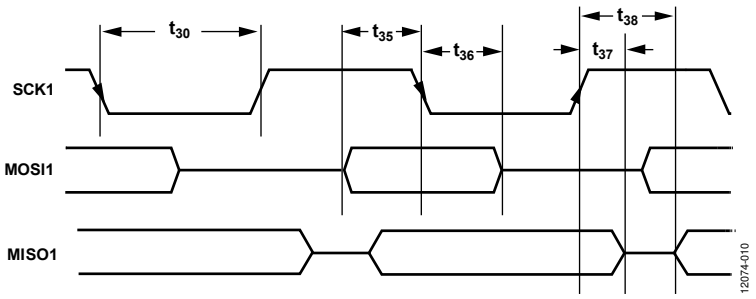

Figure 9. Serial Port 1 Slave Mode Timing (SPI Mode 1 and SPI Mode 2)

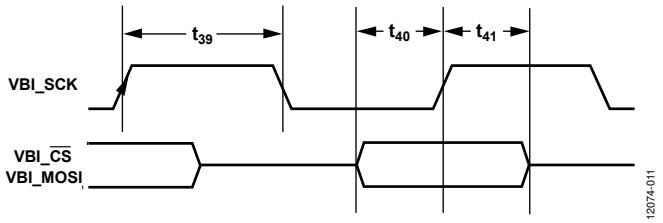

Figure 10. Serial Port 3 Slave Mode Timing (SPI Mode 0 Only)

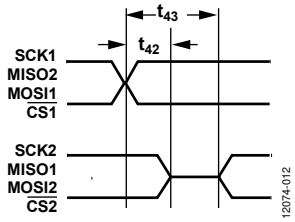

Figure 11. SPI Passthrough Mode (Serial Port 1 and Serial Port 2)

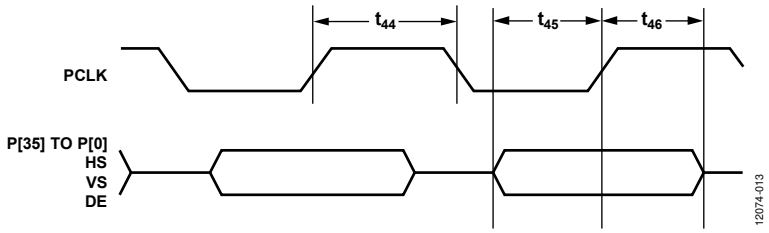

Figure 12. Main Video Input, Noninterleaved SDR Video Data and Control Timing

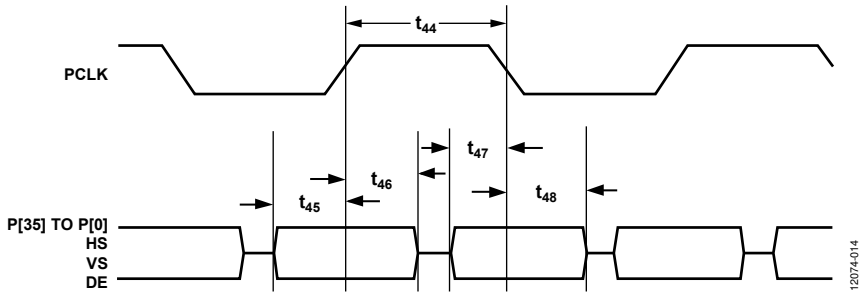

Figure 13. Main Video Input, Noninterleaved DDR Video Data and Control Timing

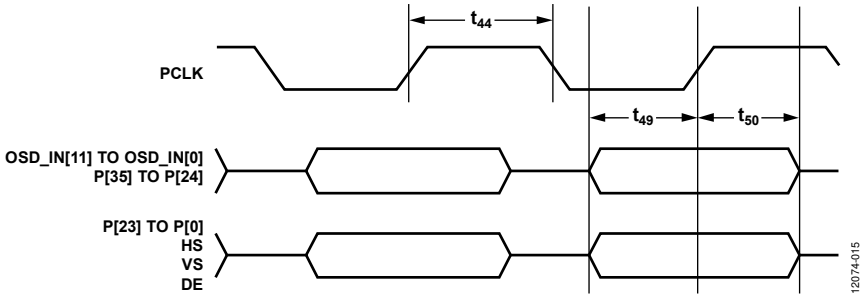

Figure 14. Interleaved SDR Video Data and Control Input Timing

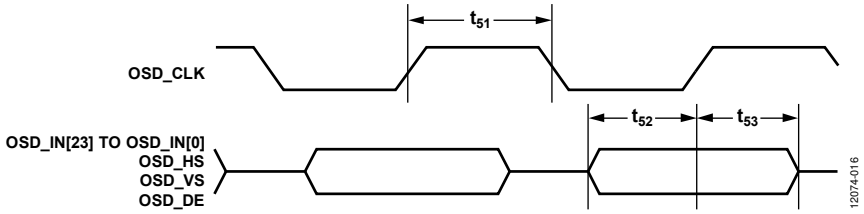

Figure 15. External OSD Input, Noninterleaved SDR Video Data and Control Timing

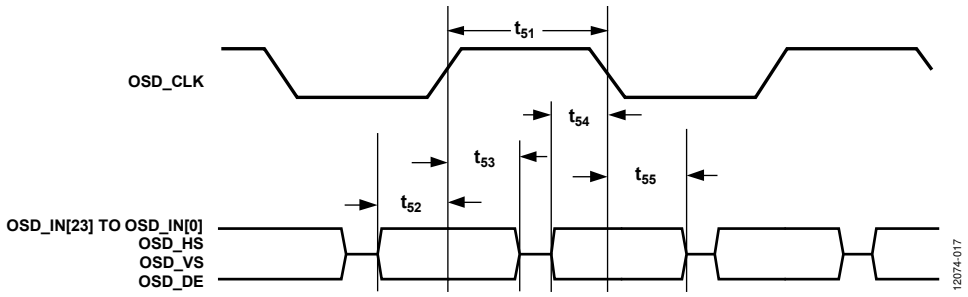

Figure 16. External OSD Input, Noninterleaved DDR Video Data and Control Timing

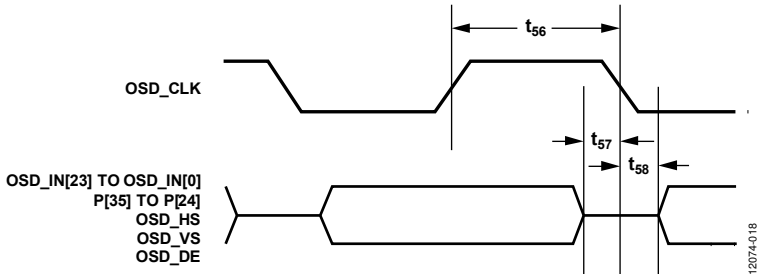

Figure 17. SDR Video Data and Control Output Timing (Data Launched on Falling Edge)

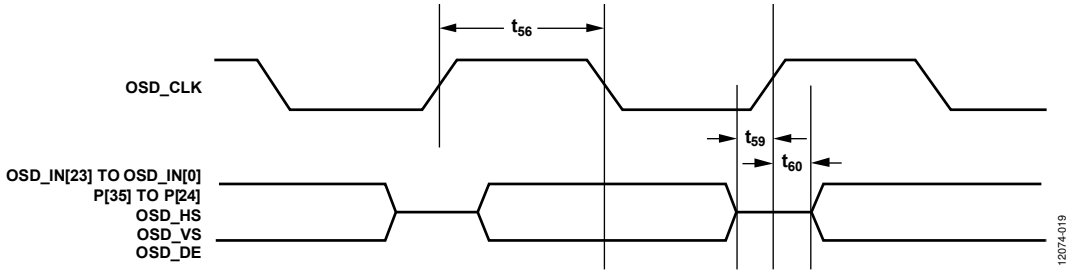

Figure 18. SDR Video Data and Control Output Timing (Data Launched on Rising Edge)

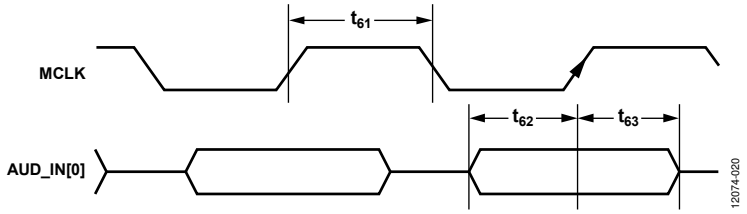

Figure 19. S/PDIF Input Timing, Data Latched on Rising Edge

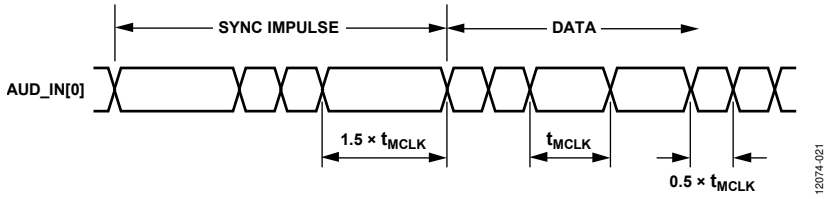

Figure 20. S/PDIF Data Timing

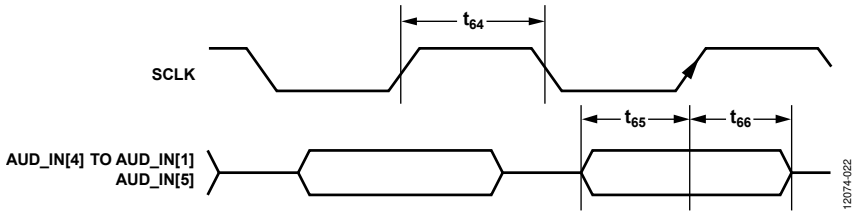

Figure 21. I²S Timing

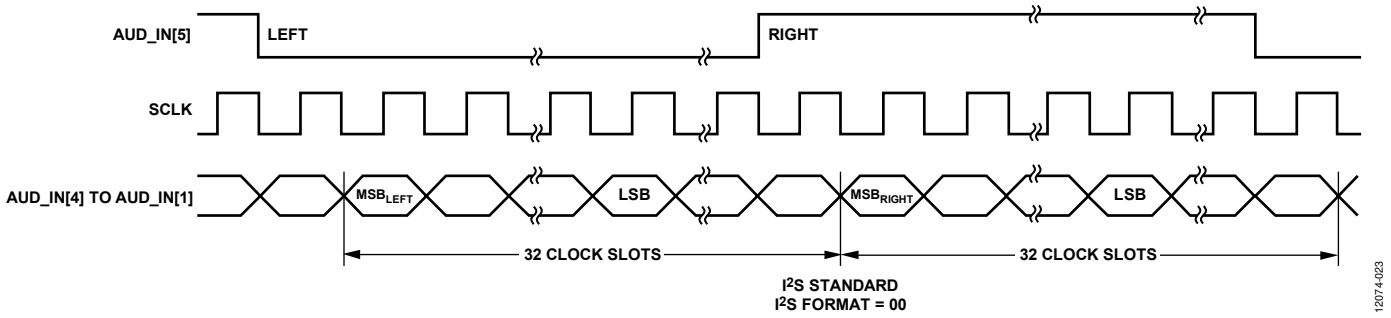

Figure 22. I²S Standard Audio—Data Width of 16 Bits to 24 Bits per Channel

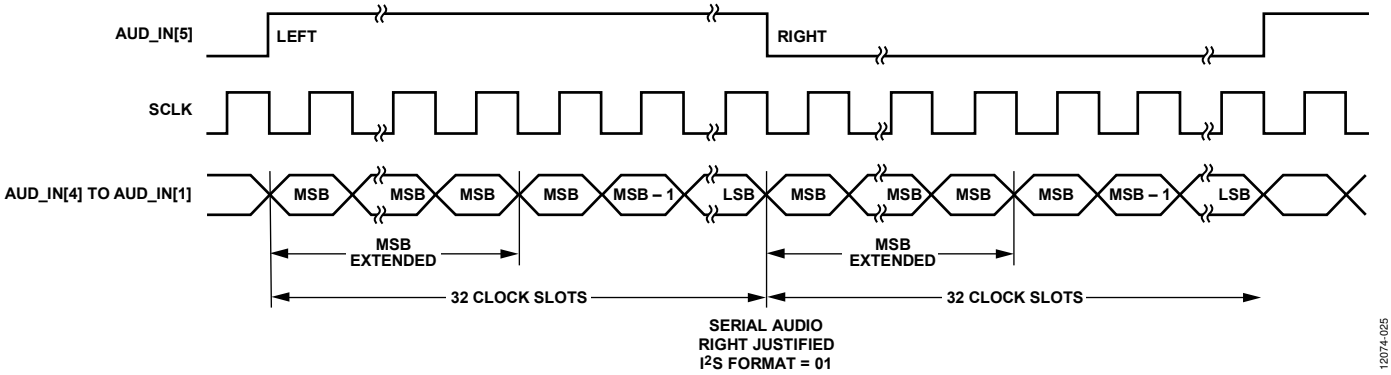

Figure 23. Serial Audio—Right Justified

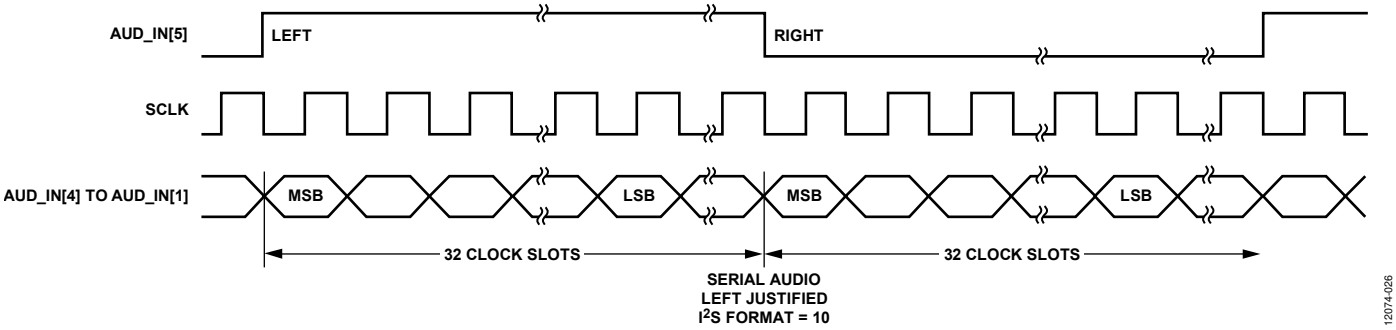

Figure 24. Serial Audio—Left Justified

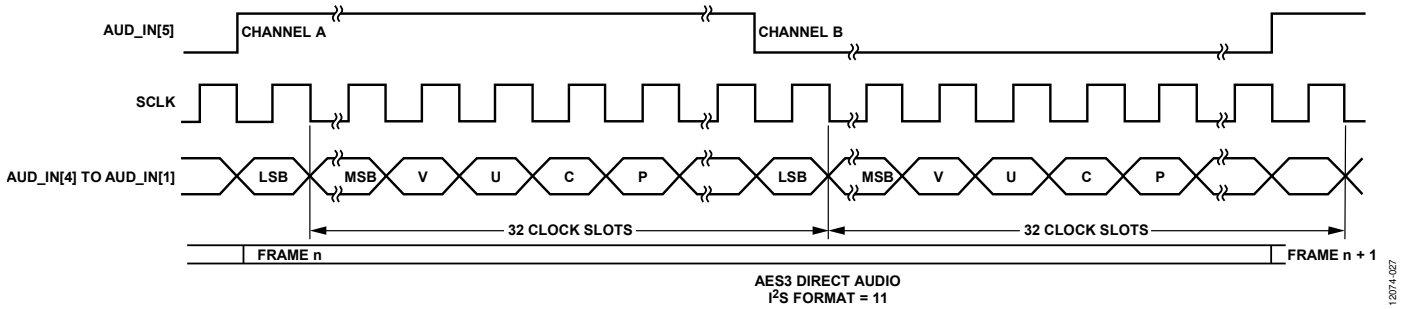

Figure 25. AES3 Direct Audio

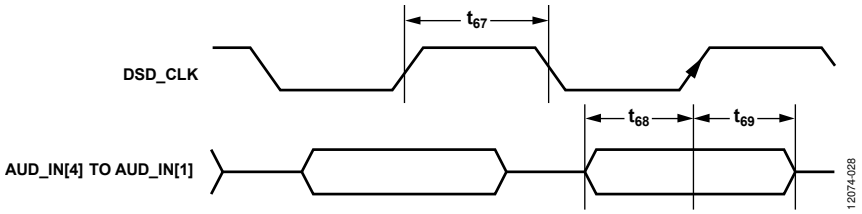

Figure 26. DSD Timing

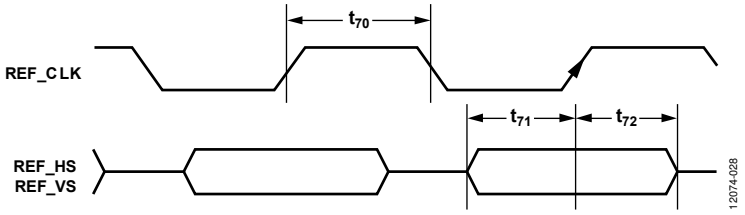

Figure 27. External Sync Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1, ADDD2, DVDD_IO to GND	3.9 V
DVDD, PVDDx, CVDD1, AVDD3, AVDD4, DVDD_DDR, PVDD_DDR to GND	2.2 V
DVDD to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD1 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD2 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD3 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD5 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD6 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
CVDD1 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
AVDD3 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
AVDD4 to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
DVDD_DDR to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
PVDD_DDR to Other 1.8 V Power Supplies[1]	−0.3 V to +0.3 V
Digital Inputs to GND	−0.3 V to DVDD_IO + 0.3 V
Serial Video Inputs to GND	−0.3 V to CVDD1 + 0.3 V
DDR_VREF to GND	−0.3 V to DVDD_DDR + 0.3 V
DDR Inputs to GND	−0.3 V to DVDD_DDR + 0.3 V
DDR Outputs to GND	−0.3 V to DVDD_DDR + 0.3 V
5 V Tolerant Digital Inputs to GND[2]	−0.3 V to +5.5 V
1.8 V Analog Inputs to GND	−0.3 V to AVDD3 + 0.3 V
3.3 V Analog Inputs to GND	−0.3 V to AVDD2 + 0.3 V
HDMI Digital Outputs to GND	−0.3 V to AVDD3 + 0.3 V
Digital Outputs Voltage to GND	−0.3 V to DVDD_IO + 0.3 V
Analog Outputs Voltage to GND[3]	−0.3 V to AVDD2 + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] This includes the 1.8 V power supplies (DVDD, PVDD1, PVDD2, PVDD3, CVDD1, AVDD3, AVDD4, DVDD_DDR, and PVDD_DR) and the 1.845 V supplies (PVDD5 and PVDD6).
[2] The following inputs are 5 V tolerant:, DDC1_SCL, DDC2_SCL, DDC1_SDA, DDC2_SDA, HEAC_1−, HEAC_1+, HEAC_2−, HEAC_2+, RX_5V, and RX_HPD.
[3] Except the ELPF1 and ELPF2 outputs, which are kept to −0.3 V to PVDD3 + 0.3 V; the RTERM output, which is kept to −0.3 V to CVDD1 + 0.3 V; and the R_TX1 and R_TX2 outputs, which are kept to −0.3 V to PVDD5 + 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

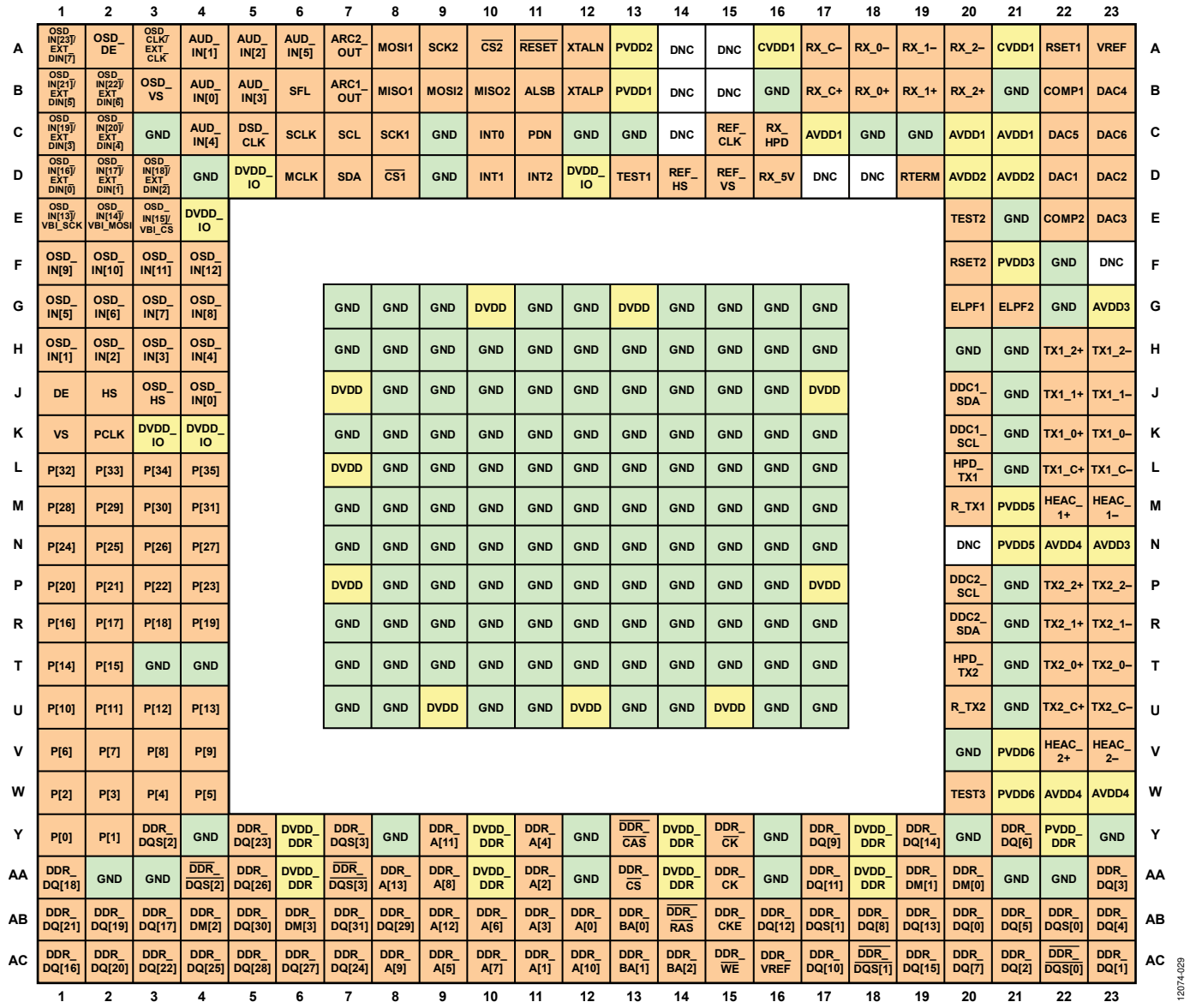

Figure 28. ADV8005KBCZ-8A and ADV8005KBCZ-8N Pin Configuration

Table 5. ADV8005KBCZ-8A and ADV8005KBCZ-8N Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	OSD_IN[23]/EXT_DIN[7]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 23 (OSD_IN[23]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[7]).
A2	OSD_DE	OSD video sync	Data Enable for the OSD Input Port.
A3	OSD_CLK/EXT_CLK	OSD video sync	Pixel Clock for the OSD Input Port (OSD_CLK). Pixel Clock for External Video Data (EXT_CLK).
A4	AUD_IN[1]	Audio input	I^2S0/DSD1 Audio Input.
A5	AUD_IN[2]	Audio input	I^2S1/DSD2 Audio Input.
A6	AUD_IN[5]	Audio input	Left/Right Clock/DSD5 Audio Input.
A7	ARC2_OUT	Audio output	Audio Return Channel for HDMI Tx2.
A8	MOSI1	Serial port control	Master Output Slave Input (Serial Port 1). Serial Port 1 is used for OSD control.
A9	SCK2	Serial port control	Serial Clock (Serial Port 2). Serial Port 2 is used for the external flash ROM.
A10	$\overline{CS2}$	Serial port control	Chip Select (Serial Port 2). Serial Port 2 is used for the external flash ROM.
A11	$\overline{RESET}$	Miscellaneous digital	Reset Pin.

Pin No.	Mnemonic	Type	Description
A12	XTALN	Miscellaneous 1.8 V Analog[1]	Crystal Output Pin. Leave this pin floating if a clock oscillator is used.
A13	PVDD2	Power	PLL Digital Supply Voltage (1.8 V).
A14	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
A15	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
A16	CVDD1	Power	Comparator Supply Voltage (1.8 V).
A17	RX_C−	Rx input	Rx Clock Complement Input.
A18	RX_0−	Rx input	Rx Channel 0 Complement Input.
A19	RX_1−	Rx input	Rx Channel 1 Complement Input.
A20	RX_2−	Rx input	Rx Channel 2 Complement Input.
A21	CVDD1	Power	Comparator Supply Voltage (1.8 V).
A22	RSET1	Miscellaneous analog[1]	Resistor Current Setting for DAC1, DAC2, and DAC3. Place the RSET1 resistor as close as possible to the ADV8005.
A23	VREF	Miscellaneous analog[1]	Optional External Voltage Reference Input for DACx or Voltage Reference Output. Place VREF voltage components as close as possible to the ADV8005.
B1	OSD_IN[21]/EXT_DIN[5]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 21 (OSD_IN[21]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[5]).
B2	OSD_IN[22]/EXT_DIN[6]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 22 (OSD_IN[22]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[6]).
B3	OSD_VS	OSD video sync	Vertical Sync for the OSD Input Port.
B4	AUD_IN[0]	Audio input	S/PDIF/DSD0 Audio Input.
B5	AUD_IN[3]	Audio input	I²S2/DSD3 Audio Input.
B6	SFL	SFL	Subcarrier Frequency Lock Signal.
B7	ARC1_OUT	Audio output	Audio Return Channel for HDMI Tx1.
B8	MISO1	Serial port control	Master Input Slave Output (Serial Port 1). Serial Port 1 is used for OSD control.
B9	MOSI2	Serial port control	Master Output Slave Input (Serial Port 2). Serial Port 2 is used for the external flash ROM.
B10	MISO2	Serial port control	Master Input Slave Output (Serial Port 2). Serial Port 2 is used for the external flash ROM.
B11	ALSB	I²C control	This pin sets the LSB of the I²C address. When the ALSB pin is set low, the I²C address is 0x18; when the ALSB pin is set high, the I²C address is 0x1A.
B12	XTALP	Miscellaneous 1.8 V Analog[1]	Input Pin for 27 MHz Crystal or an External 1.8 V, 27 MHz Clock Oscillator Source to Clock the ADV8005.
B13	PVDD1	Power	PLL Analog Supply Voltage (1.8 V).
B14	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
B15	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
B16	GND	GND	Ground.
B17	RX_C+	Rx input	Rx Clock True Input.
B18	RX_0+	Rx input	Rx Channel 0 True Input.
B19	RX_1+	Rx input	Rx Channel 1 True Input.
B20	RX_2+	Rx input	Rx Channel 2 True Input.
B21	GND	GND	Ground.
B22	COMP1	Miscellaneous analog[1]	Compensation Pin. Connect a 2.2 nF capacitor from COMP1 to AVDD2.
B23	DAC4	Analog video output	Encoder DAC4 Output.
C1	OSD_IN[19]/EXT_DIN[3]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 19 (OSD_IN[19]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[3]).
C2	OSD_IN[20]/EXT_DIN[4]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 20 (OSD_IN[20]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[4]).
C3	GND	GND	Ground.
C4	AUD_IN[4]	Audio input	I²S3/DSD4 Audio Input.
C5	DSD_CLK	Audio input	DSD Audio Clock Input.
C6	SCLK	Audio input	I²S Bit Clock Input.
C7	SCL	I²C control	I²C Clock Input. SCL is open drain; use a 4.7 kΩ resistor to connect this pin to a 3.3 V supply.
C8	SCK1	Serial port control	Serial Clock (Serial Port 1). Serial Port 1 is used for OSD control.
C9	GND	GND	Ground.
C10	INT0	Miscellaneous digital	Interrupt Pin 0. When the status bits change, this pin is triggered.
C11	PDN	Miscellaneous digital	Power-Down. This pin controls the power state of the ADV8005.
C12	GND	GND	Ground.
C13	GND	GND	Ground.

Pin No.	Mnemonic	Type	Description
C14	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
C15	REF_CLK	Digital input	Reference Clock Input for the Master Timing Block.
C16	RX_HPD	Rx input	Hot Plug Assert Signal Output for the Rx Input.
C17	AVDD1	Power	HDMI Rx Inputs Analog Supply (3.3 V).
C18	GND	GND	Ground.
C19	GND	GND	Ground.
C20	AVDD1	Power	HDMI Rx Inputs Analog Supply (3.3 V).
C21	AVDD1	Power	HDMI Rx Inputs Analog Supply (3.3 V).
C22	DAC5	Analog video output	Encoder DAC5 Output.
C23	DAC6	Analog video output	Encoder DAC6 Output.
D1	OSD_IN[16]/EXT_DIN[0]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 16 (OSD_IN[16]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[0]).
D2	OSD_IN[17]/EXT_DIN[1]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 17 (OSD_IN[17]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[1]).
D3	OSD_IN[18]/EXT_DIN[2]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 18 (OSD_IN[18]). Additional TTL Input for External ITU-R BT.656 Video Data (EXT_DIN[2]).
D4	GND	GND	Ground.
D5	DVDD_IO	Power	Digital Interface Supply (3.3 V).
D6	MCLK	Audio input	Master Clock for S/PDIF Input Audio.
D7	SDA	I^2C control	I^2C Data Input. SDA is open drain; use a 4.7 kΩ resistor to connect this pin to a 3.3 V supply.
D8	$\overline{CS1}$	Serial port control	Chip Select (Serial Port 1). Serial Port 1 is used for OSD control.
D9	GND	GND	Ground.
D10	INT1	Miscellaneous digital	Interrupt Pin for HDMI Transmitter Outputs. When the status bits change, an interrupt is generated on this pin.
D11	INT2	Miscellaneous digital	Interrupt Pin for HDMI Receiver Inputs. When the status bits change, an interrupt is generated on this pin.
D12	DVDD_IO	Power	Digital Interface Supply (3.3 V).
D13	TEST1	Miscellaneous digital	Test Pin. Float this pin.
D14	REF_HS	Digital input	Reference Horizontal Sync Input for the Master Timing Block.
D15	REF_VS	Digital input	Reference Vertical Sync Input for the Master Timing Block.
D16	RX_5V	Rx input	5 V Detect Pin for the Receiver Input.
D17	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
D18	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
D19	RTERM	HDMI Rx input	This pin sets the internal termination resistance. Use a 500 Ω resistor between this pin and GND. Place the RTERM resistor as close as possible to the ADV8005.
D20	AVDD2	Power	Analog Power Supply (3.3 V).
D21	AVDD2	Power	Analog Power Supply (3.3 V).
D22	DAC1	Analog video output	Encoder DAC1 Output.
D23	DAC2	Analog video output	Encoder DAC2 Output.
E1	OSD_IN[13]/VBI_SCK	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 13 (OSD_IN[13]). Serial Clock for Video Blanking Interval (VBI) Data Serial Port 3 (VBI_SCK).
E2	OSD_IN[14]/VBI_MOSI	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 14 (OSD_IN[14]). Master Output Slave Input for VBI Data Serial Port 3 (VBI_MOSI).
E3	OSD_IN[15]/VBI_$\overline{CS}$	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 15 (OSD_IN[15]). Chip Select for VBI Data Serial Port 3(VBI_$\overline{CS}$).
E4	DVDD_IO	Power	Digital Interface Supply (3.3 V).
E20	TEST2	Miscellaneous analog	Test Pin. Float this pin.
E21	GND	GND	Ground.
E22	COMP2	Miscellaneous analog[1]	Compensation Pin. Connect a 2.2 nF capacitor to AVDD2.
E23	DAC3	Analog video output	Encoder DAC3 Output.
F1	OSD_IN[9]	OSD video input	External OSD Video Pixel Input Port 9.
F2	OSD_IN[10]	OSD video input	External OSD Video Pixel Input Port 10.
F3	OSD_IN[11]	OSD video input	External OSD Video Pixel Input Port 11.
F4	OSD_IN[12]	OSD video input/ miscellaneous digital	External OSD Video Pixel Input Port 12.
F20	RSET2	Miscellaneous analog[1]	Resistor Current Setting for DAC4, DAC5, and DAC6. Place the RSET2 resistor as close as possible to the ADV8005.
F21	PVDD3	Power	PLL Supply (1.8 V).

Pin No.	Mnemonic	Type	Description
F22	GND	GND	Ground.
F23	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
G1	OSD_IN[5]	OSD video input	External OSD Video Pixel Input Port 5.
G2	OSD_IN[6]	OSD video input	External OSD Video Pixel Input Port 6.
G3	OSD_IN[7]	OSD video input	External OSD Video Pixel Input Port 7.
G4	OSD_IN[8]	OSD video input	External OSD Video Pixel Input Port 8.
G7	GND	GND	Ground.
G8	GND	GND	Ground.
G9	GND	GND	Ground.
G10	DVDD	Power	Digital Power Supply (1.8 V).
G11	GND	GND	Ground.
G12	GND	GND	Ground.
G13	DVDD	Power	Digital Power Supply (1.8 V).
G14	GND	GND	Ground.
G15	GND	GND	Ground.
G16	GND	GND	Ground.
G17	GND	GND	Ground.
G20	ELPF1	Miscellaneous analog[1]	External Loop Filter for PLL 1. Connect to PVDD3.
G21	ELPF2	Miscellaneous analog[1]	External Loop Filter for PLL 2. Connect to PVDD3.
G22	GND	GND	Ground.
G23	AVDD3	Power	HDMI Tx1 Analog Power Supply (1.8 V).
H1	OSD_IN[1]	OSD video input	External OSD Video Pixel Input Port 1.
H2	OSD_IN[2]	OSD video input	External OSD Video Pixel Input Port 2.
H3	OSD_IN[3]	OSD video input	External OSD Video Pixel Input Port 3.
H4	OSD_IN[4]	OSD video input	External OSD Video Pixel Input Port 4.
H7	GND	GND	Ground.
H8	GND	GND	Ground.
H9	GND	GND	Ground.
H10	GND	GND	Ground.
H11	GND	GND	Ground.
H12	GND	GND	Ground.
H13	GND	GND	Ground.
H14	GND	GND	Ground.
H15	GND	GND	Ground.
H16	GND	GND	Ground.
H17	GND	GND	Ground.
H20	GND	GND	Ground.
H21	GND	GND	Ground.
H22	TX1_2+	HDMI Tx1	HDMI1 Channel 2 True Output.
H23	TX1_2−	HDMI Tx1	HDMI1 Channel 2 Complement Output.
J1	DE	Digital video sync	Data Enable for Digital Input Video.
J2	HS	Digital video sync	Horizontal Sync for Digital Input Video.
J3	OSD_HS	Digital video sync	Horizontal Sync for the OSD Input Port.
J4	OSD_IN[0]	OSD video input	External OSD Video Pixel Input Port 0.
J7	DVDD	Power	Digital Power Supply (1.8 V).
J8	GND	GND	Ground.
J9	GND	GND	Ground.
J10	GND	GND	Ground.
J11	GND	GND	Ground.
J12	GND	GND	Ground.
J13	GND	GND	Ground.
J14	GND	GND	Ground.
J15	GND	GND	Ground.
J16	GND	GND	Ground.
J17	DVDD	Power	Digital Power Supply (1.8 V).

Pin No.	Mnemonic	Type	Description
J20	DDC1_SDA	HDMI Tx1	HDCP Slave Serial Data for HDMI Tx1. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI transmitter 5 V supply.
J21	GND	GND	Ground.
J22	TX1_1+	HDMI Tx1	HDMI1 Channel 1 True Output.
J23	TX1_1−	HDMI Tx1	HDMI1 Channel 1 Complement Output.
K1	VS	Digital video sync	Vertical Sync for Digital Input Video.
K2	PCLK	Digital video sync	Pixel Clock for Digital Input Video.
K3	DVDD_IO	Power	Digital Interface Supply (3.3 V).
K4	DVDD_IO	Power	Digital Interface Supply (3.3 V).
K7	GND	GND	Ground.
K8	GND	GND	Ground.
K9	GND	GND	Ground.
K10	GND	GND	Ground.
K11	GND	GND	Ground.
K12	GND	GND	Ground.
K13	GND	GND	Ground.
K14	GND	GND	Ground.
K15	GND	GND	Ground.
K16	GND	GND	Ground.
K17	GND	GND	Ground.
K20	DDC1_SCL	HDMI Tx1	HDCP Slave Serial Clock for HDMI Tx1. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI transmitter 5 V supply.
K21	GND	GND	Ground.
K22	TX1_0+	HDMI Tx1	HDMI1 Channel 0 True Output.
K23	TX1_0−	HDMI Tx1	HDMI1 Channel 0 Complement Output.
L1	P[32]	Digital video input	Digital Video Input 32 of Bus (P[35] to P[0]).
L2	P[33]	Digital video input	Digital Video Input 33 of Bus (P[35] to P[0]).
L3	P[34]	Digital video input	Digital Video Input 34 of Bus (P[35] to P[0]).
L4	P[35]	Digital video input	Digital Video Input 35 of Bus (P[35] to P[0]).
L7	DVDD	Power	Digital Power Supply (1.8 V).
L8	GND	GND	Ground.
L9	GND	GND	Ground.
L10	GND	GND	Ground.
L11	GND	GND	Ground.
L12	GND	GND	Ground.
L13	GND	GND	Ground.
L14	GND	GND	Ground.
L15	GND	GND	Ground.
L16	GND	GND	Ground.
L17	GND	GND	Ground.
L20	HPD_TX1	HDMI Tx1	Hot Plug Assert Signal Input for HDMI Tx1.
L21	GND	GND	Ground.
L22	TX1_C+	HDMI Tx1	HDMI1 Clock True Output.
L23	TX1_C−	HDMI Tx1	HDMI1 Clock Complement Output.
M1	P[28]	Digital video input	Digital Video Input 28 of Bus (P[35] to P[0]).
M2	P[29]	Digital video input	Digital Video Input 29 of Bus (P[35] to P[0]).
M3	P[30]	Digital video input	Digital Video Input 30 of Bus (P[35] to P[0]).
M4	P[31]	Digital video input	Digital Video Input 31 of Bus (P[35] to P[0]).
M7	GND	GND	Ground.
M8	GND	GND	Ground.
M9	GND	GND	Ground.
M10	GND	GND	Ground.
M11	GND	GND	Ground.
M12	GND	GND	Ground.
M13	GND	GND	Ground.
M14	GND	GND	Ground.

Pin No.	Mnemonic	Type	Description
M15	GND	GND	Ground.
M16	GND	GND	Ground.
M17	GND	GND	Ground.
M20	R_TX1	HDMI Tx1[1]	This pin sets the internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8005.
M21	PVDD5	Power[1]	HDMI Transmitter PLL Power Supply (1.845 V).
M22	HEAC_1+	HDMI Tx1	HDMI Ethernet and Audio Channel Positive Tx1 from the HDMI Connector.
M23	HEAC_1−	HDMI Tx1	HDMI Ethernet and Audio Channel Negative Tx1 from the HDMI Connector.
N1	P[24]	Digital video input	Digital Video Input 24 of Bus (P[35] to P[0]).
N2	P[25]	Digital video input	Digital Video Input 25 of Bus (P[35] to P[0]).
N3	P[26]	Digital video input	Digital Video Input 26 of Bus (P[35] to P[0]).
N4	P[27]	Digital video input	Digital Video Input 27 of Bus (P[35] to P[0]).
N7	GND	GND	Ground.
N8	GND	GND	Ground.
N9	GND	GND	Ground.
N10	GND	GND	Ground.
N11	GND	GND	Ground.
N12	GND	GND	Ground.
N13	GND	GND	Ground.
N14	GND	GND	Ground.
N15	GND	GND	Ground.
N16	GND	GND	Ground.
N17	GND	GND	Ground.
N20	DNC	Not applicable	Do Not Connect. Do not connect to this pin.
N21	PVDD5	Power[1]	HDMI Transmitter PLL Power Supply (1.845 V).
N22	AVDD4	Power	HDMI Tx2 Analog Power Supply (1.8 V).
N23	AVDD3	Power	HDMI Tx1 Analog Power Supply (1.8 V).
P1	P[20]	Digital video input	Digital Video Input 20 of Bus (P[35] to P[0]).
P2	P[21]	Digital video input	Digital Video Input 21 of Bus (P[35] to P[0]).
P3	P[22]	Digital video input	Digital Video Input 22 of Bus (P[35] to P[0]).
P4	P[23]	Digital video input	Digital Video Input 23 of Bus (P[35] to P[0]).
P7	DVDD	Power	Digital Power Supply (1.8 V).
P8	GND	GND	Ground.
P9	GND	GND	Ground.
P10	GND	GND	Ground.
P11	GND	GND	Ground.
P12	GND	GND	Ground.
P13	GND	GND	Ground.
P14	GND	GND	Ground.
P15	GND	GND	Ground.
P16	GND	GND	Ground.
P17	DVDD	Power	Digital Power Supply (1.8 V).
P20	DDC2_SCL	HDMI Tx2	HDCP Slave Serial Clock for HDMI Tx2. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI transmitter 5 V supply.
P21	GND	GND	Ground.
P22	TX2_2+	HDMI Tx2	HDMI2 Channel 2 True Output.
P23	TX2_2−	HDMI Tx2	HDMI2 Channel 2 Complement Output.
R1	P[16]	Digital video input	Digital Video Input 16 of Bus (P[35] to P[0]).
R2	P[17]	Digital video input	Digital Video Input 17 of Bus (P[35] to P[0]).
R3	P[18]	Digital video input	Digital Video Input 18 of Bus (P[35] to P[0]).
R4	P[19]	Digital video input	Digital Video Input 19 of Bus (P[35] to P[0]).
R7	GND	GND	Ground.
R8	GND	GND	Ground.
R9	GND	GND	Ground.
R10	GND	GND	Ground.
R11	GND	GND	Ground.

Pin No.	Mnemonic	Type	Description
R12	GND	GND	Ground.
R13	GND	GND	Ground.
R14	GND	GND	Ground.
R15	GND	GND	Ground.
R16	GND	GND	Ground.
R17	GND	GND	Ground.
R20	DDC2_SDA	HDMI Tx2	HDCP Slave Serial Data for HDMI Tx2. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI transmitter 5 V supply.
R21	GND	GND	Ground.
R22	TX2_1+	HDMI Tx2	HDMI2 Channel 1 True Output.
R23	TX2_1−	HDMI Tx2	HDMI2 Channel 1 Complement Output.
T1	P[14]	Digital video input	Digital Video Input 14 of Bus (P[35] to P[0]).
T2	P[15]	Digital video input	Digital Video Input 15 of Bus (P[35] to P[0]).
T3	GND	GND	Ground.
T4	GND	GND	Ground.
T7	GND	GND	Ground.
T8	GND	GND	Ground.
T9	GND	GND	Ground.
T10	GND	GND	Ground.
T11	GND	GND	Ground.
T12	GND	GND	Ground.
T13	GND	GND	Ground.
T14	GND	GND	Ground.
T15	GND	GND	Ground.
T16	GND	GND	Ground.
T17	GND	GND	Ground.
T20	HPD_TX2	HDMI Tx2	Hot Plug Assert Signal Input for HDMI Tx2.
T21	GND	GND	Ground.
T22	TX2_0+	HDMI Tx2	HDMI2 Channel 0 True Output.
T23	TX2_0−	HDMI Tx2	HDMI2 Channel 0 Complement Output.
U1	P[10]	Digital video input	Digital Video Input 10 of Bus (P[35] to P[0]).
U2	P[11]	Digital video input	Digital Video Input 11 of Bus (P[35] to P[0]).
U3	P[12]	Digital video input	Digital Video Input 12 of Bus (P[35] to P[0]).
U4	P[13]	Digital video input	Digital Video Input 13 of Bus (P[35] to P[0]).
U7	GND	GND	Ground.
U8	GND	GND	Ground.
U9	DVDD	Power	Digital Power Supply (1.8 V).
U10	GND	GND	Ground.
U11	GND	GND	Ground.
U12	DVDD	Power	Digital Power Supply (1.8 V).
U13	GND	GND	Ground.
U14	GND	GND	Ground.
U15	DVDD	Power	Digital Power Supply (1.8 V).
U16	GND	GND	Ground.
U17	GND	GND	Ground.
U20	R_TX2	HDMI Tx2[1]	This pin sets the internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8005.
U21	GND	GND	Ground.
U22	TX2_C+	HDMI Tx2[1]	HDMI2 Clock True Output.
U23	TX2_C−	HDMI Tx2[1]	HDMI2 Clock Complement Output.
V1	P[6]	Digital video input	Digital Video Input 6 of Bus (P[35] to P[0]).
V2	P[7]	Digital video input	Digital Video Input 7 of Bus (P[35] to P[0]).
V3	P[8]	Digital video input	Digital Video Input 8 of Bus (P[35] to P[0]).
V4	P[9]	Digital video input	Digital Video Input 9 of Bus (P[35] to P[0]).
V20	GND	GND	Ground.
V21	PVDD6	Power[1]	HDMI Transmitter PLL Power Supply (1.845 V).

Pin No.	Mnemonic	Type	Description
V22	HEAC_2+	HDMI Tx2	HDMI Ethernet and Audio Channel Positive Tx2 from the HDMI Connector.
V23	HEAC_2−	HDMI Tx2	HDMI Ethernet and Audio Channel Negative Tx2 from the HDMI Connector.
W1	P[2]	Digital video input	Digital Video Input 2 of Bus (P[35] to P[0]).
W2	P[3]	Digital video input	Digital Video Input 3 of Bus (P[35] to P[0]).
W3	P[4]	Digital video input	Digital Video Input 4 of Bus (P[35] to P[0]).
W4	P[5]	Digital video input	Digital Video Input 5 of Bus (P[35] to P[0]).
W20	TEST3	Miscellaneous digital	Test Pin. Connect this pin to ground through a 0.1 µF capacitor.
W21	PVDD6	Power[1]	HDMI Transmitter PLL Power Supply (1.845 V).
W22	AVDD4	Power	HDMI Tx2 Analog Power Supply (1.8 V).
W23	AVDD4	Power	HDMI Tx2 Analog Power Supply (1.8 V).
Y1	P[0]	Digital video input	Digital Video Input 0 of Bus (P[35] to P[0]).
Y2	P[1]	Digital video input	Digital Video Input 1 of Bus (P[35] to P[0]).
Y3	DDR_DQS[2]	DDR interface	Data Strobe for DDR Data Bytes[23:16], True.
Y4	GND	GND	Ground.
Y5	DDR_DQ[23]	DDR interface	Data Line 23. Interface to external RAM data lines.
Y6	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
Y7	DDR_DQS[3]	DDR interface	Data Strobe for DDR Data Bytes[31:24], True.
Y8	GND	GND	Ground.
Y9	DDR_A[11]	DDR interface	Address Line 11. Interface to external RAM address lines.
Y10	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
Y11	DDR_A[4]	DDR interface	Address Line 4. Interface to external RAM address lines.
Y12	GND	GND	Ground.
Y13	$\overline{\text{DDR\_CAS}}$	DDR interface	Column Address Strobe for DDR Memory.
Y14	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
Y15	DDR_$\overline{\text{CK}}$	DDR interface	DDR Memory Clock. Interface to external DDR RAM clock lines.
Y16	GND	GND	Ground.
Y17	DDR_DQ[9]	DDR interface	Data Line 9. Interface to external RAM data lines.
Y18	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
Y19	DDR_DQ[14]	DDR interface	Data Line 14. Interface to external RAM data lines.
Y20	GND	GND	Ground.
Y21	DDR_DQ[6]	DDR interface	Data Line 6. Interface to external RAM data lines.
Y22	PVDD_DDR	Power	DDR Interface PLL Supply (1.8 V).
Y23	GND	GND	Ground.
AA1	DDR_DQ[18]	DDR interface	Data Line 18. Interface to external RAM data lines.
AA2	GND	GND	Ground.
AA3	GND	GND	Ground.
AA4	$\overline{\text{DDR\_DQS[2]}}$	DDR interface	Data Strobe for DDR Data Bytes[23:16], Complement.
AA5	DDR_DQ[26]	DDR interface	Data Line 26. Interface to external RAM data lines.
AA6	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
AA7	$\overline{\text{DDR\_DQS[3]}}$	DDR interface	Data Strobe for DDR Data Bytes[31:24], Complement.
AA8	DDR_A[13]	DDR interface	Address Line 13. Interface to external RAM address lines. For designs that must maintain consistency with the ADV8002 or the ADV8003, this pin can be grounded or left unconnected.
AA9	DDR_A[8]	DDR interface	Address Line 8. Interface to external RAM address lines.
AA10	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
AA11	DDR_A[2]	DDR interface	Address Line 2. Interface to external RAM address lines.
AA12	GND	GND	Ground.
AA13	DDR_$\overline{\text{CS}}$	DDR interface	DDR Chip Select. Interface to external DDR RAM chip selects.
AA14	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
AA15	DDR_CK	DDR interface	DDR Memory Clock. Interface to external DDR RAM clock lines.
AA16	GND	GND	Ground.
AA17	DDR_DQ[11]	DDR interface	Data Line 11. Interface to external RAM data lines.
AA18	DVDD_DDR	Power	DDR Interface Supply (1.8 V).
AA19	DDR_DM[1]	DDR interface	Data Mask for Data Lines[15:8].
AA20	DDR_DM[0]	DDR interface	Data Mask for Data Lines[7:0].
AA21	GND	GND	Ground.