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3-Axis, ±1.5 *g*/±3 *g*/±6 *g*/±12 *g* Digital Accelerometer

Data Sheet **ADXL312**

FEATURES

- **Ultralow power: as low as 57 µA in measurement mode and 0.1 µA in standby mode at V_S = 3.3 V (typical)**
- **Power consumption scales automatically with bandwidth**
- **User-selectable resolution**
  - **Fixed 10-bit resolution**
  - **Full resolution, where resolution increases with *g* range, up to 13-bit resolution at ±12 *g* (maintaining 2.9 mg/LSB scale factor in all *g* ranges)**
- **Embedded FIFO technology minimizes host processor load**
- **Built-in motion detection functions for activity/inactivity monitoring**
- **Supply and I/O voltage range: 2.0 V to 3.6 V**
- **SPI (3- and 4-wire) and I²C digital interfaces**
- **Flexible interrupt modes mappable to either interrupt pin**
- **Measurement ranges selectable via serial command**
- **Bandwidth selectable via serial command**
- **Wide temperature range (−40 to +105°C)**
- **10,000 *g* shock survival**
- **Pb free/RoHS compliant**
- **Small and thin: 5 mm × 5 mm × 1.45 mm LFCSP package**
- **Qualified for automotive applications**

APPLICATIONS

- **Car alarm**
- **Hill start aid (HSA)**
- **Electronic parking brake**
- **Data recorder (black box)**

GENERAL DESCRIPTION

The ADXL312[1] is a small, thin, low power, 3-axis accelerometer with high resolution (13-bit) measurement up to ±12 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either a serial port interface (SPI) (3- or 4-wire) or I²C digital interface.

The ADXL312 is well suited for car alarm or black box applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (2.9 mg/LSB) enables resolution of inclination changes of as little as 0.25°. A built-in FIFO facilitates using oversampling techniques to improve resolution to as little as 0.05° of inclination.

Several special sensing functions are provided. Activity and inactivity sensing detects the presence or absence of motion and whether the acceleration on any axis exceeds a user-set level. These functions can be mapped to interrupt output pins. An integrated 32 level FIFO can be used to store data to minimize host processor intervention.

Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

The ADXL312 is supplied in a small, thin 5 mm × 5 mm × 1.45 mm, 32-lead, LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

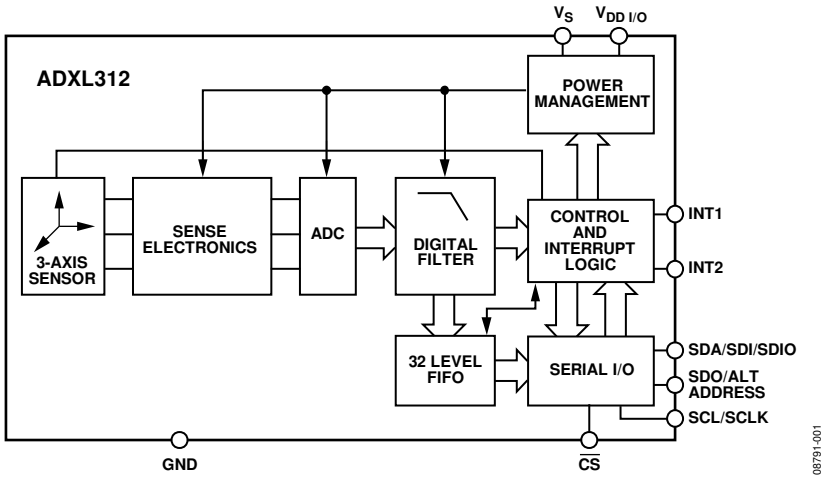

Figure 1. ADXL312 Simplified Block Diagram

[1] Protected by U.S. Patent 8,156,264B2.

Rev. B Document Feedback

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Last Content Update: 04/28/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADXL312Z Breakout Board
- Real Time Eval System for Digital Output Sensor

DOCUMENTATION

Data Sheet

- ADXL312: 3-Axis, ±1.5 *g*/±3 *g*/±6 *g*/±12 *g* Digital Accelerometer Data Sheet

User Guides

- UG-209: ADXL312 Sensor Evaluation System
- UG-281: ADXL312 Quick Start User Guide

DESIGN RESOURCES

- ADXL312 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL312 EngineerZone Discussions.

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REVISION HISTORY

4/2017—Rev. A to Rev. B

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Updated Outline Dimensions ... 31
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7/2015—Rev. 0 to Rev. A

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Added Serial Port I/O Default States Section ... 12
Added Preventing Bus Traffic Errors Section and Figure 23; Renumbered Sequentially ... 13
Changes to FIFO Section ... 18
Changes to Figure 41 ... 31

12/2010—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +105°C, V_S = $V_{DD\ I/O}$ = 3.3 V, acceleration = 0 *g*, unless otherwise noted.

Table 1. Specifications[1]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±1.5, 3, 6, 12		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Inter-Axis Alignment Error			±0.1		Degrees
Cross-Axis Sensitivity[2]			±1		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges	Default resolution		10		Bits
±1.5 *g* Range	Full resolution enabled		10		Bits
±3 *g* Range	Full resolution enabled		11		Bits
±6 *g* Range	Full resolution enabled		12		Bits
±12 *g* Range	Full resolution enabled		13		Bits
SENSITIVITY	Each axis				
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±1.5 *g*, 10-bit or full resolution	2.6	2.9	3.2	m*g*/LSB
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±3 *g*, 10-bit resolution	5.2	5.8	6.4	m*g*/LSB
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±6 *g*, 10-bit resolution	10.4	11.6	12.8	m*g*/LSB
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±12 *g*, 10-bit resolution	20.9	23.2	25.5	m*g*/LSB
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±1.5 *g*, 10-bit or full resolution	312	345	385	LSB/*g*
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±3 *g*, 10-bit resolution	156	172	192	LSB/*g*
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±6 *g*, 10-bit resolution	78	86	96	LSB/*g*
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±12 *g*, 10-bit resolution	39	43	48	LSB/*g*
Sensitivity Change Due to Temperature			±0.01		%/°C
0 *g* BIAS LEVEL	Each axis				
Initial 0 *g* Output	T = 25°C, X_{OUT}, Y_{OUT}	−150		+150	m*g*
Initial 0 *g* Output	T = 25°C, Z_{OUT}	−250		+250	m*g*
0 *g* Output over Temperature	−40°C < T < 105°C, X_{OUT}, Y_{OUT}, Z_{OUT}	−250		+250	m*g*
0 *g* Offset Tempco	X_{OUT}, Y_{OUT}		±0.8		m*g*/°C
0 *g* Offset Tempco	Z_{OUT}		±1.5		m*g*/°C
NOISE PERFORMANCE					
Noise Density (X-, Y-axes)		200	340	440	µ*g*/√Hz
Noise Density (Z-axis)		200	470	595	µ*g*/√Hz
OUTPUT DATA RATE/BANDWIDTH	User selectable				
Measurement Rate[3]		6.25		3200	Hz
SELF-TEST[4]	Data rate ≥ 100 Hz, 2.0 ≤ V_S ≤ 3.6				
Output Change in X-Axis		0.20		2.10	*g*
Output Change in Y-Axis		−2.10		−0.20	*g*
Output Change in Z-Axis		0.30		3.40	*g*

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (V_S)		2.0		3.6	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7		V_S	V
Supply Current	Data rate > 100 Hz	100	170	300	μA
	Data rate < 10 Hz	30	55	110	μA
Standby Mode Leakage Current	T = 25°C		0.1	2	μA
	Over entire operating temperature range			17	μA
Turn-On (Wake-Up) Time[5]			1.4		ms
TEMPERATURE					
Operating Temperature Range		−40		+105	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.
[2] Cross-axis sensitivity is defined as coupling between any two axes.
[3] Bandwidth is half the output data rate.
[4] Self-test change is defined as the output (*g*) when the SELF_TEST bit = 1 (in the DATA_FORMAT register) minus the output (*g*) when the SELF_TEST bit = 0 (in the DATA_FORMAT register). Due to device filtering, the output reaches its final value after 4 × τ when enabling or disabling self-test, where τ = 1/(data rate).
[5] Turn-on and wake-up times are determined by the user-defined bandwidth. At a 100 Hz data rate, the turn-on and wake-up times are each approximately 11.1 ms. For other data rates, the turn-on and wake-up times are each approximately τ + 1.1 in milliseconds, where τ = 1/(data rate).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	10,000 *g*
Any Axis, Powered	10,000 *g*
V_S	−0.3 V to 3.9 V
$V_{DD\ I/O}$	−0.3 V to 3.9 V
All Other Pins	−0.3 V to $V_{DD\ I/O}$ + 0.3 V or 3.9 V, whichever is less
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Temperature Range	
Powered	−40°C to +125°C
Storage	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP Package	27.27	30	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

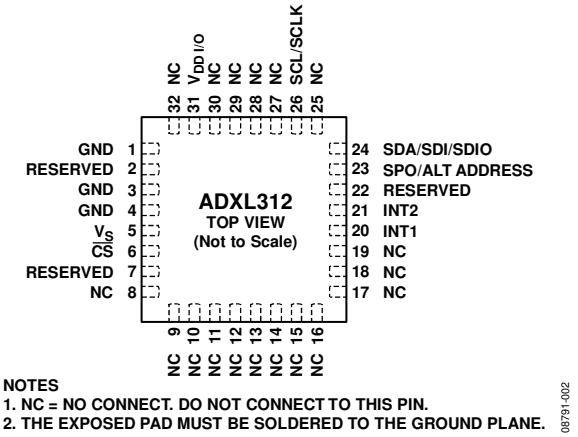


Figure 2. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	This pin must be connected to ground.
2	Reserved	Reserved. This pin must be connected to V_S or left open.
3	GND	This pin must be connected to ground.
4	GND	This pin must be connected to ground.
5	V_S	Supply Voltage.
6	$\overline{CS}$	Chip Select.
7	Reserved	Reserved. This pin must be left open.
8 to19	NC	No Connect. Do not connect to this pin.
20	INT1	Interrupt 1 Output.
21	INT2	Interrupt 2 Output.
22	Reserved	Reserved. This pin must be connected to GND.
23	SDO/ALT ADDRESS	Serial Data Out, Alternate I^2C Address Select.
24	SDA/SDI/SDIO	Serial Data (I^2C), Serial Data In (SPI 4-Wire), Serial Data In/Out (SPI 3-Wire).
25	NC	No Connect. Do not connect to this pin.
26	SCL/SCLK	Serial Communications Clock.
27 to 30	NC	No Connect. Do not connect to this pin.
31	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
32	NC	No Connect.
	EP	The exposed pad must be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

N > 1000, unless otherwise noted.

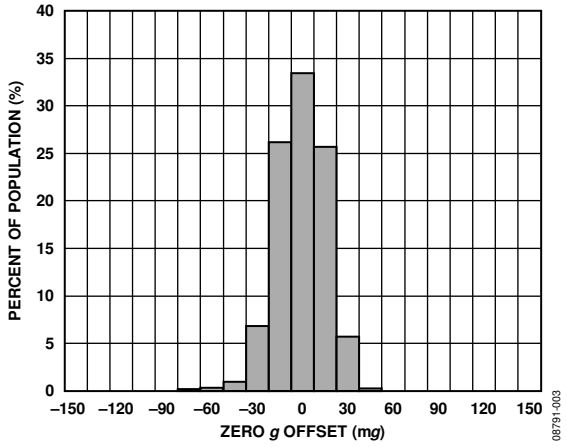


Figure 3. X-Axis Zero-g Bias. 25°C, $V_S = V_{DD\ I/O} = 3.3$ V

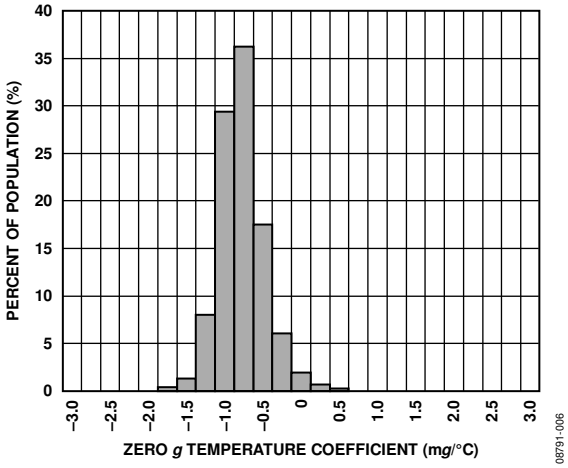


Figure 6. X-Axis Zero-g Bias Drift, $V_S = V_{DD\ I/O} = 3.3$ V

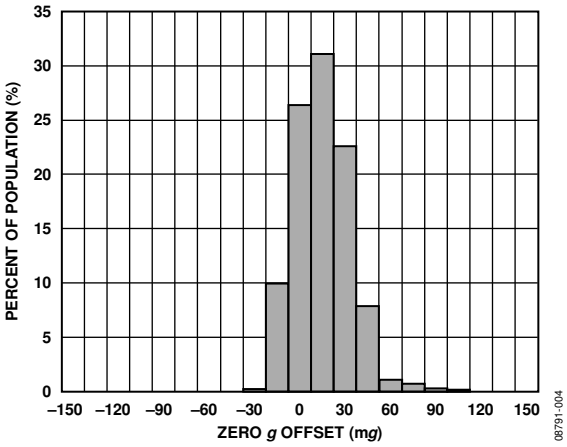


Figure 4. Y Axis Zero-g Bias, 25°C, $V_S = V_{DD\ I/O} = 3.3$ V

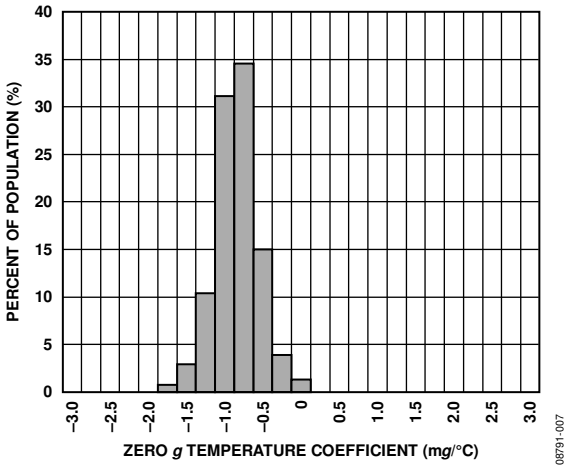


Figure 7. Y-Axis Zero-g Bias Drift, $V_S = V_{DD\ I/O} = 3.3$ V

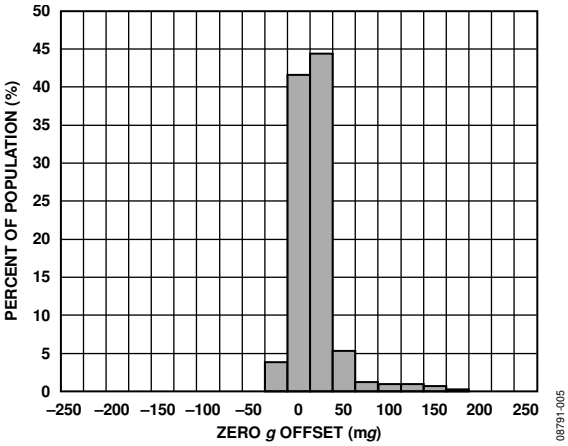


Figure 5. Z Axis Zero-g Bias, 25°C, $V_S = V_{DD\ I/O} = 3.3$ V

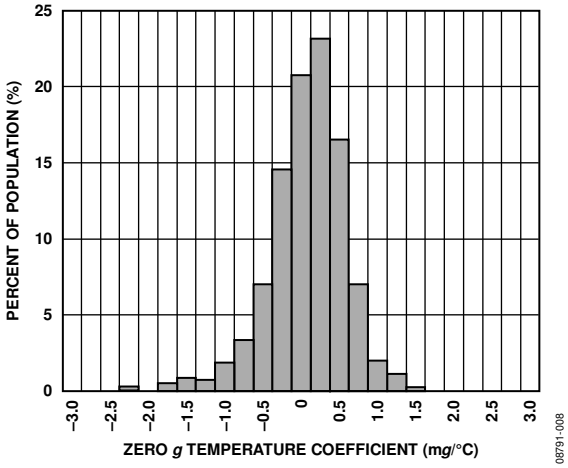


Figure 8. Z-Axis Zero-g Bias Drift, $V_S = V_{DD\ I/O} = 3.3$ V

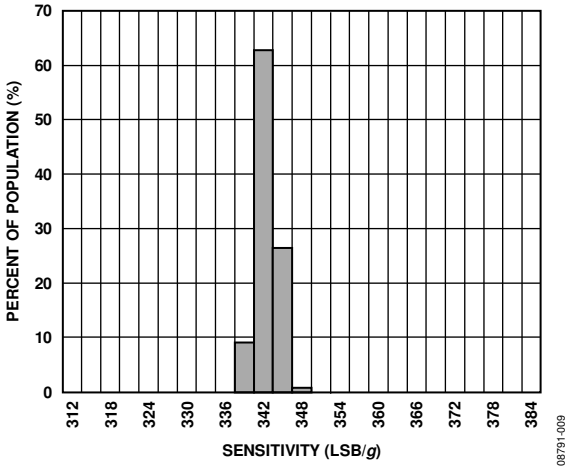


Figure 9. X-Axis Sensitivity, $V_S = V_{DD\ I/O} = 3.3$ V, 25°C

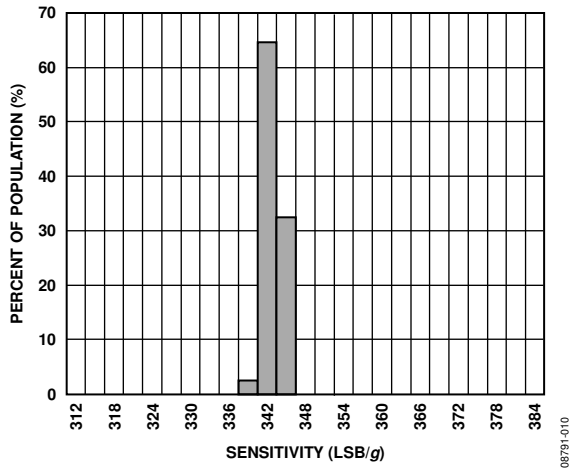


Figure 10. Y-Axis Sensitivity, $V_S = V_{DD\ I/O} = 3.3$ V, 25°C

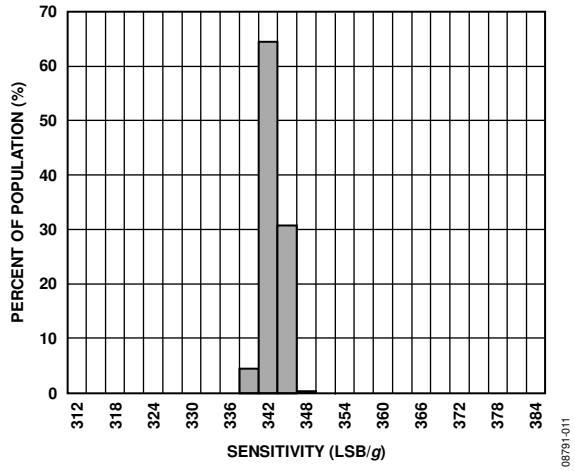


Figure 11. Z-Axis Sensitivity, $V_S = V_{DD\ I/O} = 3.3$ V, 25°C

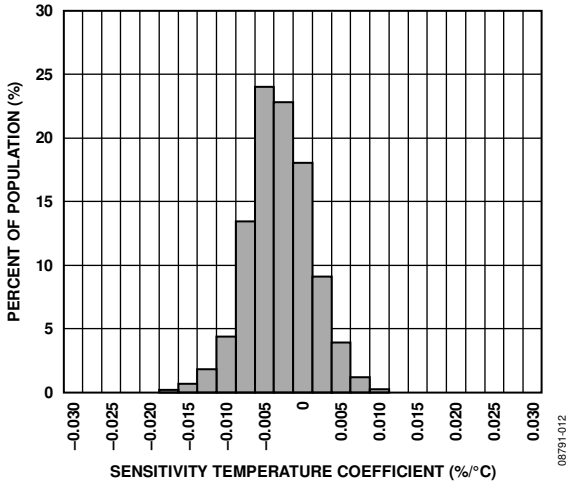


Figure 12. X-Axis Sensitivity Temperature Coefficient, $V_S = V_{DD\ I/O} = 3.3$ V

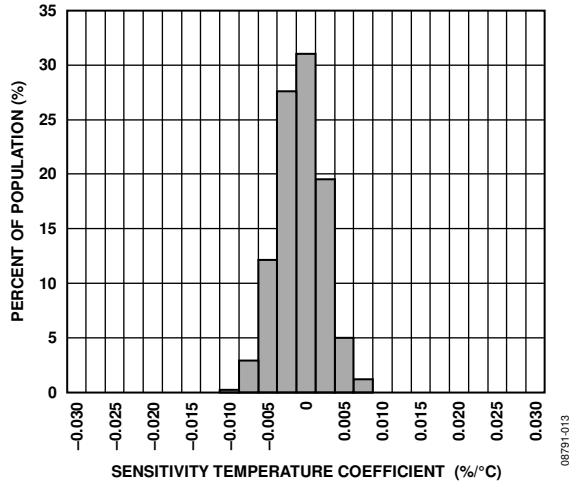


Figure 13. Y-Axis Sensitivity Temperature Coefficient, $V_S = V_{DD\ I/O} = 3.3$ V

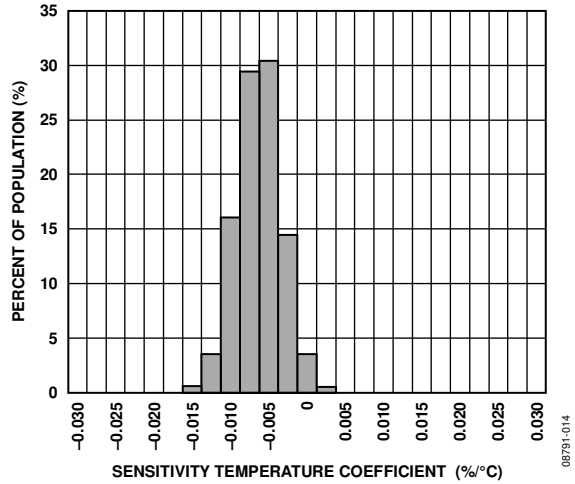


Figure 14. Z-Axis Sensitivity Temperature Coefficient, $V_S = V_{DD\ I/O} = 3.3$ V

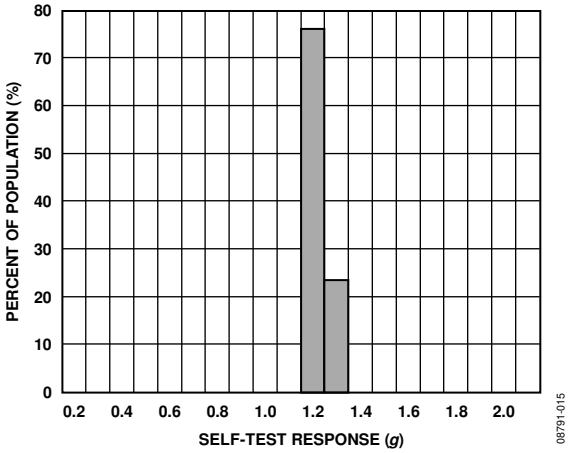


Figure 15. X-Axis Self-Test Delta, $V_S = V_{DD I/O} = 3.3$ V, 25°C

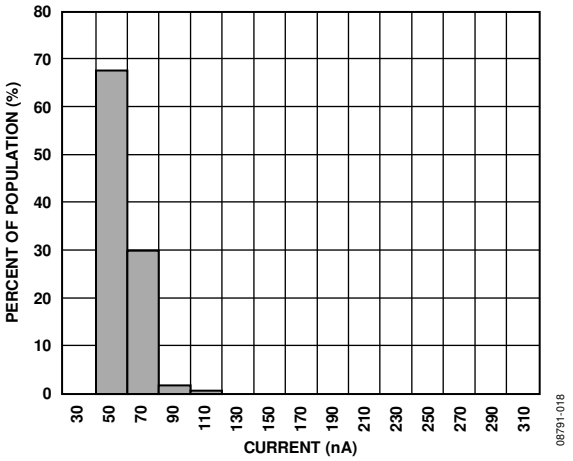


Figure 18. Standby Mode Current Consumption, $V_S = V_{DD I/O} = 3.3$ V, 25°C

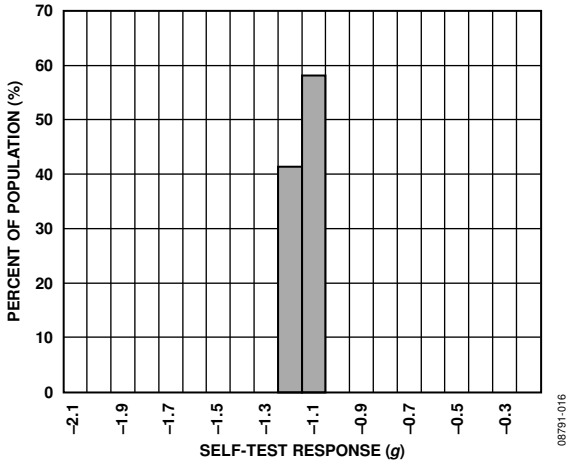


Figure 16. Y-Axis Self-Test Delta, $V_S = V_{DD I/O} = 3.3$ V, 25°C

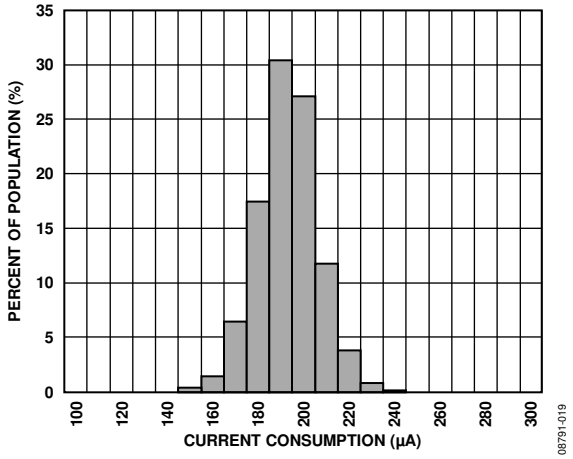


Figure 19. Current Consumption, Measurement Mode, Data Rate = 100 Hz, $V_S = V_{DD I/O} = 3.3$ V, 25°C

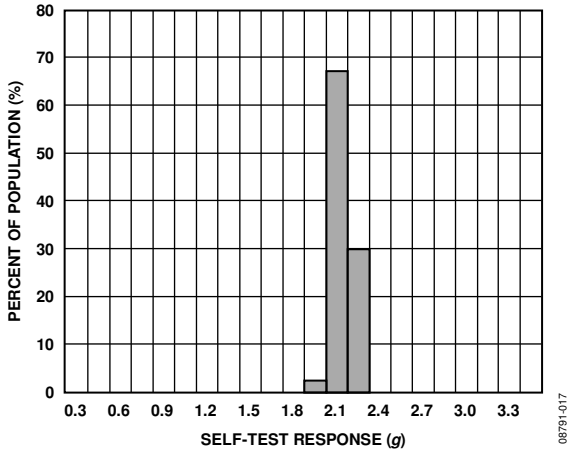


Figure 17. Z-Axis Self-Test Delta, $V_S = V_{DD I/O} = 3.3$ V, 25°C

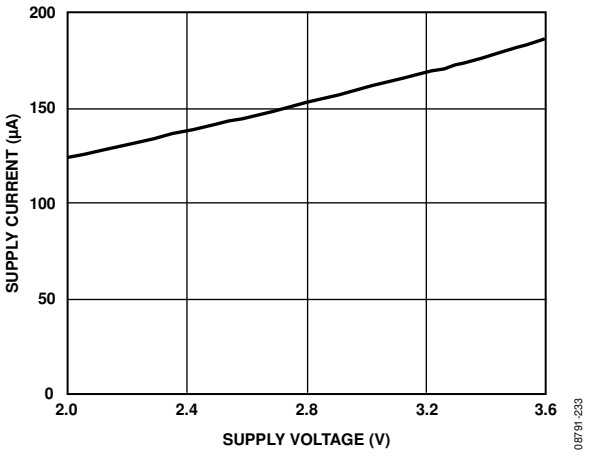


Figure 20. Supply Current vs. Supply Voltage, V_S at 25°C

THEORY OF OPERATION

The ADXL312 is a complete 3-axis acceleration measurement system with a selectable measurement range of ±1.5 *g*, ±3 *g*, ±6 *g*, or ±12 *g*. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as gravity, which allows it to be used as a tilt sensor.

The sensor is a polysilicon surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the beam and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase-sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

POWER SEQUENCING

Power can be applied to V_S or $V_{DD\ I/O}$ in any sequence without damaging the ADXL312. All possible power-on modes are summarized in Table 5. The interface voltage level is set with the interface supply voltage, $V_{DD\ I/O}$, which must be present to ensure that the ADXL312 does not create a conflict on the communication bus. For single-supply operation, $V_{DD\ I/O}$ can be the same as the main supply, V_S. In a dual-supply application, however, $V_{DD\ I/O}$ can differ from V_S to accommodate the desired interface voltage, as long as V_S is greater than or equal to $V_{DD\ I/O}$.

After V_S is applied, the device enters standby mode, where power consumption is minimized and the device waits for $V_{DD\ I/O}$ to be applied and for the command to enter measurement mode to be received. (This command can be initiated by setting the measure bit in the POWER_CTL register (Address 0x2D).) In addition, any register can be written to or read from to configure the part while the device is in standby mode. It is recommended to configure the device in standby mode and then to enable measurement mode. Clearing the measure bit returns the device to the standby mode.

Table 5. Power Sequencing

Condition	V_S	$V_{DD\ I/O}$	Description
Power Off	Off	Off	The device is completely off, but there is a potential for a communication bus conflict.
Bus Disabled	On	Off	The device is on in standby mode, but communication is unavailable and creates a conflict on the communication bus. The duration of this state must be minimized during power-up to prevent a conflict.
Bus Enabled	Off	On	No functions are available, but the device will not create a conflict on the communication bus.
Standby or Measurement	On	On	The device is in standby mode, awaiting a command to enter measurement mode, and all sensor functions are off. After the device is instructed to enter measurement mode, all sensor functions are available.

POWER SAVINGS

Power Modes

The ADXL312 automatically modulates its power consumption in proportion to its output data rate, as outlined in Table 6. If additional power savings is desired, a lower power mode is available. In this mode, the internal sampling rate is reduced, allowing for power savings in the 12.5 Hz to 400 Hz data rate range at the expense of slightly greater noise. To enter low power mode, set the LOW_POWER bit (Bit 4) in the BW_RATE register (Address 0x2C). The current consumption in low power mode is shown in Table 7 for cases where there is an advantage to using low power mode. Use of low power mode for a data rate not shown in Table 7 does not provide any advantage over the same data rate in normal power mode. Therefore, it is recommended that only data rates shown in Table 7 be used in low power mode. The current consumption values shown in Table 6 and Table 7 are for a V_S of 3.3 V.

Table 6. Current Consumption vs. Data Rate
(T_A = 25°C, V_S = $V_{DD\ I/O}$ = 3.3 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
3200	1600	1111	170
1600	800	1110	115
800	400	1101	170
400	200	1100	170
200	100	1011	170
100	50	1010	170
50	25	1001	115
25	12.5	1000	82
12.5	6.25	0111	65
6.25	3.125	0110	57

Table 7. Current Draw vs. Data Rate, Low Power Mode
(T_A = 25°C, V_S = $V_{DD\ I/O}$ = 3.3 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
400	200	1100	115
200	100	1011	82
100	50	1010	65
50	25	1001	57
25	12.5	1000	50
12.5	6.25	0111	43

Autosleep Mode

Additional power savings can be had by having the ADXL312 automatically switch to sleep mode during periods of inactivity. To enable this feature, set the THRESH_INACT register (Address 0x25) to an acceleration threshold value. Levels of acceleration below this threshold are regarded as no activity levels. Set TIME_INACT (Address 0x26) to an appropriate inactivity time period. Then set the AUTO_SLEEP bit and the link bit in the POWER_CTL register (Address 0x2D). If the device does not detect a level of acceleration in excess of THRES_INACT for TIME_INACT seconds, then the device is transitioned to sleep mode automatically. Current consumption at the sub-8 Hz data rates used in this mode is typically 30 μA for a V_S of 3.3 V.

Standby Mode

For even lower power operation, standby mode can be used. In standby mode, current consumption is reduced to 0.1μA (typical). In this mode, no measurements are made. Standby mode is entered by clearing the measure bit (Bit 3) in the POWER_CTL register (Address 0x2D). Placing the device into standby mode preserves the contents of the FIFO.

SERIAL COMMUNICATIONS

The ADXL312 can communicate via I²C and SPI digital communications interfaces. In both cases, the ADXL312 operates as a slave. If I²C is the desired interface for the application, tie the $\overline{CS}$ pin directly to $V_{DD I/O}$ as shown in Figure 27. If SPI is the desired interface for the application, drive the $\overline{CS}$ pin with an external controller, as demonstrated in Figure 21 and Figure 22.

Because the I²C interface is enabled any time the $\overline{CS}$ pin is brought up to $V_{DD I/O}$, there is a potential for bus conflicts to occur when the ADXL312 is implemented into a SPI network. Refer to the Preventing Bus Traffic Errors section for information on how to avoid such conditions. In both SPI and I²C modes of operation, ignore data transmitted from the ADXL312 to the master device during writes to the ADXL312.

Note that throughout this section, multifunction pins, such as SDA/SDI/SDIO, are referred to either by the entire pin name or by a single function of the pin, for example, SDA, when only that function is relevant.

SERIAL PORT I/O DEFAULT STATES

Ensure that all serial port I/Os are in a defined state and that no pin is allowed to float when not in use. This is applicable to all serial port I/Os, regardless of SPI or I²C operation.

For I²C applications, always tie the $\overline{CS}$ pin high to $V_{DD I/O}$. Connect the SCL and SDA pins to an external controller, with pull-up resistors implemented according to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductor. The ALT ADDRESS pin must be tied to either $V_{DD I/O}$ or ground, thereby selecting the desired I²C address for the ADXL312.

If SPI is the intended communications interface, drive the $\overline{CS}$ pin with an external controller, as shown in Figure 21 and Figure 22. When communications with the ADXL312 are suspended ($\overline{CS}$ = $V_{DD I/O}$), ensure that the SCLK, SDI/SDIO, and SDO pins are not floating.

For either SPI or I²C operation, not taking these precautions may result in an inability to communicate with the device or excessive current consumption.

SPI

For the SPI, either 3- or 4-wire configuration is possible, as shown in the connection diagrams in Figure 21 and Figure 22. Clearing the SPI bit in the DATA_FORMAT register (Address 0x31) selects 4-wire mode, whereas setting the SPI bit selects 3-wire mode. The maximum SPI clock speed is 5 MHz with 100 pF maximum loading, and the timing scheme follows clock polarity (CPOL) = 1 and clock phase (CPHA) = 1. If power is applied to the ADXL312 before the clock polarity and phase of the host processor are configured, bring the $\overline{CS}$ pin high before changing the clock polarity and phase.

When using 3-wire SPI, pull the SDO pin up to $V_{DD I/O}$ or down to ground via a 10 kΩ resistor, as shown in Figure 21.

$\overline{CS}$ is the serial port enable line and is controlled by the SPI master. This line must go low at the start of a transmission and high at the end of a transmission, as shown in Figure 24. SCLK is the serial port clock and is supplied by the SPI master. SDI and SDO are the serial data input and output, respectively.

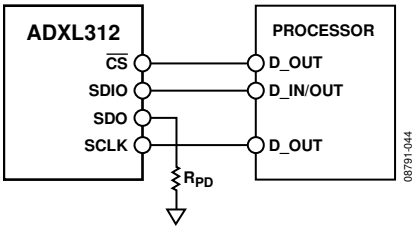


Figure 21. 3-Wire SPI Connection Diagram

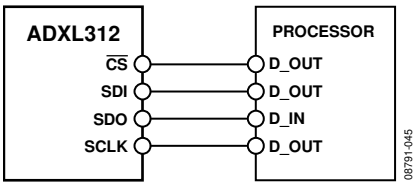


Figure 22. 4-Wire SPI Connection Diagram

To read or write multiple bytes in a single transmission, the multiple-byte bit, located after the R/$\overline{W}$ bit in the first byte transfer (MB in Figure 24 to Figure 26), must be set. After the register addressing and the first byte of data, each subsequent set of clock pulses (eight clock pulses) causes the ADXL312 to point to the next register for a read or write. This shifting continues until the clock pulses cease and $\overline{CS}$ is deasserted. To perform reads or writes on different nonsequential registers, $\overline{CS}$ must be deasserted between transmissions, and the new register must be addressed separately.

The timing diagram for 3-wire SPI reads or writes is shown in Figure 26. The 4-wire equivalents for SPI writes and reads are shown in Figure 24 and Figure 25, respectively. For correct operation of the device, the logic thresholds and timing parameters in Table 8 and Table 9 must be met at all times.

Use of the 3200 Hz and 1600 Hz output data rates is only recommended with SPI communication rates greater than or equal to 2 MHz. The 800 Hz output data rate is recommended only for communication speeds greater than or equal to 400 kHz, and the remaining data rates scale proportionally. For example, the minimum recommended communication speed for a 200 Hz output data rate is 100 kHz. Operation at an output data rate below the recommended minimum may result in undesirable effects on the acceleration data, including missing samples or additional noise.

Preventing Bus Traffic Errors

The ADXL312 $\overline{CS}$ pin initiates SPI transactions and enables I²C mode. When the ADXL312 is used on a SPI bus with multiple devices, its $\overline{CS}$ pin is held high while the master communicates with the other devices. There may be conditions where a SPI command transmitted to another device looks like a valid I²C command. In this case, the ADXL312 interprets this as an attempt to communicate in I²C mode and may interfere with other bus traffic. Unless bus traffic can be adequately controlled to ensure such a condition never occurs, it is recommended to add a logic gate in front of the SDI pin, as shown in Figure 23.

This OR gate holds the SDA line high when $\overline{CS}$ is high to prevent bus traffic at the ADXL312 from appearing as an I²C start command.

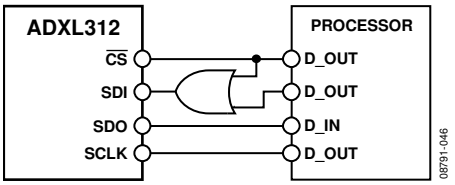


Figure 23. Recommended SPI Connection Diagram when Using Multiple SPI Devices on a Single Bus

Table 8. SPI Digital Input/Output

Parameter	Test Conditions	Limit[1] Min	Limit[1] Max	Unit
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	µA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		µA
Digital Output				
Low Level Output Voltage (V_{OL})	$I_{OL} = 10$ mA		$0.2 \times V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	$I_{OH} = -4$ mA	$0.8 \times V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	10		mA
High Level Output Current (I_{OH})	$V_{OH} = V_{OH,\ min}$		−4	mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.5$ V		8	pF

[1] Limits based on characterization results, not production tested.

Table 9. SPI Timing (T_A = 25°C, $V_S = V_{DD\ I/O}$ = 3.3 V)[1]

Parameter	Limit[2, 3] Min	Limit[2, 3] Max	Unit	Description
f_{SCLK}		5	MHz	SPI clock frequency.
t_{SCLK}	200		ns	1/(SPI clock frequency) mark-space ratio for the SCLK input is 40/60 to 60/40.
t_{DELAY}	5		ns	$\overline{CS}$ falling edge to SCLK falling edge .
t_{QUIET}	5		ns	SCLK rising edge to $\overline{CS}$ rising edge.
t_{DIS}		10	ns	$\overline{CS}$ rising edge to SDO disabled.
$t_{CS,DIS}$	150		ns	$\overline{CS}$ deassertion between SPI communications.
t_S	$0.3 \times t_{SCLK}$		ns	SCLK low pulse width (space).
t_M	$0.3 \times t_{SCLK}$		ns	SCLK high pulse width (mark).
t_{SETUP}	5		ns	SDI valid before SCLK rising edge.
t_{HOLD}	5		ns	SDI valid after SCLK rising edge.
t_{SDO}		40	ns	SCLK falling edge to SDO/SDIO output transition.
t_R[4]		20	ns	SDO/SDIO output high to output low transition.
t_F[4]		20	ns	SDO/SDIO output low to output high transition.

[1] The $\overline{CS}$, SCLK, SDI, and SDO pins are not internally pulled up or down; they must be driven for proper operation.
[2] Limits based on characterization results, characterized with f_{SCLK} = 5 MHz and bus load capacitance of 100 pF; not production tested.
[3] The timing values are measured corresponding to the input thresholds (V_{IL} and V_{IH}) given in Table 8.
[4] Output rise and fall times measured with capacitive load of 150 pF.

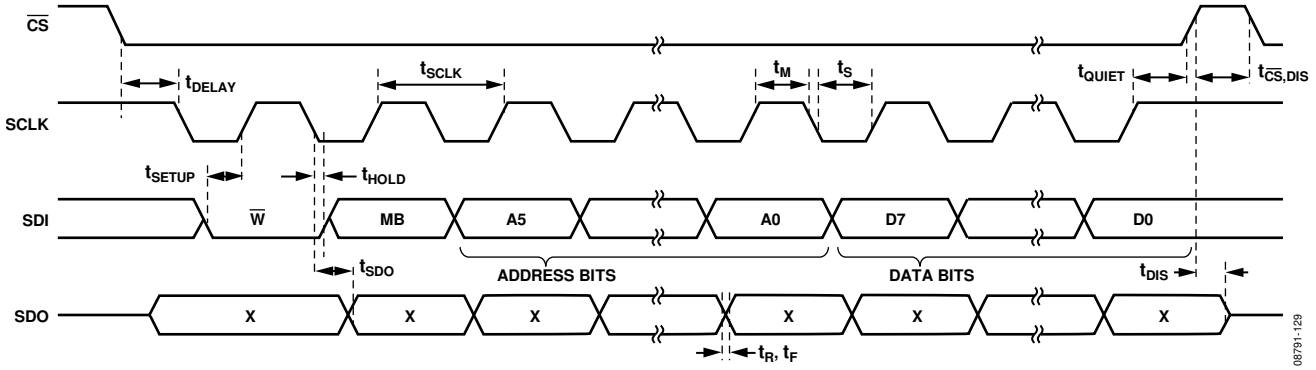


Figure 24. SPI 4-Wire Write

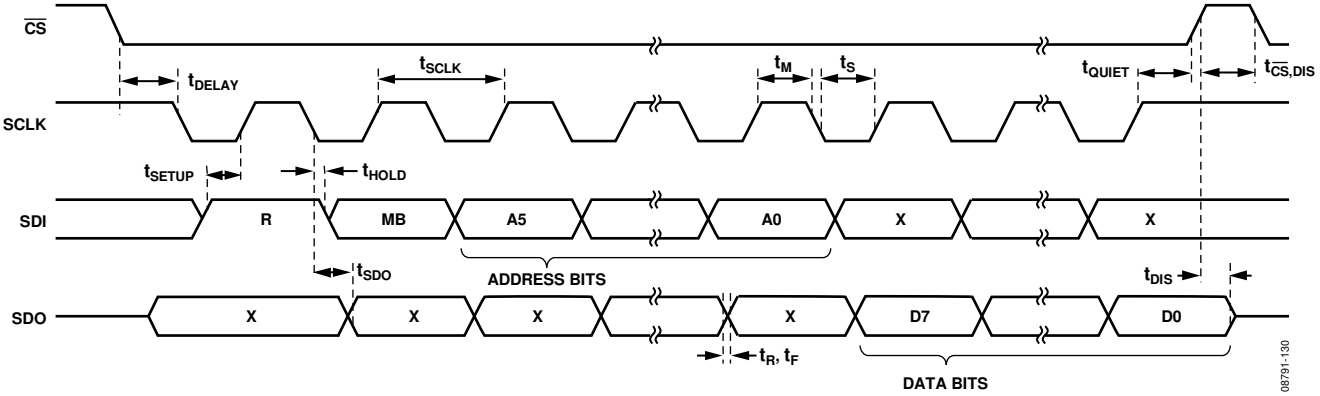
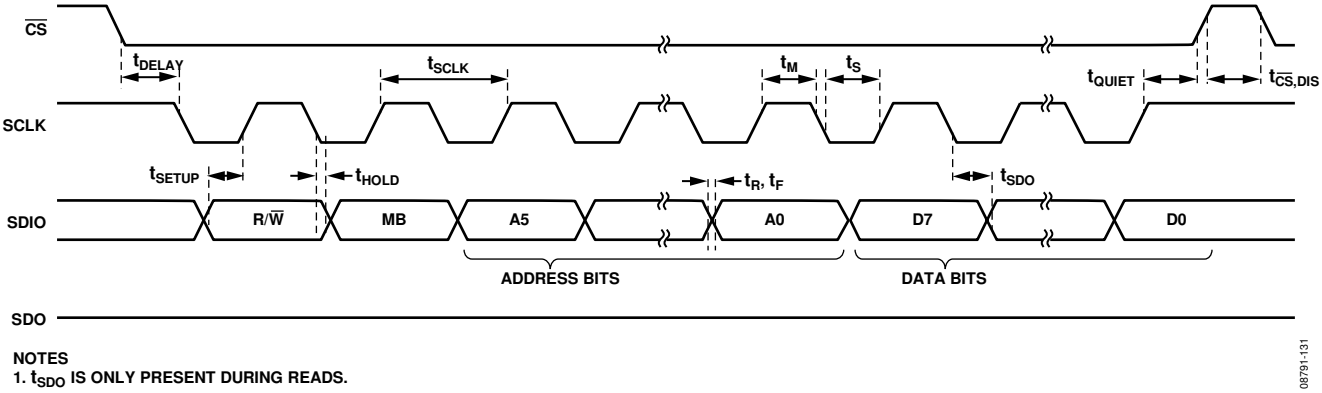


Figure 25. SPI 4-Wire Read



NOTES
1. t_{SDO} IS ONLY PRESENT DURING READS.

Figure 26. SPI 3-Wire Read/Write

I²C

With $\overline{CS}$ tied high to $V_{DD\ I/O}$, the ADXL312 is in I²C mode, requiring a simple 2-wire connection as shown in Figure 27. The ADXL312 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductor. It supports standard (100 kHz) and fast (400 kHz) data transfer modes if the bus parameters given in Table 10 and Table 11 are met. Single- or multiple-byte reads/writes are supported, as shown in Figure 28. With the ALT ADDRESS pin high, the 7-bit I²C address for the device is 0x1D, followed by the R/$\overline{W}$ bit. This translates to 0x3A for a write and 0x3B for a read. An alternate I²C address of 0x53 (followed by the R/$\overline{W}$ bit) can be chosen by grounding the ALT ADDRESS pin (Pin 7). This translates to 0xA6 for a write and 0xA7 for a read.

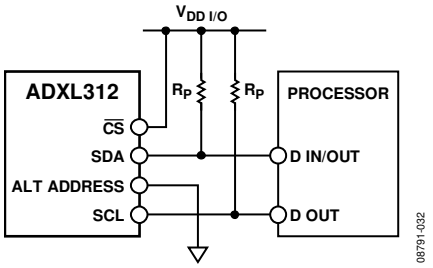


Figure 27. I²C Connection Diagram (Address 0x53)

If other devices are connected to the same I²C bus, the nominal operating voltage level of these other devices cannot exceed $V_{DD\ I/O}$ by more than 0.3 V. External pull-up resistors, R_P, are necessary for proper I²C operation. Refer to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, when selecting pull-up resistor values to ensure proper operation.

Table 10. I²C Digital Input/Output

Parameter	Test Conditions	Limit[1] Min	Limit[1] Max	Unit
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	μA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		μA
Digital Output				
Low Level Output Voltage (V_{OL})	$V_{DD\ I/O} < 2$ V, $I_{OL} = 3$ mA		$0.2 \times V_{DD\ I/O}$	V
	$V_{DD\ I/O} \geq 2$ V, $I_{OL} = 3$ mA		400	mV
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	3		mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.5$ V		8	pF

[1] Limits based on characterization results; not production tested.

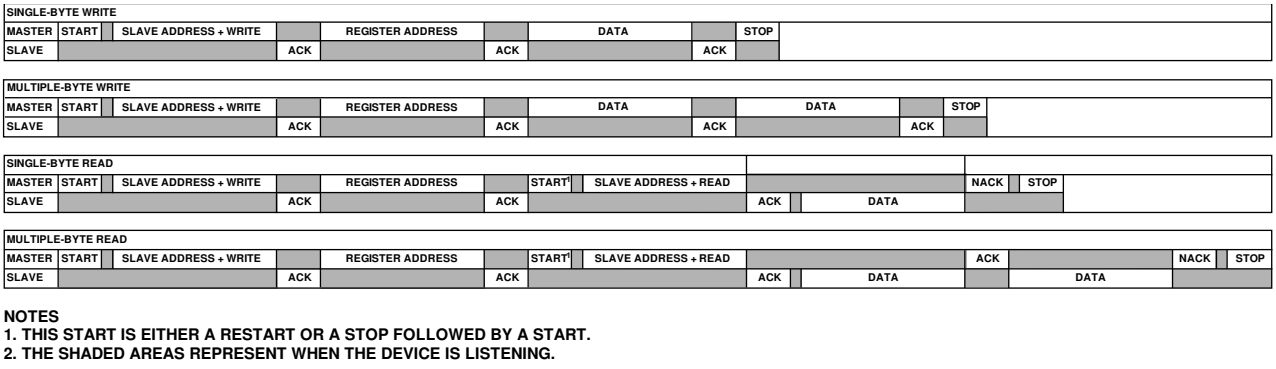


Figure 28. I²C Device Addressing

Table 11. I²C Timing (T_A = 25°C, V_S = $V_{DD\ I/O}$ = 3.3 V)

Parameter	Limit[1, 2] Min	Max	Unit	Description
f_{SCL}		400	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100		ns	$t_{SU, DAT}$, data setup time
t_6[3, 4, 5, 6]	0	0.9	µs	$t_{HD, DAT}$, data hold time
t_7	0.6		µs	$t_{SU, STA}$, setup time for repeated start
t_8	0.6		µs	$t_{SU, STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus-free time between a stop condition and a start condition
t_{10}		300	ns	t_R, rise time of both SCL and SDA when receiving
	0		ns	t_R, rise time of both SCL and SDA when receiving or transmitting
t_{11}		250	ns	t_F, fall time of SDA when receiving
		300	ns	t_F, fall time of both SCL and SDA when transmitting
	20 + 0.1 C_b[7]		ns	t_F, fall time of both SCL and SDA when transmitting or receiving
C_b		400	pF	Capacitive load for each bus line

[1] Limits based on characterization results, with f_{SCL} = 400 kHz and a 3 mA sink current; not production tested.
[2] All values referred to the V_{IH} and the V_{IL} levels given in Table 10.
[3] t_6 is the data hold time that is measured from the falling edge of SCL. It applies to data in transmission and acknowledge.
[4] A transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum t_6 value must be met only if the device does not stretch the low period (t_3) of the SCL signal.
[6] The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5(min)}$). This value is calculated as $t_{6(max)} = t_3 - t_{10} - t_{5(min)}$.
[7] C_b is the total capacitance of one bus line in picofarads.

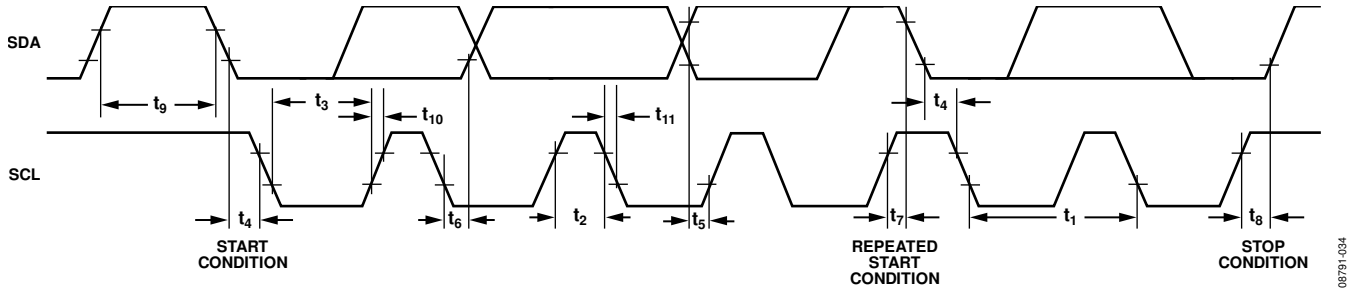


Figure 29. I²C Timing Diagram

INTERRUPTS

The ADXL312 provides two output pins for driving interrupts: INT1 and INT2. Both interrupt pins are push-pull, low impedance pins with output specifications shown in Table 12. The default configuration of the interrupt pins is active high. This can be changed to active low by setting the INT_INVERT bit in the DATA_FORMAT (Address 0x31) register. All functions can be used simultaneously, with the only limiting feature being that some functions may need to share interrupt pins.

Interrupts are enabled by setting the appropriate bit in the INT_ENABLE register (Address 0x2E) and are mapped to either the INT1 or INT2 pin based on the contents of the INT_MAP register (Address 0x2F). When initially configuring the interrupt pins, it is recommended that the functions and interrupt mapping be done before enabling the interrupts. When changing the configuration of an interrupt, it is recommended that the interrupt be disabled first, by clearing the bit corresponding to that function in the INT_ENABLE register, and then the function be reconfigured before enabling the interrupt again. Configuration of the functions while the interrupts are disabled helps to prevent the accidental generation of an interrupt before desired.

The interrupt functions are latched and cleared by either reading the data registers (Address 0x32 to Address 0x37) until the interrupt condition is no longer valid for the data-related interrupts or by reading the INT_SOURCE register (Address 0x30) for the remaining interrupts. This section describes the interrupts that can be set in the INT_ENABLE register and monitored in the INT_SOURCE register.

DATA_READY

The DATA_READY bit is set when new data is available and is cleared when no new data is available.

Activity

The activity bit is set when acceleration greater than the value stored in the THRESH_ACT register (Address 0x24) is experienced.

Inactivity

The inactivity bit is set when acceleration of less than the value stored in the THRESH_INACT register (Address 0x25) is experienced for more time than is specified in the TIME_INACT register (Address 0x26). The maximum value for TIME_INACT is 255 sec.

Watermark

The watermark bit is set when the number of samples in FIFO equals the value stored in the samples bits (Register FIFO_CTL, Address 0x38). The watermark bit is cleared automatically when FIFO is read, and the content returns to a value below the value stored in the samples bits.

Overrun

The overrun bit is set when new data replaces unread data. The precise operation of the overrun function depends on the FIFO mode. In bypass mode, the overrun bit is set when new data replaces unread data in the DATAX, DATAY, and DATAZ registers (Address 0x32 to Address 0x37). In all other modes, the overrun bit is set when FIFO is filled. The overrun bit is automatically cleared when the contents of FIFO are read.

Table 12. Interrupt Pin Digital Output

		Limit[1]		
Parameter	**Test Conditions**	**Min**	**Max**	**Unit**
Digital Output				
Low Level Output Voltage (V_{OL})	I_{OL} = 300 µA		0.2 × $V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	I_{OH} = −150 µA	0.8 × $V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	V_{OL} = $V_{OL,\ max}$	300		µA
High Level Output Current (I_{OH})	V_{OH} = $V_{OH,\ min}$		−150	µA
Pin Capacitance	f_{IN} = 1 MHz, V_{IN} = 2.5 V		8	pF
Rise/Fall Time				
Rise Time (t_R)[2]	C_{LOAD} = 150 pF		210	ns
Fall Time (t_F)[3]	C_{LOAD} = 150 pF		150	ns

[1] Limits based on characterization results, not production tested.
[2] Rise time is measured as the transition time from $V_{OL,\ max}$ to $V_{OH,\ min}$ of the interrupt pin.
[3] Fall time is measured as the transition time from $V_{OH,\ min}$ to $V_{OL,\ max}$ of the interrupt pin.

FIFO

The ADXL312 contains technology for an embedded memory management system with 32-level FIFO that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger (see Table 21). Each mode is selected by the settings of the FIFO_MODE bits in the FIFO_CTL register (Address 0x38).

Bypass Mode

In bypass mode, FIFO is not operational and, therefore, remains empty.

FIFO Mode

In FIFO mode, data from measurements of the x-, y-, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set. FIFO continues accumulating samples until it is full (32 samples from measurements of the x-, y-, and z-axes) and then stops collecting data. After FIFO stops collecting data, the device continues to operate; therefore, features such as activity detection can be used after FIFO is full. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Stream Mode

In stream mode, data from measurements of the x-, y-, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set. FIFO continues accumulating samples and holds the latest 32 samples from measurements of the x-, y-, and z-axes, discarding older data as new data arrives. The watermark interrupt continues occurring until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Trigger Mode

In trigger mode, FIFO accumulates samples, holding the latest 32 samples from measurements of the x-, y-, and z-axes. After a trigger event occurs and an interrupt is sent to the INT1 or INT2 pin (determined by the trigger bit in the FIFO_CTL register), FIFO keeps the last n samples (where n is the value specified by the samples bits in the FIFO_CTL register) and then operates in FIFO mode, collecting new samples only when FIFO is not full. A delay of at least 5 µs must be present between the trigger event occurring and the start of reading data from the FIFO to allow the FIFO to discard and retain the necessary samples. Additional trigger events cannot be recognized until the trigger mode is reset. To reset the trigger mode, set the device to bypass mode and then set the device back to trigger mode. Note that the FIFO data must be read first because placing the device into bypass mode clears FIFO.

Retrieving Data from FIFO

The FIFO data is read through the DATAX, DATAY, and DATAZ registers (Address 0x32 to Address 0x37). When the FIFO is in FIFO, stream, or trigger mode, reads to the DATAX, DATAY, and DATAZ registers read data stored in the FIFO. Each time data is read from the FIFO, the oldest x-, y-, and z-axes data is placed into the DATAX, DATAY and DATAZ registers.

If a single-byte read operation is performed, the remaining bytes of data for the current FIFO sample are lost. Therefore, all axes of interest must be read in a burst (or multiple-byte) read operation. To ensure that the FIFO has completely popped (that is, that new data has completely moved into the DATAX, DATAY, and DATAZ registers), there must be at least 5 µs between the end of reading the data registers and the start of a new read of the FIFO or a read of the FIFO_STATUS register (Address 0x39). The end of reading a data register is signified by the transition from Register 0x37 to Register 0x38 or by the $\overline{CS}$ pin going high.

For SPI operation at 1.6 MHz or less, the register addressing portion of the transmission is a sufficient delay to ensure that the FIFO has completely popped. For SPI operation greater than 1.6 MHz, it is necessary to deassert the $\overline{CS}$ pin to ensure a total delay of 5 µs; otherwise, the delay will not be sufficient. The total delay necessary for 5 MHz operation is at most 3.4 µs. This is not a concern when using I^2C mode because the communication rate is low enough to ensure a sufficient delay between FIFO reads.

SELF-TEST

The ADXL312 incorporates a self-test feature that effectively tests its mechanical and electronic systems simultaneously. When the self-test function is enabled (via the SELF_TEST bit in the DATA_FORMAT register, Address 0x31), an electrostatic force is exerted on the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change in the x-, y-, and z-axes. Because the electrostatic force is proportional to V_S^2, the output change varies with V_S. This effect is shown in Figure 30. The scale factors shown in Table 13 can be used to adjust the expected self-test output limits for different supply voltages, V_S. The self-test feature of the ADXL312 also exhibits a bimodal behavior. However, the limits shown in Table 1 and Table 14 to Table 17 are valid for both potential self-test values due to bimodality. Use of the self-test feature at data rates less than 100 Hz or at 1600 Hz may yield values outside these limits. Therefore, the part must be in normal power operation (LOW_POWER bit = 0 in BW_RATE register, Address 0x2C) and be placed into a data rate of 100 Hz through 800 Hz or 3200 Hz for the self-test function to operate correctly.

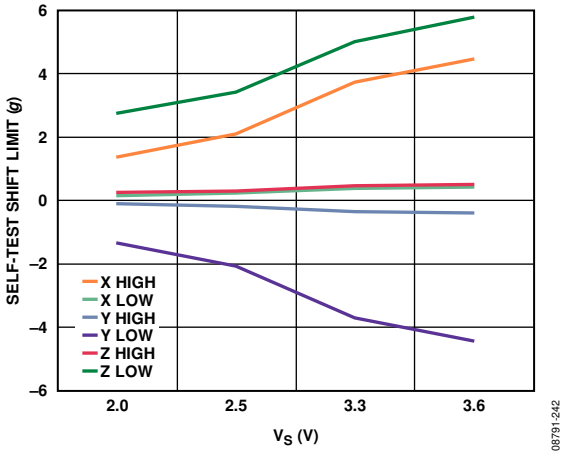


Figure 30. Self-Test Output Change Limits vs. Supply Voltage

Table 13. Self-Test Output Scale Factors for Different Supply Voltages, V_S

Supply Voltage, V_S	X-, Y-Axes	Z-Axis
2.00 V	0.64	0.8
2.50 V	1.00	1.00
3.00 V	1.77	1.47
3.30 V	2.11	1.69

Table 14. Self-Test Output in LSB for ±1.5 *g*, 10-Bit or Full Resolution (T_A = 25°C, V_S = $V_{DD\ I/O}$ = 2.5 V)

Axis	Min	Max	Unit
X	65	725	LSB
Y	−725	−65	LSB
Z	100	1175	LSB

Table 15. Self-Test Output in LSB for ±3 *g*, 10-Bit Resolution (T_A = 25°C, V_S = $V_{DD\ I/O}$ = 2.5 V)

Axis	Min	Max	Unit
X	32	362	LSB
Y	−362	−32	LSB
Z	50	588	LSB

Table 16. Self-Test Output in LSB for ±6 *g*, 10-Bit Resolution (T_A = 25°C, V_S = $V_{DD\ I/O}$ = 2.5 V)

Axis	Min	Max	Unit
X	16	181	LSB
Y	−181	−16	LSB
Z	25	294	LSB

Table 17. Self-Test Output in LSB for ±12 *g*, 10-Bit Resolution (T_A = 25°C, V_S = $V_{DD\ I/O}$ = 2.5 V)

Axis	Min	Max	Unit
X	8	90	LSB
Y	−90	−8	LSB
Z	12	147	LSB

REGISTER MAP

Table 18. Register Map

Address					
Hex	**Dec**	**Name**	**Type**	**Reset Value**	**Description**
0x00	0	DEVID	R	11100101	Device ID.
0x01 to 0x1D	1 to 29	Reserved			Reserved. Do not access.
0x1E	30	OFSX	R/$\overline{W}$	00000000	X-axis offset.
0x1F	31	OFSY	R/$\overline{W}$	00000000	Y-axis offset.
0x20	32	OFSZ	R/$\overline{W}$	00000000	Z-axis offset.
0x21	33	Reserved			Reserved. Do not access.
0x22	34	Reserved			Reserved. Do not access.
0x23	35	Reserved			Reserved. Do not access.
0x24	36	THRESH_ACT	R/$\overline{W}$	00000000	Activity threshold.
0x25	37	THRESH_INACT	R/$\overline{W}$	00000000	Inactivity threshold.
0x26	38	TIME_INACT	R/$\overline{W}$	00000000	Inactivity time.
0x27	39	ACT_INACT_CTL	R/$\overline{W}$	00000000	Axis enable control for activity and inactivity detection.
0x28	40	Reserved			Reserved. Do not access.
0x29	41	Reserved			Reserved. Do not access.
0x2A	42	Reserved			Reserved. Do not access.
0x2B	43	Reserved			Reserved. Do not access.
0x2C	44	BW_RATE	R/$\overline{W}$	00001010	Data rate and power mode control.
0x2D	45	POWER_CTL	R/$\overline{W}$	00000000	Power-saving features control.
0x2E	46	INT_ENABLE	R/$\overline{W}$	00000000	Interrupt enable control.
0x2F	47	INT_MAP	R/$\overline{W}$	00000000	Interrupt mapping control.
0x30	48	INT_SOURCE	R	00000010	Source of interrupts.
0x31	49	DATA_FORMAT	R/$\overline{W}$	00000000	Data format control.
0x32	50	DATAX0	R	00000000	X-Axis Data 0.
0x33	51	DATAX1	R	00000000	X-Axis Data 1.
0x34	52	DATAY0	R	00000000	Y-Axis Data 0.
0x35	53	DATAY1	R	00000000	Y-Axis Data 1.
0x36	54	DATAZ0	R	00000000	Z-Axis Data 0.
0x37	55	DATAZ1	R	00000000	Z-Axis Data 1.
0x38	56	FIFO_CTL	R/$\overline{W}$	00000000	FIFO control.
0x39	57	FIFO_STATUS	R	00000000	FIFO status.

REGISTER DEFINITIONS

Register 0x00—DEVID (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	1

The DEVID register holds a fixed device ID code of 0xE5.

Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers are each eight bits and offer user-set offset adjustments in twos complement format with a scale factor of 11.6 mg/LSB (that is, 0x7F = +1.5 *g*). The value stored in the offset registers is automatically added to the acceleration data, and the resulting value is stored in the output data registers.

Register 0x24—THRESH_ACT (Read/Write)

The THRESH_ACT register is eight bits and holds the threshold value for detecting activity. The data format is unsigned; therefore, the magnitude of the activity event is compared with the value in the THRESH_ACT register. The scale factor is 46.4 mg/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

Register 0x25—THRESH_INACT (Read/Write)

The THRESH_INACT register is eight bits and holds the threshold value for detecting inactivity. The data format is unsigned; therefore, the magnitude of the inactivity event is compared with the value in the THRESH_INACT register. The scale factor is 46.4 mg/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

Register 0x26—TIME_INACT (Read/Write)

The TIME_INACT register is eight bits and contains an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH_INACT register for inactivity to be declared. The scale factor is 1 sec/LSB. Unlike the other interrupt functions, which use unfiltered data (see the Threshold section), the inactivity function uses filtered output data. At least one output sample must be generated for the inactivity interrupt to be triggered. This results in the function appearing unresponsive if the TIME_INACT register is set to a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH_INACT register.

Register 0x27—ACT_INACT_CTL (Read/Write)

D7	D6	D5	D4
ACT ac/dc	ACT_X enable	ACT_Y enable	ACT_Z enable
D3	**D2**	**D1**	**D0**
INACT ac/dc	INACT_X enable	INACT_Y enable	INACT_Z enable

ACT AC/DC and INACT AC/DC Bits

A setting of 0 selects dc-coupled operation, and a setting of 1 enables ac-coupled operation.

In dc-coupled operation, the current acceleration magnitude is compared directly with THRESH_ACT and THRESH_INACT to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value and, if the magnitude of the difference exceeds the THRESH_ACT value, the device triggers an activity interrupt.

Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. After the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with THRESH_INACT. If the difference is less than the value in THRESH_INACT for the time in TIME_INACT, the device is considered inactive and the inactivity interrupt is triggered.

ACT_x Enable Bits and INACT_x Enable Bits

A setting of 1 enables x-, y-, or z-axis participation in detecting activity or inactivity. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR'ed, causing the activity function to trigger when any of the participating axes exceeds the threshold. For inactivity detection, all participating axes are logically AND'ed, causing the inactivity function to trigger only if all participating axes are below the threshold for the specified period of time.

Register 0x2C—BW_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LOW_POWER	Rate			

LOW_POWER Bit

A setting of 0 in the LOW_POWER bit selects normal operation, and a setting of 1 selects reduced power operation, which has somewhat higher noise (see the Power Modes section for details).

Rate Bits

These bits select the device bandwidth and output data rate (see Table 6 and Table 7 for details). The default value is 0x0A, which translates to a 100 Hz output data rate. An output data rate must be selected that is appropriate for the communication protocol and frequency selected. Selecting too high of an output data rate with a low communication speed results in samples being discarded.

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

Link Bit

A setting of 1 in the link bit with both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. After activity is detected, inactivity detection begins, preventing the detection of activity. This bit serially links the activity and inactivity functions.

When this bit is set to 0, the inactivity and activity functions are concurrent. Additional information can be found in the Link Mode section.

When clearing the link bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

AUTO_SLEEP Bit

If the link bit is set, a setting of 1 in the AUTO_SLEEP bit sets the ADXL312 to switch to sleep mode when inactivity is detected (that is, when acceleration has been below the THRESH_INACT value for at least the time indicated by TIME_INACT). A setting of 0 disables automatic switching to sleep mode. See the description of the sleep bit in this section for more information.

When clearing the AUTO_SLEEP bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the AUTO_SLEEP bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Measure Bit

A setting of 0 in the measure bit places the part into standby mode, and a setting of 1 places the part into measurement mode. The ADXL312 powers up in standby mode with minimum power consumption.

Sleep Bit

A setting of 0 in the sleep bit puts the part into the normal mode of operation, and a setting of 1 places the part into sleep mode. Sleep mode suppresses DATA_READY (see Register 0x2E, Register 0x2F, and Register 0x30), stops transmission of data to FIFO, and switches the sampling rate to one specified by the wake-up bits. In sleep mode, only the activity function can be used.

When clearing the sleep bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the sleep bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Wake-Up Bits

These bits control the frequency of readings in sleep mode as described in Table 19.

Table 19. Frequency of Readings in Sleep Mode

Setting		
D1	**D0**	**Frequency (Hz)**
0	0	8
0	1	4
1	0	2
1	1	1

Register 0x2E—INT_ENABLE (Read/Write)

D7 DATA_READY	**D6** N/A	**D5** N/A	**D4** Activity
D3 Inactivity	**D2** N/A	**D1** Watermark	**D0** Overrun

Setting bits in this register to a value of 1 enables their respective functions to generate interrupts, whereas a value of 0 prevents the functions from generating interrupts. The DATA_READY, watermark, and overrun bits enable only the interrupt output; the functions are always enabled. It is recommended that interrupts be configured before enabling their outputs.

Register 0x2F—INT_MAP (Read/Write)

D7 DATA_READY	**D6** N/A	**D5** N/A	**D4** Activity
D3 Inactivity	**D2** N/A	**D1** Watermark	**D0** Overrun

Any bits set to 0 in this register send their respective interrupts to the INT1 pin, whereas bits set to 1 send their respective interrupts to the INT2 pin. All selected interrupts for a given pin are OR'ed.

Register 0x30—INT_SOURCE (Read Only)

D7 DATA_READY	**D6** N/A	**D5** N/A	**D4** Activity
D3 Inactivity	**D2** N/A	**D1** Watermark	**D0** Overrun

Bits set to 1 in this register indicate that their respective functions have triggered an event, whereas a value of 0 indicates that the corresponding event has not occurred. The DATA_READY, watermark, and overrun bits are always set if the corresponding events occur, regardless of the INT_ENABLE register settings, and are cleared by reading data from the DATAX, DATAY, and DATAZ registers. The DATA_READY and watermark bits may require multiple reads, as indicated in the FIFO mode descriptions in the FIFO section. Other bits, and the corresponding interrupts, are cleared by reading the INT_SOURCE register.

Register 0x31—DATA_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SPI	INT_INVERT	0	FULL_RES	Justify	Range	

The DATA_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37. All data, except that for the ±12 *g* range, must be clipped to avoid rollover.

SELF_TEST Bit

A setting of 1 in the SELF_TEST bit applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force.

SPI Bit

A value of 1 in the SPI bit sets the device to 3-wire SPI mode, and a value of 0 sets the device to 4-wire SPI mode.

INT_INVERT Bit

A value of 0 in the INT_INVERT bit sets the interrupts to active high, and a value of 1 sets the interrupts to active low.

FULL_RES Bit

When this bit is set to a value of 1, the device is in full resolution mode, where the output resolution increases with the *g* range set by the range bits to maintain a 2.9 mg/LSB scale factor. When the FULL_RES bit is set to 0, the device is in 10-bit mode, and the range bits determine the maximum *g* range and scale factor.

Justify Bit

A setting of 1 in the justify bit selects left (MSB) justified mode, and a setting of 0 selects right justified mode with sign extension.

Range Bits

These bits set the *g* range as described in Table 20.

Table 20. *g* Range Setting

Setting		
D1	D0	***g* Range**
0	0	±1.5 *g*
0	1	±3 *g*
1	0	±6 *g*
1	1	±12 *g*

Register 0x32 to Register 0x37—DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, DATAZ1 (Read Only)

These six bytes (Register 0x32 to Register 0x37) are eight bits each and hold the output data for each axis. Register 0x32 and Register 0x33 hold the output data for the x-axis, Register 0x34 and Register 0x35 hold the output data for the y-axis, and Register 0x36 and Register 0x37 hold the output data for the z-axis.

The output data is twos complement, with DATAx0 as the least significant byte and DATAx1 as the most significant byte, where x represent X, Y, or Z. The DATA_FORMAT register (Address 0x31) controls the format of the data. It is recommended that a multiple-byte read of all registers be performed to prevent a change in data between reads of sequential registers.

Register 0x38—FIFO_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_MODE		Trigger	Samples				

FIFO_MODE Bits

These bits set the FIFO mode, as described in Table 21.

Table 21. FIFO Modes

Setting			
D7	D6	Mode	Function
0	0	Bypass	FIFO is bypassed.
0	1	FIFO	FIFO collects up to 32 values and then stops collecting data, collecting new data only when FIFO is not full.
1	0	Stream	FIFO holds the last 32 data values. When FIFO is full, the oldest data is overwritten with newer data.
1	1	Trigger	When triggered by the trigger bit, FIFO holds the last data samples before the trigger event and then continues to collect data until full. New data is collected only when FIFO is not full.

Trigger Bit

A value of 0 in the trigger bit links the trigger event of trigger mode INT1, and a value of 1 links the trigger event to INT2.

Samples Bits

The function of these bits depends on the FIFO mode selected (see Table 22). Entering a value of 0 in the samples bits immediately sets the watermark status bit in the INT_SOURCE register, regardless of which FIFO mode is selected. Undesirable operation may occur if a value of 0 is used for the samples bits when trigger mode is used.

Table 22. Samples Bits Functions

FIFO Mode	Samples Bits Function
Bypass	None.
FIFO	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Stream	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Trigger	Specifies how many FIFO samples are retained in the FIFO buffer before a trigger event.

0x39—FIFO_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_TRIG	0	Entries					

FIFO_TRIG Bit

A 1 in the FIFO_TRIG bit corresponds to a trigger event occurring, and a 0 means that a FIFO trigger event has not occurred.

Entries Bits

These bits report how many data values are stored in FIFO. Access to collect the data from FIFO is provided through the DATAX, DATAY, and DATAZ registers. FIFO reads must be done in burst or multiple-byte mode because each FIFO level is cleared after any read (single- or multiple-byte) of FIFO. FIFO stores a maximum of 32 entries, which equates to a maximum of 33 entries available at any given time because an additional entry is available at the output filter of the device.