
Chipsmall
深圳市津利帝科技有限公司
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Chipsmall
采购部

Low Noise, Low Drift, Low Power, 3-Axis MEMS Accelerometers

Data Sheet **ADXL356/ADXL357**

FEATURES

Hermetic package offers excellent long-term stability
0 *g* offset vs. temperature (all axes): 0.75 m*g*/°C maximum
Ultralow noise density (all axes): 80 μ*g*/√Hz
Low power, V_{SUPPLY} (LDO enabled)
- **ADXL356 in measurement mode: 150 μA**
- **ADXL357 in measurement mode: 200 μA**
- **ADXL356/ADXL357 in standby mode: 21 μA**

ADXL356 has user adjustable analog output bandwidth
ADXL357 digital output features
- **Digital serial peripheral interface (SPI)/limited I²C interfaces supported**
- **20-bit analog-to-digital converter (ADC)**
- **Data interpolation routine for synchronous sampling**
- **Programmable high- and low-pass digital filters**

Integrated temperature sensor
Voltage range options
- **V_{SUPPLY} with internal regulators: 2.25 V to 3.6 V**
- **V_{1P8ANA}, V_{1P8DIG} with internal low dropout (LDO) regulator bypassed: 1.8 V typical ± 10%**

Operating temperature range: −40°C to +125°C
14-terminal, 6 mm × 5.6 mm × 2.05 mm, LCC package, 0.26 g

APPLICATIONS

Inertial measurement units (IMUs)/altitude and heading reference systems (AHRSs)
Platform stabilization systems
Structural health monitoring
Seismic imaging
Tilt sensing
Robotics
Condition monitoring

FUNCTIONAL BLOCK DIAGRAMS

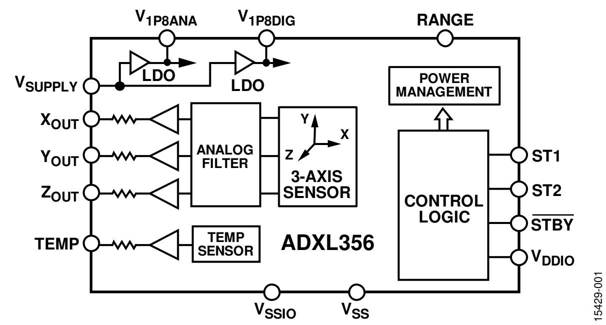

Figure 1. ADXL356

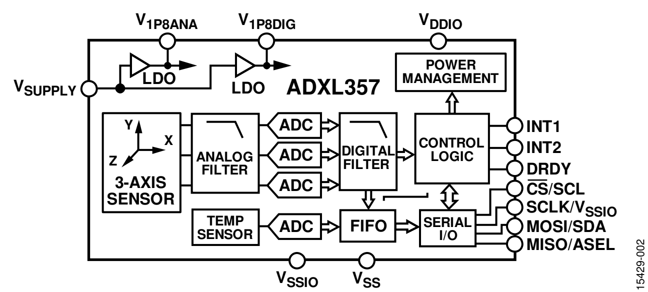

Figure 2. ADXL357

GENERAL DESCRIPTION

The analog output ADXL356 and the digital output ADXL357 are low noise density, low 0 *g* offset drift, low power, 3-axis accelerometers with selectable measurement ranges. The ADXL356B supports the ±10 *g* and ±20 *g* ranges, the ADXL356C supports the ±10 *g* and ±40 *g* ranges, and the ADXL357 supports the ±10.24 g, ±20.48 g, and ±40.96 *g* ranges.

The ADXL356/ADXL357 offer industry leading noise, minimal offset drift over temperature, and long-term stability, enabling precision applications with minimal calibration.

The low drift, low noise, and low power ADXL357 enables accurate tilt measurement in an environment with high vibration, such as airborne IMUs. The low noise of the ADXL356 over higher frequencies is ideal for wireless condition monitoring.

The ADXL357 multifunction pin names may be referenced only by their relevant function for either the SPI or limited I²C interface.

[1] Protected by U.S. Patents 8,472,270; 9,041,462; 8,665,627; 8,917,099; 6,892,576; 9,297,825; and 7,956,621.

Rev. 0 **Document Feedback**

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REVISION HISTORY

2/2017—Revision 0: Initial Version

SPECIFICATIONS

ANALOG OUTPUT FOR THE ADXL356

T_A = 25°C, V_{SUPPLY} = 3.3 V, x-axis acceleration and y-axis acceleration = 0 *g*, z-axis acceleration = 1 *g*, and full-scale range = ±10 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Output Full-Scale Range (FSR)	ADXL356B, supports two ranges		±10/±20		*g*
	ADXL356C, supports two ranges		±10/±40		*g*
Resonant Frequency[1]			5.5		kHz
Nonlinearity	±10 *g*		0.1		%
Cross Axis Sensitivity			1		%
SENSITIVITY	Ratiometric to V_{1P8ANA}				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±10 *g*	73.6	80	86.4	mV/*g*
	±20 *g*	36.8	40	43.2	mV/*g*
	±40 *g*	18.4	20	21.6	mV/*g*
Sensitivity Change due to Temperature	T_A = −40°C to +125°C		±0.01		%/°C
0 *g* OFFSET	Each axis, ±10 *g*				
0 *g* Output for X_{OUT}, Y_{OUT}, Z_{OUT}	Referred to $V_{1P8ANA}/2$	−375	±125	+375	m*g*
0 *g* Offset vs. Temperature (X-Axis, Y-Axis, and Z-Axis)[2]	T_A = −40°C to +125°C	−0.75	±0.5	+0.75	m*g*/°C
Vibration Rectification Error (VRE)[3]	Offset due to 7.5 *g* rms vibration, ±10 *g* range, in a 1 *g* orientation		<0.1		*g*
NOISE DENSITY	±10 *g*				
X-Axis, Y-Axis, and Z-Axis			80		µ*g*/√Hz
Velocity Random Walk	X-axis and y-axis		45		µm/sec/√Hr
	Z-axis		65		µm/sec/√Hr
BANDWIDTH					
Internal Low-Pass Filter Frequency	Fixed frequency, 50% response attenuation		1500		Hz
SELF TEST					
Output Change					
Z-Axis	±10 *g* range		1.25		*g*
POWER SUPPLY					
Voltage Range					
V_{SUPPLY}[4]		2.25	2.5	3.6	V
V_{DDIO}		V_{1P8DIG}	2.5	3.6	V
V_{1P8ANA}, V_{1P8DIG} with Internal Low Dropout Regulator (LDO) Bypassed	V_{SUPPLY} = 0 V	1.62	1.8	1.98	V
Current					
Measurement Mode					
V_{SUPPLY} (LDO Enabled)			150		µA
V_{1P8ANA} (LDO Disabled)			138		µA
V_{1P8DIG} (LDO Disabled)			12		µA
Standby Mode					
V_{SUPPLY} (LDO Enabled)			21		µA
V_{1P8ANA} (LDO Disabled)			7		µA
V_{1P8DIG} (LDO Disabled)			10		µA
Turn On Time[5]	10 *g* range		<10		ms
	Power-off to standby		<10		ms
OUTPUT AMPLIFIER					
Swing	No load	0.03		V_{1P8ANA} − 0.03	V
Output Series Resistance			32		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Output at 25°C			892.2		mV
Scale Factor			3.0		mV/°C
TEMPERATURE					
Operating Temperature Range		−40		+125	°C

[1] The resonant frequency is a sensor characteristic. An integrated analog 1.5 kHz (−6 dB) sinc low-pass filter that cannot be bypassed limits the actual output response.
[2] The temperature change is −40°C to +25°C or +25°C to +125°C.
[3] The VRE measurement is the shift in dc offset while the device is subject to 12.5 *g* rms of random vibration from 50 Hz to 2 kHz. The device under test (DUT) is configured for the ±10 *g* range and an output data rate of 4 kHz. The VRE scales with the range setting.
[4] When V_{1P8ANA} and V_{1P8DIG} are generated internally, V_{SUPPLY} is valid. To disable the LDO and drive V_{1P8ANA} and V_{1P8DIG} externally, connect V_{SUPPLY} to V_{SS}.
[5] Standby to measurement mode; valid when the output is within 5 m*g* of the final value.

DIGITAL OUTPUT FOR THE ADXL357

T_A = 25°C, V_{SUPPLY} = 3.3 V, x-axis acceleration and y-axis acceleration = 0 *g*, z-axis acceleration = 1 *g*, full-scale range = ±10.24 *g*, and output data rate (ODR) = 500 Hz, unless otherwise noted. Note that multifunction pin names may be referenced only by their relevant function.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Output Full Scale Range (FSR)	User selectable		±10.24		*g*
			±20.48		*g*
			±40.96		*g*
Nonlinearity	±10 *g*		0.1		% FSR
Cross Axis Sensitivity			1		%
SENSITIVITY	Each axis				
X-Axis, Y-Axis, and Z-Axis Sensitivity	±10 *g*	47,104	51,200	55,296	LSB/*g*
	±20 *g*	23,552	25,600	27,648	LSB/*g*
	±40 *g*	11,776	12,800	13,824	LSB/*g*
X-Axis, Y-Axis, and Z-Axis Scale Factor	±10 *g*		19.5		µ*g*/LSB
	±20 *g*		39		µ*g*/LSB
	±40 *g*		78		µ*g*/LSB
Sensitivity Change due to Temperature	T_A = −40°C to +125°C		±0.01		%/°C
0 *g* OFFSET	Each axis, ±10 *g*				
X-Axis, Y-Axis, and Z-Axis 0 *g* Output		−375	±125	+375	m*g*
0 *g* Offset vs. Temperature (X-Axis, Y-Axis, and Z-Axis)[1]	T_A = −40°C to +125°C	−0.75	±0.50	+0.75	m*g*/°C
Vibration Rectification Error (VRE)[2]	Offset due to 7.5 *g* rms vibration, ±10 *g* range, in a 1 *g* orientation		<0.1		*g*
NOISE DENSITY	±10 *g*				
X-Axis, Y-Axis, and Z-Axis			80		µ*g*/√Hz
Velocity Random Walk	X-axis and y-axis		45		µm/sec/√Hr
	Z-axis		65		µm/sec/√Hr
OUTPUT DATA RATE AND BANDWIDTH					
ADC Resolution			20		bits
Low-Pass Filter Passband Frequency	User programmable, Register 0x28	1		1000	Hz
High-Pass Filter Passband Frequency When Enabled (Disabled by Default)	User programmable, Register 0x28 for 4 kHz ODR	0.0095		10	Hz
SELF TEST					
Output Change					
Z-Axis	±10 *g* range		1.25		*g*

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Voltage Range					
V_{SUPPLY} Operating[3]		2.25	2.5	3.6	V
V_{DDIO}		V_{1P8DIG}	2.5	3.6	V
V_{1P8ANA} and V_{1P8DIG} with Internal LDO Bypassed	V_{SUPPLY} = 0 V	1.62	1.8	1.98	V
Current					
Measurement Mode					
V_{SUPPLY} (LDO Enabled)			200		µA
V_{1P8ANA} (LDO Disabled)			160		µA
V_{1P8DIG} (LDO Disabled)			35.5		µA
Standby Mode					
V_{SUPPLY} (LDO Enabled)			21		µA
V_{1P8ANA} (LDO Disabled)			7		µA
V_{1P8DIG} (LDO Disabled)			10		µA
Turn On Time[4]	±10 *g* range		<10		ms
	Power-off to standby		<10		ms
TEMPERATURE SENSOR					
Output at 25°C			1852		LSB
Scale Factor			−9.05		LSB/°C
TEMPERATURE					
Operating Temperature Range		−40		+125	°C

[1] The temperature change is −40°C to +25°C or +25°C to +125°C.
[2] The VRE measurement is the shift in dc offset while the device is subject to 12.5 *g* rms random vibration from 50 Hz to 2 kHz. The DUT is configured for the ±2 *g* range and an output data rate of 4 kHz. The VRE scales with the range setting.
[3] When V_{1P8ANA} and V_{1P8DIG} are generated internally, V_{SUPPLY} is valid. To disable the LDO and drive V_{1P8ANA} and V_{1P8DIG} externally, connect V_{SUPPLY} to V_{SS}.
[4] Standby to measurement mode; valid when the output is within 1 m*g* of final value.

SPI DIGITAL INTERFACE CHARACTERISTICS FOR THE ADXL357

Note that multifunction pin names may be referenced by their relevant function only.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC INPUT LEVELS						
Input Voltage						
Low Level	V_{IL}				$0.3 \times V_{DDIO}$	V
High Level	V_{IH}		$0.7 \times V_{DDIO}$			V
Input Current						
Low Level	I_{IL}	$V_{IN} = 0$ V	−0.1			μA
High Level	I_{IH}	$V_{IN} = V_{DDIO}$			0.1	μA
DC OUTPUT LEVELS						
Output Voltage						
Low Level	V_{OL}	$I_{OL} = I_{OL, MIN}$			$0.2 \times V_{DDIO}$	V
High Level	V_{OH}	$I_{OH} = I_{OH, MAX}$	$0.8 \times V_{DDIO}$			V
Output Current						
Low Level	I_{OL}	$V_{OL} = V_{OL, MAX}$	−10			mA
High Level	I_{OH}	$V_{OH} = V_{OH, MIN}$			4	mA
AC INPUT LEVELS						
SCLK Frequency			0.1		10	MHz
SCLK High Time	t_{HIGH}		40			ns
SCLK Low Time	t_{LOW}		40			ns
$\overline{CS}$ Setup Time	t_{CSS}		20			ns
$\overline{CS}$ Hold Time	t_{CSH}		20			ns
$\overline{CS}$ Disable Time	t_{CSD}		40			ns
Rising SCLK Setup Time	t_{SCLKS}		20			ns
MOSI Setup Time	t_{SU}		20			ns
MOSI Hold Time	t_{HD}		20			ns
AC OUTPUT LEVELS						
Propagation Delay	t_P	$C_{LOAD} = 30$ pF			30	ns
Enable MISO Time	t_{EN}		30			ns
Disable MISO Time	t_{DIS}				20	ns

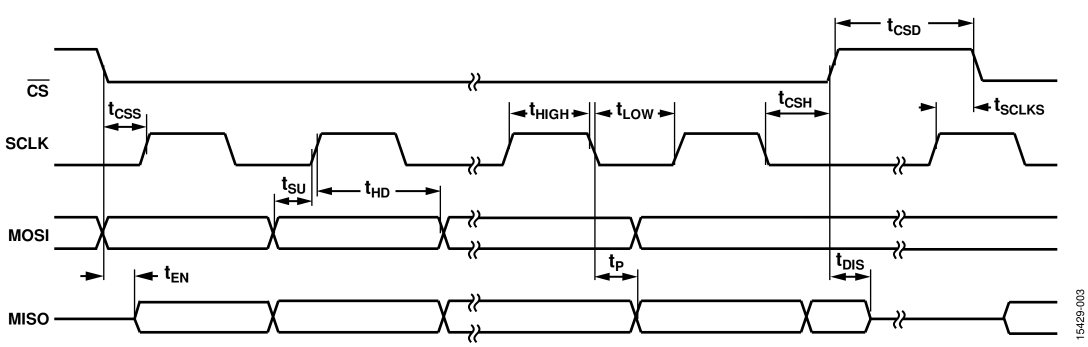


Figure 3. SPI Interface Timing Diagram

I²C DIGITAL INTERFACE CHARACTERISTICS FOR THE ADXL357

Note that multifunction pin names may be referenced only by their relevant function.

Table 4.

Parameter	Symbol	Test Conditions/ Comments	I2C_HS = 0 (Fast Mode) Min	Typ	Max	I2C_HS = 1 (High Speed Mode) Min	Typ	Max	Unit
DC INPUT LEVELS									
Input Voltage									
Low Level	V_{IL}				$0.3 \times V_{DDIO}$			$0.3 \times V_{DDIO}$	V
High Level	V_{IH}		$0.7 \times V_{DDIO}$			$0.7 \times V_{DDIO}$			V
Hysteresis of Schmitt Triggered Inputs	V_{HYS}		$0.05 \times V_{DDIO}$			$0.1 \times V_{DDIO}$			µA
Input Current	I_{IL}	$0.1 \times V_{DDIO} < V_{IN} < 0.9 \times V_{DDIO}$	−10		+10				µA
DC OUTPUT LEVELS									
Output Voltage		$I_{OL} = 3$ mA							
Low Level	V_{OL1}	$V_{DDIO} > 2$ V			0.4				V
	V_{OL2}	$V_{DDIO} \leq 2$ V			$0.2 \times V_{DDIO}$				V
Output Current									
Low Level	I_{OL}	$V_{OL} = 0.4$ V	20						mA
		$V_{OL} = 0.6$ V	6						mA
AC INPUT LEVELS									
SCL Frequency			0		1	0		3.4	MHz
SCL High Time	t_{HIGH}		260			60			ns
SCL Low Time	t_{LOW}		500			160			ns
Start Setup Time	t_{SUSTA}		260			160			ns
Start Hold Time	t_{HDSTA}		260			160			ns
SDA Setup Time	t_{SUDAT}		50			10			ns
SDA Hold Time	t_{HDDAT}		0			0			ns
Stop Setup Time	t_{SUSTO}		260			160			ns
Bus Free Time	t_{BUF}		500						ns
SCL Input Rise Time	t_{RCL}				120			80	ns
SCL Input Fall Time	t_{FCL}				120			80	ns
SDA Input Rise Time	t_{RDA}				120			160	ns
SDA Input Fall Time	t_{FDA}				120			160	ns
Width of Spikes to Suppress	t_{SP}	Not shown in Figure 4			50			10	ns
AC OUTPUT LEVELS									
Propagation Delay		$C_{LOAD} = 500$ pF							
Data	t_{VDDAT}		97		450	27		135	ns
Acknowledge	t_{VDACK}				450				ns
Output Fall Time	t_F	Not shown in Figure 4	$20 \times (V_{DDIO}/5.5)$		120				ns

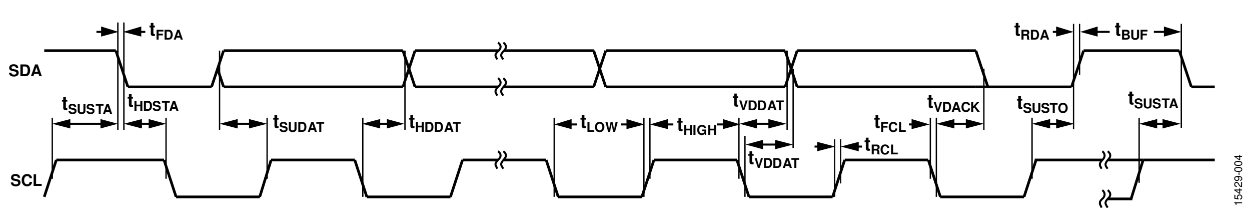


Figure 4. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Acceleration (Any Axis, 0.1 ms)	5000 g
V_{SUPPLY}, V_{DDIO}	5.4 V
V_{1P8ANA}, V_{1P8DIG} Configured as Inputs	1.98 V
ADXL356	
Digital Inputs (RANGE, ST1, ST2, $\overline{STBY}$)	−0.3 V to V_{DDIO} + 0.3 V
Analog Outputs (X_{OUT}, Y_{OUT}, Z_{OUT}, TEMP)	−0.3 V to V_{1P8ANA} + 0.3 V
ADXL357	
Digital Pins ($\overline{CS}$/SCL, SCLK/V_{SSIO}, MOSI/SDA, MISO/ASEL, INT1, INT2, DRDY)	−0.3 V to V_{DDIO} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−55°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
E-14-1[1]	42	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

RECOMMENDED SOLDERING PROFILE

Figure 5 and Table 7 provide details about the recommended soldering profile.

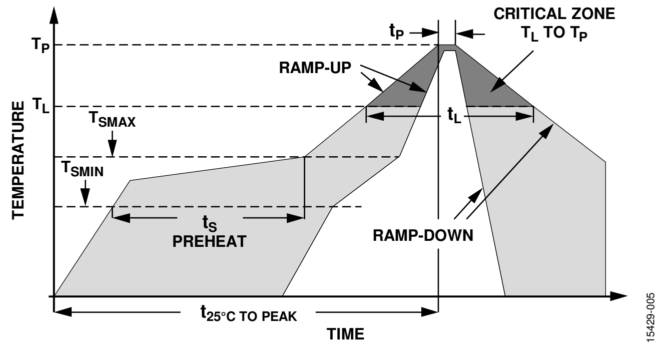
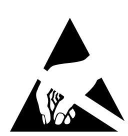


Figure 5. Recommended Soldering Profile

Table 7. Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate from Liquid Temperature (T_L) to Peak Temperature (T_P)	3°C/sec maximum	3°C/sec maximum
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time from T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum	3°C/sec maximum
Liquid Temperature (T_L)	183°C	217°C
Time Maintained Above T_L (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240°C + 0°C/−5°C	260°C + 0°C/−5°C
Time of Actual T_P − 5°C (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec maximum	6°C/sec maximum
Time from 25°C to Peak Temperature ($t_{25°C\ TO\ PEAK}$)	6 minutes maximum	8 minutes maximum

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

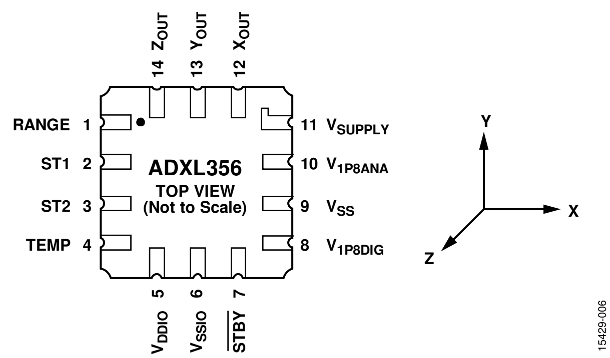


Figure 6. ADXL356 Pin Configuration

Table 8. ADXL356 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RANGE	Range Selection Pin. Set this pin to ground to select the ±10 *g* range, or set this pin to V_{DDIO} to select the ±20 *g* or ±40 *g* range. This pin is model dependent (see the Ordering Guide section).
2	ST1	Self Test Pin 1. This pin enables self test mode.
3	ST2	Self Test Pin 2. This pin activates the electromechanical self test actuation.
4	TEMP	Temperature Sensor Output.
5	V_{DDIO}	Digital Interface Supply Voltage.
6	V_{SSIO}	Digital Ground.
7	$\overline{STBY}$	Standby or Measurement Mode Selection Pin. Set this pin to ground to enter standby mode, or set this pin to V_{DDIO} to enter measurement mode.
8	V_{1P8DIG}	Digital Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS}, supply the voltage to this pin externally.
9	V_{SS}	Analog Ground.
10	V_{1P8ANA}	Analog Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS}, supply the voltage to this pin externally.
11	V_{SUPPLY}	Supply Voltage. When V_{SUPPLY} equals 2.25 V to 3.6 V, V_{SUPPLY} enables the internal LDO regulators to generate V_{1P8DIG} and V_{1P8ANA}. For $V_{SUPPLY} = V_{SS}$, V_{1P8DIG} and V_{1P8ANA} are externally supplied.
12	X_{OUT}	X-Axis Output.
13	Y_{OUT}	Y-Axis Output.
14	Z_{OUT}	Z-Axis Output.

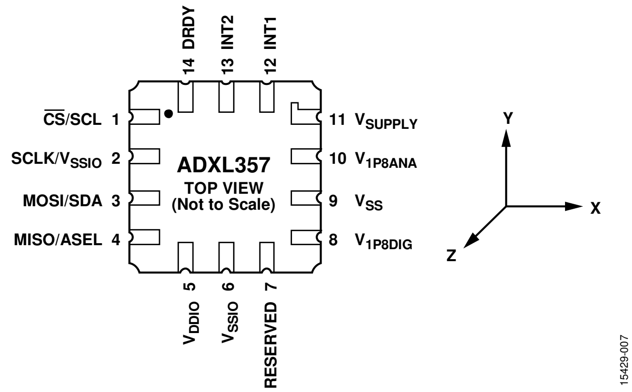


Figure 7. ADXL357 Pin Configuration (SPI/I²C)

Table 9. ADXL357 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$/SCL	Chip Select for SPI ($\overline{CS}$). Serial Communications Clock for I²C (SCL).
2	SCLK/V_{SSIO}	Serial Communications Clock for SPI (SCLK). I²C Mode Enable (V_{SSIO}). Connect this pin to Pin 6 (V_{SSIO}) to enable I²C mode.
3	MOSI/SDA	Master Output, Slave Input for SPI (MOSI). Serial Data for I²C (SDA).
4	MISO/ASEL	Master Input, Slave Output for SPI (MISO). Alternate I²C Address Select for I²C (ASEL).
5	V_{DDIO}	Digital Interface Supply Voltage.
6	V_{SSIO}	Digital Ground.
7	RESERVED	Reserved. This pin can be connected to ground or left open.
8	V_{1P8DIG}	Digital Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS}, supply the voltage to this pin externally.
9	V_{SS}	Analog Ground.
10	V_{1P8ANA}	Analog Supply. This pin requires a decoupling capacitor. If V_{SUPPLY} connects to V_{SS}, supply the voltage to this pin externally.
11	V_{SUPPLY}	Supply Voltage. When V_{SUPPLY} equals 2.25 V to 3.6 V, V_{SUPPLY} enables the internal LDOs to generate V_{1P8DIG} and V_{1P8ANA}. For V_{SUPPLY} = V_{SS}, V_{1P8DIG} and V_{1P8ANA} are externally supplied.
12	INT1	Interrupt Pin 1.
13	INT2	Interrupt Pin 2.
14	DRDY	Data Ready Pin.

TYPICAL PERFORMANCE CHARACTERISTICS

All figures include data for multiple devices and multiple lots, and they were taken in the ±10 *g* range, unless otherwise noted.

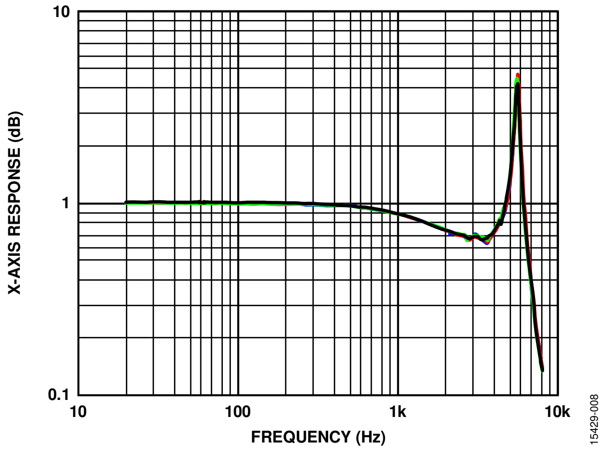


Figure 8. ADXL356 Frequency Response for X-Axis

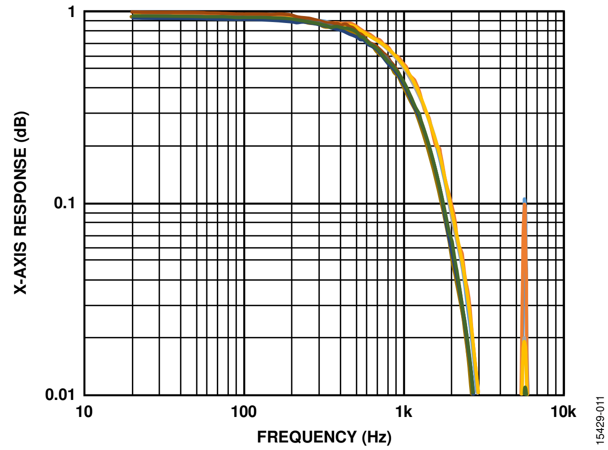


Figure 11. ADXL357 Normalized Frequency Response for X-Axis at 4 kHz ODR

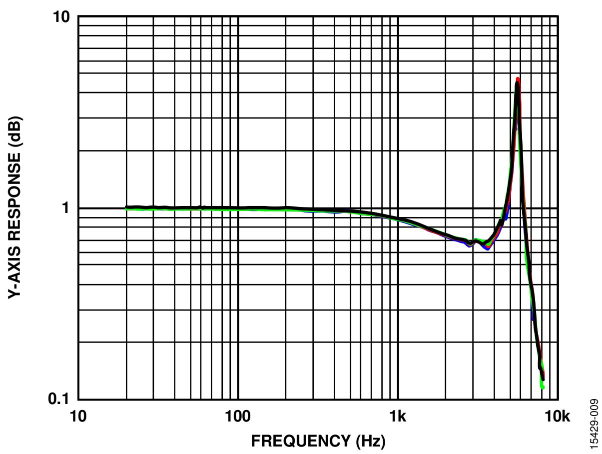


Figure 9. ADXL356 Frequency Response for Y-Axis

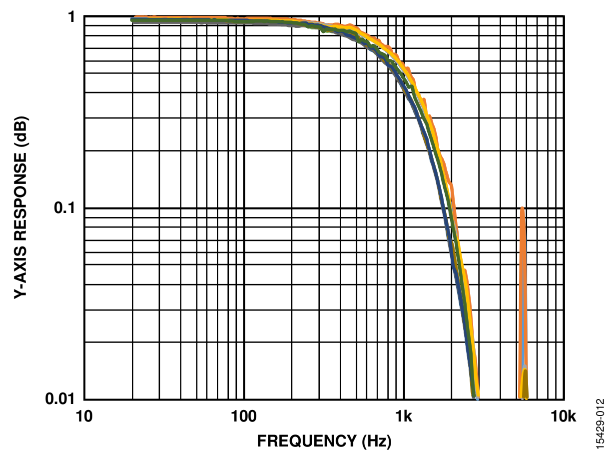


Figure 12. ADXL357 Normalized Frequency Response for Y-Axis at 4 kHz ODR

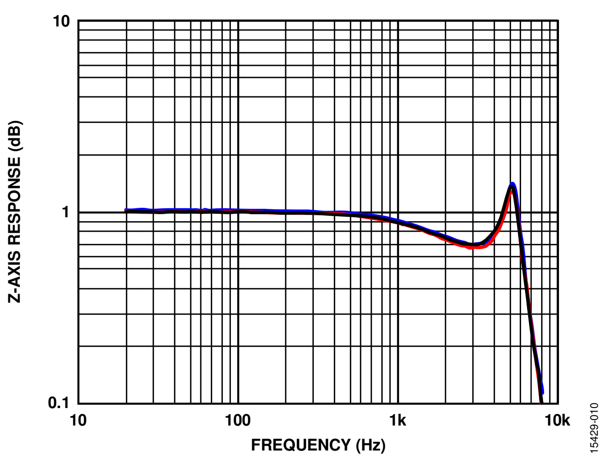


Figure 10. ADXL356 Frequency Response for Z-Axis

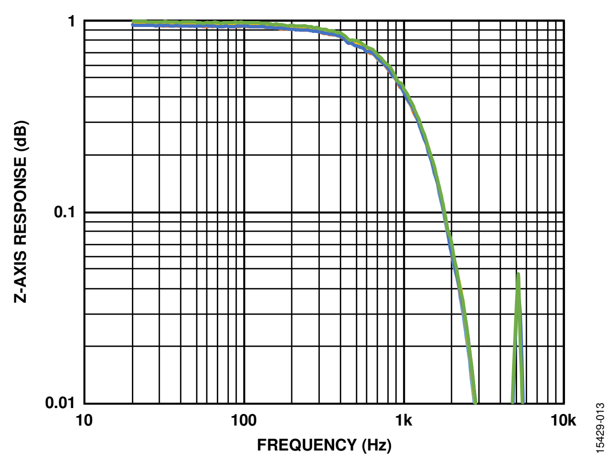


Figure 13. ADXL357 Normalized Frequency Response for Z-Axis at 4 kHz ODR

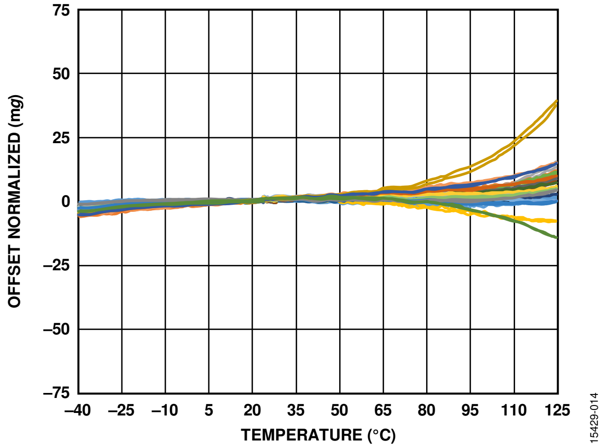


Figure 14. ADXL356 X-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

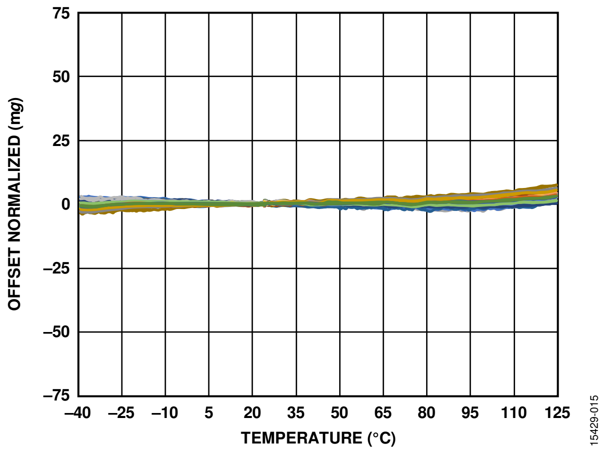


Figure 15. ADXL356 Y-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

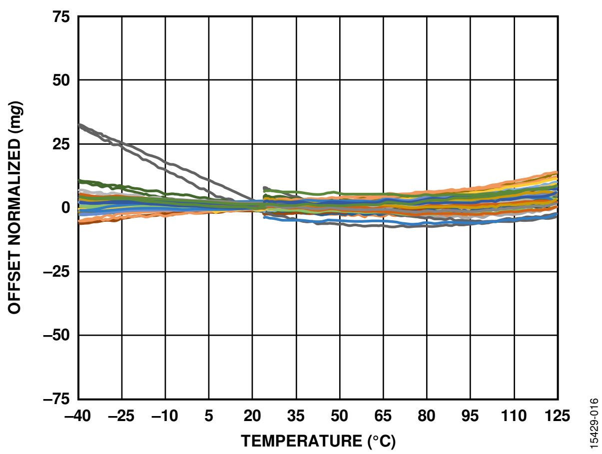


Figure 16. ADXL356 Z-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

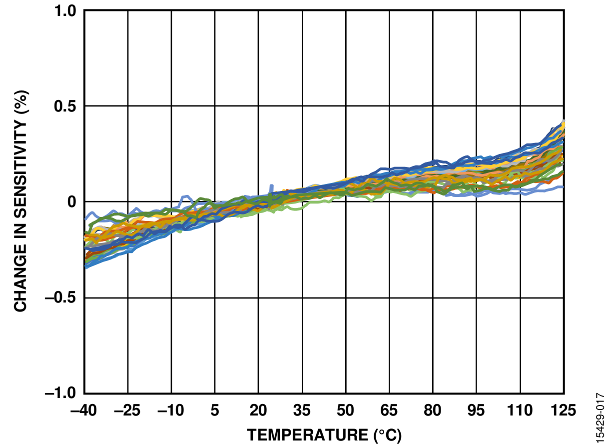


Figure 17. ADXL356 X-Axis Change in Sensitivity Relative to 25°C vs. Temperature

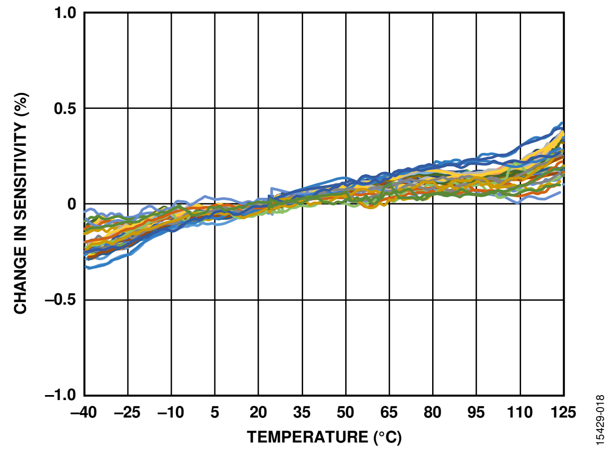


Figure 18. ADXL356 Y-Axis Change in Sensitivity Relative to 25°C vs. Temperature

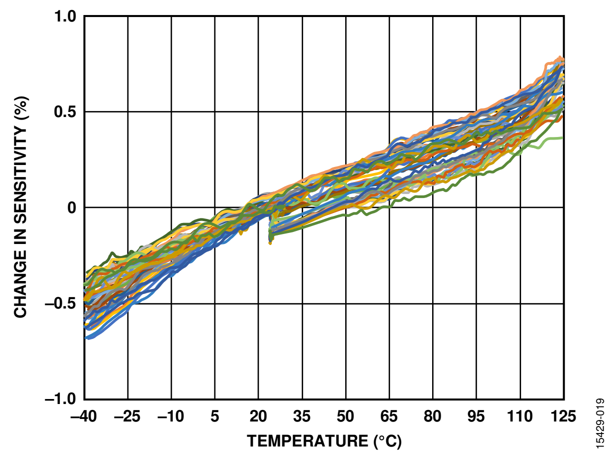


Figure 19. ADXL356 Z-Axis Change in Sensitivity Relative to 25°C vs. Temperature

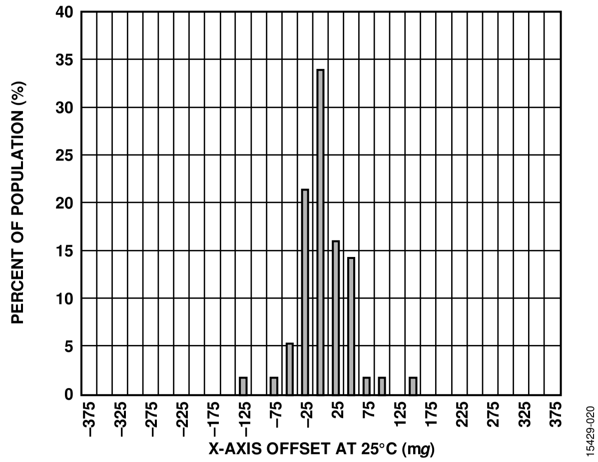


Figure 20. ADXL356 Zero g Offset Histogram at 25°C, X-Axis

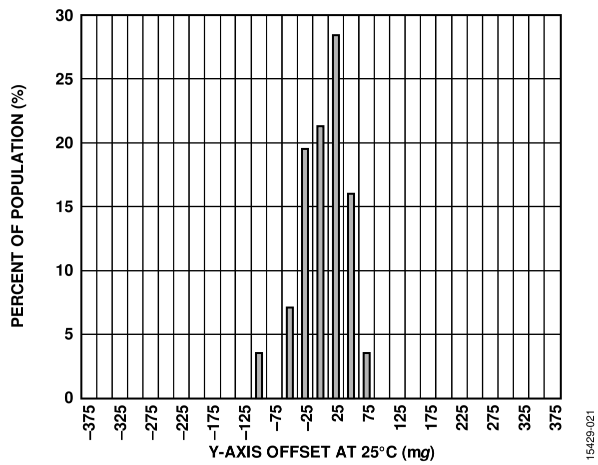


Figure 21. ADXL356 Zero g Offset Histogram at 25°C, Y-Axis

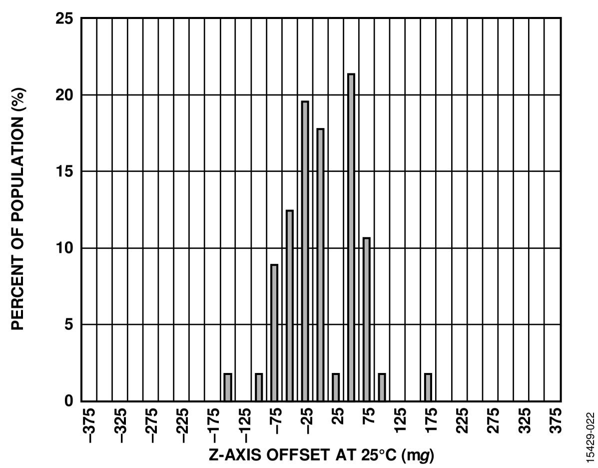


Figure 22. ADXL356 Zero g Offset Histogram at 25°C, Z-Axis

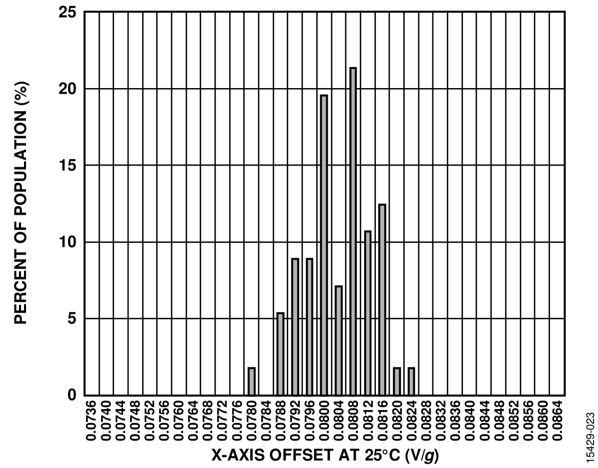


Figure 23. ADXL356 Sensitivity Histogram at 25°C, X-Axis

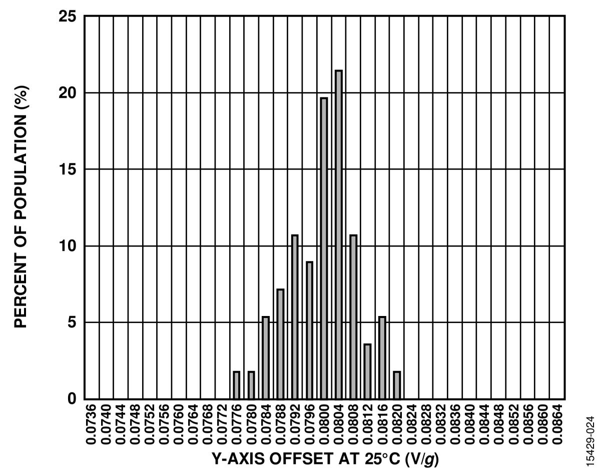


Figure 24. ADXL356 Sensitivity Histogram at 25°C, Y-Axis

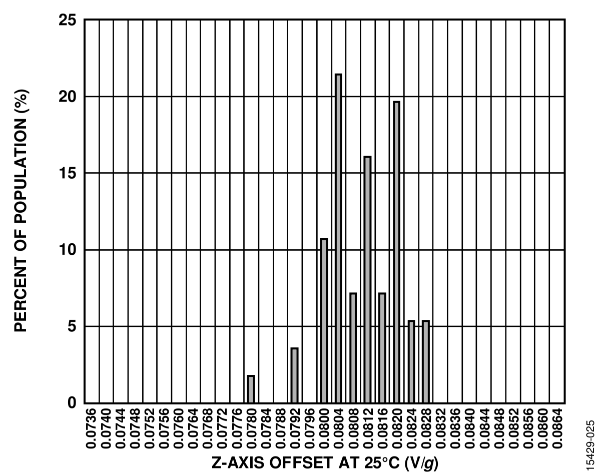


Figure 25. ADXL356 Sensitivity Histogram at 25°C, Z-Axis

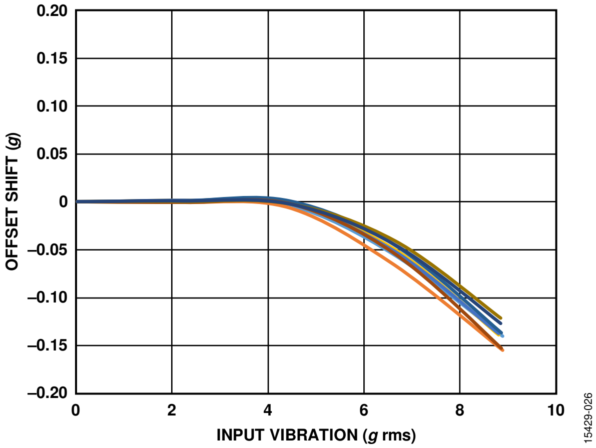


Figure 26. ADXL356 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±10 g Range, X-Axis Orientation = −1 g

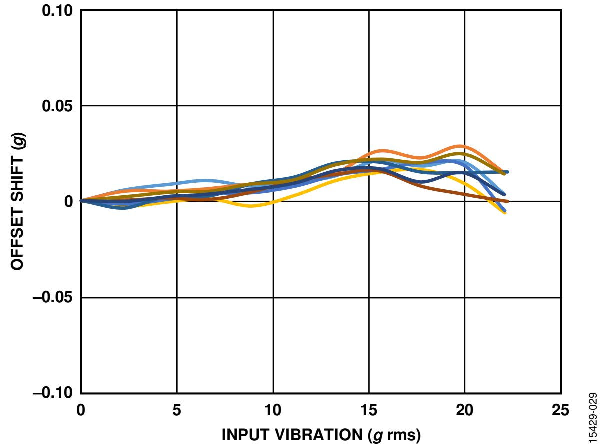


Figure 29. ADXL356 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±40 g Range, X-Axis Orientation = −1 g

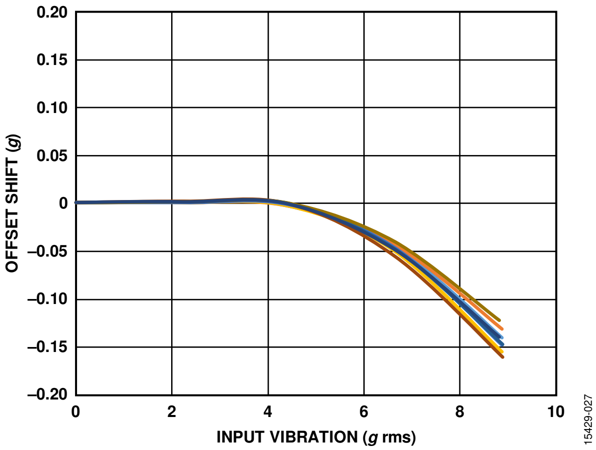


Figure 27. ADXL356 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±10 g Range, Y-Axis Orientation = +1 g

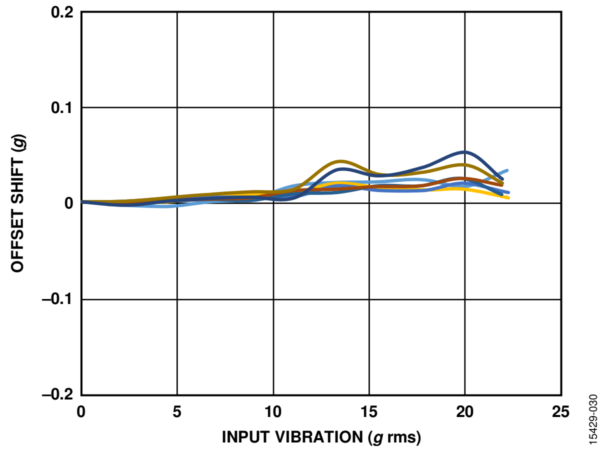


Figure 30. ADXL356 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±40 g Range, Y-Axis Orientation = +1 g

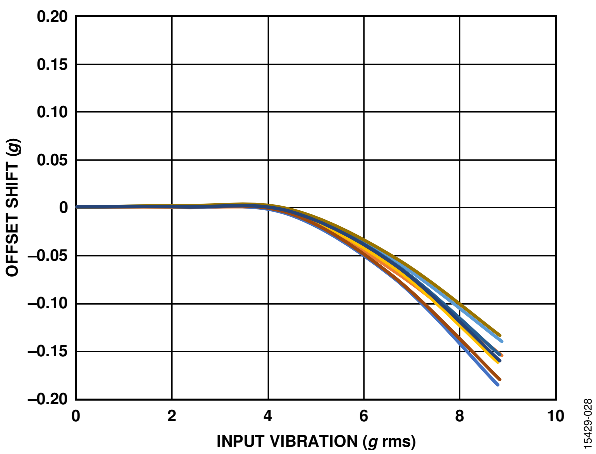


Figure 28. ADXL356 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±10 g Range, Z-Axis Orientation = +1 g

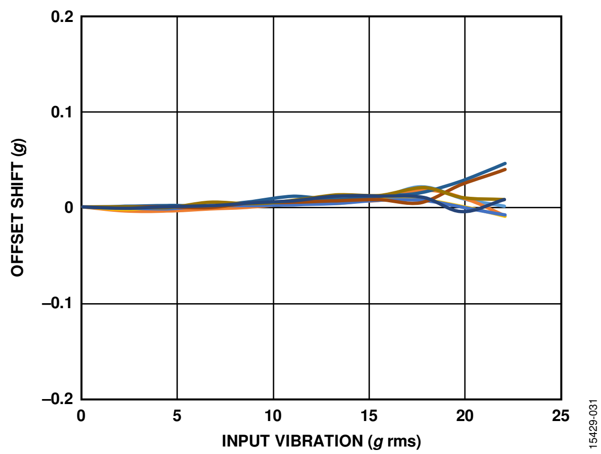


Figure 31. ADXL356 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±40 g Range, Z-Axis Orientation = +1 g

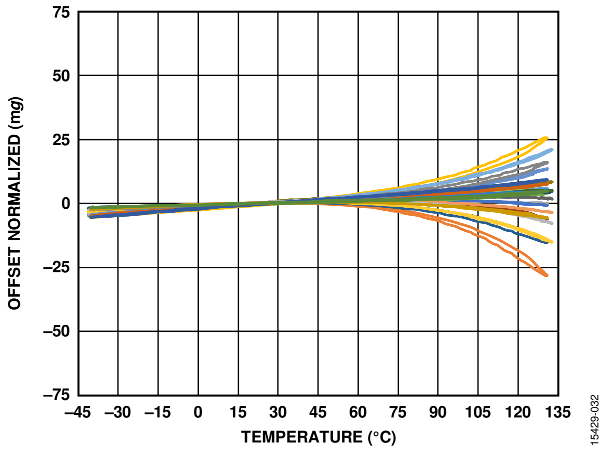


Figure 32. ADXL357 X-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

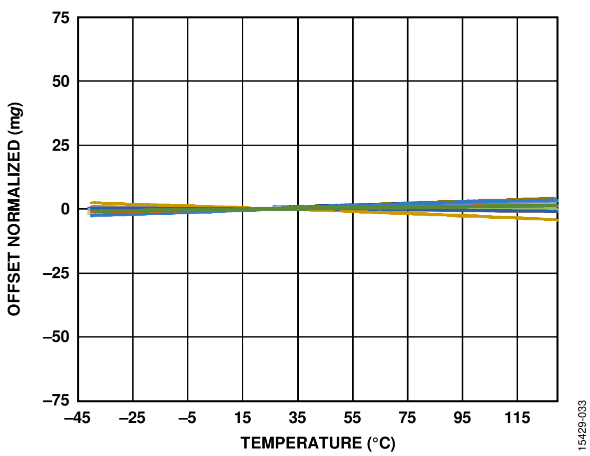


Figure 33. ADXL357 Y-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

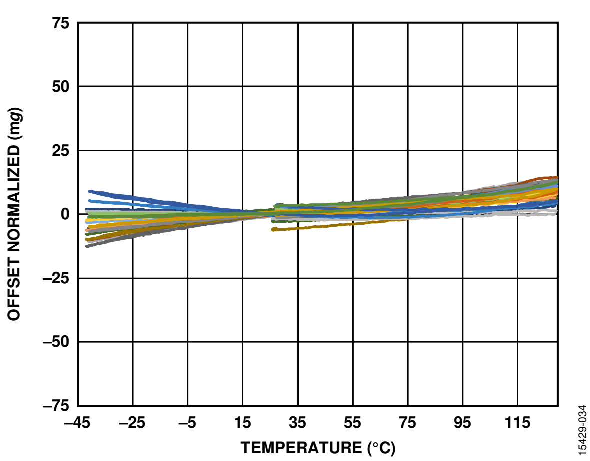


Figure 34. ADXL357 Z-Axis Zero g Offset Normalized Relative to 25°C vs. Temperature

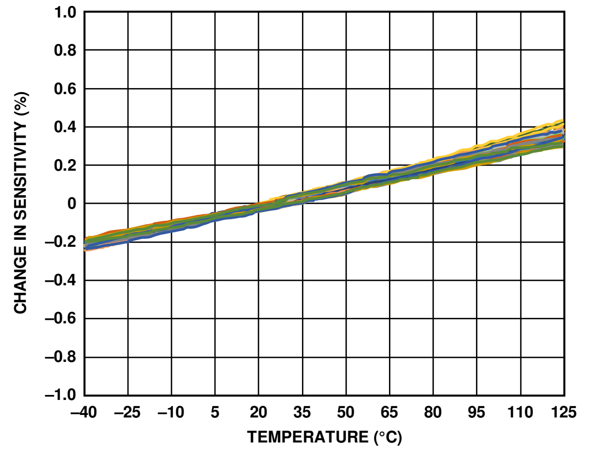


Figure 35. ADXL357 X-Axis Change in Sensitivity Relative to 25°C vs. Temperature

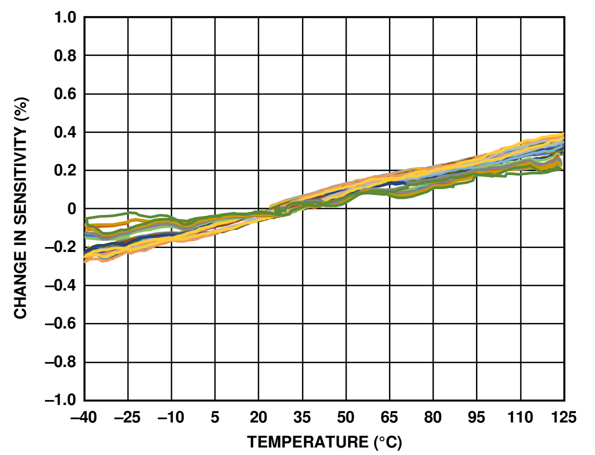


Figure 36. ADXL357 Y-Axis Change in Sensitivity Relative to 25°C vs. Temperature

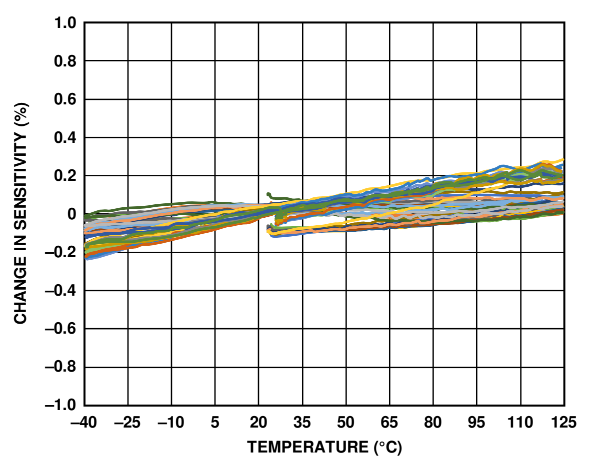


Figure 37. ADXL357 Z-Axis Change in Sensitivity Relative to 25°C vs. Temperature

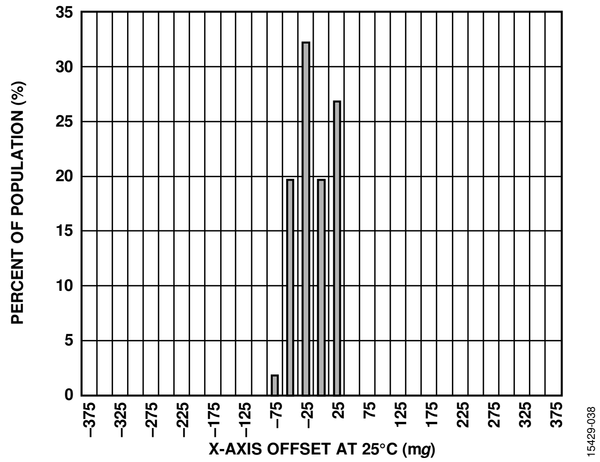


Figure 38. ADXL357 Zero g Offset Histogram at 25°C, X-Axis

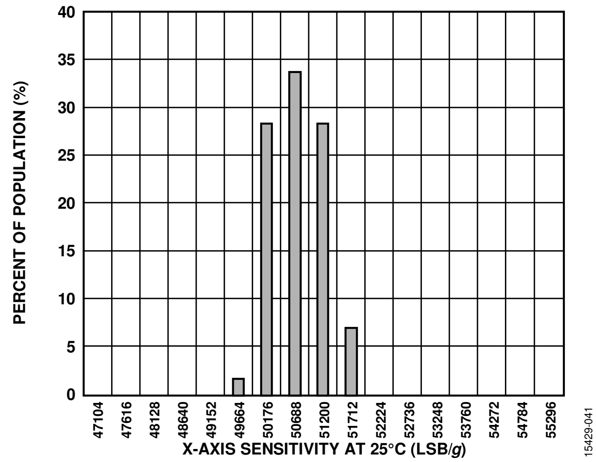


Figure 41. ADXL357 Sensitivity Histogram at 25°C, X-Axis

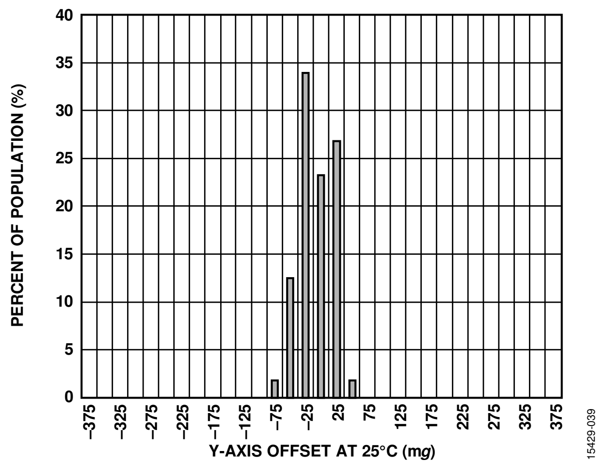


Figure 39. ADXL357 Zero g Offset Histogram at 25°C, Y-Axis

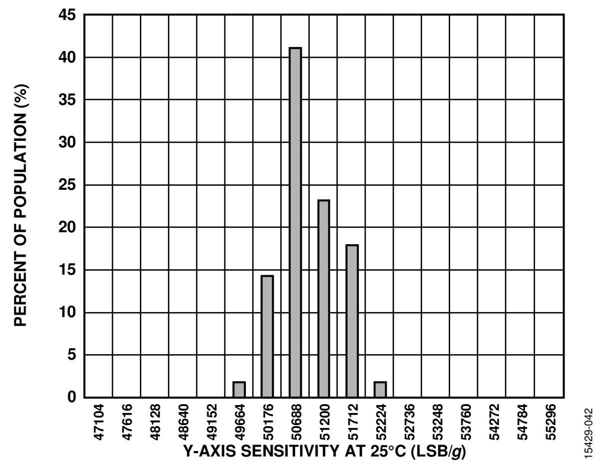


Figure 42. ADXL357 Sensitivity Histogram at 25°C, Y-Axis

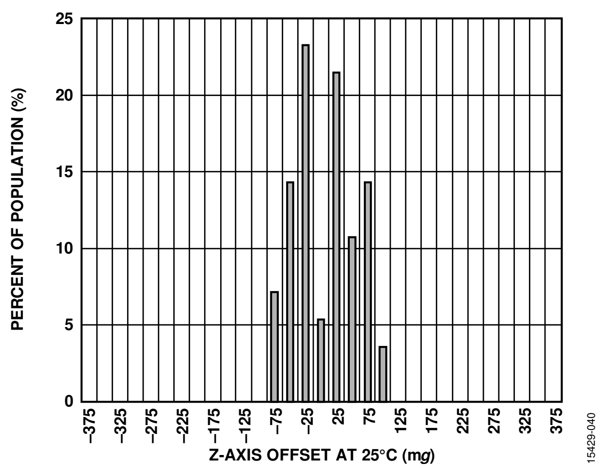


Figure 40. ADXL357 Zero g Offset Histogram at 25°C, Z-Axis

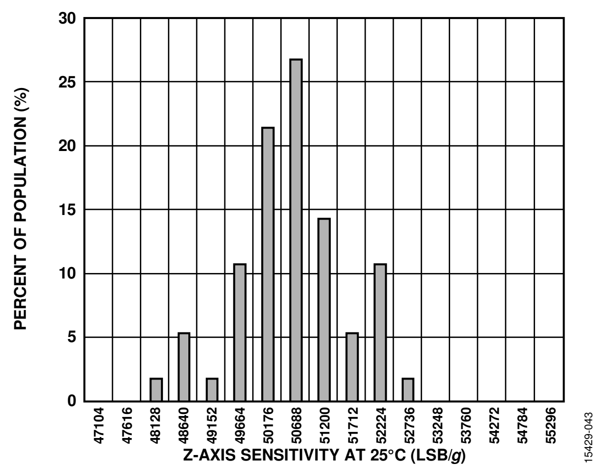


Figure 43. ADXL357 Sensitivity Histogram at 25°C, Z-Axis

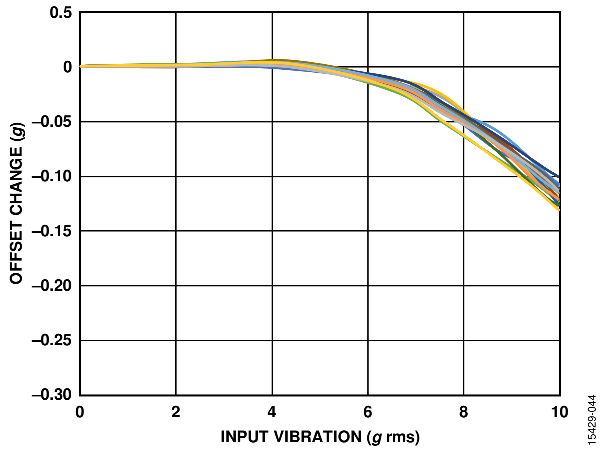


Figure 44. ADXL357 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±10 g Range, X-Axis Orientation = −1 g

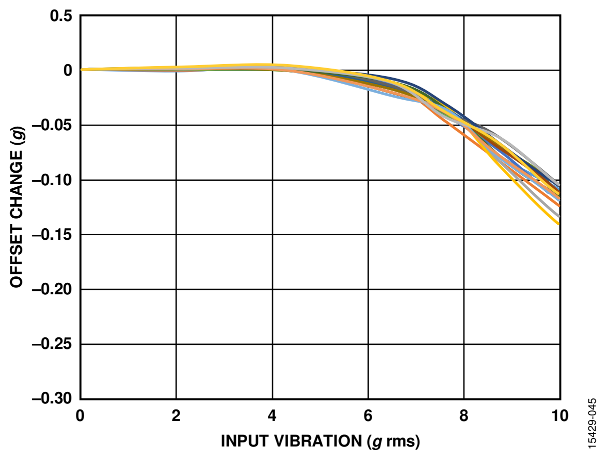


Figure 45. ADXL357 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±10 g Range, Y-Axis Orientation = +1 g

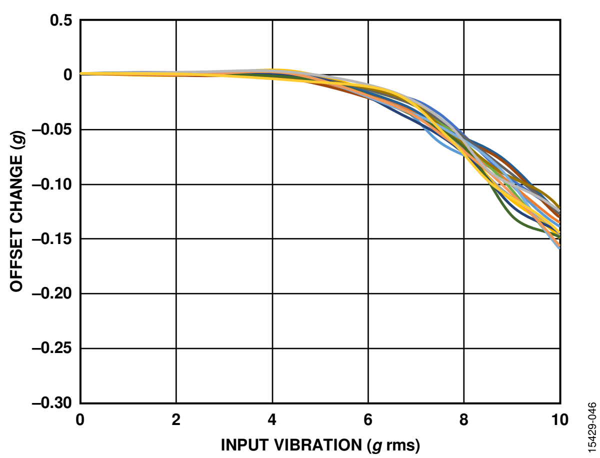


Figure 46. ADXL357 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±10 g Range, Z-Axis Orientation = +1 g

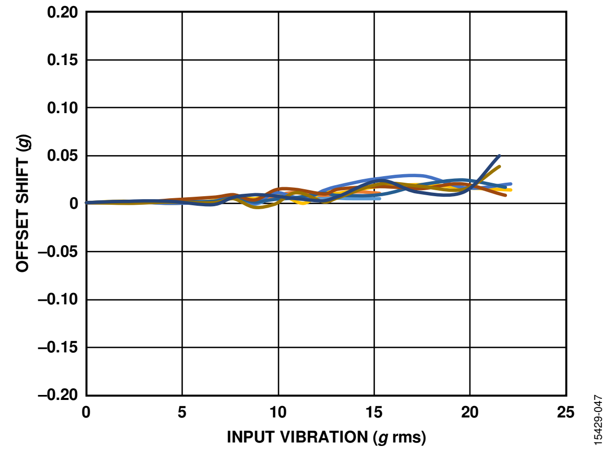


Figure 47. ADXL357 Vibration Rectification Error (VRE), X-Axis Offset from +1 g, ±40 g Range, X-Axis Orientation = −1 g

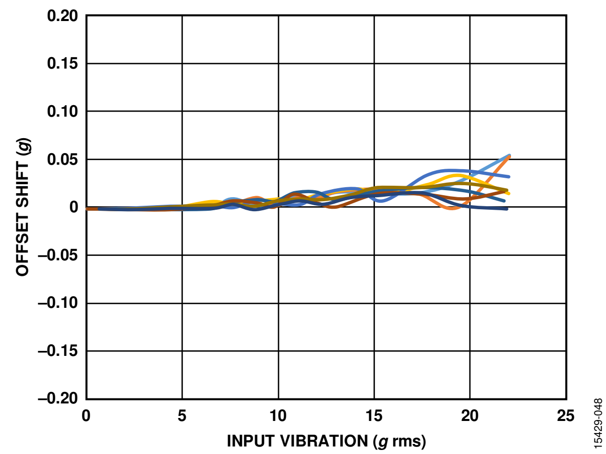


Figure 48. ADXL357 Vibration Rectification Error (VRE), Y-Axis Offset from +1 g, ±40 g Range, Y-Axis Orientation = +1 g

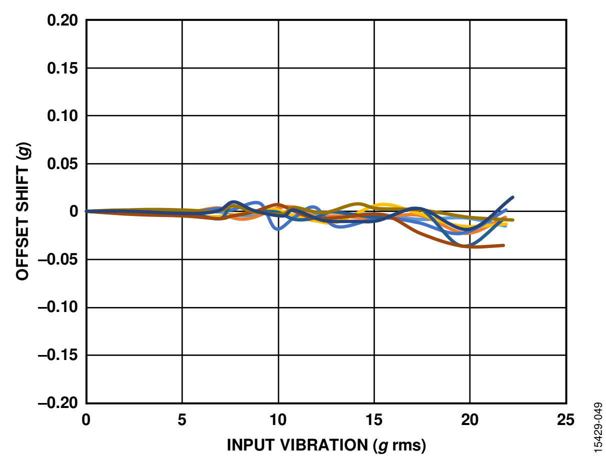


Figure 49. ADXL357 Vibration Rectification Error (VRE), Z-Axis Offset from +1 g, ±40 g Range, Z-Axis Orientation = +1 g

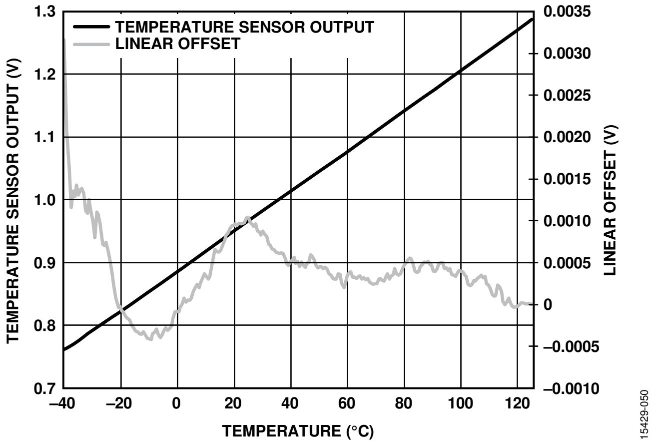


Figure 50. ADXL356 Temperature Sensor Output and Linearity Offset vs. Temperature

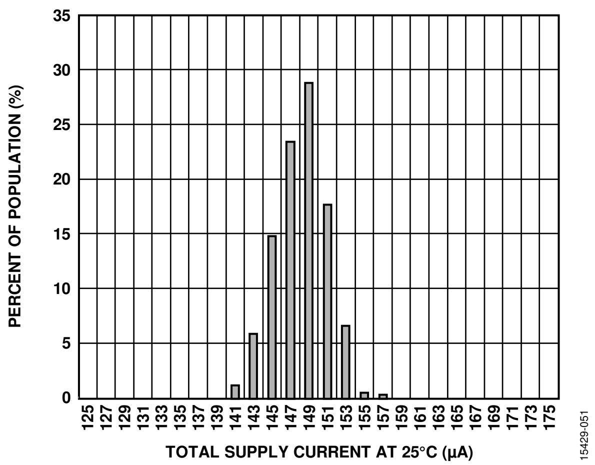


Figure 51. ADXL356 Total Supply Current, 3.3 V

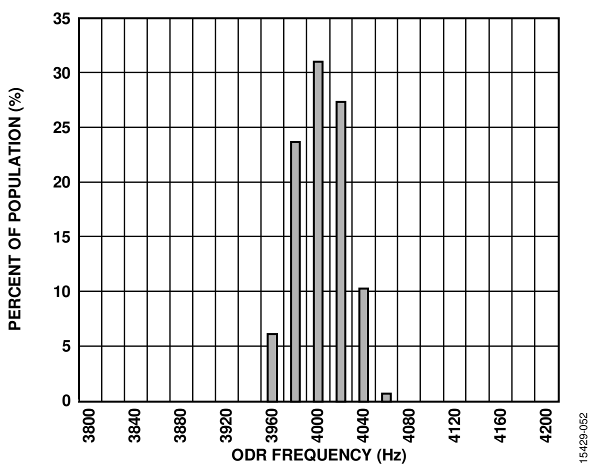


Figure 52. ADXL357 Internal ODR Frequency Histogram

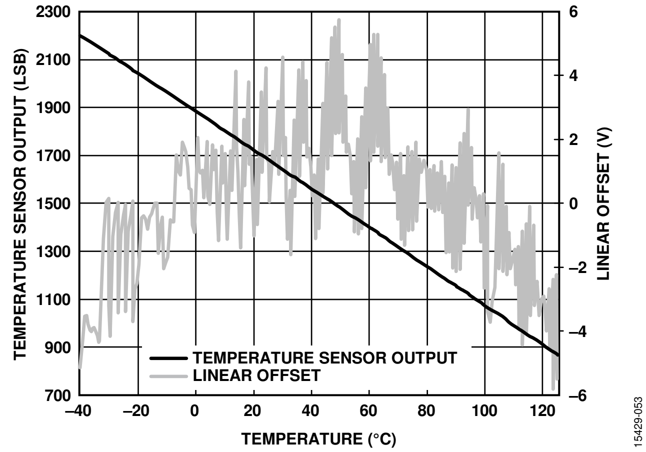


Figure 53. ADXL357 Temperature Sensor Output and Linearity Offset vs. Temperature

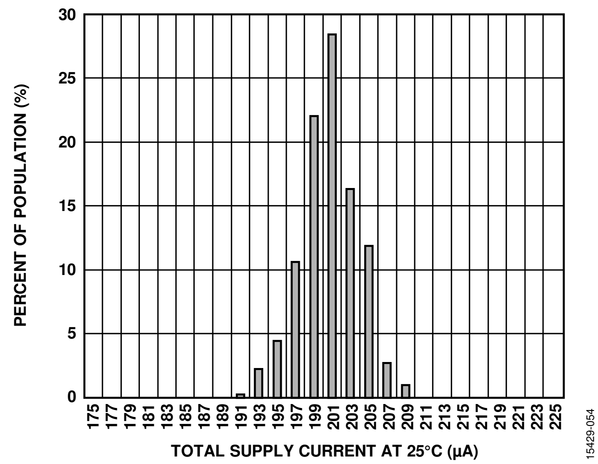


Figure 54. ADXL357 Total Supply Current, 3.3 V

ROOT ALLAN VARIANCE (RAV) ADXL357 CHARACTERISTICS

Figure 55 to Figure 57 include data for multiple devices and multiple lots, and they were taken in the ±10 *g* range, unless otherwise noted.

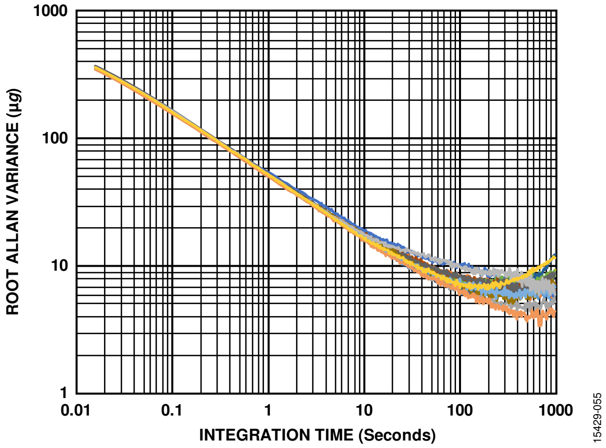


Figure 55. ADXL357 Root Allan Variance (RAV), X-Axis

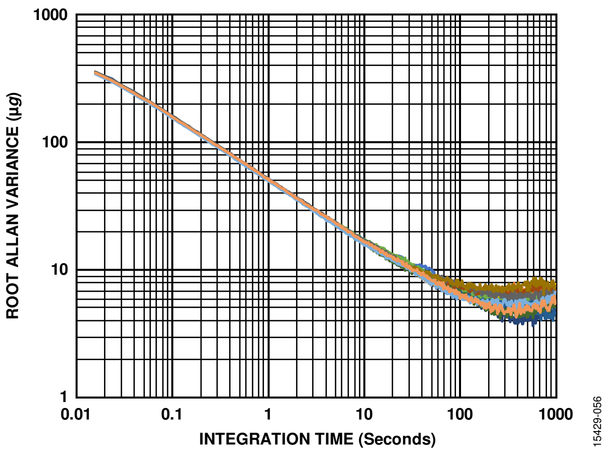


Figure 56. ADXL357 Root Allan Variance (RAV), Y-Axis

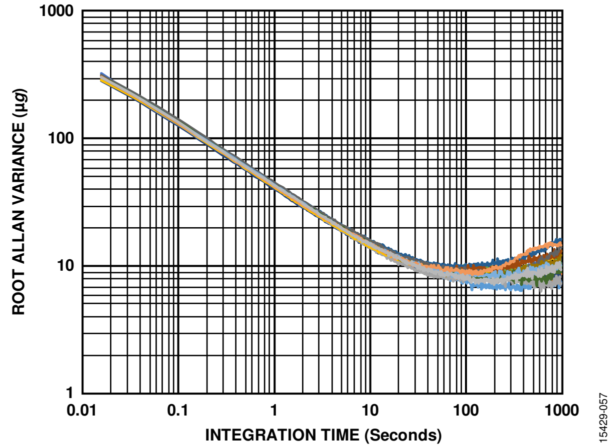


Figure 57. ADXL357 Root Allan Variance (RAV), Z-Axis

THEORY OF OPERATION

The ADXL356 is a complete 3-axis, ultralow noise and ultrastable offset MEMS accelerometer with outputs ratiometric to the analog 1.8 V supply, V_{1P8ANA}. The ADXL357 adds three high resolution ADCs that use the analog 1.8 V supply as a reference to provide digital outputs insensitive to the supply voltage. The ADXL356B is pin selectable for ±10 *g* or ±20 *g* full scale, the ADXL356C is pin selectable for ±10 *g* or ±40 *g* full scale, and the ADXL357 is programmable for ±10.24 *g*, ±20.48 *g*, and ±40.96 *g* full scale. The ADXL357 offers both SPI and I^2C communications ports.

The micromachined, sensing elements are fully differential, comprising the lateral x-axis and y-axis sensors and the vertical, teeter totter z-axis sensors. The x-axis and y-axis sensors and the z-axis sensors go through separate signal paths that minimize offset drift and noise. The signal path is fully differential, except for a differential to single-ended conversion at the analog outputs of the ADXL356.

The analog accelerometer outputs of the ADXL356 are ratiometric to V_{1P8ANA}; therefore, carefully digitize them correctly. The temperature sensor output is not ratiometric. The X_{OUT}, Y_{OUT}, and Z_{OUT} analog outputs are filtered internally with an antialiasing filter. These analog outputs also have an internal 32 kΩ series resistor that can be used with an external capacitor to set the bandwidth of the output.

The ADXL357 includes antialias filters before and after the high resolution Σ-Δ ADC. User-selectable output data rates and filter corners are provided. The temperature sensor is digitized with a 12-bit successive approximation register (SAR) ADC.

APPLICATIONS INFORMATION

ANALOG OUTPUT

Figure 58 shows the ADXL356 application circuit. The analog outputs (X_{OUT}, Y_{OUT}, and Z_{OUT}) are ratiometric to the 1.8 V analog voltage from the V_{1P8ANA} pin. V_{1P8ANA} can be powered with an on-chip LDO regulator that is powered from V_{SUPPLY}. V_{1P8ANA} can also be supplied externally by forcing V_{SUPPLY} to V_{SS}, which disables the LDO regulator. Due to the ratiometric response, the analog output requires referencing to the V_{1P8ANA} supply when digitizing to achieve the inherent noise and offset performance of the ADXL356. The 0 *g* bias output is nominally equal to $V_{1P8ANA}/2$. The recommended option is to use the ADXL356 with a ratiometric ADC (for example, the Analog Devices, Inc., AD7682) with V_{1P8ANA} providing the voltage reference. This configuration results in self cancellation of errors due to minor supply variations.

The ADXL356 outputs two forms of filtering: internal anti-aliasing filtering with a cutoff frequency of approximately 1.5 kHz, and external filtering. The external filter uses a fixed, on-chip, 32 kΩ resistance in series with each output in conjunction with the external capacitors to implement the low-pass filter antialiasing and noise reduction prior to the external ADC. The antialias filter cutoff frequency must be significantly higher than the desired signal bandwidth. If the antialias filter corner is too low, ratiometricity can degrade where the signal attenuation is different from the reference attenuation.

DIGITAL OUTPUT

Figure 59 shows the ADXL357 application circuit with the recommended bypass capacitors. The communications interface is either SPI or I²C (see the Serial Communications section for additional information).

The ADXL357 includes an internal configurable digital band-pass filter. Both the high-pass and low-pass poles of the filter are adjustable, as detailed in the Filter Settings Register section and Table 44. At power-up, the default conditions for the filters are as follows:

- High-pass filter (HPF) = dc (off)
- Low-pass filter (LPF) = 1000 Hz
- Output data rate = 4000 Hz

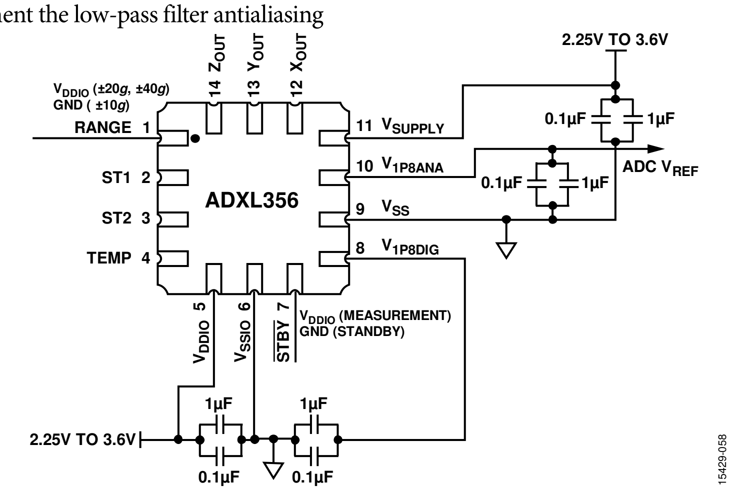


Figure 58. ADXL356 Application Circuit

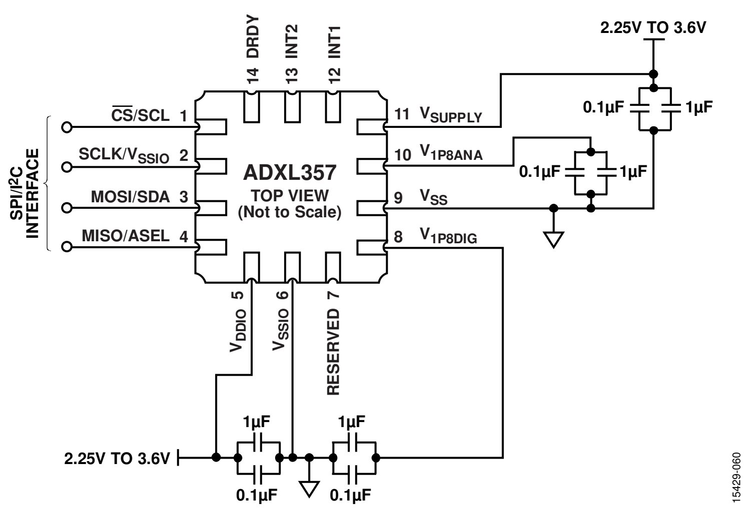


Figure 59. ADXL357 Application Circuit

AXES OF ACCELERATION SENSITIVITY

Figure 60 shows the axes of acceleration sensitivity. Note that the output voltage increases when accelerated along the sensitive axis.

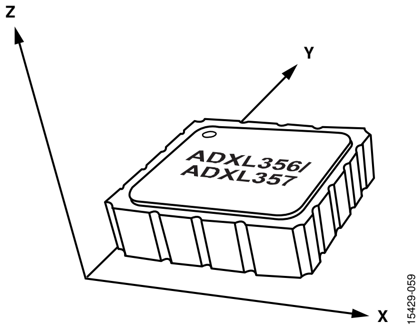


Figure 60. Axes of Acceleration Sensitivity

POWER SEQUENCING

There are two methods for applying power to the device. Typically, internal LDO regulators generate the 1.8 V power for the analog and digital supplies, V_{1P8ANA} and V_{1P8DIG}, respectively. Optionally, connecting V_{SUPPLY} to V_{SS} and driving V_{1P8ANA} and V_{1P8DIG} with an external supply can supply V_{1P8ANA} and V_{1P8DIG}.

When using the internal LDO regulators, connect V_{SUPPLY} to a voltage source between 2.25 V to 3.6 V. In this case, V_{DDIO} and V_{SUPPLY} can be powered in parallel. V_{SUPPLY} must not exceed the V_{DDIO} voltage by greater than 0.5 V. If necessary, V_{DDIO} can be powered before V_{SUPPLY}.

When disabling the internal LDO regulators and using an external 1.8 V supply to power V_{1P8ANA} and V_{1P8DIG}, tie V_{SUPPLY} to ground, and set V_{1P8ANA} and V_{1P8DIG} to the same final voltage level. In the case of bypassing the LDOs, the recommended power sequence is to apply power to V_{DDIO}, followed by V_{1P8DIG} approximately 10 µs later, and then V_{1P8ANA} approximately 10 µs later. If necessary, V_{1P8DIG} and V_{DDIO} can be powered from the same 1.8 V supply, which can also be tied to V_{1P8ANA} with proper isolation. In this case, proper decoupling and low frequency isolation is important to maintain the noise performance of the sensor.

POWER SUPPLY DESCRIPTION

The ADXL356/ADXL357 have four different power supply domains: V_{SUPPLY}, V_{1P8ANA}, V_{1P8DIG}, and V_{DDIO}. The internal analog and digital circuitry operates at 1.8 V nominal.

V_{SUPPLY}

V_{SUPPLY} is 2.25 V to 3.6 V, which is the input range to the two LDO regulators that generate the nominal 1.8 V outputs for V_{1P8ANA} and V_{1P8DIG}. Connect V_{SUPPLY} to V_{SS} to disable the LDO regulators, which allows driving V_{1P8ANA} and V_{1P8DIG} from an external source.

V_{1P8ANA}

All sensor and analog signal processing circuitry operates in this domain. Offset and sensitivity of the analog output ADXL356 are ratiometric to this supply voltage. When using external ADCs, use V_{1P8ANA} as the reference voltage. The digital output ADXL357 includes ADCs that are ratiometric to V_{1P8ANA}, thereby rendering offset and sensitivity insensitive to the value of V_{1P8ANA}. V_{1P8ANA} can be an input or an output as defined by the state of the V_{SUPPLY} voltage.

V_{1P8DIG}

V_{1P8DIG} is the supply voltage for the internal logic circuitry. A separate LDO regulator decouples the digital supply noise from the analog signal path. V_{1P8ANA} can be an input or an output as defined by the state of the V_{SUPPLY} voltage. If driven externally, V_{1P8DIG} must be the same voltage as the V_{1P8ANA} voltage.

V_{DDIO}

The V_{DDIO} value determines the logic high levels. On the analog output ADXL356, V_{DDIO} sets the logic high level for the self test pins, ST1 and ST2, as well as the $\overline{\text{STBY}}$ pin. On the digital output ADXL357, V_{DDIO} sets the logic high level for communications interface ports, as well as the interrupt and DRDY outputs.

The LDO regulators are operational when V_{SUPPLY} is between 2.25 V and 3.6 V. V_{1P8ANA} and V_{1P8DIG} are the regulator outputs in this mode. Alternatively, when tying V_{SUPPLY} to V_{SS}, V_{1P8ANA} and V_{1P8DIG} are supply voltage inputs with a 1.62 V to 1.98 V range.

OVERRANGE PROTECTION

To avoid electrostatic capture of the proof mass when the accelerometer is subject to input acceleration beyond its full-scale range, all sensor drive clocks turn off for 0.5 ms. In the ±10 *g*/±10.24 *g* range setting, the overrange protection activates for input signals beyond approximately ±40 *g* (±25%), and for the ±20 *g*/±20.48 *g* and ±40 *g*/±40.95 *g* range settings, the threshold corresponds to about ±80 *g* (±25%).

When overrange protection occurs, the X_{OUT}, Y_{OUT}, and Z_{OUT} pins on the ADXL356 begin to drive to midscale. The ADXL357 floats toward zero, and first in, first out (FIFO) buffer begins filling with this data.

SELF TEST

The ADXL356 and ADXL357 incorporate a self test feature that effectively tests the mechanical and electronic system. Enabling self test stimulates the sensor electrostatically to produce an output corresponding to the test signal applied as well as the mechanical force exerted. Only the z-axis response is specified to validate device functionality.

In the ADXL356, drive the ST1 pin to V_{DDIO} to invoke self test mode. Then, by driving the ST2 pin to V_{DDIO}, the ADXL356 applies an electrostatic force to the mechanical sensor and induces a change in output in response to the force. The self test delta (or response) is the difference in output voltage in the z-axis when ST2 is high vs. ST2 is low, while ST1 is asserted. After the self test measurement is complete, bring both pins low to resume normal operation.

The self test operation is similar in the ADXL357, except ST1 and ST2 can be accessed through the SELF_TEST register (Register 0x2E).

The self test feature rejects externally applied acceleration and only responds to the self test force, which allows an accurate measurement of the self test, even in the presence of external mechanical noise.

FILTER

The ADXL356/ADXL357 use an analog, low-pass, antialiasing filter to reduce out of band noise and to limit bandwidth. The ADXL357 provides further digital filtering options to maintain excellent noise performance at various ODRs.

The analog, low-pass antialiasing filter in the ADXL356/ ADXL357 provides a fixed bandwidth of approximately 1.5 kHz, the frequency at which the output response is attenuated by approximately 50%. The shape of the filter response in the frequency domain is that of a sinc3 filter.

The ADXL356 x-axis, y-axis, and z-axis analog outputs include an amplifier followed by a series 32 kΩ resistor, and output to the X_{OUT}, the Y_{OUT}, and the Z_{OUT} pins, respectively.

The ADXL357 provides an internal 20-bit, Σ-Δ ADC to digitize the filtered analog signal. Additional digital filtering (beyond the analog, low-pass, antialiasing filter) consists of a low-pass digital decimation filter and a bypassable high-pass filter that supports output data rates between 4 kHz and 3.906 Hz. The decimation filter consists of two stages. The first stage is fixed decimation with a 4 kHz ODR with a low-pass filter cutoff (50% reduction in output response) at about 1 kHz. A variable second stage decimation filter is used for the 2 kHz output data rate and below (it is bypassed for 4 kHz ODR). Figure 61 shows the low-pass filter response with a 1 kHz corner (4 kHz ODR) for the ADXL357. Note that Figure 61 does not include the fixed frequency analog, low-pass, antialiasing filter with a fixed bandwidth of approximately 1.5 kHz.

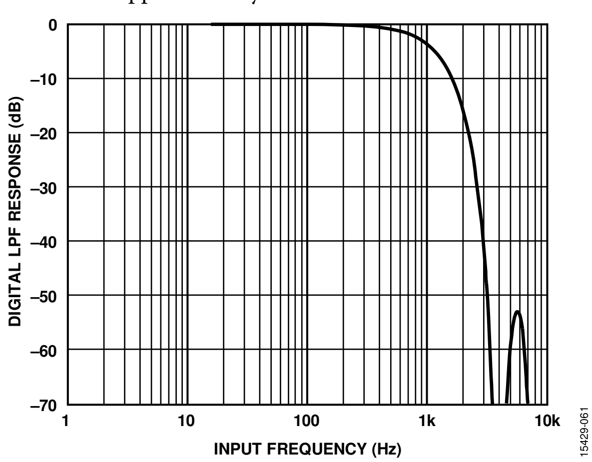


Figure 61. ADXL357 Digital Low-Pass Filter (LPF) Response for 4 kHz ODR

The ADXL357 pass band of the signal path relates to the combined filter responses, including the analog filter previously described, and the digital decimation filter/ODR setting. Table 10 shows the delay associated with the decimation filter for each setting and provides the attenuation at the ODR/4 corner.

The ADXL357 also includes an optional digital high-pass filter with a programmable corner frequency. By default, the high-pass filter is disabled. The high-pass corner frequency, where the output is attenuated by 50%, is related to the ODR, and the HPF_CORNER setting in the filter register (Register 0x28, Bits[6:4]). Table 11 shows the HPF_CORNER response. Figure 62 and Figure 63 show the simulated high-pass filter response and delay for a 10 Hz cutoff.

The ADXL357 also includes an interpolation filter, after the decimation filters, that produces oversampled/upconverted data and provides an external synchronization option. See the Data Synchronization section for more details. Table 12 shows the delay and attenuation relative to the programmed ODR.

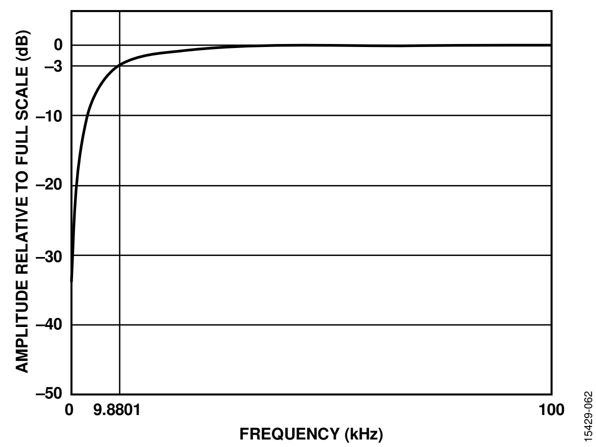


Figure 62. High-Pass Filter Pass-Band Response for a 4 kHz ODR and an HPF_CORNER Setting of 001 (Register 0x28, Bits[6:4])

Group delay is the digital filter delay from the input to the ADC until data is available at the interface (see the Filter section). This delay is the largest component of the total delay from sensor to serial interface.

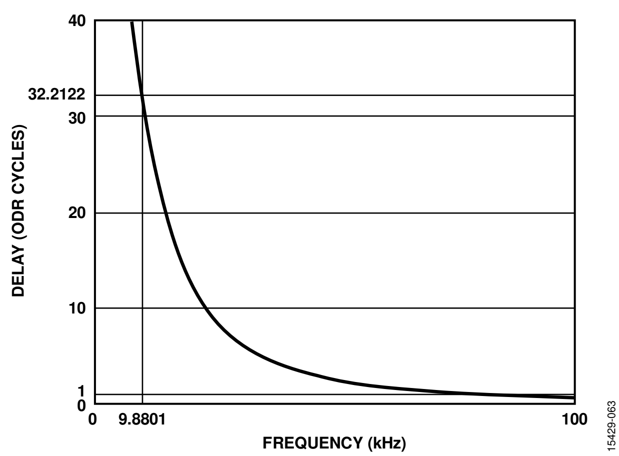


Figure 63. High-Pass Filter Delay Response for a 4 kHz ODR and an HPF_CORNER Setting of 001 (Register 0x28, Bits[6:4])

Table 10. Digital Filter Group Delay and Profile

	Delay		Attenuation	
Programmed ODR (Hz)	ODR (Cycles)	Time (ms)	Decimator at ODR/4 (dB)	Full Path at ODR/4 (dB)
4000	2.52	0.63	−3.44	−3.63
4000/2 = 2000	2.00	1.00	−2.21	−2.26
4000/4 = 1000	1.78	1.78	−1.92	−1.93
4000/8 = 500	1.63	3.26	−1.83	−1.83
4000/16 = 250	1.57	6.27	−1.83	−1.83
4000/32 = 125	1.54	12.34	−1.83	−1.83
4000/64 = 62.5	1.51	24.18	−1.83	−1.83
4000/128 ~ 31	1.49	47.59	−1.83	−1.83
4000/256 ~ 16	1.50	96.25	−1.83	−1.83
4000/512 ~ 8	1.50	189.58	−1.83	−1.83
4000/1024 ~ 4	1.50	384.31	−1.83	−1.83

Table 11. Digital High-Pass Filter Response

HPF_CORNER Register Setting (Register 0x28, Bits[6:4])	HPF_CORNER Frequency, −3 dB Point Relative to ODR Setting	−3 dB at 4 kHz ODR (Hz)
000	Not applicable, no high-pass filter enabled	Off
001	$247 \times 10^{-3} \times$ ODR	9.88
010	$62.084 \times 10^{-3} \times$ ODR	2.48
011	$15.545 \times 10^{-3} \times$ ODR	0.62
100	$3.862 \times 10^{-3} \times$ ODR	0.1545
101	$0.954 \times 10^{-3} \times$ ODR	0.03816
110	$0.238 \times 10^{-3} \times$ ODR	0.00952

Table 12. Combined Digital Interpolation Filter and Decimation Filter Response

Interpolator Data Rate Resolution Relative to 64 × ODR (Hz)	Combined Interpolator/ Decimator Delay (ODR Cycles)	Combined Interpolator/ Decimator Delay (ms)	Combined Interpolator/Decimator Output Attenuation at ODR/4 (dB)
64 × 4000 = 256000	3.51661	0.88	−6.18
64 × 2000 = 128000	3.0126	1.51	−4.93
64 × 1000 = 64000	2.752	2.75	−4.66
64 × 500 = 32000	2.6346	5.27	−4.58
64 × 250 = 16000	2.5773	10.31	−4.55
64 × 125 = 8000	2.5473	20.38	−4.55
64 × 62.5 = 4000	2.53257	40.52	−4.55
64 × 31.25 = 2000	2.52452	80.78	−4.55
64 × 15.625 = 1000	2.52045	161.31	−4.55
64 × 7.8125 = 500	2.5194	322.48	−4.55
64 × 3.90625 = 250	2.51714	644.39	−4.55

SERIAL COMMUNICATIONS

The 4-wire serial interface communicates in either the SPI or I^2C protocol. It affectively autodetects the format being used, requiring no configuration control to select the format.

SPI PROTOCOL

Wire the ADXL357 for SPI communication as shown in the connection diagram in Figure 64. The SPI protocol timing is shown in Figure 65 to Figure 68. The timing scheme follows the clock polarity (CPOL) = 0 and clock phase (CPHA) = 0. The SPI clock speed ranges from 100 kHz to 10 MHz.

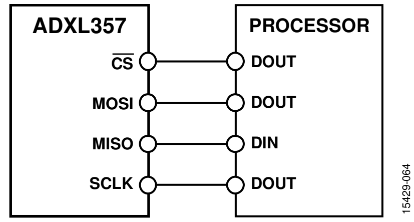


Figure 64. 4-Wire SPI Connection

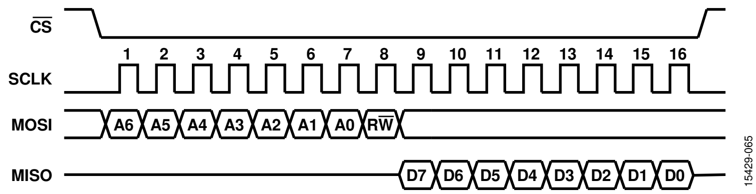


Figure 65. SPI Timing Diagram—Single-Byte Read

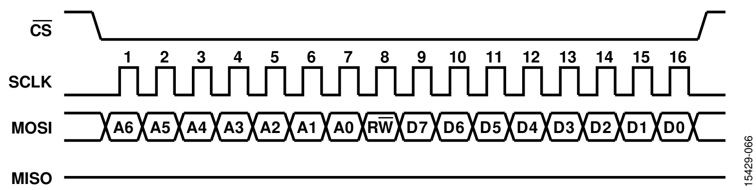


Figure 66. SPI Timing Diagram—Single-Byte Write

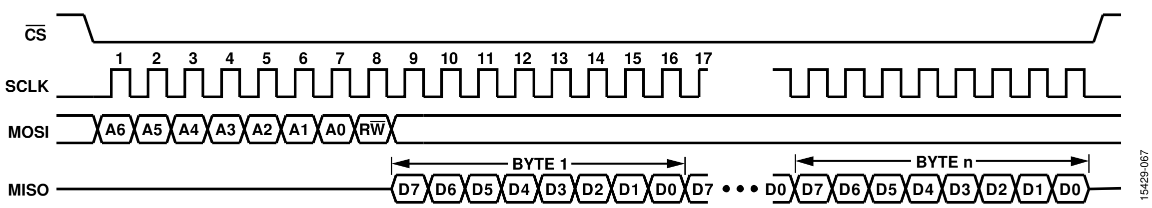


Figure 67. SPI Timing Diagram—Multibyte Read

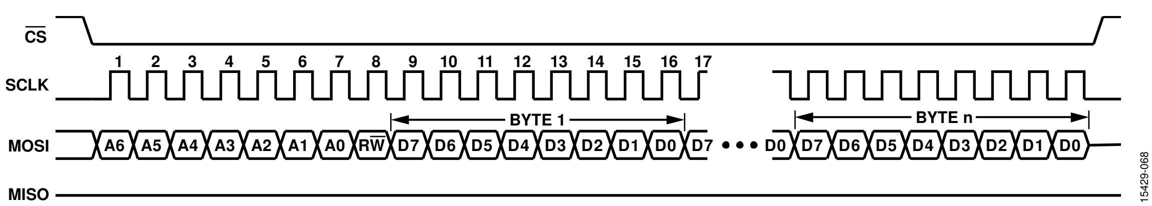


Figure 68. SPI Timing Diagram—Multibyte Write